Radiation Report

TMS570LC4357-SEP TID Radiation Report

ABSTRACT

This report discusses the radiation characterization results of the TMS570LC4357-SEP ARM Cortex-R based microcontroller. The study was done to determine Total Ionizing Dose (TID) effects under low dose rate (LDR, unbiased) and high dose rate (HDR, biased) conditions. All samples passed post-irradiation electrical tests within the specified data sheet limits up to 30krad(Si) LDR and HDR. TID effects on ADC (Analog to Digital Converter) and Flash Memory Program and Erase Cycles are shown at differing HDR (High Dose Rate, biased) conditions. This report also functions as the RLAT report for TI lot number (2009899ADT).

Table of Contents

List of Tables

Trademarks

Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

1 Device Information

The TMS570LC4357-SEP is a high-performance Arm® Cortex® R-based microcontroller that features on-chip diagnostic features, including dual CPUs in lockstep, Built-In Self-Test (BIST) logic for CPU, the N2HET coprocessors, and for on-chip SRAMs, as well as ECC protection on the L1 caches, L2 flash, and SRAM memories. The device supports ECC or parity protection on peripheral memories and loopback capability on peripheral I/Os.

The TMS570LC4357 device features 4MB of integrated flash and 512KB of data RAM with single-bit error and double-bit error detection. The flash memory on this device is a nonvolatile, electrically erasable, and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3V supply input (the same level as the I/O supply) for all read, program, and erase operations. The SRAM supports read and write accesses in byte, halfword, and word modes.

The device integrates two ARM Cortex-R5F floating-point CPUs, operating in lockstep, which offer 1.66 DMIPS/MHz and can run up to 300MHz, providing up to 498DMIPS. The device supports the big-endian (BE32) format.

With integrated safety features and a wide choice of communication and control peripherals, the TMS570LC4357-SEP device is designed for high-performance real-time control applications with safety-critical requirements.

For more information, see the product page.

Table 1-1. Device Information Table

Description	Device Information
TI Device Number	TMS570LC4357-SEP
Package	337 GWT (nFBGA)
Die Lot Number	6021835ADT; 2009899ADT
A/T Lot Number / Date Code	7378840 / 78AICXW; 2529561PHI / 2AC99TW
Quantity Tested	29 irradiated devices
Lot Accept/Reject	Devices passed up to 30 krad(Si)
HDR Radiation Facility	Aeroflex RADs, Colorado Springs, CO; TI CLAB, Dallas, TX
HDR Dose Level	Aeroflex (Three units): 3 krad(Si) = TI CLAB (20 units): 10krad(Si), 20krad(Si), 30krad(Si), 40krad(Si)
HDR Dose Rate	Aeroflex: 65 rad(Si)/sec TI CLAB: 188 rad(Si)/sec
HDR Radiation Source	Gammacell 220 Excel (GC-220E) Co-60
LDR Radiation Facility	Aeroflex RADs, Colorado Springs, CO
LDR Dose Level	20krad(Si), 30krad(Si)
LDR Dose Rate	.01rad(Si) / s
LDR Radiation Source	Gammacell JLSA 81-24 Co-60
Irradiation Temperature	Ambient (room temperature)

Note

TI may provide technical, applications, or design advice, quality characterization, and reliability data or service, providing these items shall not expand or otherwise affect TI's warranties as outlined in the Texas Instruments Incorporated Standard Terms and Conditions of Sale for Semiconductor Products, and no obligation or liability shall arise from TI's provision of such items.

2 Total Dose Test Setup

Test Overview

The TMS570LC4357-SEP F021 is built with TI's F021 CMOS process technology. Both HDR (biased) and LDR (unbiased) tests were performed, per MIL-STD-883, Test Method 1019.9, Condition A and B. The TMS570LC4357-SEP was irradiated up to 30krad(Si) and then put through complete electrical parametric testing on production Automated Test Equipment (ATE). Post irradiation, the devices were functional and passed all electrical parametric tests with readings within guard bands of the data sheet electrical specification limits.

Test Description and Facilities

The TMS570LC4357-SEP LDR exposure was performed on unbiased devices in a Co60 gamma cell under a 10 mrad(Si)/s exposure rate. The dose rate of the irradiator used in the exposure ranges from less than 10mrad(Si) / s to a maximum of approximately 65 rad(Si)/s is determined by the distance from the source. The exposure boards are housed in a lead-aluminum box (as specified in MIL-STD-883 TM 1019.9) to harden the gamma spectrum and minimize dose enhancement effects. The initial TMS570LC4357-SEP HDR exposure (three units) was performed on biased devices in a Co60 gamma cell at Aeroflex RADs, Colorado Springs, CO.: the unattenuated dose rate of this cell is 65 rad(Si)/s. After exposure, the devices were packed in dry ice (per MIL-STD-883 Method 1019.9 section 3.10) and returned to TI Dallas for a full post radiation electrical evaluation using Texas Instruments production Automated Test Equipment (ATE). Post radiation measurements were taken within 30 minutes of removal of the devices form the dry ice container. The devices were allowed to reach room temperature prior to electrical post radiation measurements. Follow-up HDR characterization on the ADC and FLASH content of TMS570LC4357-SEP was performed in Texas Instruments Dallas area lab (CLAB), also using a Co60 gamma cell with an unattenuated dose rate of 188rad(Si) / s. Total elapsed time from the end of the Gamma-cell exposure to test on ATE was approximately 45 minutes, with test at room temperature. ATE guard band test limits are set within data sheet electrical limits to meet a minimum C_{pk} and test error margin based on initial qualification and characterization data.

Test Setup Details

The LDR exposure was performed under unbiased conditions, and the HDR exposure was performed under biased conditions as described below:

For the unbiased LDR conditions, the exposure was performed with all pins grounded.

For the biased HDR conditions, the device was biased as shown below during HDR exposure with supply conditions as PS1 = 2.1V, PS2 = 4V, and PS3=4.2V.

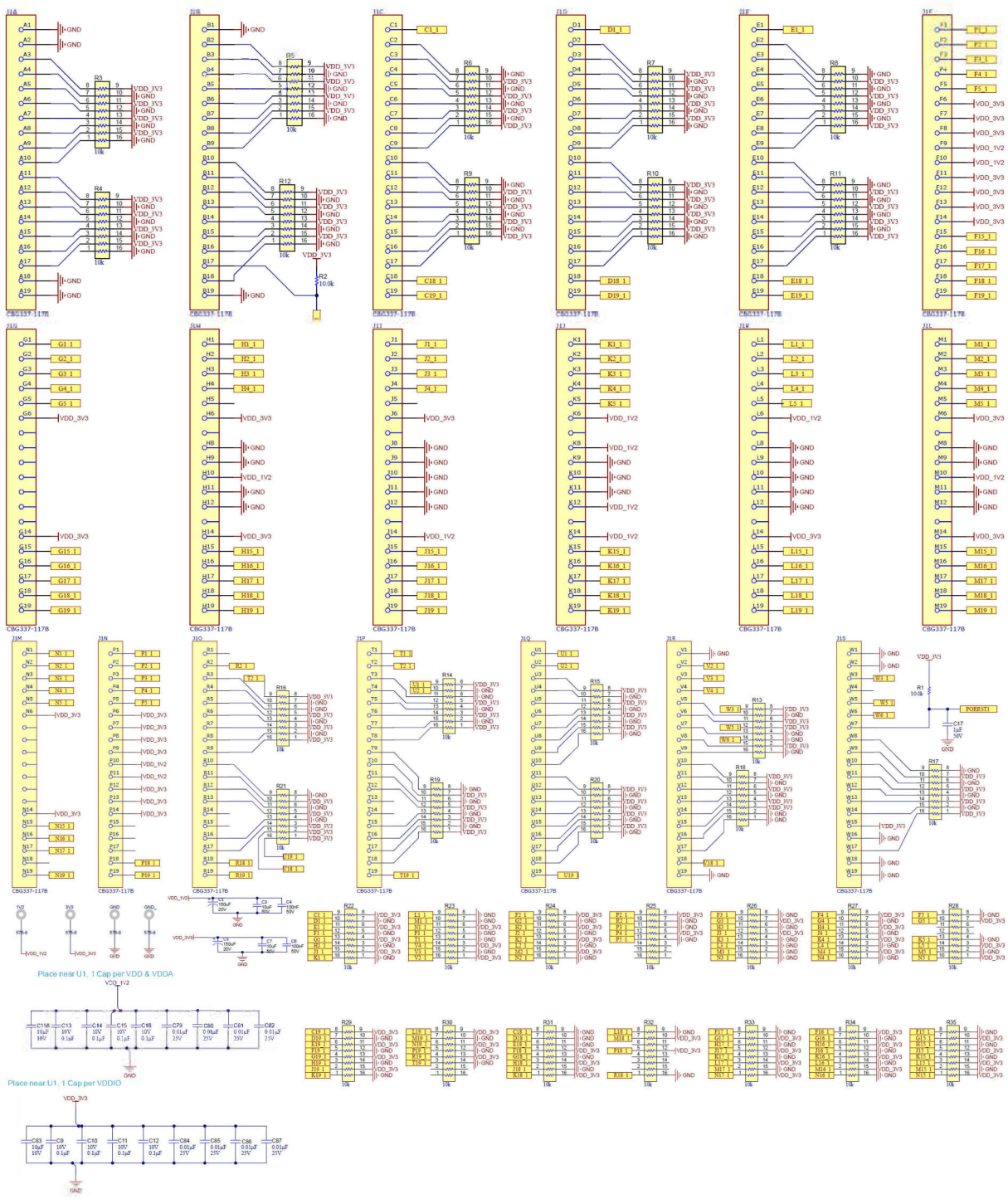

Figure 2-1. TMS570LC4357-SEP Bias Diagram

Test Configuration and Condition

A step-stress (for LDR: 20k and 30k, for HDR: 10k, 20k, 30k, 40k) test method was used to determine the TID hardness level. After a predetermined TID level was reached, an electrical test was performed on a given sample of parts to verify that the units are within specified data sheet electrical test limits. MIL-STD-883, Test Method 1019.9, Conditions A and B was used.

Table 2-1. TMS570LC4357-SEP Total Ionizing Dose LDR Conditions (Full Functional Testing)

LDR = 10 mrad(Si)/s; Aeroflex RAD, Colorado Springs, CO	
Total Samples: Six units, unbiased	
Exposure Levels (2)	
20krad(Si)	30krad(Si)
Unbiased	Unbiased
Units 1,2,3	Units 4, 5, 6

Table 2-2. TMS570LC4357-SEP Total Ionizing Dose HDR Conditions (Full Functional Testing)

HDR = 65rad(Si) / s; Aeroflex RAD, Colorado Springs, CO.
Total Samples: Three units, biased
Exposure Levels (1)
30krad(Si)
Biased
Units 7, 8, 9

Table 2-3. TMS570LC4357-SEP Total Ionizing Dose HDR Conditions (Full Functional and ADC and Flash Characterization)

HDR = 188rad(Si)/s; Texas Instruments, Dallas, TX.
Total Samples: 20 units, biased
Exposure Levels (4)
10krad(Si), 20krad(Si), 30krad(Si), 40krad(Si)
Biased
Five units at each dose level (units 10-29)

3 Tested Parameters

Table 3-1 and Table 3-2 list critical parametric tests with significant shift pre- and post irradiation, as measured on ATE (Automated Test Equipment) in this study.

Table 3-1. Data Sheet Parameter Table

Parameter	Test Description	Data Sheet Literature Number: SPNS195		
		MIN	MAX	UNIT
ADC $LEAK_{HI}$ M_{OFF}	ADC Leakage Hi-Range; analog off at $V_{cc}AD$ = 5.25V	-0.25	1	µA
ADC $LEAK_{MID}$ M_{OFF}	ADC Leakage Mid-Range; analog off at $V_{cc}AD$ = 5.25V	-0.25	.25	µA
ADC $LEAK_{LO}$ M_{OFF}	ADC Leakage Low-Range; analog off at $V_{cc}AD$ = 5.25V	-1	.25	µA
ADC $LEAK_{HI}$ M_{ON}	ADC Bias Hi-Range; analog on at $V_{cc}AD$ = 5.25V	-5	18	µA
ADC VA525 $LEAK_{MID}$ M_{ON}	ADC Bias Mid-Range; analog on at $V_{cc}AD$ = 5.25V	-5	3	µA
ADC VA525 $LEAK_{LO}$ M_{ON}	ADC Bias Low-Range; analog on at $V_{cc}AD$ = 5.25V	-12	3	µA

Table 3-2. TI Test Parameter Table

Parameter	Test Description	TI-Specified		
		MIN	MAX	UNIT
B0 ERS PLS	Flash pump pulses required to erase Bank0 (2MB)	NA	2000	N(cycles)
B1 ERS PLS	Flash pump pulses required to erase Bank1 (2MB)	NA	2000	N(cycles)
B2 ERS PLS	Flash pump pulses required to erase Bank2 (128KB)	NA	4000	N(cycles)
VHV ER MN	Flash pump volts during erase cycle at V_{min}	10.25	14	V
VHV ER MX	Flash pump volts during erase cycle at V_{max}	10.25	14	V
VHV PG MN	Flash pump volts during program cycle at V_{min}	8.9	12	V
VHV PV MN	Flash pump volts during program verify cycle at V_{min}	2.85	3.85	V
VREAD MN	Flash pump volts during read cycle at V_{min}	2.5	3.5	V

4 Total Ionizing Dose Characterization Test Results

Total Ionizing Dose Summary Results

The TMS570LC4357-SEP passed post electrical test over the following conditions.

- LDR (0.01rad(Si) / s) unbiased: Post 20krad(Si), 30krad(Si)
- HDR (188 rad(Si) / s) biased: Post 10krad(Si), 20krad(Si), 30krad(Si)

There were no functional or parametric failures at any read point up to 30krad(Si). All data sheet parameters passed up to this exposure level.

The measurements taken post-irradiation for each sample set showed a minimal shift for most parameters at each dose level for both biased and unbiased units. A few parameters (specifically, the ADC current measurements, and flash memory program and erase cycle measurements) did show a greater degree of change between pre- and post-irradiation that were still within the electrical specifications up to 30krad(Si), but marginal to spec at 40krad(Si). All units up to 30krad(Si) dose successfully program and erase immediately after radiation exposure. Noticeable flash pump voltage attenuation occurs with higher dosage, which resulted in increased cycles to complete the erase. Repeat measurements on the 30krad(Si) units show that these parameters recover to near baseline values within hours of the radiation exposure (read points at 45 minutes, two hours, and 72 hours after irradiation. Units were kept under biased conditions between read-points). At 40krad(Si) dose, several of the units failed to erase 45 minutes after irradiation; these units recovered after 72 hours.

Please see Appendix A for HDR report on ADC parameter drift across dosage.

Please see Appendix B for HDR report on flash memory parameter drift across dosage.

5 Appendix A: Effect of HDR Dose on ADC Leakage at VccAD = 5.25V

All measurements collected approximately 45 minutes after HDR exposure.

Table 5-1. Total Ionizing Dose Raw Data for ADC Leakage Parameters at Varied HDR Dosage

Units:		uA	uA	uA	uA	uA	uA
Upper Spec Limit:		1	0.25	0.25	18	3	3
Lower Spec Limit:		-0.25	-0.25	-1	-5	-5	-12
HDR Dose (krad)	Unit Number	LEAKHI MOFF	LEAKMID MOFF	LEAKLO MOFF	LEAKHI MON	LEAKMID MON	LEAKLO MON
0	10	0.42	0.03	0	0.37	0.01	-0.03
0	11	0.38	0.03	0.01	0.32	0.02	-0.02
0	12	0.04	0.02	0.01	0.04	0.01	-0.02
0	13	0.03	0.01	0	0.03	0.01	-0.01
0	14	0.04	0.02	0.01	0.04	0.01	-0.02
0	15	0.4	0.02	0.01	0.38	0.02	-0.03
0	16	0.37	0.03	0.01	0.34	0.02	-0.02
0	17	0.03	0.02	0	0.03	0.01	-0.01
0	18	0.02	0.01	0	0.02	0	-0.01
0	19	0.45	0.03	-0.01	0.39	0.02	-0.03
0	20	0.42	0.03	-0.01	0.38	0.01	-0.03
0	21	0.38	0.03	0	0.33	0.02	-0.02
0	22	0.04	0.02	0	0.04	0.02	-0.01
0	23	0.03	0.01	0.01	0.02	0.01	-0.01
0	24	0.03	0.02	0	0.04	0.01	-0.02
0	25	0.42	0.03	0	0.38	0.02	-0.03
0	26	0.37	0.03	0.01	0.33	0.02	-0.02
0	27	0.03	0.02	0.01	0.04	0.01	-0.01
0	28	0.04	0.02	0	0.03	0.01	-0.02
0	29	0.79	0.03	0	0.67	0.01	-0.02
10	10	0.41	0.03	0	0.45	0.03	-0.03
10	11	0.38	0.03	0	0.41	0.03	-0.03
10	12	0.04	0.02	0.01	0.05	0.03	-0.02
10	13	0.02	0.01	0	0.04	0.01	-0.02
10	14	0.04	0.02	0	0.05	0.02	-0.03
20	15	0.42	0.02	0	1.09	0.28	-0.09
20	16	0.38	0.03	0	1.03	0.31	-0.09
20	17	0.04	0.02	0	0.92	0.64	-0.07
20	18	0.02	0.01	0	0.81	0.59	-0.08
20	19	0.04	0.02	-0.01	0.25	0.15	-0.09
30	20	0.42	0.02	-0.01	2.57	1.15	-0.22
30	21	0.38	0.03	0	1.67	0.69	-0.17
30	22	0.04	0.02	0	1.72	1.33	-0.19
30	23	0.02	0.01	0	1.76	1.32	-0.16
30	24	0.03	0.02	-0.01	1.65	1.23	-0.25
40	25	0.42	0.03	-0.01	7.98	3	-0.54
40	26	0.38	0.03	-0.01	3	1.39	-0.52
40	27	0.04	0.02	0	3.26	2.51	-0.58
40	28	0.02	0.01	-0.01	3.95	3.1	-0.48
40	29	0.03	0.01	-0.02	3.16	2.39	-0.59

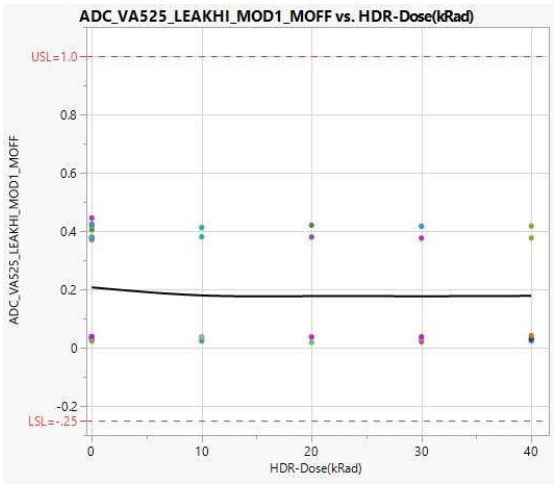

Figure 5-1. ADC Leakage (µA), High-Range, Analog Off

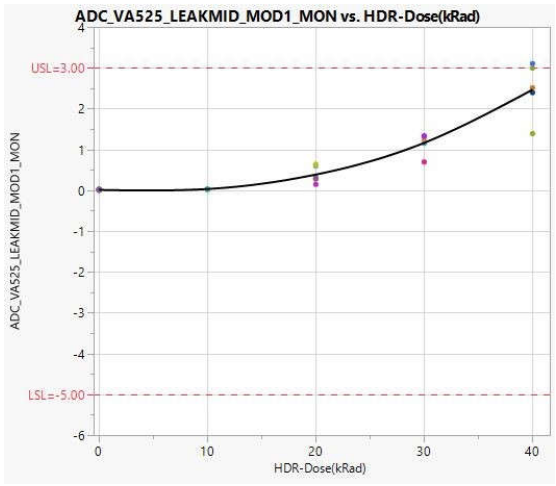

Figure 5-2. ADC Bias (µA), High-Range, Analog On

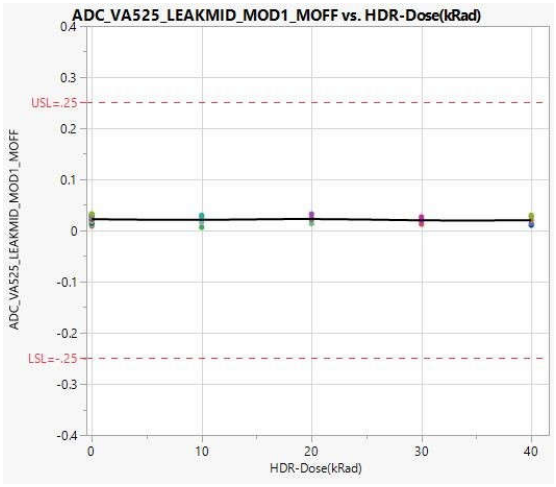

Figure 5-3. ADC Leakage (µA), Mid-Range, Analog Off

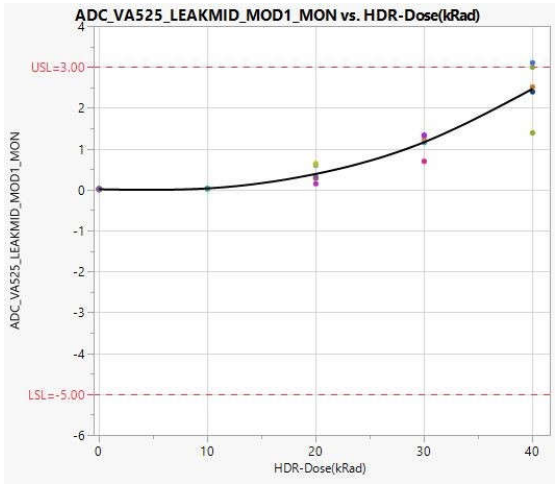

Figure 5-4. ADC Bias (µA), Mid-Range, Analog On

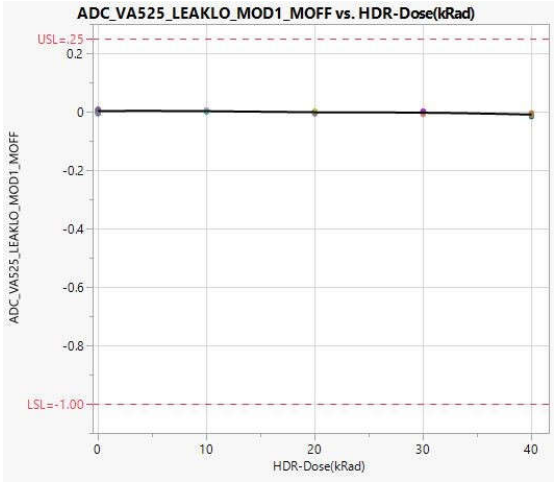

Figure 5-5. ADC Leakage (µA), Low-Range, Analog Off

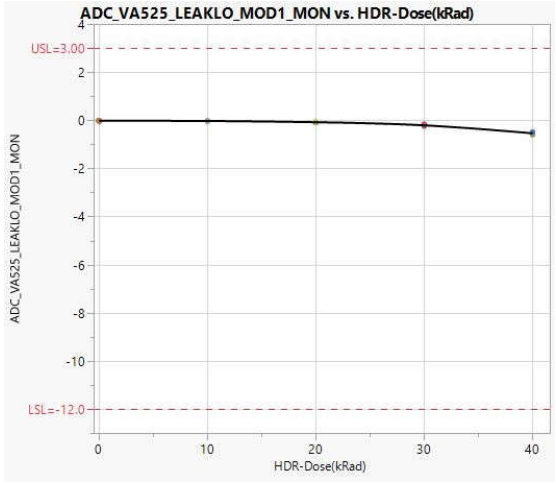

Figure 5-6. ADC Bias (µA), Low-Range, Analog On

6 Appendix B: Effect of HDR Dose & Time on Flash Memory Critical Parameters

All measurements collected approximately 45 minutes after HDR exposure.

Table 6-1. Total Ionizing Dose Raw Data for Flash Memory Critical Parameters at Varied HDR Dosage

Units:		N (Cycles)	N (Cycles)	N (Cycles)	V	V	V	V	V
Upper Spec Limit:		2000	2000	4000	14	14	12	3.85	3.5
Lower Spec Limit:		NA	NA	NA	10.25	10.25	8.90	2.85	2.5
HDR Dose (krad)	Unit	BANK0 ERS PLS	BANK1 ERS PLS	BANK2 ERS PLS	VHV ER MN	VHV ER MX	VHV PG MN	VHV PV MN	VREAD MN
0	10	10	9	7	13.24	13.19	11.29	3.61	2.96
0	11	11	10	7	13.11	13.04	11.22	3.58	2.96
0	12	10	10	7	13.21	13.17	11.30	3.60	2.96
0	13	8	9	7	13.10	13.05	11.19	3.60	2.96
0	14	9	8	7	13.01	12.96	11.15	3.56	2.97
0	15	8	9	7	13.03	12.99	11.18	3.57	2.96
0	16	9	10	7	13.18	13.12	11.27	3.62	2.96
0	17	12	8	7	13.29	13.23	11.32	3.59	2.96
0	18	8	8	7	13.27	13.21	11.38	3.61	2.96
0	19	9	8	7	13.39	13.33	11.42	3.6	2.96
0	20	8	9	7	13.23	13.18	11.32	3.6	2.96
0	21	9	11	7	12.97	12.93	11.20	3.57	2.94
0	22	10	9	7	13.05	13.02	11.2	3.57	2.95
0	23	8	9	7	13.19	13.15	11.27	3.59	2.96
0	24	9	10	7	13.05	13.01	11.19	3.57	2.96
0	25	9	12	7	13.00	12.95	11.18	3.58	2.96
0	26	10	9	7	13.21	13.15	11.29	3.59	2.97
0	27	7	8	7	13.26	13.23	11.33	3.61	2.96
0	28	9	9	7	13.19	13.14	11.26	3.58	2.96
0	29	8	7	7	13.54	13.52	11.47	3.63	2.96
10	10	11	11	7	12.91	12.87	11.12	3.60	2.96
10	11	15	13	7	12.84	12.78	11.08	3.59	2.96
10	12	11	12	7	12.94	12.89	11.16	3.60	2.95
10	13	10	13	7	12.76	12.72	11.01	3.58	2.96
10	14	10	10	7	12.70	12.66	10.98	3.55	2.97
20	15	19	13	7	12.44	12.39	10.82	3.54	2.95
20	16	16	20	8	12.54	12.48	10.88	3.58	2.95
20	17	76	42	12	12.23	12.17	10.65	3.50	2.96
20	18	23	21	9	12.49	12.44	10.90	3.56	2.96
20	19	21	21	8	12.52	12.47	10.89	3.55	2.94
30	20	698	1148	80	11.45	11.39	10.11	3.43	2.90
30	21	1842	2831	150	11.25	11.20	9.91	3.35	2.90
30	22	1430	1209	136	11.26	11.23	9.92	3.36	2.88
30	23	94	156	19	11.78	11.75	10.33	3.46	2.96
30	24	3847	2000	662	10.89	10.86	9.66	3.33	2.89
40	25	9999	9999	9999	0	0	0.40	0.67	0
40	26	9999	9999	9999	0	0	0	0.52	0
40	27	9999	9999	9999	0	0	0.37	0.55	0
40	28	9999	9999	9999	8.10	8.13	7.32	2.82	2.53
40	29	9999	9999	9999	0	0	0.11	0.35	0

Table 6-2. Total Ionizing Dose Raw Data for Flash Memory Critical Parameters at fixed HDR dosage (30 krad) and varied time after dosage (in hours, while device is V_{min} voltage biased.)

Units:		N (Cycles)	N (Cycles)	N (Cycles)	V	V	V	V	V
Upper Spec Limit:		2000	2000	4000	14	14	12	3.85	3.5
Lower Spec Limit:		NA	NA	NA	10.25	10.25	8.9	2.85	2.5
HDR Dose (krad)	Unit	BANK0 ERS PLS	BANK1 ERS PLS	BANK2 ERS PLS	VHV ER MIN	VHV ER MAX	VHV PG MIN	VHV PV MIN	VREAD MIN
0	10	10	9	7	13.24	13.19	11.29	3.61	2.96
0	11	11	10	7	13.11	13.04	11.22	3.58	2.96
0	12	10	10	7	13.21	13.17	11.30	3.60	2.96
0	13	8	9	7	13.10	13.05	11.19	3.60	2.96
0	14	9	8	7	13.01	12.96	11.15	3.56	2.97
0	15	8	9	7	13.03	12.99	11.18	3.57	2.96
0	16	9	10	7	13.18	13.12	11.27	3.62	2.96
0	17	12	8	7	13.29	13.23	11.32	3.59	2.96
0	18	8	8	7	13.27	13.21	11.38	3.61	2.96
0	19	9	8	7	13.39	13.33	11.42	3.6	2.96
0	20	8	9	7	13.23	13.18	11.32	3.6	2.96
0	21	9	11	7	12.97	12.93	11.2	3.57	2.94
0	22	10	9	7	13.05	13.02	11.2	3.57	2.95
0	23	8	9	7	13.19	13.15	11.27	3.59	2.96
0	24	9	10	7	13.05	13.01	11.19	3.57	2.96
0	25	9	12	7	13.00	12.95	11.18	3.58	2.96
0	26	10	9	7	13.21	13.15	11.29	3.59	2.97
0	27	7	8	7	13.26	13.23	11.33	3.61	2.96
0	28	9	9	7	13.19	13.14	11.26	3.58	2.96
0	29	8	7	7	13.54	13.52	11.47	3.63	2.96
10	10	11	11	7	12.91	12.87	11.12	3.60	2.96
10	11	15	13	7	12.84	12.78	11.08	3.59	2.96
10	12	11	12	7	12.94	12.89	11.16	3.6	2.95
10	13	10	13	7	12.76	12.72	11.01	3.58	2.96
10	14	10	10	7	12.70	12.66	10.98	3.55	2.97
20	15	19	13	7	12.44	12.39	10.82	3.54	2.95
20	16	16	20	8	12.54	12.48	10.88	3.58	2.95
20	17	76	42	12	12.23	12.17	10.65	3.5	2.96
20	18	23	21	9	12.49	12.44	10.90	3.56	2.96
20	19	21	21	8	12.52	12.47	10.89	3.55	2.94
30	20	698	1148	80	11.45	11.39	10.11	3.43	2.9
30	21	1842	2831	150	11.25	11.2	9.91	3.35	2.9
30	22	1430	1209	136	11.26	11.23	9.92	3.36	2.88
30	23	94	156	19	11.78	11.75	10.33	3.46	2.96
30	24	3847	2000	662	10.89	10.86	9.66	3.33	2.89
40	25	9999	9999	9999	0	0	0.4	0.67	0
40	26	9999	9999	9999	0	0	0	0.52	0
40	27	9999	9999	9999	0	0	0.37	0.55	0
40	28	9999	9999	9999	8.1	8.13	7.32	2.82	2.53
40	29	9999	9999	9999	0	0	0.11	0.35	0

Table 6-3. Total Ionizing Dose Raw Data for Flash Memory Critical Parameters at Fixed HDR Dosage (30krad) and Varied Time after Dosage (Hours)

Units:		N (Cycles)	N (Cycles)	N (Cycles)	V	V	V	V	V
Upper Spec Limit:		2000	2000	4000	14	14	12	3.85	3.5
Lower Spec Limit:		NA	NA	NA	10.25	10.25	8.9	2.85	2.5
Time(Hours) Post 30krad Dose	Unit	BANK0 ERS PLS	BANK1 ERS PLS	BANK2 ERS PLS	VHV ER MN	VHV ER MX	VHV PG MN	VHV PV MN	VREAD MN
PreHDR	20	9	13	7	13.08	13.01	11.24	3.59	2.96
PreHDR	21	11	13	7	13.04	12.99	11.17	3.57	2.96
PreHDR	22	10	8	7	13.12	13.09	11.25	3.58	2.94
PreHDR	23	8	9	7	13.26	13.22	11.33	3.61	2.96
PreHDR	24	8	9	7	13.28	13.22	11.33	3.61	2.96
0.75	20	698	1148	80	11.45	11.39	10.11	3.43	2.9
0.75	21	1842	2831	150	11.25	11.2	9.91	3.35	2.9
0.75	22	1430	1209	136	11.26	11.23	9.92	3.36	2.88
0.75	23	94	156	19	11.78	11.75	10.33	3.46	2.96
0.75	24	3847	2000	662	10.89	10.86	9.66	3.33	2.89
2	20	101	180	25	11.87	11.82	10.42	3.48	2.95
2	21	268	571	33	11.66	11.61	10.23	3.41	2.94
2	22	128	84	20	11.82	11.77	10.35	3.44	2.95
2	23	27	38	10	12.2	12.15	10.63	3.51	2.95
2	24	427	676	42	11.54	11.48	10.14	3.43	2.95
72	20	10	17	8	12.85	12.79	11.1	3.58	2.96
72	21	14	16	7	12.73	12.68	10.98	3.55	2.96
72	22	10	9	7	12.88	12.85	11.11	3.57	2.95
72	23	8	9	7	13.03	13	11.21	3.6	2.95
72	24	9	12	7	12.92	12.87	11.13	3.59	2.94

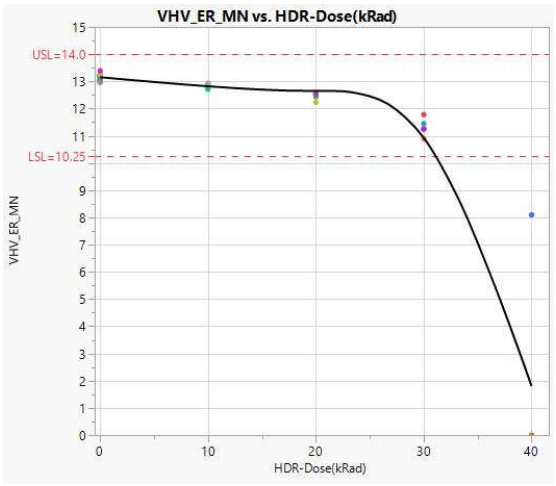

Figure 6-1. Flash Pump Voltage During Erase at Vmin 45min After HDR Dose

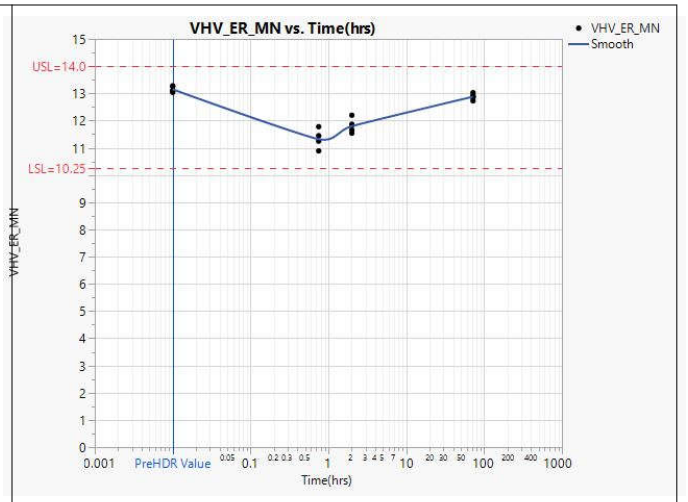

Figure 6-2. Flash Pump Voltage During Erase at Vmin, 30krad, Units Biased Between Reads

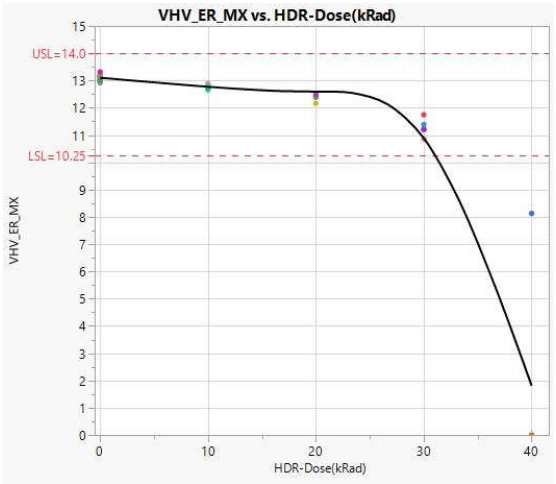

Figure 6-3. Flash Pump Voltage During Erase at Vmax, 45 Minutes After HDR Dose

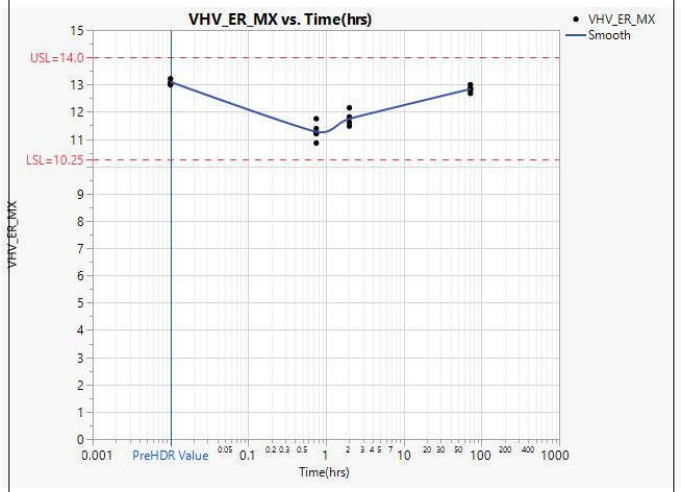

Figure 6-4. Flash Pump Voltage During Erase at Vmax, 30krad, Units Biased Between Reads

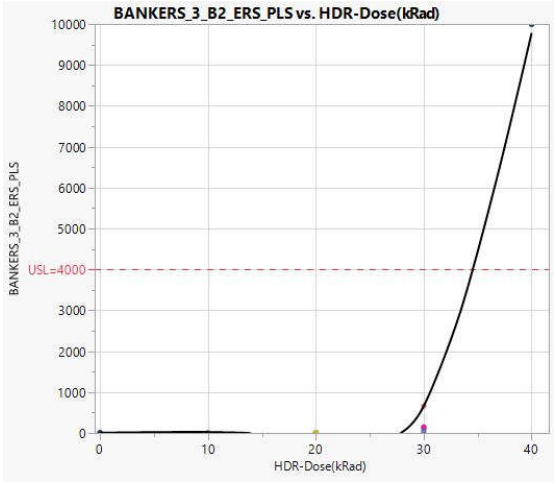

Figure 6-5. Flash Pump Voltage During Program at Vmin, 45 Minutes Post-HDR

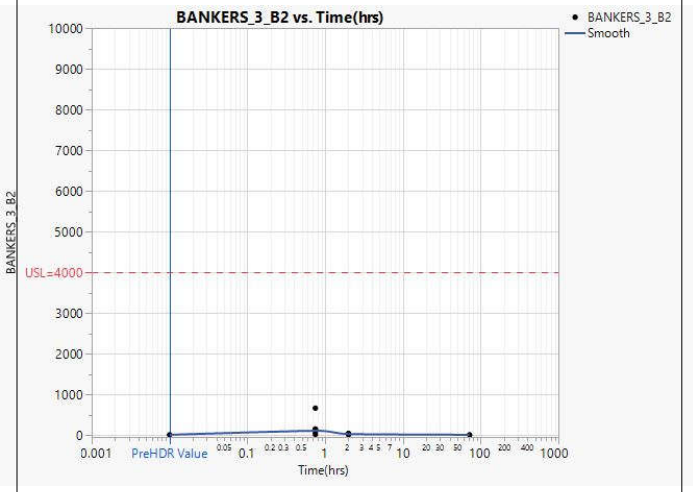

Figure 6-6. Flash Pump Voltage During Program at Vmin, 30krad, Units Biased Between Reads

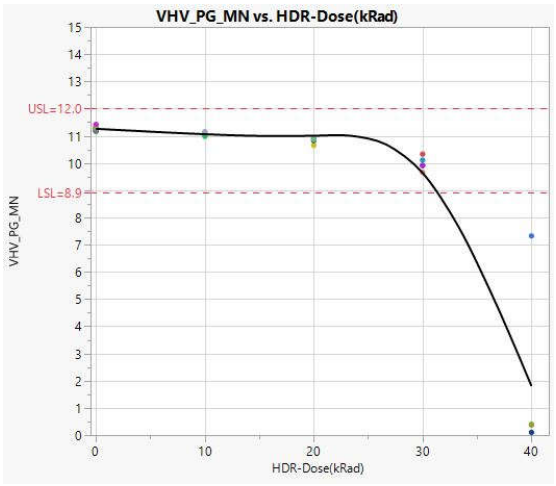

Figure 6-7. Flash Pump Voltage, Program Verify at Vmin, 45 Minutes Post-HDR

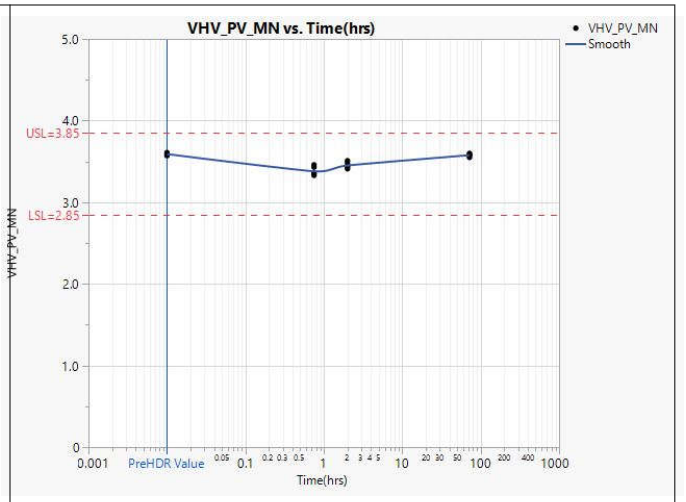

Figure 6-8. Flash Pump Voltage, Program Verify at Vmin, Units Biased Between Reads

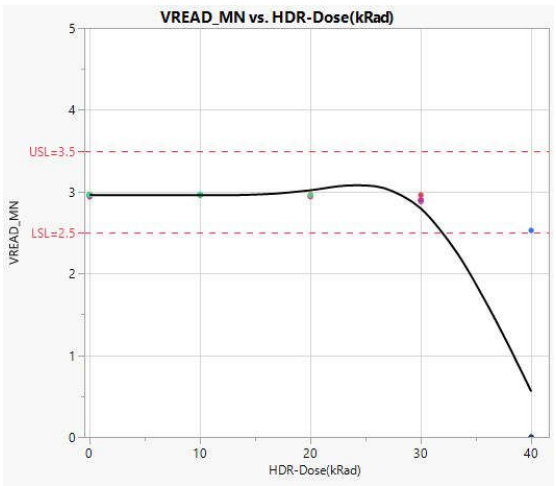

Figure 6-9. Flash Pump Voltage During Read at Vmin 45 Minutes Post-HDR

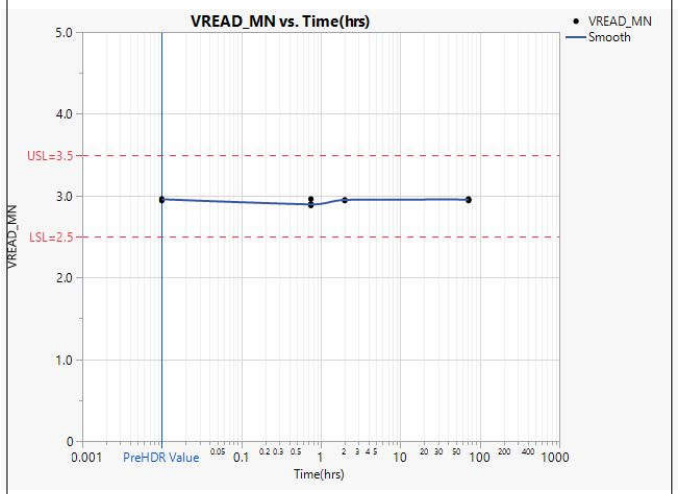

Figure 6-10. Flash Pump Voltage During Read at Vmin, 30krad, Units Biased Between Reads

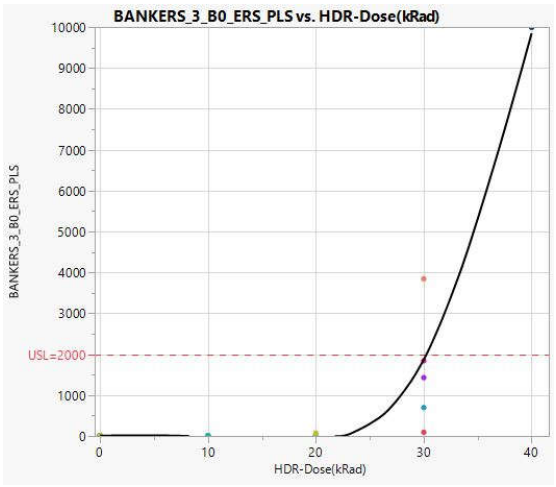

Figure 6-11. Flash Pump Pulses to Erase Bank0 at Vmin, 45 Minutes Post-HDR

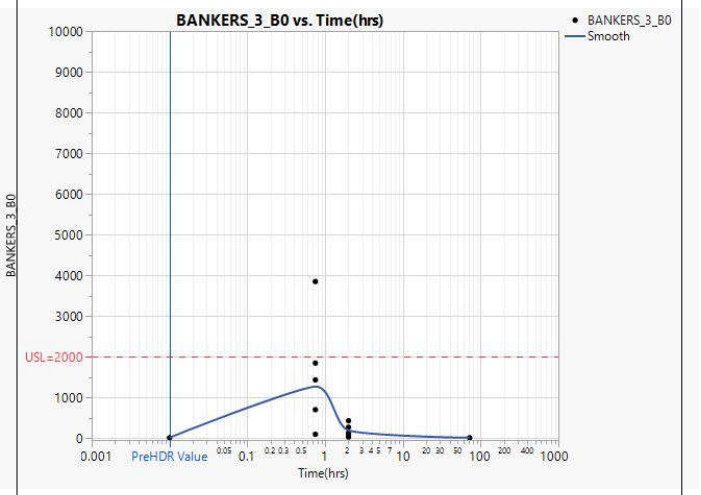

Figure 6-12. FlashPump Pulses to Erase Bank0 at Vmin, 30krad, Units Biased Between Reads

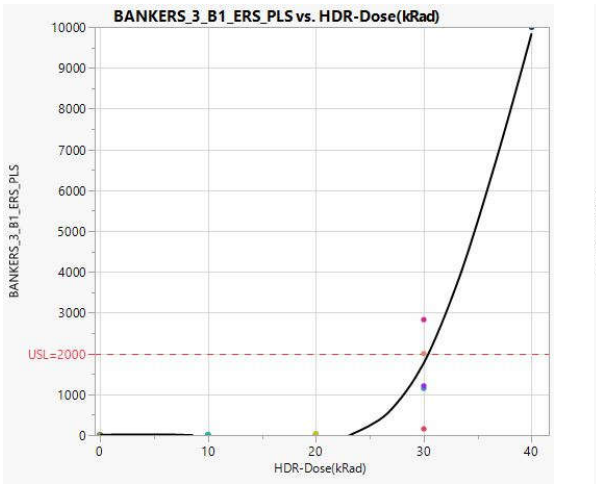

Figure 6-13. Flash Pump Pulses to Erase Bank1 at Vmin, 45min Post-HDR

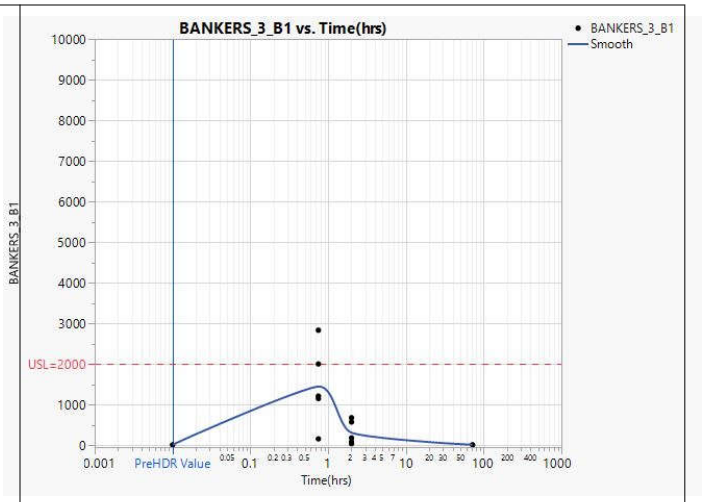

Figure 6-14. Flash Pump Pulses to Erase Bank1 at Vmin, 30krad, Units Biased Between Reads

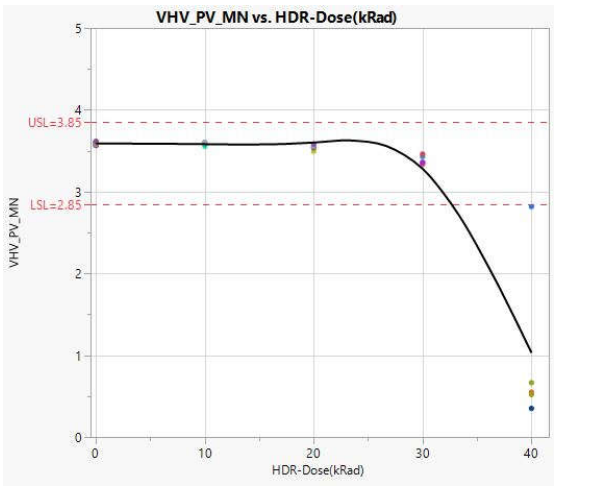

Figure 6-15. Flash Pump Pulses to Erase Bank2 at Vmin, 45min Post-HDR

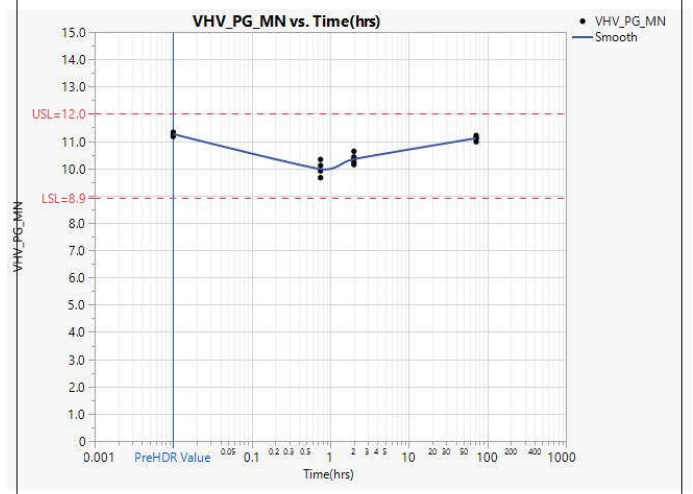

Figure 6-16. Flash Pump Pulses to Erase Bank2 at Vmin, 30krad, Units Biased Between Reads

Important Limitations on Use of Data Exceeding Specified Limits

TI is providing this data for your convenience. However, we want to make clear the significant limitations of its usefulness as an indicator of how devices may perform in various applications.

THIS DATA IS PROVIDED "AS IS" WITHOUT ANY EXPRESS OR IMPLIED WARRANTY OF ANY KIND INCLUDING WARRANTIES OF MERCHANTABILITY, NONINFRINGEMENT OF INTELLECTUAL PROPERTY, OR FITNESS FOR ANY PARTICULAR PURPOSE. IN NO EVENT SHALL TI OR ITS SUPPLIERS BE LIABLE FOR ANY DAMAGES WHATSOEVER (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, LOSS OF INFORMATION) ARISING OUT OF THE USE OF OR INABILITY TO USE THE INFORMATION, EVEN IF TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Your use of this data, and all consequences of such use, is solely your responsibility. You must perform sufficient engineering and additional qualification testing in order to properly evaluate your application and determine whether a candidate device is suitable for use in that application.

TI semiconductor components are specifically designed and manufactured to be used within the electrical, thermal, mechanical and other parameters set forth in TI's product data sheets. Quality and reliability data provided by Texas Instruments, such as MTBF and fit rate data, is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet for a device.

Plastic encapsulated TI semiconductor devices are neither designed nor warranted as suitable for use in military applications and/or military environments.

THIS INFORMATION SHOULD NOT BE USED TO ASSIST IN THE PRACTICE OF "UPRATING" OR "UPSCREENING" DEVICES FOR USE IN MILITARY OR OTHER CRITICAL APPLICATIONS. There are significant limitations of this information as an indicator of how commercial, off-the-shelf (COTS) devices may perform in such applications or environments, and about the hazards of using COTS devices in such applications. TI strongly believes that semiconductor components should never be used outside their specified tolerance levels as up-screening can lead directly to system or component failure. Such failures may present distinct risks to end-users and to third parties. TI cannot accept any responsibility for component or system failures that occur due to the misuse of its products, including misuse that may result from the practice of up-screening.

Any use of TI components beyond their rated limits voids all warranty responsibility of TI with respect to such devices, and also voids all responsibility of TI with respect to any applications assistance, product design, software performance or services of any kind that were or may have been performed in connection with the sale of any such devices. Further, resale of TI's products or services with statements different from or beyond the parameters stated by TI for that product or service in official TI data books or data sheets, or without the warnings or instructions provided by TI, voids all express and any implied warranties for the associated TI product or service, and is an unfair and deceptive business practice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265