TEXAS INSTRUMENTS

# Calculation of TMS320C5x Power Dissipation

## Application Report

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Digital Signal Processing Products


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# Calculation of TMS320C5x Power Dissipation Application Report

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## Introduction

The TMS320C5x devices are the latest and most powerful 16-bit fixed-point members in the TMS320 family of digital signal processors (DSPs). Architectural features and raw processing power of this generation of processors yields performance far beyond that of previous DSP devices.

The TMS320C5x family of DSPs are capable of processing speeds as high as 40 million instructions per second (MIPS) to handle the requirements of today's high performance applications. In addition to its performance capabilities, the device is designed to exhibit very low power dissipation, and features flexible power management modes which allow further savings on power requirments.

The TMS320C5x devices are fabricated in CMOS technology, the workhorse of the modern semiconductor industry. This sophisticated approach to IC fabrication combines high density with low power dissipation, yielding virtually the ideal fabrication technology. These characteristics make the TMS320C5x devices uniquely well-suited to portable power-sensitive and battery-operated applications such as digital cellular telephones, laptop modems, etc.

Because CMOS devices ideally draw current only when switching, this technology offers the potential for fully static devices with standby modes exhibiting near zero current drain.

Typical active current requirements for the TMS320C5x are a low 2.3 mA/MIPS for 5V, and 1.4 mA/MIPS for 3V operation. These characteristics are complemented by the following power management modes:

- The **Peripheral mode** (IDLE) conserves power by halting the CPU while maintaining all peripheral functions. Serial ports and timers continue operation, restarting the CPU only when additional data processing is needed. Current requirement in this mode is only 10mA for 5V , and 6mA for 3V operation.
- The **Sleep mode** (IDLE2) consumes as little as 5 μA or less with clocks turned off. The peripherals and CPU are halted until an external interrupt occurs.

This application report describes techniques for analyzing system and device conditions to determine operating current levels. From this analysis, power dissipation for the device can be determined. Knowledge of power dissipation can in turn, be used to determine device thermal management requirements.

The major topics covered in this document include

- General Device Current Characteristics
  - Current Components
  - Basic Current Dependencies
  - Algorithm Partitioning
  - Test Set-Up Description
- Current Due to Internal Components
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## General Device Current Characteristics

In general, device current requirements vary according to several system- and device-related considerations. Among these are supply voltage, temperature, and device program activity, along with other considerations normally associated with integrated circuit operation.

Additionally, because current requirements of CMOS technology are related to charging and discharging capacitances internal and external to the device, operating current also depends on considerations such as clock frequency, external load capacitance, and data patterns.

The TMS320C5x devices exhibit power supply current requirements consistent with CMOS device characteristics. Aspects of these characteristics necessary for analysis of device power supply current requirements are discussed in detail in this application report.

A thorough working knowledge of device architecture and operation is critical in performing the power analysis described in this document. Detailed information regarding TMS320C5x devices is found in the *TMS320C5x User's Guide* (literature number SPRU056B).

### Current Components

The TMS320C5x $V_{DD}$ supply pins are divided into groups according to the sections of internal circuitry to which they are connected. These four groups of supply pins are

- Control
- Data
- Internal, and
- Address

The **address** and **data** groups supply the output drivers on the address and data buses respectively. The **control** group supplies all other outputs except X1, and the **internal** group supplies all inputs, internal circuitry, and the X1 output.

In most systems, $V_{DD}$ and ground pins are connected together to the $V_{DD}$ and ground planes external to the device, respectively, unless separate $V_{DD}$ supplies are required because of specific system considerations. It is useful, however, to consider each group of power supply connections independently, since this greatly simplifies analysis of current requirements for the device. Therefore, current requirements for each group of power supply connections may be analyzed separately and then combined to determine total power supply current.

Within the four major groups of power supply connections on the TMS320C5x device are numerous distinct subgroups that contribute to its overall operating current. Extensive testing has been performed to identify the relative level of contribution of each area to the overall current . Although each functional area of the device contributes to the overall operating current, discussion is confined to parts of the device that contribute a significant amount of current to the total. This facilitates accurate and straightforward power dissipation analysis.

## Basic Current Dependencies

A variety of device- and system-related factors affect actual TMS320C5x power supply current requirements. Among these are the following:

- Signal switching rates
- Signal DC and capacitive loading levels
- $V_{DD}$ supply voltage levels
- Device operating temperature
- Bus data switching patterns

The most significant of these are signal switching rates and capacitive loading levels of the signals being switched. Device current requirements also vary depending on $V_{DD}$ voltage level and device operating temperature. Variation due to $V_{DD}$ is less significant than switching rate and capacitive effects, however, and temperature effects are even less significant.

Current dependence on switching rate and capacitance is due to the fact that, inherent to CMOS devices, current is required only during switching, and the magnitude of that current is relative to the capacitance being charged. Switching rate is significant due to the fact that the total current required for the device is the average of the sum of all the components of required current for each independent element switching. The more densely concentrated these are over time, the greater the average current. Therefore, the current required is directly proportional to the switching rate; the higher the switching rate, the higher the current. The same relationship exists for current requirement and capacitance; the larger the capacitance being charged during switching, the more current required.

As a consequence of current dependence on internal and external load capacitances, current requirements vary depending on data values being switched on internal and external address and data buses. This dependency results from the fact that, on signal connections grouped together as buses, parasitic capacitances exist which form intersignal coupling, causing the relative logical states of the bits within the bus to have an effect on current drain. The impact of this intersignal capacitance is that more current is required when adjacent bits on the bus are both switching to opposite values. In other words, significantly more current is required when switching from As to 5s than when switching from 0s to Fs. Accordingly, to obtain current values for switching data and address buses under actual operating conditions, current drain values obtained for worst case switching of As to 5s are scaled according to actual data patterns present for a particular application.

The total $I_{DD}$ power supply current can be described in an equation applying the basic power supply current components and the dependencies described above. This equation is as follows:

$$I_{tot} = (I_{int} + I_{add} + I_{data} + I_{cntl}) \times V \times T$$

where

$I_{tot}$ is the total $I_{DD}$ supply current,

$I_{int}$ is the current component due to all internal circuitry,

$I_{add}$ is the current component due to address bus outputs,

$I_{data}$ is the current component due to data bus outputs,

$I_{cntl}$ is the current component due to control outputs,

$V$ is a scale factor due to supply voltage, and

$T$ is a scale factor due to operating temperature.

Using this equation and determining all of its dependencies are described in detail in this application report.

## Algorithm Partitioning

Partitioning of algorithmic activity into independent segments plays an important role in analysis of device current requirements. The intent of algorithm partitioning is to identify periods of significant unique device activity over the course of program execution. A period of device activity is considered significant and unique if it lasts for a comparable or longer period of time with respect to, and is distinguishable from, other types of device activity. Such device activity can include reading external data tables, internal computations, writing results, initializing internal memory, idle, etc. Once the predominant periods of device activity within a program are identified, the current component associated with each period of activity is identified and calculated. Other current components are typically insignificant and can be ignored.

Algorithm partitioning is therefore typically an important first step in device current requirement analysis. Once this task is accomplished, the current for each period can then be easily calculated independent of other periods of program activity, and the net effect of all the different periods of program activity may easily be calculated by averaging the current for all of the program segments. In general, analysis of device current requirements is greatly simplified by this approach, as opposed to analyzing current at a more detailed level, which typically does not yield a significant increase in accuracy in comparison with the increased complexity of analysis.

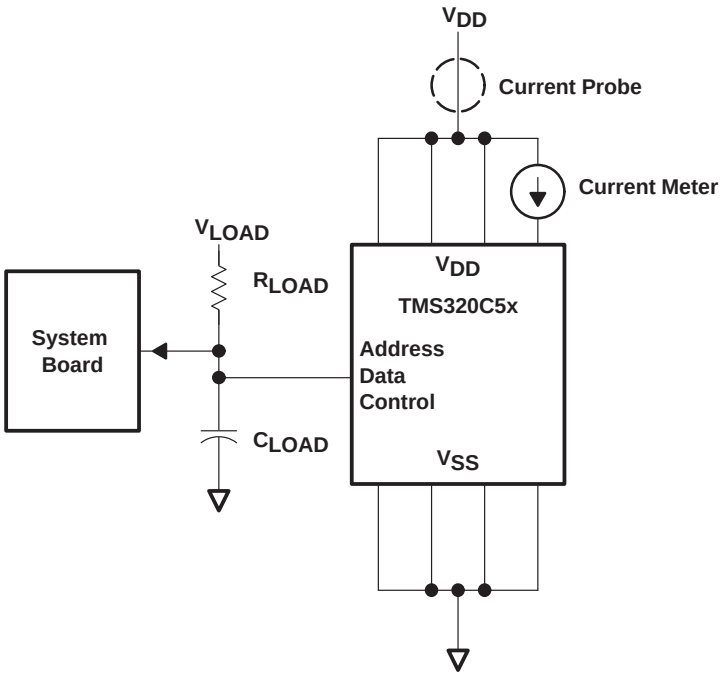
## Test Setup Description

Power supply current measurements were made with a specially designed TMS320C5x system board that allows power supply connections to the device to be isolated so that current measurements can be made on each of the four groups of power supply connections separately or together (see Figure 1).

A Tektronix AM 503 DC–50 MHz current probe is used to measure current on a variety of power supply connections. In addition, an inline digital current meter is used on the internal power supply connection for improved accuracy and correlation with results obtained with the Tektronix current probe. This test setup allows variations in DC load resistance, load capacitance, and load voltage to enable measurements to be made over a variety of system conditions.

Unless specified, measurements are made with a V load of 5 volts, a 20-kilohm load resistance, a 20-MHz system clock rate, and an ambient temperature of 25° C. The load capacitance was varied during many tests in order to establish dependence of power supply current requirements on this parameter. Note that the maximum rated total output load capacitance for the device is 80 pf.

**Figure 1. Test Setup**



## Current Due to Internal Components

Internal current components supply internal device logic. This includes current for the input buffers, oscillator, CPU, and all other internal device circuitry.

This section discusses only the internal current components that make significant contributions to overall device current requirements. Other current components are insignificant and are not discussed in detail. The internal current components discussed in this section are current due to internal CPU activity, memory usage, and current variation due to device clocking option selection.

### Current Due to Internal CPU Activity

Current due to internal CPU activity is dependent on the same characteristics as any other current components, but because individual signals internal to the device are not easily distinguishable, a more global approach to current analysis is required. The first step is to identify the predominant type of device activity involved.

Internal CPU current requirements start at a baseline of approximately 3 mA for periods of inactivity when executing an IDLE2, with a system clock rate of 20 MHz. When the device input clock is turned off while executing IDLE2, the device enters the low current standby mode, in which power supply current is greatly reduced. Under these conditions, current requirements are typically less than 5 μA.

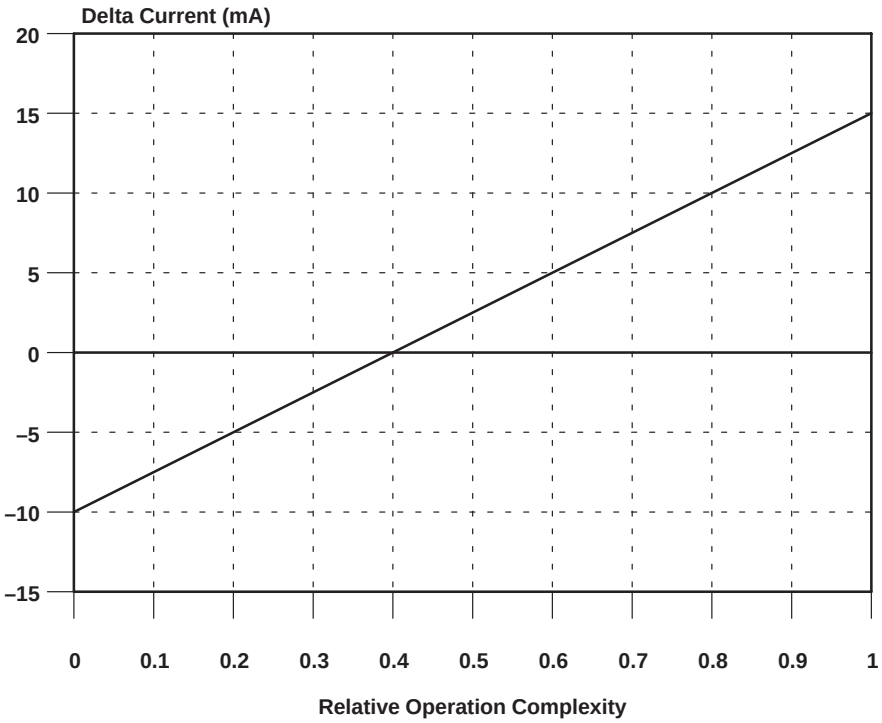
The IDLE instruction suspends CPU activity but retains clock to the internal device logic. Accordingly, current requirements in IDLE represent device clocking current requirements without any CPU activity. Executing IDLE typically requires 10 mA of current with a system clock rate of 20 MHz.

To fetch and execute instructions from on-chip memory requires a minimum of 42 mA. For the simplest instructions such as NOPs and simple internal operations, using the repeat function reduces this by approximately 10 mA, but only for the duration of the repeated instruction. In this case, the current is reduced because the repeat function does not refetch the instruction. For the more current-intensive instructions such as MACD, current is actually *increased* when using repeat, because instruction execution requires more current than fetching and decoding the instruction, contrary to the case of simpler instructions. Here, current requirements increase by 15 mA when using repeat. The break-even point for instructions in the repeated and the non-repeated modes is roughly in the area of ALU operations. This information is presented graphically in Figure 2.

Relationships of CPU activity to power supply current requirements for various types of CPU activity are shown in Figure 3 and are described in Table 1. This information can be used to determine current requirements for the full spectrum of internal CPU operations. Note that these current values are for internal components only; any current required for external device activity represents an additional current component. Note also that if program execution is from off-chip memory, current due to internal CPU activity may actually decrease by 1–2 mA (depending on memory usage) because of reduction in internal memory accesses. This is usually more than offset by an increase in current due to external memory accesses, resulting in an increase in total operating current. Current due to internal memory accesses is discussed in further detail later in this section.

As shown in Table 1, when executing programs utilize a variety of CPU resources, device current requirements start at 42 mA and increase according to the various instructions being executed. Current requirements of several versions of the VSELP speech coding algorithm have been measured and are typically in the range of 47-51 mA, depending on implementation. For a generic DSP application program using a variety of CPU resources and employing a nominal 20% usage of the MACD instruction, current requirements are approximately 55 mA.

**Figure 2. $I_{DD}$ Delta When Repeating Instructions**




When the device's on-chip multiplier is used extensively, such as in a sequence of contiguous multiplications, there is an increase in current above the generic typical current requirement, because the multiplier requires additional current to perform high-speed multiplications. This type of activity results in CPU current requirements of 60 mA.

If levels of device activity are increased by performing additions to the accumulator in parallel with multiplications using the MAC instruction, current requirements are increased to 75 mA when code is executed in line.

When multiplications are combined with additions, concentrated memory usage, and the DMOV operation with rapidly varying data values using the MACD instruction, current requirements are increased further to 76 mA.

At these levels of CPU activity, the repeat instruction causes current requirements to increase further, as described earlier. In the previous two examples, the MAC and the MACD current requirements increase to 76 and 90 mA, respectively, when these instructions are repeated. These are the highest internal current level requirements for the device. Note that these current levels occur when the full parallelism of the device is being utilized (that is, when the operands of the MAC or MACD are in different blocks of memory so that both operands are fetched simultaneously). When both operands are in one block of memory which does not support dual accessing, or are off chip, the current requirement for these operations is reduced by a factor of two, because this affects all aspects of the MAC or MACD instruction execution.

**Figure 3. TMS320C5x Power Dissipation Characteristics**

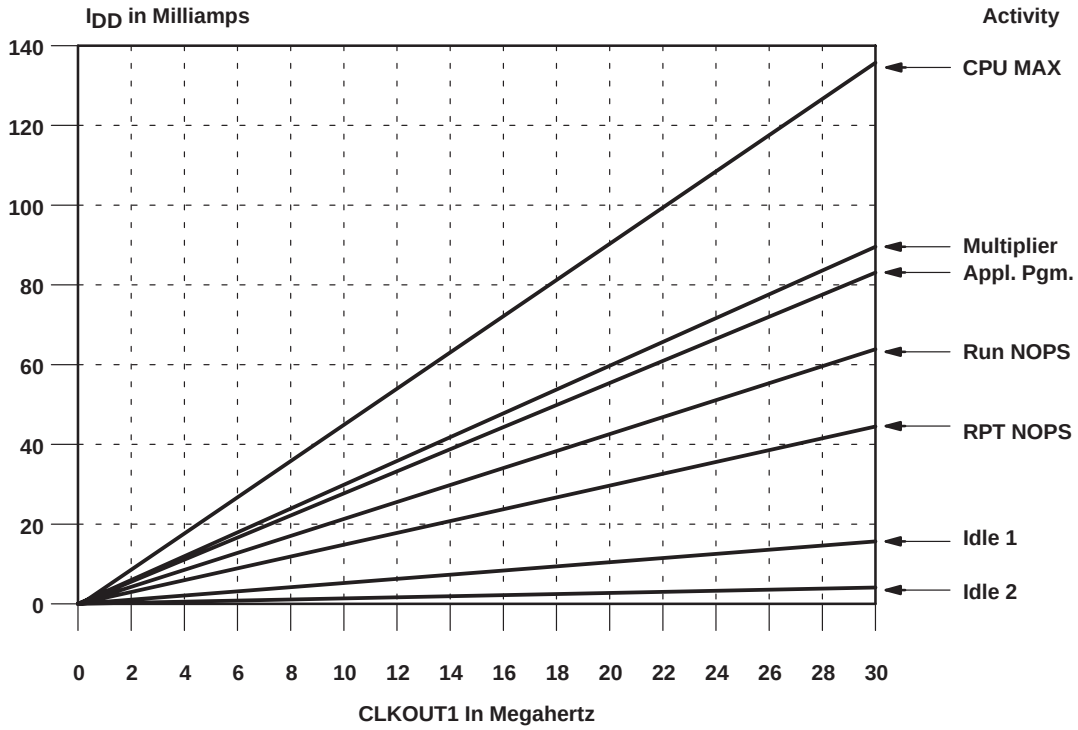



**Table 1. Current for Various CPU Activities**

| Current | Activity |
|---|---|
| 3 mA | IDLE2 |
| 10 mA | IDLE |
| 30 mA | Repeat NOPS |
| 42 mA | Execute NOPS |
| 42 mA | Bulk data transfer to on-chip memory using REPEAT, same data |
| 47–51 mA | VSELP speech encoding routine (implementation dependent) |
| 55 mA | Application program with nominal 20% MACD usage |
| 60 mA | Inline multiplies with immediate multiplicand, changing data |
| 57 mA | Bulk data transfer to on-chip memory without REPEAT, changing data. |
| 63 mA | Write 5/A to A/5 to external (internal component only). |
| 75 mA | Inline multiplies from memory, changing data. |
| 74 mA | Inline MAC's with changing data. |
| 76 mA | Inline MACD's with changing data. |
| 76 mA | Repeated MAC with changing data. |
| 90 mA | Repeated MACD with changing data. |

### Current Due to Memory Usage

In addition to instruction execution and processing operations within the CPU, accessing on- and off-chip memory also contributes to overall device current requirements. When memory accesses are performed randomly in conjunction with CPU operations, the additional current required is not significant in comparison with overall CPU current requirements. In fact, the difference between these two current components is virtually indistinguishable. However, when memory accesses are concentrated enough to become a significant unique and identifiable period of device activity, the current required becomes noteworthy. In these cases, this period of device activity becomes a separate consideration for current requirements, and must be analyzed separately from other device activity. Examples of these types of device activities include bulk data transfers to and from internal memory.

Because the major part of the memory arrays on the device are inactive even during memory access, it is in fact, the buses being used for memory access which require a significant amount of current during this type of activity. There are four main internal bus systems on the TMS320C5x: the data and address buses for the separate program and data spaces implemented in the device architecture. CPU activity and internal memory and bus usage are closely related because all program activity (except repeated instructions) utilizes the program address and data buses, while data operations utilize the data address and data buses and sometimes the program address and data buses (as in the case of MAC and MACD instructions). Examining the types of activity present on each bus yields significant information about how much a given sequence of device activity contributes to power supply current requirements.

For bulk data transfers to memory which generally utilize only the data bus heavily, 57 mA are required. Because internal bit-line and intersignal capacitances are low, this current requirement is effectively independent of data values and the current required is the same for reads or writes, and looped or straightline code. Current is reduced only when reads are repeated with very few data bits changing. In this case, current is reduced linearly from 57 mA to 42 mA according to the number of bits on which data is changing.

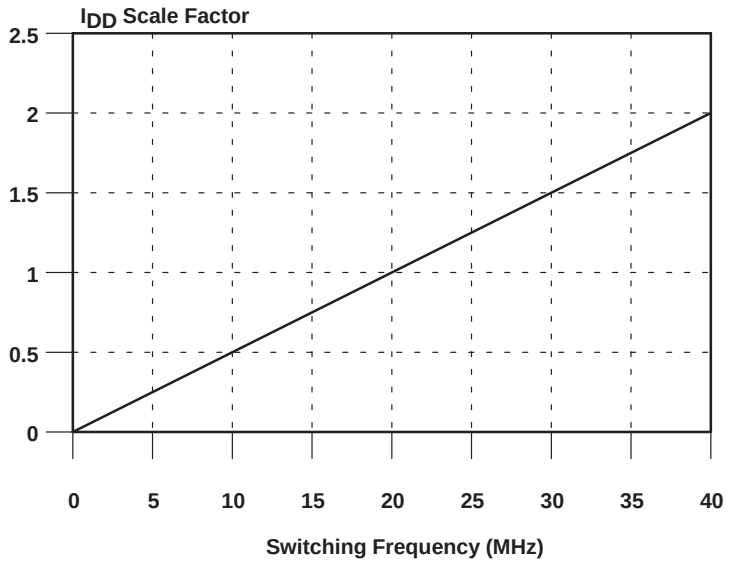
For bulk data transfers using two of the internal buses heavily, such as writing rapidly changing data to off-chip locations with rapidly varying addresses, current requirements increase to 63 mA.

Note that the power supply current due to CPU activity alone, for bulk data transfers to memory is approximately 42 mA. Therefore, the internal memory bus usage component of internal power supply current in the examples above ranges between 15–21 mA, depending on bus usage. These examples use instructions that execute in a single cycle; instructions which execute in two or more cycles reduce this component in a linear fashion. For example, a generic bulk data transfer requiring 57 mA, implemented using single cycle instructions, requires approximately 49 mA when implemented using two cycle instructions.

### Current Due to Clock Generation Circuitry

The choice of clock generation options also effects device power supply current requirements. The two main device clocking modes are divide-by-one and divide-by-two clocking. Two separate clock inputs are used for these two different clocking modes. The discussions above regarding device operating current are applicable to both clocking modes with the following exception. If divide-by-two clocking, with the internal oscillator enabled, is selected, more current is required. Using this mode of clock generation to allow an external crystal to be used to generate clock, requires an additional 20 mA of current at a frequency of 40 MHz (which results in a system clock rate of 20 MHz). When using different frequencies, this current value should be adjusted as shown in Figure 4.

**Figure 4. $I_{DD}$ Variation With Switching Frequency**



## Current Due to Outputs

Current due to outputs includes current on the **address**, **data**, and **control** power supply connections. **Address** and **data** supply connections include currents for the address and data bus outputs, respectively, and the **control** supply connections include currents due to parallel bus control output signals, such as $\overline{PS}$, R/$\overline{W}$, and $\overline{STRB}$, and system control outputs such as $\overline{IACK}$, $\overline{IAQ}$, $\overline{HOLDA}$, and CLKOUT1.

### Categories of Outputs

From the standpoint of power supply current requirements, device outputs may be categorized into several logical groupings, according to their relative contribution to the total overall supply current. These categories are:

- **Address** and **data bus supply connections** can be grouped together because they both contribute current components related to the overall parallel bus switching rate or memory cycle time. These signals are synchronous and switch at approximately the same rate. Considering the outputs in each of these buses as a group greatly simplifies analysis of their current requirements.

- The second group of outputs is the fast-switching outputs, of which the main contributor is CLKOUT1, but also includes $\overline{IAQ}$, and may include R/$\overline{W}$, $\overline{PS}$, $\overline{RD}$, $\overline{WE}$, $\overline{STRB}$, $\overline{DS}$, $\overline{IS}$, TOUT and XF depending on system configuration. These outputs contribute a smaller magnitude of current than a comparably loaded fast-switching 16-bit bus, but if the external bus is switching slowly or not at all, these outputs may be an important concern from the standpoint of system current requirements.

- The last major grouping of outputs is system control outputs which are relatively slowly switching, such as $\overline{HOLDA}$ and $\overline{IACK}$. Because these outputs switch much slower and are typically much less loaded than other signals, they contribute a relatively small amount of current to the total device current. Therefore, this component is typically insignificant enough to be negligible.

Current due to contributions from device outputs comprises three components and is summarized in the following equation:

$$I_{ext} = I_{add} + I_{data} + I_{cntl}$$

where,

$I_{ext}$ is the total current due to external components,

$I_{add}$ is the current component due to address bus outputs,

$I_{data}$ is the current component due to data bus outputs, and

$I_{cntl}$ is the current component due to control signal outputs.

The remainder of this section describes the calculation of output signal current components in detail.

### Parallel Interface Bus Current Requirements

Although the external parallel interface bus exhibits a wide range of characteristics over a variety of conditions, it is convenient to consider its current requirements from the perspective of maximum current and then derate current values to actual operating conditions.

Under worst case conditions, the 16-bit parallel address bus requires 64 mA to switch between 5's and A's when performing contiguous zero wait-state reads with a CLKOUT rate of 20 MHz at the device's maximum rated capacitive load of 80 pF. Note that this corresponds to an address bus switching rate of 10 MHz.

For the data bus, because the maximum write rate is half the maximum read rate, 32 mA are required when performing contiguous zero wait-state writes. In this case the corresponding switching rate is 5 MHz.

If either the switching rate or capacitive load is not at a maximum level, the current required is reduced according to the derating curves shown in Figure 4 and Figure 5.

Because intersignal capacitance causes bus switching current requirements to be dependent upon data values present on the external buses, current should also be derated if values being switched are not 5's and A's. Figure 6 shows derating characteristics for current over varying data values.

If program execution is from internal memory and no external access is being made, switching of the address outputs may be disabled through the use of the AVIS bit in the PMST status register. This feature can be used to save significant power in the system, however, note that once AVIS is set, the address ouputs are still driven in their previous state. Therefore, if any DC load is present, a dummy external cycle may be necessary to set the address outputs to zero if minimum power supply current is desired.

**Figure 5. Capacitive Load Derating Curve**

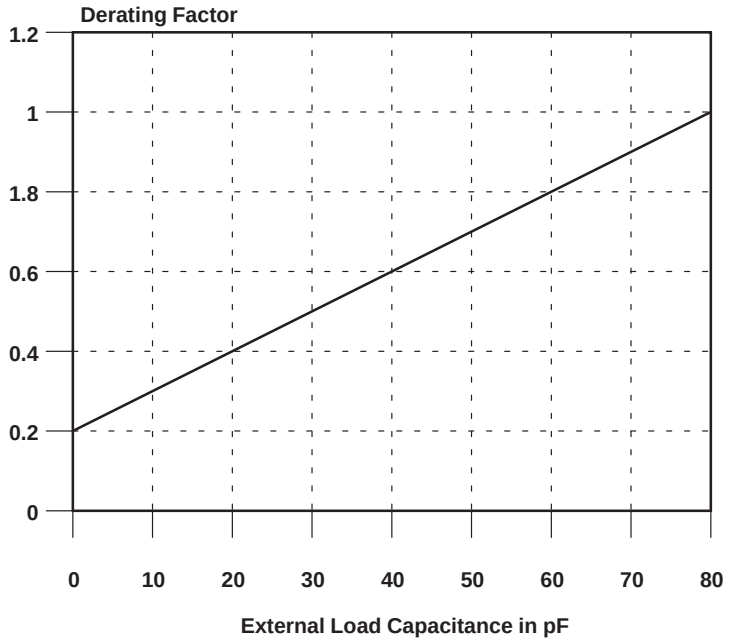
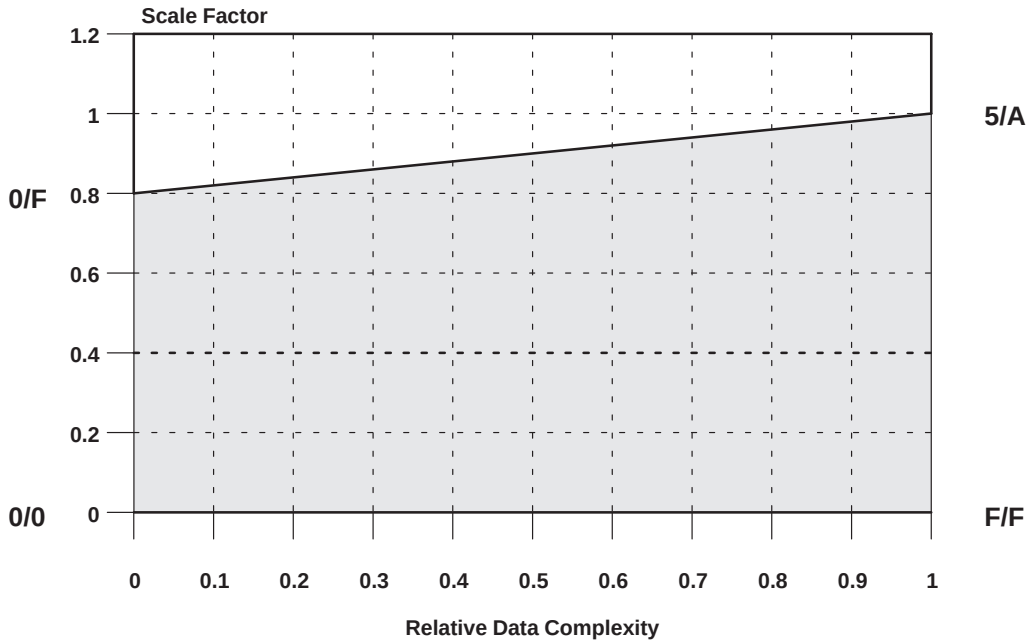


**Figure 6. Scale Factor for Data/Address Switching**




## Current Due to Other Outputs

Several other device outputs will, under various circumstances, make significant contribution to current requirements. The most significant of these is CLKOUT1 because this signal is always active and switching at the system clock rate, which is the fastest switching signal on the device unless the internal oscillator is being used. The $\overline{\text{IAQ}}$ signal also pulses at a rate which can be as fast as the system clock, especially if single cycle instructions are being executed. Other outputs that can switch at high rates include the parallel interface bus control signals ($\overline{\text{STRB}}$, $\overline{\text{RD}}$, $\overline{\text{WE}}$, etc.), XF, the timer output signal TOUT, and the serial port output signals. Because all of these signals may be switching at different rates and under different loading conditions, current should be calculated for each separately. The following equation should be used to calculate current required to drive any of these types of outputs:

$$I = C \times V \times F$$

where,

*I* is current in amperes,

*C* is capacitance in farads,

*V* is signal switching voltage swing, and

*F* is the switching frequency in hertz.

Performing this calculation yields the current due to any output under any conditions of switching rate or loading.

Note that when calculating current, the actual frequency of the waveform in question should be used, not the rate at which edges occur in the waveform. For example, the proper frequency to be used for a waveform that switches every 100 ns is 5 MHz, not 10 MHz.

### Considerations of TTL and Other DC Loads

If any device outputs experience TTL or other predominantly DC loads, consideration must be made for this in power supply current calculations.

The net result of DC loading to an output is that the current required to drive that output is increased by the magnitude of the average DC source current loading on the output.

As an example, consider a DC loading of 300 µA of source current per bit on the address bus outputs when driving alternating 0s and 1s with a 50% duty cycle. Here, the increase in current is calculated as follows:

$$0.50 \times 300\ \mu A \times 16 = 2.4\ mA$$

In this case, an extra 2.4 mA of current is added to the current value required to drive the capacitive portion of the address bus output loading calculated as described above.

## Total Power Dissipation

The previous sections have discussed power supply current components contributed by several different sources on the TMS320C5x device. Because determinations of actual current values are unique and independent for each source, each current source has been discussed separately. In an actual application, however, the sum of the independent contributions from each component determines the total current requirement for the device. This total current value is exhibited as the total current supplied to the device through all of the $V_{DD}$ inputs and returned through the $V_{SS}$ connections.

Note that numerous $V_{DD}$ and $V_{SS}$ pins on the device are routed to a variety of internal connections, not all of which are common. Externally, however, all of these pins should generally be connected together in parallel to the 5-volt and ground planes, respectively, with as low impedance as possible.

As mentioned previously, because different operations are performed during independent and unique periods of device activity, it is typically appropriate to consider current for each of the different sequences independently. Once this is done, peak current requirements are readily identified. Furthermore, average current calculations can be made to determine heating effects of power dissipation. These effects, in turn, can be used to determine thermal management requirements for the device.

### Calculation of Total Supply Current

Once all of the power supply current components are calculated for each of the periods of device activity, calculation of total power supply current is straightforward. To determine the total supply current, the power supply current values calculated for the **control**, **data**, **address**, and **internal** components are summed together for each unique period of device activity. This total supply current is then scaled according to effects of $V_{DD}$ and temperature, after which the average current can be calculated.

### Effects of Temperature and Supply Voltage on Current

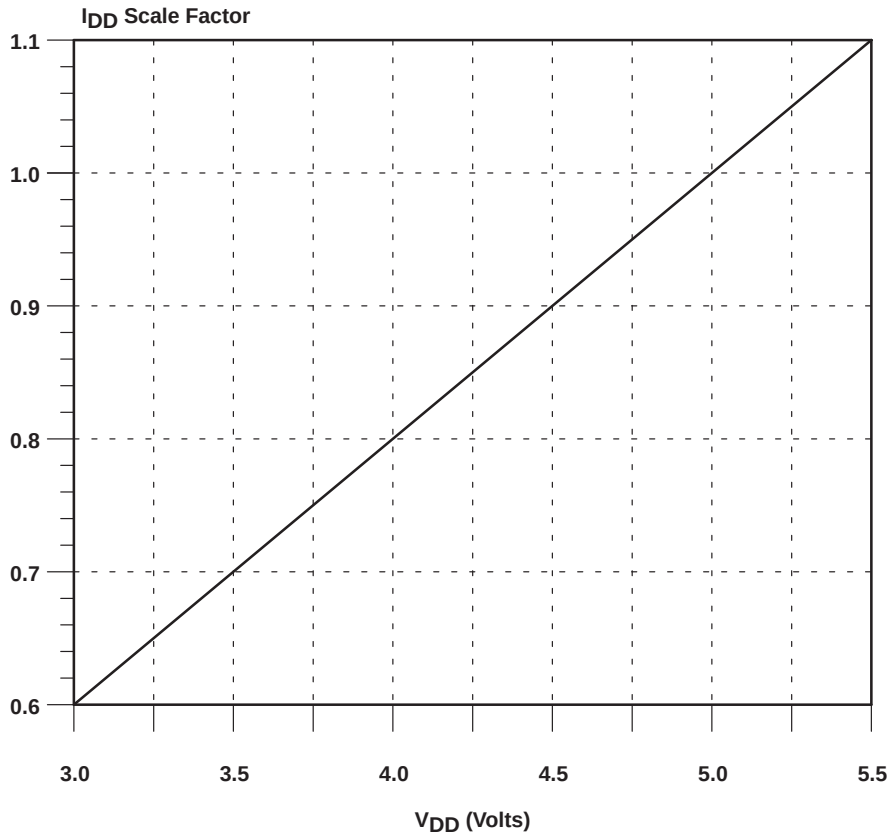
Two system factors, temperature and $V_{DD}$ supply voltage, affect all components of device operating current equally. Their effects should be applied to current values after total current for a given period of device activity has been calculated. Note that supply voltages and temperature must be maintained within required device specifications.

Power supply current is proportional to temperature, however, its variation due to temperature is small and is therefore generally not significant. If necessary, to account for absolute worst case effects including temperature across the total operating range of the device, power supply current values obtained above may be scaled approximately ±1% for operation at device operating temperature extremes above and below room temperature, respectively.

Power supply current requirements also vary depending on $V_{DD}$ supply voltage levels. Figure 7 shows variation of supply current depending on $V_{DD}$ voltage levels. This data can be used to determine the scale factor that is applied to the total current calculated for any given period of device activity.

Effects due to temperature and $V_{DD}$ are the final factors to be applied to current values for any given period of unique device activity. Once this is done, actual current levels for each period of device activity are produced, and average current for the entire duration of device operation can then be calculated, as described in the following sections.

**Figure 7. $I_{DD}$ Variation With $V_{DD}$**




### Total Current Calculation Equation

The relationships that characterize device power supply current requirements can be summarized in the following equation:

$$I_{tot} = (I_{int} + I_{add} + I_{data} + I_{cntl}) \times V \times T$$

where,

$I_{tot}$ is the total $I_{DD}$ supply current for a given sequence of device activity, with

$I_{int}$ $= (I_{prog} + I_{rpt} + I_{clk}) \times F_{cpu}$

$I_{add}$ $= I_{amax} \times D_{add} \times F_{add} \times C_{add}$

$I_{data}$ $= I_{dmax} \times D_{data} \times F_{data} \times C_{data}$

$$I_{cntl} = \sum_{n=1}^{N} C_n \; V_n \; F_n$$

$n$ is the total number of significant single outputs,

$V$ is the scale factor due to supply voltage, and

$T$ is the scale factor due to temperature

Table 2 describes the symbols used in the power supply current equation. The table also displays the figure number or page number, etc., where the value can be obtained.

**Table 2. Current Equation Symbols**

| | Symbol | Description | Value |
|---|---|---|---|
| $I_{int}$ | $I_{prog}$ | Program Activity Current | Table 1 |
| | $I_{rpt}$ | Repeat Scale Factor | Figure 2 |
| | $I_{clk}$ | Clock Oscillator Component | See page 8 |
| | $F_{cpu}$ | CPU Clock Frequency Scale Factor | Figure 4 |
| $I_{add}$ | $I_{amax}$ | Maximum Address Output Current | 64 mA |
| | $D_{add}$ | Address Bus Value Scale Factor | Figure 6 |
| | $F_{add}$ | Address Bus Switching Frequency Scaling | Figure 4 |
| | $C_{add}$ | Address Bus Load Capacitance Scaling | Figure 5 |
| $I_{data}$ | $I_{dmax}$ | Maximum Data Bus output Current | 32 mA |
| | $D_{data}$ | Data Bus Value Scale Factor | Figure 6 |
| | $F_{data}$ | Data Bus Switching Frequency Scaling | Figure 4 |
| | $C_{data}$ | Data Bus Load Capacitance Scaling | Figure 5 |
| $I_{cntl}$ | $C_n$ | Control Line *n* Load Capacitance | See page 11 |
| | $V_n$ | Control Line *n* Switching Voltage | See page 11 |
| | $F_n$ | Control Line *n* Switching Frequency | See page 11 |
| | V | $V_{DD}$ Supply Voltage Scale Factor | Figure 7 |
| | T | Temperature Scale Factor | See page 12 |

Note that the frequency scaling factors $F_{cpu}$, $F_{add}$, and $F_{data}$ are used in the same way as shown in Figure 4, however, they should be applied relative to the reference frequency for the quantity being scaled. Figure 4 shows a reference frequency of 20 MHz — applicable for scaling CPU values — however, scaling values for address, data, control, etc., should be applied for their own particular reference frequency. Using this technique yields the same scale factor as using the equivalent relationship $f_x/f_{ref}$. Thus, the scale factor can be calculated as:

$$scale\ factor = f_x/f_{ref}$$

where,

$f_x$ is the actual switching frequency, and

$f_{ref}$ is the appropriate reference frequency.

For example, in calculating the scale factor for the address bus switching at 5 MHz instead of 10 MHz, Figure 4 would yield a scale factor of 0.5 reading from a frequency of 20 MHz to 10 MHz because these frequencies are related by a factor of 2.

Using the above equation, the same scale factor is calculated as follows:

$$f_x/f_{ref} = 5\ MHz/10\ MHz = 0.5$$

This approach is often preferrable since it yields a more general solution to frequency scaling issues.

### Calculation of Average Current

If power supply current is observed over the full duration of device activity, different segments of activity will exhibit different levels of current required for different lengths of time. For example, a program may spend 80% of its time performing internal operations and drawing a current of 70 mA but spend the remaining 20% of its time performing writes at full speed to an external device drawing 110 mA.

While identifying peak current levels is important in order to establish power supply requirements, determining average current is often more important. This is particularly significant if periods of high peak current are short in duration. Average current can be obtained by performing a weighted summation of the currents due to the various independent program segments over time. In the example just mentioned, the average current can be calculated as follows:

$$I = 0.8 \times 70\ mA + 0.2 \times 110\ mA = 78\ mA$$

### Thermal Management Considerations

Heating characteristics of the TMS320C5x device are dependent upon power dissipation, which in turn is dependent upon power supply current. When making thermal management calculations, several considerations must be made that relate to the manner in which power supply current contributes to power dissipation and to the TMS320C5x thermal characteristics' time constant.

Depending on sources and destinations of current on the device, some current contributions to $I_{DD}$ do not constitute a component of power dissipation at 5 volts. Accordingly, if the total current flowing into $V_{DD}$ is used to calculate power dissipation at 5 volts, excessive values for power dissipation are obtained. Power dissipation is defined as:

$$P = I \times V$$

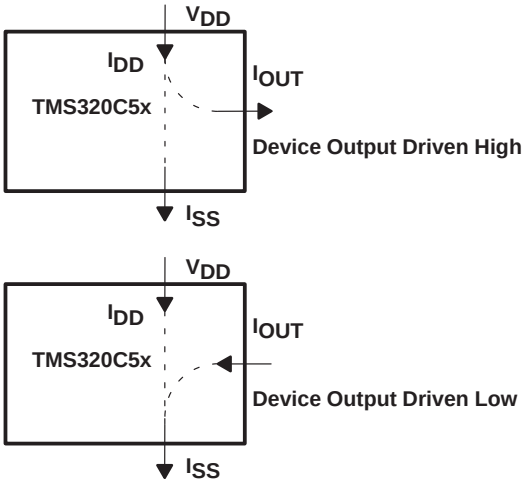
where $P$ is power, $I$ is current, and $V$ is voltage. If device outputs are driving any DC load to a logic high level, only a minor contribution is made to power dissipation because CMOS outputs typically drive to a level within a few tenths of a volt of the power supply rails. If this is the case, these current components should be subtracted out of the total supply current value, and their contribution to power dissipation calculated separately and then added to the total power dissipation (see Figure 8). If this is not done, these currents resulting from driving a logic high level into a DC load causes unrealistically high power dissipation values. The error occurs because the currents resulting from driving a logic high level into a DC load appears as a portion of the current used to calculate power dissipation due to $V_{DD}$ at 5 volts.

Furthermore, external loads draw supply current only when outputs are being driven high, because when outputs are in the logic zero state, the device is sinking current supplied from an external source. Therefore, the power dissipation due to outputs being driven low does not have a contribution through $I_{DD}$, but does contribute to power dissipation with a magnitude of:

$$P = Vol \times Iol$$

where *Vol* is the low level output voltage and *Iol* is the current being sunk by the output as shown in Figure 8. The power dissipation component due to outputs being driven low should be calculated and added to the total power dissipation.

**Figure 8. Device I/O Currents**




When outputs with DC loads are switched, the power dissipation components from outputs being driven high and outputs being driven low are averaged and added to the total power device power dissipation. Calculating power components due to DC loading of the outputs should be made separately for each independent and unique period of device activity before average power is calculated.

When using power dissipation values to determine thermal management, the average power should be used unless the time duration of individual periods of device activity is long. The thermal characteristics of the TMS320C5x package are exponential in nature with a time constant on the order of several minutes. Therefore, when the device is subjected to a change in power, the package temperature will require several minutes or more to reach thermal equilibrium. If the time duration of periods of device activity exhibiting high power dissipation values is short (on the order of a few seconds or less) in comparison to the package thermal characteristics' time constant, the average power, calculated in the same manner as average current described previously, should be used.

Maximum device temperature should be calculated on the basis of actual time duration for the periods of device activity involved. For example, if a particular device activity lasts for 12 minutes, the device essentially reaches thermal equilibrium due to the total power dissipation during the period of device activity.

Note that the average power should be determined by calculating the power for each period of device activity (including all considerations described above) and performing a time average of these values, rather than simply multiplying the average current by $V_{DD}$, as determined in the previous subsection.

Specific device temperature calculations can be made using the thermal impedance characteristics included in the TMS320C5x data sheet in the *TMS320C5x User's Guide* (literature number SPRU056B).

## Power Calculation Example

Filtering is a common operation in DSP applications. In order to illustrate the techniques described earlier in this document, this section presents an FIR filter routine as an example of a typical power dissipation calculation. The example program reads in data and coeffecients from external memory, performs an FIR filter calculation executing from internal memory, and writes out a table of results to external memory. This illustrates most of the significant aspects of device power requirements as described in the previous sections of this document. A listing of the program is provided in Appendix A.

### Data and Coefficient Input

Data and coefficients are read from a 1K-word block of external memory. The coefficients are in the first half of the block (512 words), and the data is in the second half of the block. For the read operation involved in this transfer, each of the four components of power supply current (control, data, internal, and address) must be considered.

During this period, most control outputs are inactive except CLKOUT1 and $\overline{RD}$. Both of these signals are heavily capacitively loaded and switching at 20 MHz, so calculating $C \times V \times F$ yields 16-mA total current for the two outputs. Data is *only* being read and *not* being written, so the data output component is zero.

Because a block data transfer is being performed involving the internal device memory and buses, and a significant data value variation is involved, the internal current component is nearly the maximum value for internal data transfers of 57 mA. This current value accounts for one internal bus being used heavily, and one internal bus being used minimally.

The address output component in this case is small due to the fact that on the average only two address lines switch each cycle during the reads. Scaling the 64-mA maximum address output current by 0.125 (2/16) yields 8 mA at maximum capacitive loading. The sum of these four components for the period of device activity during the external read operation yields a total of 81 mA.

### Processing

The processing portion of the program consists of single register load operation as initialization for the filter and then a repeat/MACD instruction pair which repeats the MACD instruction implementing the FIR filter function.

As with the data read portion of the program, most of the control outputs are inactive, and during the processing portion of the program, only CLKOUT1 is active; $\overline{IAQ}$ is inactive because repeat is being used to perform the sequence of MACDs implementing the filter. The current required for the fully loaded CLKOUT1 signal at 20 MHz is calculated to be 8 mA,using CVF.

During the processing portion of the program no external writes are being performed, therefore, the data output component of power supply current is zero.

The internal power supply current is the dominant component during the processing portion of the program. The actual implementation of the filter function is achieved using a repeat of a MACD instruction. As described previously, the current required for this operation when executing in full parallel is 90 mA with maximum data variation. With this program, the MACD operands are both obtained from the same block of memory, reducing the effective data transfer bandwidth by a factor of 50% since full parallelism cannot be achieved in this case. Applying this consideration to the 90-mA maximum value yields a calculated value of 45 mA required for internal current.

Because the initialization portion of the program sets the AVIS bit and clears the address bus, and no external bus cycles are performed, the address output component of power supply current is zero.

The sum of these four components for the period of device activity during the internal processing operation yields a total of 53 mA.

### Data Output Operation

The data output operation writes 512 words to an external block of memory.

The external control signals active during the data output portion of the program are CLKOUT1, $\overline{\text{STRB}}$, and $\overline{\text{WE}}$. The current required for the $\overline{\text{STRB}}$ and $\overline{\text{WE}}$ is calculated using CVF. Both these signals are switching at a frequency of 10 MHz and are heavily loaded, yielding a current requirement of 4 mA for each output. The current required for the CLKOUT1 output is 8 mA, the same as calculated for the previous two portions of the program. This yields a total calculated control supply current of 16 mA for these three outputs.

During the output portion of the program, the data bus is being driven by the processor. Because the maximum switching rate for the data bus outputs at a CLKOUT1 rate of 20 MHz is 5 MHz, to calculate the actual supply current required, the 64 mA maximum current per 16-bit bus is first reduced by 50% to 32 mA. Furthermore, since in this application the data bus is only loaded at 40 pF, rather than 80 pF, this reduces the calculated required current by another factor of 50% to 16 mA.

For the internal power supply current component, the write output rate of two cycles per write slows down the internal data transfer rate. This therefore reduces the internal component for this operation from 57 mA to approximately 49 mA.

The address component calculation for the data output portion of the program is the same as the calculation for the input portion of the program with the following exception. The switching rate for the address bus is only half that of the input portion since write operations require two cycles, whereas read operations require one cycle. This reduces the current required to drive the address bus outputs by a factor of 50%, in this case, in comparison with the data input case. This yields a value of 4 mA required for the address bus outputs.

The sum of these four components for the period of device activity during the data output operation yields a total of 85 mA.

The calculated values for all four current components are summarized in Table 3.

**Table 3. Sample Program Current Calculation Summary**

| | Read | Processing | Write |
|---|---|---|---|
| **Control** | 16 mA | 8 mA | 16 mA |
| **Data** | 0 | 0 | 16 mA |
| **Internal** | 57 mA | 45 mA | 49 mA |
| **Address** | 8 mA | 0 | 4 mA |
| **Total** | 81 mA | 53 mA | 85 mA |

### Average Current

The execution time for the complete program including all three segments of device activity is 175 μs; the input operation requires 50 μs, the calculation operation requires 75 μs, and the output operation requires 50 μs. Calculating a weighted sum of these values yields the average current for this program as follows:

$$Iavg = (0.29)(81\ mA) + (0.43)(53\ mA) + (0.29)(85\ mA) = 71\ mA$$

From the thermal characteristics specified in the *TMS320C5x User's Guide*, and assuming the use of the 132-pin PLCC package, it can be shown that this current level meets the maximum device case operating temperature specification of 85° C (with an ambient operating temperature of 70° C), and therefore, requires no forced-air cooling.

### Experimental Results

In order to confirm the values of current calculated for the sample program, the actual power supply current for this filter routine was measured using the test setup described at the beginning of this document. During the data input operation, the current measured was 79 mA. During the processing portion of the program, the current measured was 54 mA. During the output portion of the program, the current was 87 mA. The example power supply current calculations yielded results that were extremely close to the actual measured power supply current values.

A listing of the sample program used and a photograph of the actual current waveforms observed during its operation are contained in Appendix A of this document.

## System Design for Minimum Power Dissipation

Knowledge of CMOS device current requirements, and device and system considerations that affect them, can be utilized to develop concepts which can be used to design systems that exhibit the lowest possible power dissipation.

Designing systems for minimum power dissipation involves minimizing device operating current requirements due to signal switching rate, capacitive loading, and other effects. Selective consideration of these effects allows system performance to be optimized while utilizing the lowest power possible. This section describes current reduction techniques based on device operating current dependencies discussed in previous sections of this document.

### System Clock and Signal Switching Rates

Since current (and therefore power) requirements of CMOS devices are directly proportional to switching frequency, one potential approach to minimizing operating power is to minimize system clock frequency and signal switching rates. Although performance is often directly proportional to system clock and signal switching rates, tradeoffs can be made in both these areas to optimize power/performance tradeoffs in the design of a system.

If power is of primary concern, and a given system design does not have particularly demanding performance requirements, the system clock rate can be reduced with the corresponding savings in power. Minimum power is realized when system clock rates are only as fast as is necessary to achieve required system performance. Additionally, if overall system clock rates cannot be reduced, an alternative power reduction approach is to reduce clock speed wherever possible during periods of inactivity. Note that if the divide-by-one clock input is being used, its minimum input clock frequency specification must be observed for proper device operation.

Also, the appropriate choice of clock generation approach will insure minimum system power dissipation. The use of an external oscillator rather than the on-chip oscillator can result in lower device and system power dissipation levels. As described previously, the internal oscillator can require as much as 10 mA when operating at 40 MHz. If an external oscillator that requires less than 10 mA is used for clock generation, overall system power is reduced. This can result in significant power savings especially if the divide-by-one clock input is used.

When considering switching rates of signals other than the system clock, the main consideration is that switching should be minimized. Specifically, any unnecessary switching should be avoided. Outputs or inputs that are unused should either be disabled, tied high, or grounded, whichever is appropriate. Additionally, outputs connected to external circuitry should drive other power dissipating elements only when absolutely necessary.

Another straightforward mechanism that can result in significant device power savings is the use of the AVIS control bit feature. This feature allows switching of the external address bus to be disabled when external bus cycles are not being performed. Therefore, when executing out of on-chip memory, the power required to switch the address bus is saved.

### Capacitive Loading of Signals

Similar to considerations related to switching rates, current requirements are also directly proportional to capacitive loading. Therefore, all capacitive loading should be minimized. This is especially significant for device outputs.

The approaches to minimizing capacitive loading are also consistent with efficient PC board layout and construction practices. Specifically, signal runs should be as short as possible, especially signals with high switching rates. Also, signals should not be run long distances across PC boards to edge connectors unless absolutely necessary.

Note that buffering device outputs that must drive high capacitive loads reduces supply current for the TMS320C5x, but this current is translated to the buffering device. Whether or not this is a valid tradeoff must be made at the system level. The two main considerations regarding this are: 1) whether or not the power required by the buffers is more or less than the power required from the TMS320C5x to drive the load in question, and 2) whether or not offloading the power to the buffers has any implications with respect to system powerdown modes. It may be desirable to use buffers to drive high capacitive loads even though they may require more current than the TMS320C5x in cases where part of the system may be powered down but the TMS320C5x is still required to interface to other low capacitance loads.

### DC Component of Signal Loading

The internal and external DC load component of device input and output signal loading must also be minimized for lowest device current requirements.

Any device inputs that are unused and left floating may cause excessively high DC current to be drawn by their input buffer circuitry. This occurs due to the fact that, if an input is left unconnected, the voltage on the input may float to a level that causes the input buffer to be biased at a point within its range of linear operation. This can cause the input buffer circuit to draw a significant DC current directly from $V_{DD}$ to ground. Therefore, any unused device inputs should be pulled up to $V_{DD}$ using a resistor pullup of nominally 20 kilohms, or driven high with an unused gate. Input-only pins that are not used may be pulled up in parallel with other inputs of the same type with a single gate or resistor to minimize system component count. In this case, up to 15 or more standard device inputs may be pulled up with a single resistor.

Any device I/O pins that are unused should be selected as outputs, and be set low. This avoids the requirement for pullups to insure that the I/O input stage is not biased in the linear region and therefore eliminates an unnecessary current component.

If DC currents are being sourced from the address bus outputs and the AVIS feature is used to disable address bus switching when executing internally, the address bus outputs should be set to zeroes after the AVIS bit is set. This can be accomplished by performing a dummy read from program address zero after setting AVIS using the TBLR instruction.

For other device outputs that must drive high, any DC load present is directly reflected in the required power supply current. Therefore, DC loading of outputs should be reduced to a minimum.

For I/O pins that must be used in both the input and output modes, pullup resistors of nominally 20 kilohms should be used to insure minimum power dissipation if these pins are not always driven to a valid logic state. This is particularly true of the data bus pins that are I/Os and which are commonly used in both the input and output modes. At times when the bus is not being driven explicitly, it is left floating which can cause excessively high currents to be drawn on the input buffer section of all 16 bits of the bus. In this case, because all 16 data bus bits are normally used independently in most applications, each data bus pin should be pulled up with a separate resistor for minimum power.

### Use of Device Powerdown Modes

The TMS320C5x device has several powerdown modes that allow minimum system power dissipation. The most significant of these powerdown modes is implemented with the IDLE and IDLE2 instructions. The IDLE instruction halts CPU activity while still maintaining clocks to the internal device circuitry, and allows peripherals such as the serial ports to continue operation. The use of the IDLE instruction can save significant power in the system while still maintaining operation of critical portions of the device logic.

The IDLE2 instruction also halts CPU activity, but in addition, deactivates clocks to all portions of the device except the actual clock generator itself. This achieves the lowest device power possible while still maintaining clocks to the device.

Because the TMS320C5x uses a fully static design, clocks may be stopped at any point during device operation for even lower power, while still maintaining the internal device state. Unless the IDLE2 instruction is being executed, however, this must be performed synchronously in order that input clock minimum pulse-width specifications not be violated. Violating these specifications can cause misclocking of internal logic and therefore potentially cause device malfunction.

When executing the IDLE2 instruction, clocks may be stopped totally asynchronously. Any misclocking which occurs is not propagated to the internal device logic, and therefore cannot cause any device malfunction. This greatly simplifies system design because circuitry is not required to accomplish a synchronous clock turn-on and turn-off. Therefore, simple gating of clock on and off may be used to accomplish this function.

In addition to the IDLE and IDLE2 powerdown functions, the timer and serial ports may be individually enabled or disabled through bits in their respective control registers. When disabled, these peripherals also enter low power modes, since switching stops when they are disabled. The serial ports are controlled by the XRST and RRST bits in the serial port control (SPC and TSPC) registers, and the timer is controlled by the timer start/stop (TSS) bit in the timer control register (TCR). Although these peripherals consume only small amounts of power, for minimum power dissipation, they should always be disabled when not used.

### Low Voltage Operation

Current requirements for the TMS320C5x devices are directly proportional to power supply voltage. Operating at lower supply voltage levels can save significant power in a system. As more devices operate at 3-volt $V_{DD}$ levels, low voltage system designs will become more feasible and offer unprecedented reductions in power supply current requirements.

TMS320C5x device current requirements vary linearly with $V_{dd}$ as shown in Figure 7. Therefore, to establish operating current requirement levels at $V_{dd}$ voltages other than 5 volts, the values at 5 volts are simply multiplied by $V_{dd}/5$ (or refer to Figure 7). Note that $V_{dd}$ variation also affects device logic levels, which must be accounted for in overall system design.

## Summary and Conclusion

The power supply current requirement for the TMS320C5x DSPs cannot be expressed simply in terms of operating frequency, supply voltage, and output load capacitance. A more complete specification — one based on device functionality — must be used to determine an accurate power supply current requirement. This application report presents the information necessary for an accurate analysis of power supply current requirements. These requirements are based on a knowledge of the various periods of device activity and their operation on the TMS320C5x in terms of internal and external activity. As devices become more complex, the approach presented in this document must be applied.

The power supply current requirements for the TMS320C5x DSPs depend on system parameters as well as device functionality. Dependencies related to system parameters are those due to operating frequency, supply voltage, output load capacitance, and operating temperature. The components of current related to device functionality are those due to internal device activity and external bus operations.

Taking into account the concepts involved in analysis of device power dissipation, system design may be performed proactively so that minimum device and system power dissipation is achieved. With the combination of a 40-MIPS operating rate and a super-low power dissipation design, the TMS320C5x generation of DSPs is the ideal solution for today's demanding applications.

# Appendix A

## Program Listing for FIR Filter Routine

```
        .mmregs
        .text
        B       START
        .sect   ”INIT”
START
        LACC    #0BEh           ; GENERATE PMST CONTENTS
        SAMM    PMST            ; LOAD PMST
        LACC    #08h            ; GEN. TIMER CTL CONTENTS
        SAMM    TCR             ; POWER DOWN TIMER
        ZAC                     ; Acc = >0000.
        SAMM    GREG            ; greg = >0000.
        SAMM    PDWSR           ; PGM/DATA S/W Wait States = 0.
        SAMM    IOWSR           ; I/O Port S/W Wait States = 0.
        SAMM    CWSR            ; Control S/W Wait States = 0.
*
*  LOAD PROGRAM INTO INTERNAL RAM B0
*
        CNFD                    ; B0 is Data Memory
        MAR     *,0             ; ARP=0
        LAR     0,#0100h        ; POINT ARO TO BO
        RPT     #PGMEND–PGMTOP  ; RPT FOR LENGTH OF PGM
        BLPD    #PGMTOP,*+      ; LOAD PGM TO DATA B0
        NOP                     ; PAD BEFORE CHANGING
        NOP                     ; CONFIGURATION
        CNFP                    ; SET B0 TO PROGRAM
        NOP                     ; PAD AFTER CHANGING
        NOP                     ; .....CONFIGURATION
        B       BEGIN           ; BRANCH INTERNAL
*
*  PROGRAM SEGMENT
*
        .asect  ”PROGRAM”,0FE00h
        label   PGMTOP
*
BEGIN                           ; READ COEFFS AND DATA
        SETC    XF              ; SET XF
        CLRC    XF              ; CLEAR XF
        MAR     *,7             ; POINT TO AR7
        LAR     AR7,#0800h      ; AR4=EXTERNAL ADDRESS
        RPT     #03FFh          ; REPEAT FOR 512 COUNTS
        BLDD    #02C00h,*+      ; LOAD RAM WITH DATA
*
        LDP     #0h             ; DP=0, AVIS IS OFF
        TBLR    TIM             ; READ LOC 0 TO SET ABUS=0
```

## Program Listing for FIR Filter Routine (Continued)

```
*************************************************************************
        LAR     AR7,#0BFFh      ;  POINT  TO  DATA
        RPT     #01FFh          ; RUN  FILTER
        MACD    #0800h,*-       ; START  FROM  BOTTOM
*************************************************************************
WRITE                           ; WRITE  DATA  TO  EXTERNAL
        MAR     *,7             ; POINT  TO  AR7
        LAR     AR7,#0A00h      ; AR7=INTERNAL  ADDRESS
        RPT     #01FFh          ; REPEAT  FOR  512  COUNTS
        BLDD    *+,#03000h      ; OUTPUT  DATA
        B       BEGIN           ; LOOP  PROGRAM
        .LABEL  PGMEND
        .END
```

**Figure 9. Actual Measured Current**