Application Report
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TMS320x281x to TMS320x280x Migration Overview

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ABSTRACT

This application report describes differences between the Texas Instruments TMS320x281x and the TMS320x280x/2801x/2804x DSPs to assist in application migration. While the main focus of this document is migration from 281x to 280x/2801x/2804x, users considering migrating in the reverse direction will also find this document useful. Functions that are identical in both devices are not necessarily included. All efforts have been made to provide a comprehensive list of the differences between the two device groups in the 28x generation.

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1 Introduction

The TMS320x281x, TMS320x280x, TMS3202801x and TMS3202804x devices are members of the C2000 DSP generation for use within embedded control applications. The TMS230x280x, 2801x and 2804x devices feature newly developed enhanced peripherals that are not available on the 281x devices. These new peripherals enable the firmware engineer to solve challenging control problems effectively.

For purposes of migration, these devices can be thought of in two groups:

1. TMS320x281x
2. TMS320x280x, TMS320x2801x and TMS320x2804x. In this document this group will be referenced as 280x/2801x/2804x.

As the focus of this document is to describe the differences between the two device groups, the descriptions are explained only to the extent of highlighting areas that require attention when moving an application from one device to the other. For a detailed description of features specific to each device, see the device specific data manuals and user guides available on the TI website. This report does not cover the silicon exceptions or advisories that may be present on each device. Consult the following silicon errata for specific advisories and workarounds:

- *TMS320F2810\F2811\F2812\TMS320C2810\C2811\C2812 DSP Silicon Errata* (SPRZ193)
- *TMS320R2811 and TMS320R2812 DSP Silicon Errata* (SPRZ226)
- *TMS320F280x, TMS320C280x, TMS320F2801x, and UCD9501 DSP Silicon Errata* (SPRZ171)

1.1 Abbreviations

The following abbreviations are used in this document:

- 281x: Refers to the TMS320x281x devices. For example, TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812, TMS320R2811 and TMS320R2812.
- 280x: Refers to the TMS320x280x devices. For example, TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2801 and TMS320C2802. The UCD9501 also falls into this category. The individual parts in this group are abbreviated 2809, 2808, 2806, 2802, 2801 and 9501.
- 2804x: Refers to the TMS320x2804x devices. For example, TMS320F28044 which is abbreviated as 28044.
- 2801x: Refers to the TMS320x2801x devices. For example, TMS320F28015 and TMS320F28016. Individual parts are abbreviated 28015 and 28016.
- 280x/2801x/2804x: Refers to the group of devices made up of TMS320x280x, TMS320x2801x and TMS320x2804x. For the purpose of migration, these three device families are very similar and can be thought of as one group.

For a full list of devices currently available within the 281x, 280x, 2801x and 2804x family, see the TI website.

2 Package and Pinout

The 281x and 280x/2801x/2804x DSPs are neither package nor pin-compatible. Any application being moved from 281x to the 280x/2801x/2804x will require a new board layout to accommodate the changes in pinout and package.

3 Operating Frequency and Power Supply

The required core voltage supply for the 281x devices depends on the operating frequency of the device. The 281x devices can operate up to 150 MHz with a core voltage of 1.9 V. At 135 MHz and below, only a 1.8-V core voltage is required. The 280x/2801x/2804x devices require a 1.8 V core voltage at all operating frequencies with a top operating frequency of 100 MHz. Some of the 280x and 2801x devices are also available in a 60 MHz version. Both the 281x and 280x/2801x/2804x devices require a 3.3-V I/O supply.

See the following data manuals for the most recent detailed electrical specifications:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Processors Data Manual* (SPRS174)
- *TMS320F2809, F2808, F2806, F2802, F2801, F2801x UCD9501, C2802, C2801 Digital Signal Processors Data Manual* (SPRS230)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)

4 Power Sequencing

The restrictions placed on power sequencing have been relaxed. For the 281x devices, the power sequencing requirements dictate that the 3.3-V rail must begin its ramp prior to the 1.8-V (or 1.9-V) rail. For 280x/2801x/2804x devices, the 3.3-V and 1.8-V rail can instead ramp together. For customers migrating their design from the 281x, the sequencing scheme used for the 281x devices can still be applied to a 280x/2801x/2804x device.

See the appropriate data manual for each device for details related to power sequencing:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811,TMS320C2812 Digital Signal Processors Data Manual* (SPRS174)
- *TMS320F2809, F2808, F2806, F2802, F2801, F2801x UCD9501, C2802, C2801 Digital Signal Processors Data Manual* (SPRS230)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)

5 Memory Map

The memory map of the 280x/2801x/2804x devices is similar to that of the 281x except for the changes described in this section.

5.1 SARAM

The H0 SARAM block was moved from memory location 0x3F 8000 on 281x to 0x3F A000 and is also dual mapped in low memory at 0x00 A000. In addition, L0 and L1 are also dual mapped in both low and high memory on 280x/2801x/2804x devices as shown in Table 1. On the 281x devices, these memory blocks are only mapped to one memory region.

Table 1. SARAM Addresses

Block	281x Single Mapped Address	280x/2801x/2804x Dual Mapped Address	
L0	0x00 8000 – 0x00 8FFF	0x00 8000 – 0x00 8FFF	0x3F 8000 – 0x3F 8FFF
L1	0x00 9000 – 0x00 9FFF	0x00 9000 – 0x00 9FFF	0x3F 9000 – 0x3F 9FFF
H0	0x3F 8000 – 0x3F 9FFF	0x00 A000 – 0x00 BFFF	0x3F A000 – 0x3F BFFF

Moving the H0 memory and dual mapping of memory blocks creates a continuous 16K block of SARAM memory for applications requiring large data structures. The dual mapping of the memory gives flexibility when partitioning it as required by the application. The memory region in the upper 64K range is required when running 24x compatible code while the stack pointer (SP) can only access memory in the lower 64K.

When migrating from the 281x devices, the memory map used by the compiler must be updated to reflect these changes and the code rebuilt. The H0 memory block moved and L0 and L1 are now dual mapped in its place. Thus, if code compiled for 281x is loaded without changing the memory map, data or code that was originally in the memory region 0x3F 8000 – 0x3F 9FFF may be overwritten by the data or code from the L0 and L1 memory blocks.

Not all of the SARAM blocks are available on all family derivatives. Table 2 summarizes the SARAM memory available on each device in the 280x/2801x/2804x family. Refer to the device specific data sheet for further details.

Table 2. SARAM Memory Per Device

Device	H0 (8K X 16)	L1 (4K X 16)	L0 (4K X 16)
281x	Yes	Yes	Yes
2809	Yes	Yes	Yes
2808	Yes	Yes	Yes
2806	No	Yes	Yes
2802	No	No	Yes
2801/9501	No	No	Yes
28044	No	Yes	Yes
28015	No	No	Yes
28016	No	No	Yes

5.2 Flash and OTP

The size and number of sectors has changed and code must be rebuilt accordingly. The exact flash size as well as sector configuration varies from device to device as shown in Table 3.

Table 3. Sector Configuration Per Device

	F2812 F2811	F2810	F2809	F2808 F28044	F2806 F2802	F2801 9501 F28016 F28015
	6 Sectors 16K X 16 + 4 sectors 8K X 16	3 Sectors 16K X 16 + 2 sectors 8K X 16	8 Sectors 16K X 16	4 Sectors 16K X 16	4 Sectors 8K X 16	4 Sectors 4K X 16
Total	128K X 16	64K X 16	128K X 16	64K X 16	32K X 16	16K X 16

The 128-bit code security module (CSM) password location (0x3F 7FF8-0x3F 7FFF) Flash boot ROM entry point (0x3F 7FF6) and OTP boot entry point remain at the same location. The access time of the flash, and thus the required wait states at a given frequency are compatible between all of the devices shown in Table 3. Always refer to the device specific data manual for the most recent timing information.

The Flash API and programming algorithms for the F281x devices cannot be used on the F280x/F2801x/F2804x. New Flash APIs are required in order to program these devices . The Flash API function prototypes, however, remain compatible.

5.3 External Memory Interface (XINTF)

The XINTF is not available on any of the 280x/2801x/2804x devices.

5.4 BOOT-ROM

The boot ROM has been updated to include boot loaders for the I2C-A module and the eCAN-A module. The boot mode pin configuration has changed to enable the different boot loaders and is shown in Table 4. You must configure each of the 3 pins before reset in order for the boot loader to properly start. The data stream format used is identical to that used on the 281x devices.

Table 4. 280x/2801x/2804x Boot Loader Selection

	GPIO18 SPICLKA SCITXB	GPIO29 SCITXDA	GPIO34
Jump to Flash 0x3F 7FF6	1	1	1
Call SCI-A boot loader	1	1	0
Call SPI-A boot loader	1	0	1
Call I2C-A boot loader	1	0	0
Call eCAN-A boot loader (1)	0	1	1
Jump to M0 SARAM 0x00 0000	0	1	0
Jump to OPT	0	0	1
Parallel GPIO Loader	0	0	0

(1) On devices without an eCAN-A module, this mode is reserved and should not be used.

The location of the “boot to SARAM” entry point location has changed from the H0 memory block to the starting address of M0 at 0x00 0000. The entry points into the Flash memory block and the OTP memory block have not changed.

See the following reference guides for more information on Boot ROM:

- *TMS320x281x Boot ROM Reference Guide* (SPRU095)
- *TMS320x280x, 2801x, 2804x Boot ROM Reference Guide* (SPRU722)

6 Clocks and System Control

This section describes changes that affect device clocking and system control. This includes new and renamed registers, pin functionality, new logic, and other enhancements. For more information on system control, see the following reference guides:

- *TMS320x281x System Control and Interrupts Reference Guide* (SPRU078)
- *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712)

6.1 Register Changes

Table 5 shows a summary of registers that were added, renamed, or modified from the 281x devices. The sections following further describe changes that were made. This section does not include the new ePWM, eCAP, and eQEP registers as they can be considered as all new.

Table 5. New, Renamed, and Removed Registers

Register	Change	Description
XCLK	New	XCLKOUT Register. Used to control the XCLKOUT frequency, disable XCLKOUT, and read the current state of the XCLKOUT pin.
PLLSTS	New	PLL Status Register. Includes the PLL lock status bit and information from the missing oscillator-detect logic.
PCLKCR0	Renamed Updated	This register is named PCLKCR on the 281x devices. Bits have been added to enable clocks to new peripherals.
PCLKCR1	New	New register used to enable/disable clocks to the ePWM, eCAP, and eQEP modules.
PCLKCR2	New	New register used to enable/disable clocks to the ePWM modules (2804x only).
LPMCR0	Updated	Updated so you can enable the watchdog interrupt to wake the device from STANDBY mode. On 281x this bit is in the LPMCR1 register.

Table 5. New, Renamed, and Removed Registers (continued)

LPMCR1	Removed	This register is replaced by the GPIOLPMSEL register located in the GPIO register file.
GPIOPLMSEL	New	Selects the GPIO signal that can wake the device from HALT and STANDBY.
GPAMCFG	New	Selects the pinout configuration for the ePWM modules (2804x only).

6.2 Input Oscillator

Separate XCLKIN and X1 pins

The pins X1 and X2 are 1.8-V pins on both the 281x and 280x/2801x/2804x devices. On 281x devices, if an external 3.3-V oscillator is used, the input clock has to be level shifted before it can be sent into the device. This requirement has been removed by providing a separate 3.3-V XCLKIN pin. If a crystal is not used, an external oscillator can be connected to the XCLKIN pin and the X2 pin can be left unconnected.

Oscillator Missing Detect Logic

Logic has been added to detect whether the main oscillator clock is missing. If neither XCLKIN or X1 has a clock and therefore the oscillator clock is missing, the device switches to a “limp mode” frequency output by the PLL and resets.

6.3 Phase Locked Loop (PLL)

PLL Lock Status Bit

When a new PLL ratio is selected in the PLL control register (PLLCR), there is a required number of cycles that must pass before the PLL locks at the new frequency. A PLL lock status bit has been added to the PLL status register (PLLSTS) to indicate when the PLL has locked. On the 281x devices, a software delay is used to wait for these cycles to pass.

PLL Disable and PLL OFF

On the 281x devices, the XF_PLLDIS signal is sampled at reset and, if found to be low, the PLL on the device is disabled. On the 280x/2801x/2804x devices, the XF_PLLDIS signal is no longer available. Instead, to disable the PLL, a bit has been added to turn off the PLL for system noise and low power operation when the PLL is not required. To use this feature, the PLL must first be in bypass mode (PLLCR = 0x0000).

Procedure to Change PLLCR

With the introduction of oscillator-missing-detect logic, the procedure to change the PLLCR register has changed slightly. On the 280x/2801x/2804x, the missing clock status must be checked before changing the PLLCR register. If the status bit is set (missing clock detected) appropriate action must be taken by the firmware. If a missing clock has not been detected, then the PLLCR can be modified by the following sequence:

1. Disable oscillator missing detect logic.
2. Modify PLLCR register.
3. Wait for PLL lock status to indicate that the PLL has locked.
4. Re-enable the oscillator-missing-detect logic.

6.4 Peripheral Clock Enable Registers

Due to new peripherals and additional instances of old peripherals, the registers to enable and disable the clocks to individual peripherals have been updated. On the 281x devices there is one peripheral clock control register named PCLKCR. There are now additional registers (PCLKCR0, PCLKCR1 and PCLKCR2) that enable and disable the clocks to the individual peripheral modules.

6.5 XCLKOUT

XCLKOUT can be configured to be a divide-down of the system clock SYSCLKOUT instead of using the external interface (XINTF) clock (XTIMCLK). There is no XINTF, therefore the XTIMCLK domain is not present on the 280x/2801x/2804x devices.

6.6 Low Power Modes: STANDBY and HALT Wake Up Signal Selection

On 280x/2801x/2804x devices, you can enable any input signal corresponding to pins GPIO0 through GPIO31 to wake up the device from the STANDBY and HALT low-power modes. the selected pin or pins can be configured either as general-purpose inputs (GPIO) or as peripheral inputs. While more than one signal can be specified, but typically only one will be used. The signal selection is made in the GPIOLPMSEL register. On the 281x, only a select few signals can wake the device from STANDBY and only the XNMI and $\overline{\text{XRS}}$ signals can wake the device from HALT mode.

7 Peripherals

New peripherals have been added and others have been updated. This section briefly describes the changes. For an overview of all peripherals available see the *TMS320x28xx, 28xxx Peripherals Reference Guide* (SPRU566).

7.1 New Peripherals

The 280x/2801x/2804x devices include new peripherals that are not available on the 281x devices.

7.1.1 Control Peripherals

The Event Manager (EV) module on the 281x devices was originally developed for the 240x DSPs. This module has been removed on 280x/2801x/2804x devices and the functionality has been replaced by three new peripherals: ePWM, eCAP and eQEP. The peripherals available per device are shown in Table 6. Each of the 280x/2801x/2804x control peripherals are described in the following section.

Table 6. Available Communication Peripherals

Device	Event Manager	(1)ePWM With High Resolution (HRPWM)	ePWM	eCAP	eQEP
281x	EV-A, EV-B	-	-	-	-
2809	-	ePWM1 - ePWM6		eCAP1 - eCAP4	eQEP1, eQEP2
2808	-	ePWM1 - ePWM4	ePWM5, ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2
2806	-	ePWM1 - ePWM4	ePWM5, ePWM6	eCAP1 - eCAP4	eQEP1, eQEP2
2802	-	ePWM1 - ePWM3		eCAP1, eCAP2	eQEP1
2801/9501	-	ePWM1 - ePWM3		eCAP1, eCAP2	eQEP1
28044	-	ePWM1 - ePWM16		-	-
28016	-	ePWM1 - ePWM4		eCAP1, eCAP2	-
28015	-	ePWM1 - ePWM4		eCAP1, eCAP2	-

(1) The High Resolution extension (HRPWM) is available on the A channel output of the ePWM module. The B channel has normal ePWM control.

- **Enhanced Pulse Width Modulator (ePWM) Module**

  The ePWM peripheral is used to control many power-related systems in both commercial and industrial equipment. The main systems include digital motor control, switch mode power supply control, uninterruptible power supplies (UPS) and other forms of power conversion. The ePWM can perform a DAC function where the duty cycle is equivalent to a DAC analog value sometimes referred to as a power DAC.

  Each ePWM module on a device is daisy-chained together via a synchronization scheme that allows them to operate as a either individual units or as a single system if required. Details of the ePWM module can be found in the *TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module*

Reference Guide (SPRU791).

Table 7 shows an overview of the ePWM resources available on the 2808 as compared to that of the 281x event manager (EV).

Table 7. 2808 ePWM Compared to 281x Event Manager

	2808 ePWM	281x EV-A, EV-B
Timers	16-bit x 6	16-bit – x2 (EV-A), x2 (EV-B) (shared with PWM, CAP, QEP)
PWM	12 independent 16-bit + 4 independent (eCAP in APWM mode)	10 independent 16-bit
High-Resolution PWM Control	4 EPWMxA Channel Outputs	No
Compare	2 per time-base	1 per time-base
Time-Base Sync	Yes	No
Phase Control	Yes	No
Dead-Band	10-bit Independent falling edge delay Independent rising edge delay	~7-bit Rising edge = falling edge delay
Chopper	Yes	No
Trip (Fault) Zones	6 Assign to any PWM module Cycle-by-cycle or one-shot Can force PWM pins high, low, or high-impedance on trip	6 Hard-wired to a specific PWM Forces high-impedance on trip
Interrupts	6 Can be pre-scaled to all, second, or third event	24 no pre-scaling
ADC Start of Conversion	Counter = zero, period, compare A, compare B	Counter = zero, period, and compare of TxPWM only

Some ePWM instances on the 280x/2801x/2804x include a high-resolution extension. The high-resolution PWM (HRPWM) module extends the time resolution capabilities of the conventionally derived digital pulse width modulator (PWM). HRPWM is typically used when PWM resolution falls below ~ 9-10 bits. This occurs at PWM frequencies greater than ~200 kHz when using a CPU/system clock of 100 MHz. Details of the HRPWM module can be found in the *TMS320x28xx, 28xxx High-Resolution Pulse Width Modulator (HRPWM) Reference Guide* (SPRU924).

The key features of HRPWM are:

- Extended time resolution capability.
- Used in both duty cycle and phase-shift control methods.
- Finer time granularity control or edge positioning using extensions to the compare and phase registers.
- Implemented using the "A" signal path of the ePWM, i.e., on the EPWMxA output. The EPWMxB output has conventional PWM capabilities.
- Self-check diagnostics software mode to check if the micro edge positioner (MEP) logic is running optimally.

- **Enhanced Capture (eCAP) Module**

  The eCAP module is essential in systems where accurate timing of external events is important. When not being used to capture external events, the eCAP peripheral can be used to implement a single channel PWM generator. Table 8 shows a comparison of eCAP with EV.

Table 8. 2808 eCAP Compared to 281x Event Manager

	2808 eCAP	281x EV-A, EV-B
Timers	32-bit X 4	16-bit - X2 (EV-A), X2 (EV-B) (shared among PWM, CAP, QEP)
Channels	4 channels	3 channels shared with QEP
Timestamp	32-bit	16-bit
Capture buffers per channel	4 memory-mapped registers	2-level FIFO
Edge qualifier	4 total, one per buffer	1
Sequencer	Yes	No
Delta time mode	Yes	No
Absolute time mode	Yes	Yes
APWM mode	Yes	No
Event pre-scaler	Yes	No
Interrupts	4 Can be pre-scaled to all, second, or third event	6 No pre-scaling

Details of the eCAP module can be found in the *TMS320x28xx, 28xxx Enhanced Capture (eCAP) Module Reference Guide* (SPRU807).

- **Enhanced Quadrature Encoded Pulse (eQEP) Module**

  The eQEP module is used for interfacing to a linear or rotary incremental encoder in order to get position, direction, and speed information from a rotating machine in high performance motion and position control system. Table 9 shows a comparison of 2808 eQEP and 281x EV.

Table 9. 2808 eQEP Compared to 281x Event Manager

	2808 eQEP	281x EV-A, EV-B
Timers	32-bit X 2	16-bit - X2 (EV-A), X2 (EV-B) (shared among PWM, CAP, QEP)
Channels	2 channels 32-bit position counter	2 channels 16-bit shared counter
Speed measurement support	Yes Frequency and period based	No
Frequency measurement	Yes Unit timer	No
Position compare	Yes Position compare register	No
Shaft stall detect	Yes Built-in watchdog	No
Error checking	Yes Phase and count errors	No
External strobes	Index and home	Index
Interrupts	2 Can be pre-scaled to all, second, or third event	0

Details of the eQEP module can be found in the *TMS320x28xx, 28xxx Enhanced Quadrature Encoder Pulse (eQEP) Module Reference Guide* (SPRU790).

7.1.2 Inter-IC (I^2C) Bus

An I2C bus has been added to the 280x/2801x/2804x devices. This module is not available on the 281x.

7.2 Updated Peripherals

The following peripherals have been updated in the 280x/2801x/2804x devices and are documented in new reference guides specific to the 280x/2801x/2804x:

- *TMS320x280x, 2801x, 2804x Analog-to-Digital (ADC) Reference Guide* (SPRU716)
- *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712)
- *TMS320x280x, 2801x, 2804x Boot ROM Reference Guide* (SPRU722)

The 281x guides should be replaced with these guides if you are using a 280x/2801x/2804x device. The highlights of the changes made to these peripherals are detailed in this section.

Analog-to-Digital Converter (ADC)

The ADC on the 280x/2801x/2804x is different than that on the 281x in the following areas:

- RefP/RefM capacitors reduced from 10 μF on 281x to 2.2 μF on 280x, resulting in lower cost/smaller body size.
- RESEXT resistor reduced from 24.9 kΩ on 281x to a standard 22 kΩ 5% resistor.
- External reference option reduced to one pin, 2.048 V standard reference.
- Two main power pins moved from 3.3-V node to 1.8-V, cutting power consumption by half for analog block.
- Maximum sampling speed of 6.25 MSPS (half of 281x ADC) with the exception of the 2809 and 28044. On these two devices, the ADC sampling speed remains at 12 MSPS.
- Gain error reduced from +/-5 percent to +/- 1.5%.
- Added offset correction register (OFFTRIM) dynamically removes offset from ADC results.
- Result registers are dual mapped to zero wait state data space and are right justified for continuous run applications.
- Two new interrupts have been defined for the ADC to handle SEQ1 and SEQ2 interrupt conditions separately. The existing 281x ADCINT has been retained. Thus, you can choose to use either the ADC interrupt or the new SEQ1 and SEQ2 interrupts.

7.2.1 Code Security Module (CSM)

No functional changes were made to the CSM. This module protects the Flash, OTP, and L0/L1 SARAM blocks as it did on the 281x devices. On the 280x/2801x/2804x, the module was modified to protect both mappings of the L0 and L1 blocks of memory. The CSM password is still a 128-bit password programmed into 0x3F7FF8-0x3F7FFF of the flash.

Information on the CSM is included in the *TMS320x281x System Control and Interrupts Reference Guide* (SPRU078) and *TMS320x280x, 2801x, 2804x System Control and Interrupts Reference Guide* (SPRU712).

7.2.2 General-Purpose I/O (GPIO)

The GPIO ports have been completely redesigned to allow for a larger number of peripherals to be MUXed per pin. This allows you to pick and choose which peripherals to enable for your particular application. Changes to the GPIO module include:

GPIO Ports

On the 281x devices, GPIO signals are divided into 16-bit ports. On the 280x/2801x/2804x devices, the GPIO signals are assigned to 32-bit ports. Port A consists of GPIO0-GPIO31 and Port B consists of GPIO32-GPIO34. The GPIO control and data registers have been moved from peripheral frame 2 (16-bit access only) to peripheral frame 1 which allows for 32-bit as well as 16-bit operations on the registers.

GPIO MUX Registers

The GPIO MUX logic has been redesigned to allow for a higher level of peripheral multiplexing. The 280x/2801x/2804x GPIO MUX can multiplex up to three independent peripheral signals into a signal GPIO pin in addition to providing individual pin toggling I/O capability. There are two MUX registers for each GPIO port.

GPIO Qualification

On 280x/2801x/2804x devices, the type of qualification required for each incoming signal can be specified by you. Three options are available:

- Synchronization to the system clock (SYSCLKOUT) only. This is the default mode of all pins at reset.
- Qualified using a sampling window specified by window size and sampling period. The sampling window size is the number of times the signal must be sampled at the same level in order to be qualified. You can specify a sampling window size of either 6 samples or 3 samples for each of the GPIO signals. On the 281x device the sampling window size is fixed to 6 samples only.

  The qualification sampling period is or how often the signal is sampled within the sampling window. The sampling period is specified for each group of 8 signals. For example GPIO0-GPIO7 all use the same qualification sampling period. On the 281x device the sampling period is specified per 16-bit port.
- No synchronization applied. This mode is only valid when the pin is configured as an input to a peripheral.

On the 281x devices, the type of input qualification available depends on the function of the pin in its peripheral mode:

- 281x Type 1 qualification allows the signal to be qualified via a sampling window or synchronized to SYSCLKOUT. This applied to pins connected to the Event Manager (EV).
- In 281x Type 2 in the asynchronous signal is fed to the peripheral without qualification. This applies to pins that connected to communications ports such as SCI, SPI, and eCAN. In this case if these pins are used as GPIO, the input qualification defaults to synchronize to SYSCLKOUT only.

  The 280x/2801x/2804x input qualification is much more flexible then on the 281x. Users should take care, however, to select their input qualification. The default mode, synchronize to SYSCLKOUT, may not be desired for communication peripherals such as SCI, SPI, I2C and eCAN.

Internal Pullup Configuration

For each of the GPIO pins, you can enable or disable an internal pullup resister through software.

On the 281x devices, internal pullup resisters are included by default for specific input signals while other signals do not have an internal pullup. This is not configurable on the 281x devices.

External Interrupt Signal Selection

You can now assign a GPIO signal from Port A (GPIO0 – GPIO31) to be the interrupt source for XINT1, XINT2 and XNMI. On the 281x device, these are fixed signals. This selection is made in the GPIOXIN1SEL, GPIOXINT2SEL and GPIOXNMISEL registers.

Low-Power Mode Wake Up Signal Selection

You can now select signals from GPIO Port A (GPIO0-GPIO31) to wake up the device from the STANDBY and HALT low power modes. More then one signal can be specified, but typically only one will be used. The signal selection is made in the GPIOLPMSEL register. On the 281x only a select few signals can wake the device from STANDBY and only XNMI and $\overline{\text{XRS}}$ can wake the device from the HALT mode.

7.3 Unmodified Peripherals

The Serial Peripheral Interface (SPI) and the Serial Communications Interface (SCI) remain functionally the same as on the 281x devices. Only the title of the reference guide changed to include the new devices (i.e., *TMS320x28xx, 28xxx Serial Peripheral Interface Reference Guide*).The Enhanced Controller Area Network (eCAN) remains the same with the exception of the fixed errata mentioned in Section 9.

More instances of the SPI and eCAN communication peripherals are available on the 280x/2801x/2804x devices (see Table 10) than are available on the 281x. On the 281x one SPI module is available and now up to four are available. For the eCAN module, the 281x offers one instance while the 280x offers up to two.

Table 10. Available Communication Peripherals

Device	I2C	SCI Modules	SPI Modules	eCAN Modules
281x	-	SCI-A, SCI-B	SPI-A	eCAN-A
2809	I2C-A	SCI-A, SCI-B	SPI-A, SPI-B, SPI-C, SPI-D	eCAN-A, eCAN-B
2808	I2C-A	SCI-A, SCI-B	SPI-A, SPI-B, SPI-C, SPI-D	eCAN-A, eCAN-B
2806	I2C-A	SCI-A, SCI-B	SPI-A, SPI-B, SPI-C, SPI-D	eCAN-A
2802	I2C-A	SCI-A	SPI-A, SPI-B	eCAN-A
2801	I2C-A	SCI-A	SPI-A, SPI-B	eCAN-A
28044	I2C-A	SCI-A	SPI-A	-
28016	I2C-A	SCI-A	SPI-A	eCAN-A
28015	I2C-A	SCI-A	SPI-A	-

The register set for the SCI, SPI, and eCAN peripherals are identical on the 281x and the 280x/2801x/2804x. The memory addresses of the registers for the A instance of the SPI and eCAN peripheral are also identical. Likewise, the memory-mapping of the register set for both the A and B instance of the SCI peripheral are identical. In addition, the interrupt vector location in the PIE vector table is identical to that on the 281x for SCI-A, SCI-B, SPI-A and eCAN-A. New interrupt vectors have been added to the PIE vector table for the additional peripheral instances (SPI-B, SPI-C, SPI-D and eCAN-B).

Code that has been written for the SCI, SPI, and eCAN on the 281x can be directly targeted for the 280x/2801x/2804x with one exception. The GPIO setup for the peripheral must be updated to accommodate the new GPIO MUXing scheme.

7.4 Removed Peripherals

The following peripherals are available on the 281x devices but are not available on 280x/2801x/2804x derivatives:

- Multi-Buffered Serial Port (McBSP)
- External Memory Interface (XINTF)
- Event Manager (EV) - The Event Manager functionality has been replaced on 280x/2801x/2804x devices with three newly designed peripherals: ePWM, eCAP and eQEP.

8 Interrupts

Changes to interrupts include updates to the peripheral interrupt expansion (PIE) module and handling of external interrupts.

8.1 Peripheral Interrupt Expansion (PIE) Module

The PIE vector table has been updated to accommodate the interrupts issued by the new peripheral blocks – ePWM, eCAP, eQEP, I2C as well as multiple instances of the SPI, and eCAN peripherals.

Two new interrupts have been defined for the ADC to handle SEQ1 and SEQ2 interrupt conditions separately. SEQ1 has been assigned to INT1.1 and SEQ2 to INT1.2. The existing ADCINT has been retained. You can choose to use the ADC interrupt or the new SEQ1 and SEQ2 interrupts

The functionality of the PIE module and of the PIE configuration registers (PIEACK, PIEIFRx, PIEIERx etc.) is identical to the 281x devices.

8.2 External Interrupts

Selecting Interrupt Polarity

The polarity of the XINT1, XINT2 and XNMI interrupts can be configured three ways on the 280x/2801x/2804x devices:

- Positive edge triggered
- Negative edge triggered
- Both positive and negative edge triggered

  On the 281x devices configuring the polarity as both positive and negative edge triggered is not supported. This configuration is done in the XINT1CR, XINT2CR and XNMICR registers.

XNMI Interrupt Configuration

For the XNMCR register, the functionality for ENABLE = 1 and SELECT = 1 has been changed slightly. On the 281x devices, this configuration setting enables both the NMI and the INT13 interrupts to the CPU on 281x devices. This configuration has been changed to be more useful; when ENABLE = 1 and SELECT = 1, the following functionality occurs:

- NMI interrupt disabled
- INT13 connected to the GPIO Port A signal selected as the XNMI interrupt
- Time stamp counter enabled

External Interrupt Selection

You can now assign the interrupt source signal for XINT1, XINT2 and XNMI. Any GPIO signal from GPIO0 to GPIO31 can be selected as the interrupt source. On the 281x device, the signals are fixed. This selection is made in the GPIOXIN1SEL, GPIOXINT2SEL and GPIOXNMISEL registers that are part of the GPIO register set.

9 Errata Fixes

For more information on the various advisories, see the TI website for the most recent device specific silicon errata. This includes:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 DSP Silicon Errata* (SPRZ193)
- *TMS320R2811, TMS320R2812 DSP Silicon Errata* (SPRZ226)
- TMS320F280x, TMS320C280x, TMS320F2801x, and UCD9501 DSP Silicon Errata (SPRZ171)

The following 281x errata have been fixed:

- Analog-to-Digital Converter (ADC)
  - ADC - EOS BUF1/2 Bits in ADCST Corrupted at the End of Conversion of Sequencer 1/2 When INT MOD SEQ1/2 is Enabled
  - ADC - Reserved Bits in Autosequence Status Register (ADCASEQSR)
  - ADC Result Register Update
  - ADC Sequencer Reset While Dual Sequencers Are Running
- Enhanced Controller Area Network (eCAN)

  If contention existed between the CPU and the eCAN controller for access to certain eCAN register areas, then a CPU read may erroneously read all zeros (0x00000000) and a CPU write may fail to execute.
- Logic Level for XCLKIN Pin

  On 281x devices, when using an external oscillator to clock the device, the input level of the clock could not exceed V_{DD} rather then the 3.3-V I/O voltage. On the 280x/2801x/2804x devices, a separate XCLKIN pin has been provided to allow for a 3.3-V external input clock. The X1 pin remains as is and can be used along with X2 to connect a crystal.
- Serial Peripheral Interface (SPI) Slave Mode

  On the 281x, when in slave mode, the SPI does not synchronize received words based on $\overline{\text{SPISTE}}$ because a spurious clock pulse on SPICLK could throw the data stream out of sync. This has been corrected and when the SPI port is configured for slave mode, a high-to-low transition on the $\overline{\text{SPISTE}}$ signal always resets the bit counter state machine so that it is re-synchronized on every word transfer.
- Watchdog Timer Reset Flag

  The watchdog flag (WDFLAG) is used to determine if a reset is caused by the watchdog or an external reset. On the 281x devices, this flag is not reliable since the sampling window for the reset line is too short. On the 280x/2801x/2804x devices, the sampling interval has been increased to allow more time for the reset line to go high after a watchdog reset occurs.

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