OMAP3530 Easy CUS Package PCB Escape Routing

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ABSTRACT

The OMAP3530 CUS package is designed with a new technology called Via Channel™ array. This technology allows for easy routing of the device in two signal and two power layers using standard 20 mil diameter and 10 mil finished hole size via; it is cost and time effective. This application report shows how to easily route the entire package by first routing one quadrant only and then copying it to the rest of the device. For this purpose, the Allegro® layout tool was used; other tools could be used in a similar way.

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1   OMAP PCB Layout Technology

1.1   *Via Channel Layout Advantages*

Via Channel technology is a way of depopulating balls on the BGA chip package in a shape that makes it possible to have the vias concentrated in channels. This allows several advantages.

First, the via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the balls, since all of the vias are placed in special areas called via channels. This makes PCB manufacturing less expensive because 20/10 vias (vias with an outside diameter of 20 mils and a finished hole size of 10 mils) are possible.

Second, the vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of vias.

Figure 1 shows the resulting OMAP3530 footprint.
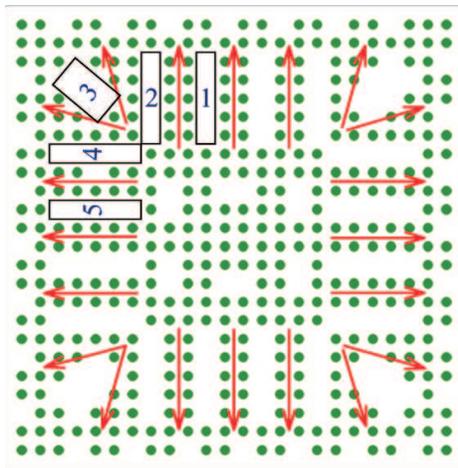
Figure 1. OMAP3530 Footprint With Via Channel Array

The unique outer row routing and the via channel inner routing are two important parts of this technology on the OMAP3530.

1.2   *Outer Row Routing*

For the first two rows (from the outside in) of the BGA array, the balls have been arranged to allow wider traces than would otherwise be possible. The first row (the outside row) supports any size trace desired, since the trace simply comes from the PCB ball land and goes out on the PCB. Normally, the second row traces must be routed in between the first row of the PCB ball lands. On this package, the second row traces are routed through an open channel where the BGA ball has been removed to allow wider traces. The OMAP3530 parts allow a 5 mil (0.125mm) trace/space in all areas, if routed correctly. To use the larger 20/10 via size, 4 mil traces are necessary.

> **NOTE:**   A layout using 5 mil traces is shown in *OMAP35x 0.65mm Pitch Layout Methods* (SPRAAV6) using slightly smaller 18 mil diameter vias with an 8 mil finished hole size.

Figure 2 shows the quadrant symmetry of the OMAP3530 CUS package. Because of this arrangement, routing could be completed on 1/4 of the device and then pasted over the other three.

A1
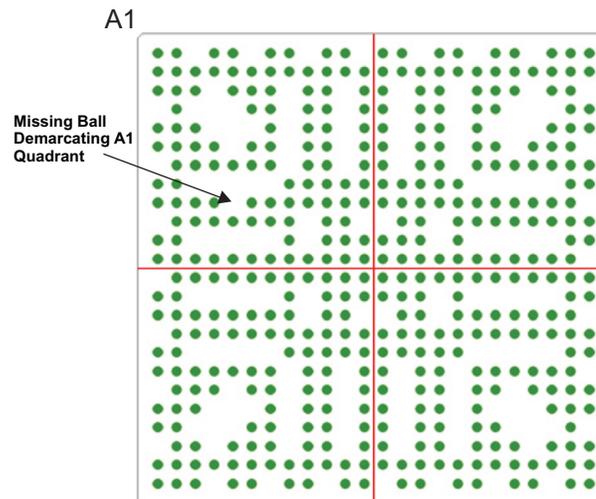
Figure 2. OMAP3530 Quadrant Symmetry

For clarity, the channels for the first quadrant will be numbered 1-5 with 3 being the corner channel.

Quadrants will be 1-4 in a CCW direction.

The printed circuit board (PCB) layout rules are as follows:

- 4 mil (0.125mm) maximum trace
- 20 mil (0.50mm) maximum via diameter
- 10 mil (0.25mm) maximum finished hole diameter

If done correctly, the results will be:

- No blind, stacked, buried, or micro vias necessary
- Only two signal layers needed

Each quadrant is identical to the next except for the top left quadrant, which is missing one pin to delimitate the A1 corner. This application report shows an easy method to route all signal pins and get from Figure 3 to Figure 4 in only a few steps. This involves copying sections and pasting them to minimize effort.
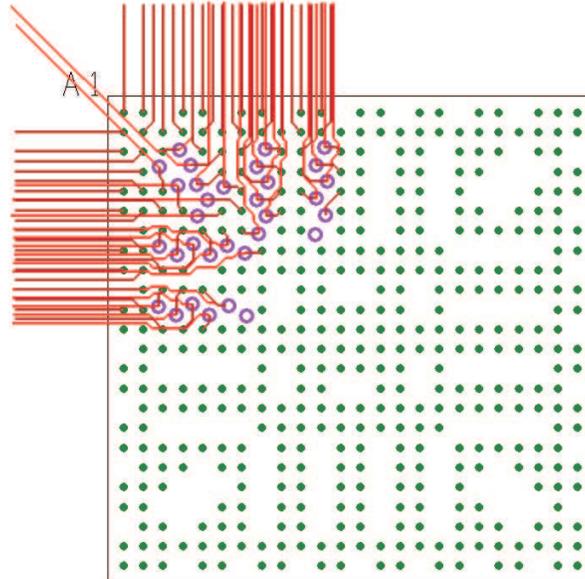
Figure 3. Quadrant 1 Routed
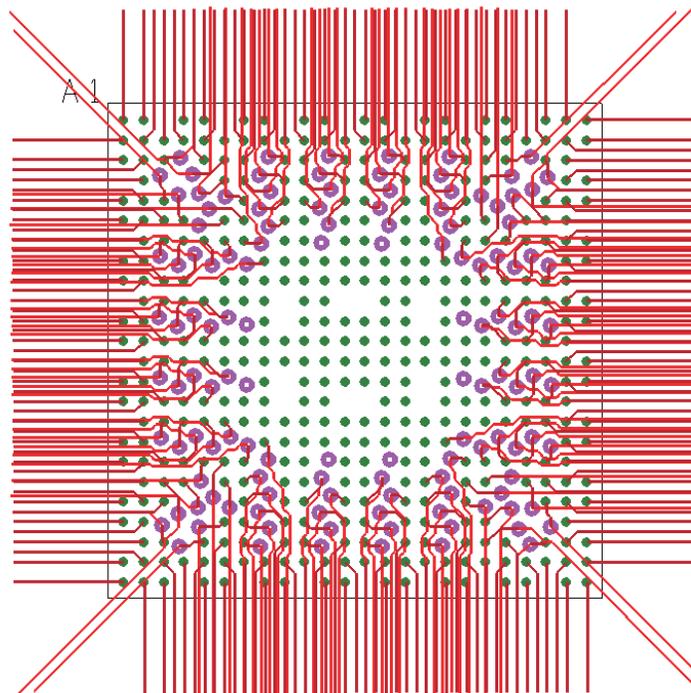
Figure 4. All Signals Routed

1.3 STEP 1: Routing the First Quadrant Top Layer

1.3.1 Routes for the Top Two Rows

1. Route the first quadrant. This is the first step in routing the OMAP3530 CUS package.

   Careful examination of the symmetrical nature of the CUS package allows for the least amount of steps in the routing procedure for the OMAP3530. The top left five pads are used as a starting point route, as shown in Figure 5. These routes constitute the simplest routing cluster of the top two rows of this Via Channel array, which will be copied to the rest of the perimeter of the device. Paste these routes three times in the direction of the arrow.

   NOTE: Grids should be changed to 0.65mm for centering the routes on the pads.
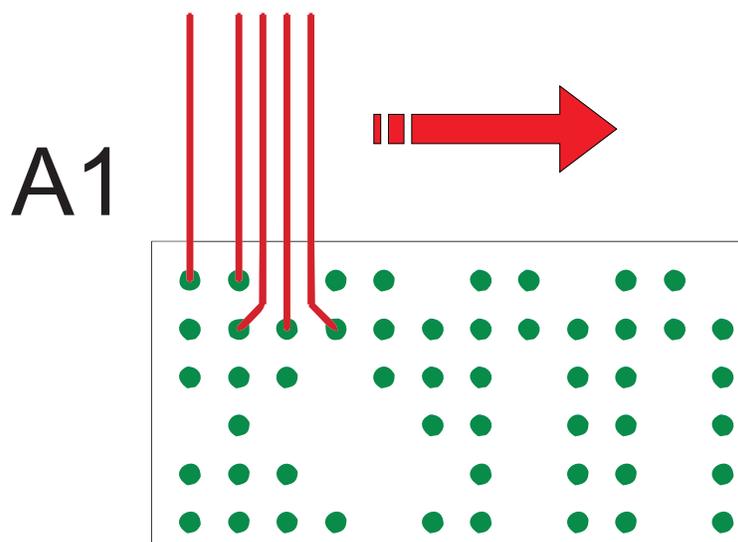
Figure 5. A1 Corner Routes

2. Copy the initial five traces to complete the routing for the top two rows of the first quadrant, as shown in Figure 6.
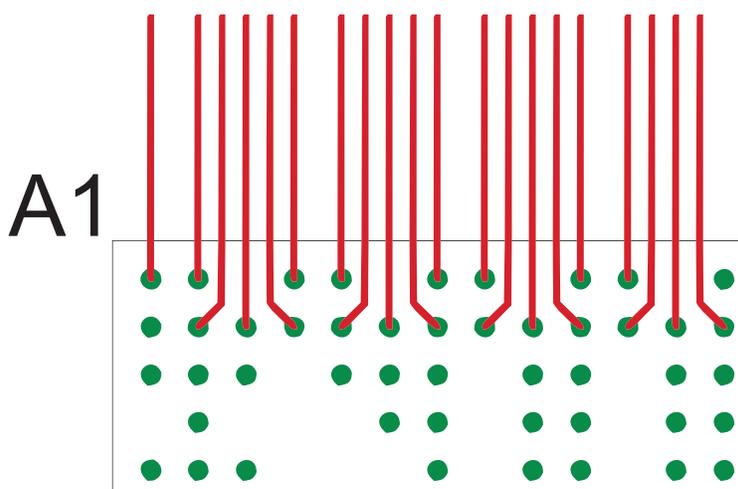
Figure 6. Completing the Top Two Rows of the First Quadrant

3. Route three pads from the third row, as shown in Figure 7.
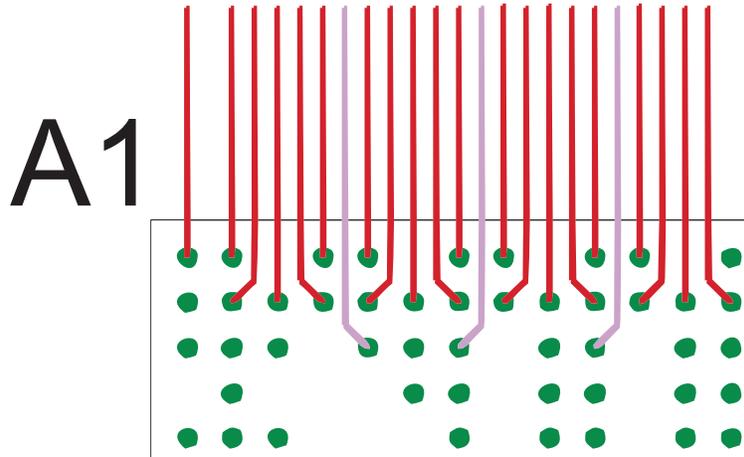
Figure 7. Three Routes From the Third Row

4. Copy the routes shown in the rectangle in Figure 8
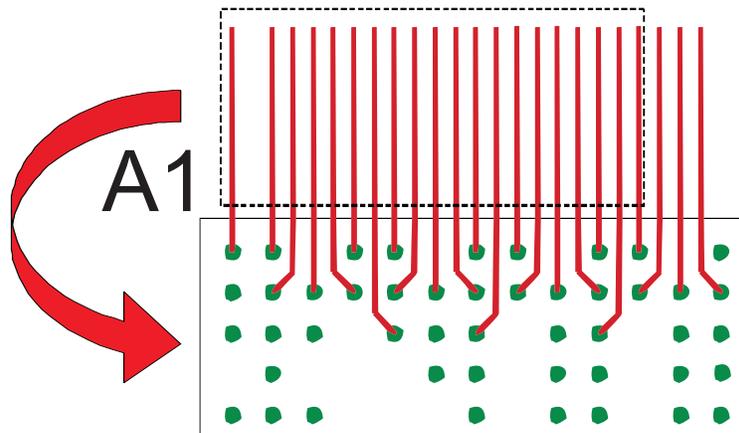
Figure 8. Routes to be Copied for the Left Side of First Quadrant

5. Mirror and rotate 90º CCW.
   The result is shown in Figure 9.
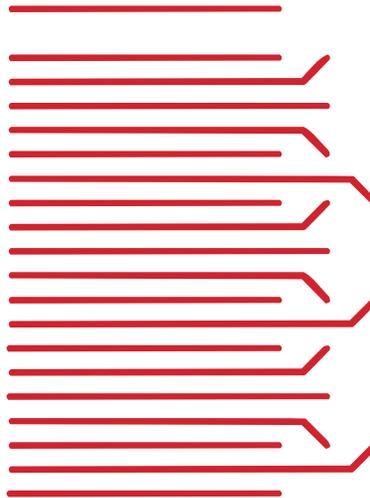
Figure 9. Copied Routes are Mirrored and Rotated 90° CCW

6. Paste these routes starting at pin B1.
7. Mirror two of the copied routes from the third row (arrows) to connect to their respective pads.
   This extra step is necessary due to non-symmetry within quadrant edges.
   This completes the routing of the outside rows for quadrant 1. The final result is shown in Figure 10.

NOTE: The six routes from the third row are done in this step to maximize efficiency.
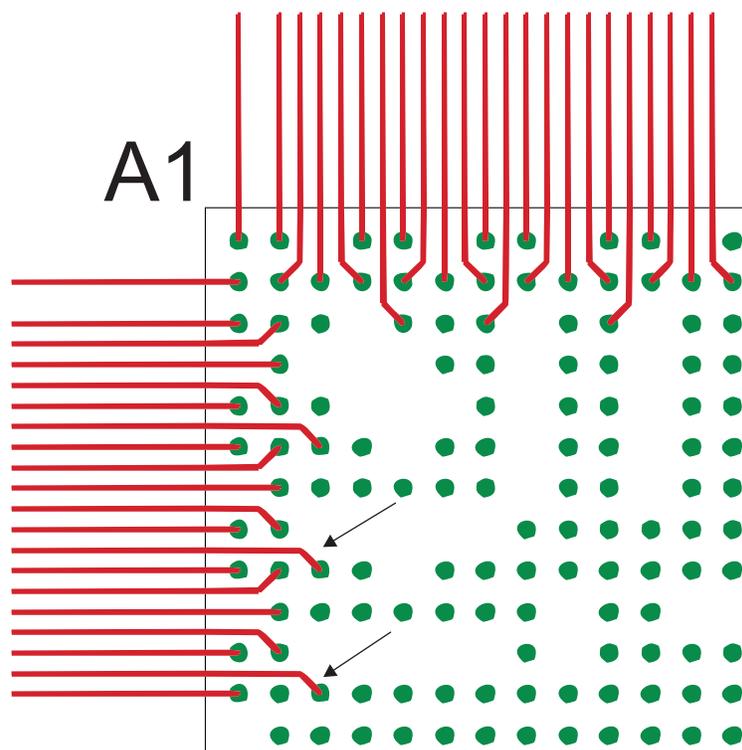
Figure 10. Completed Outer Row Routing of First Quadrant

1.3.2 Adding Vias in Via Channels

Figure 11 shows the OMAP3530 CUS package with the power and ground nets highlighted in red and gray, respectively. From this point on, the ground and power pads will be highlighted to aid in the clarity of the routing process. Arrangement of the power pins and how best to route them is discussed later in this document.
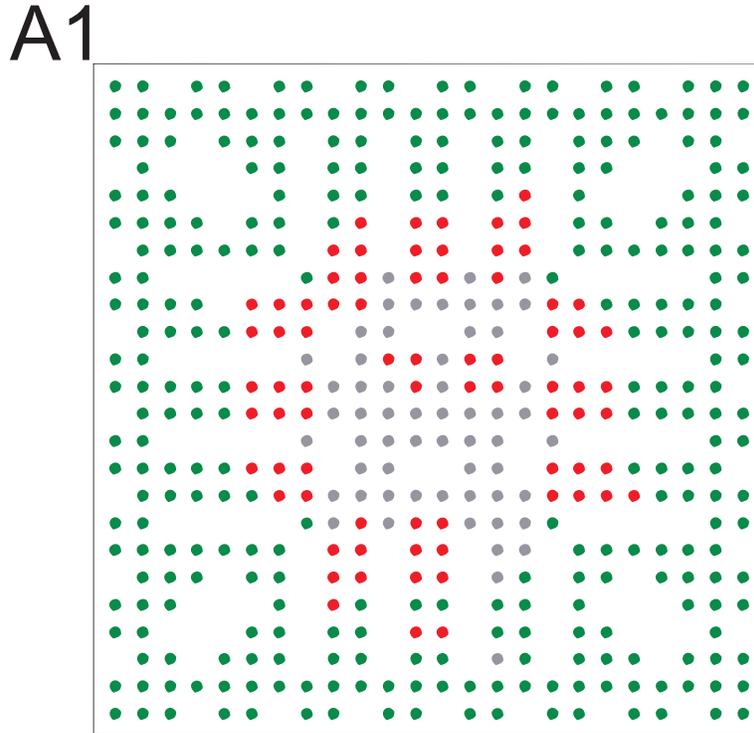
Figure 11. OMAP3530 CUS Package Highlighting Power and Ground Nets

20/10 vias can fit in the Via Channels in different ways. 8-9 vias in the corner channels are easily possible.

The arrangement in Figure 12 was chosen to best fit the routing channel 3 in this example. Once the vias are added to the channel they are connected to the pins on the channel's perimeter.
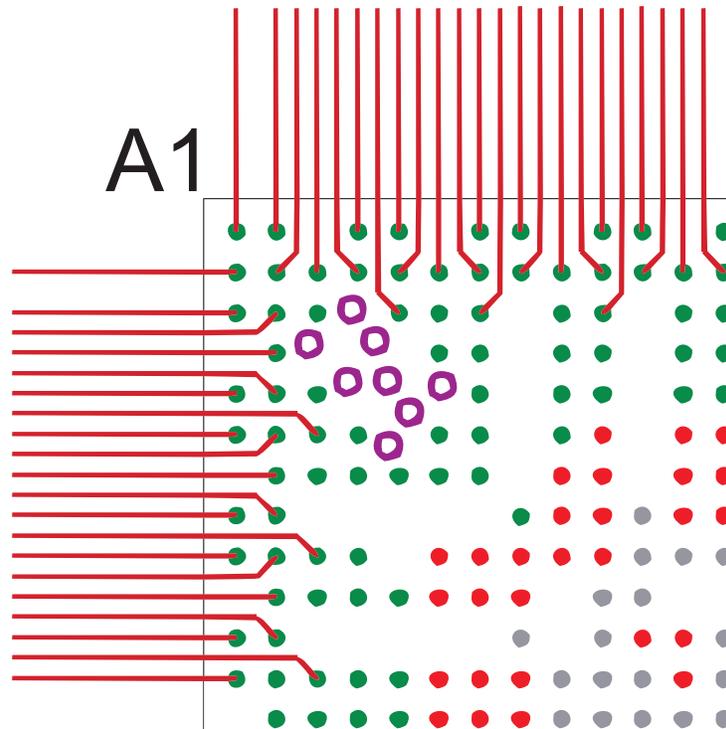
Figure 12. Adding Vias to Corner Channel

After adding vias to the corner channel 3:

- Six more vias will be added to the adjacent channel 1 and 2 as seen in Figure 13
- Copy them once again to the right
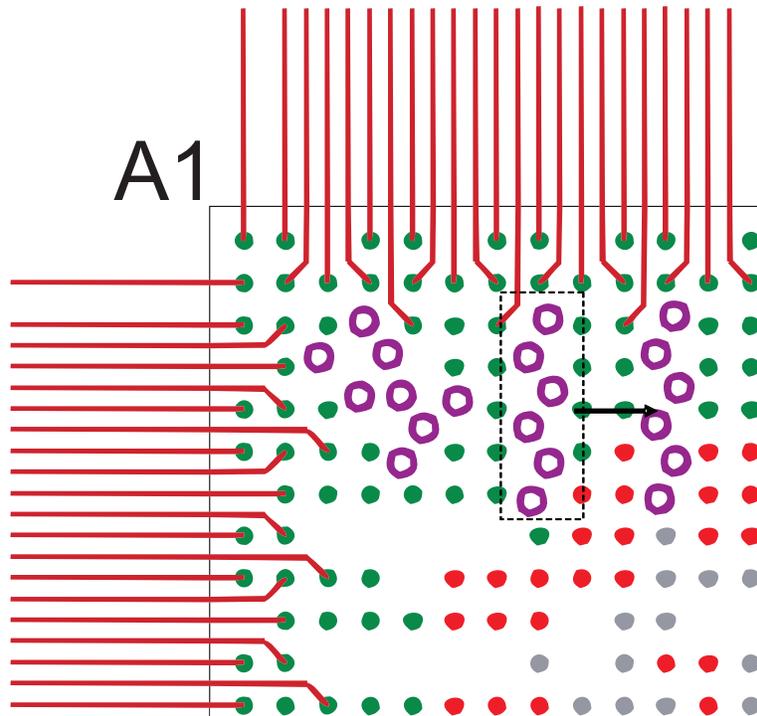
Figure 13. Adding Vias to the Top Two Channels

1.3.3   Routing the Via Channels Pins to the Vias

Once these three channels are filled, as shown in Figure 13, the signal pins surrounding the channel can be connected to the vias. If routed as shown in Figure 14, they can easily be copied to the other two channels left in the first quadrant.

The power pins shown in red, in Figure 14, need at least one via to connect to the power layers. For this reason, the bottom vias in the inner channels, with the exception of two, will be left unconnected for now. Using this vias in conjunction with the power and ground sections of the device will be discussed later in the document.
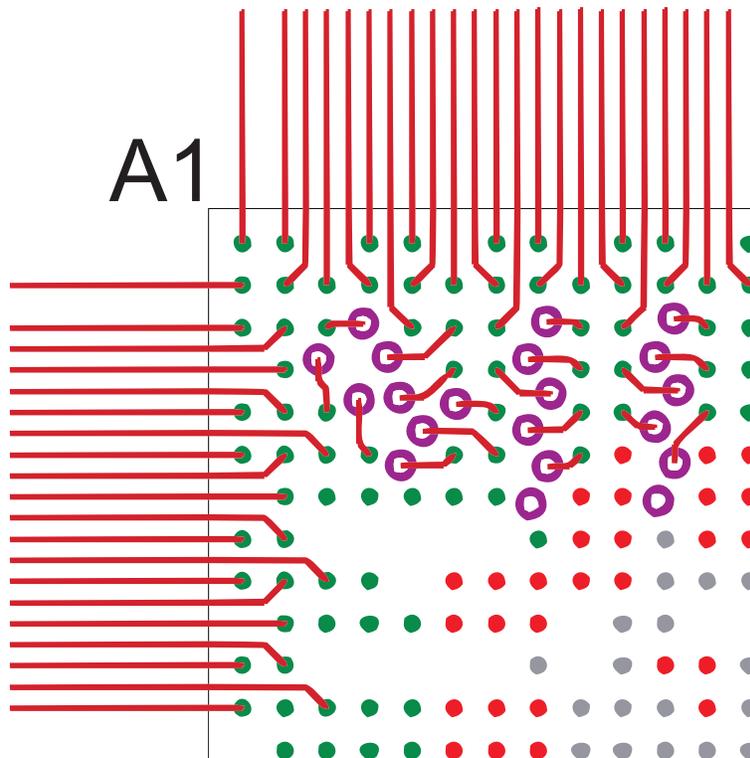
Figure 14. Connecting the Vias in the Filled Via Channels

- Set the copy filter to copy vias and Clines together
- Copy Channel 1 to channel 5
- Channel 2 to channel 4

The vias and Clines to be copied are shown in Figure 15. The vias were routed such that each channel should be copied individually to the remaining two channels, taking in consideration the missing ball at location J5.
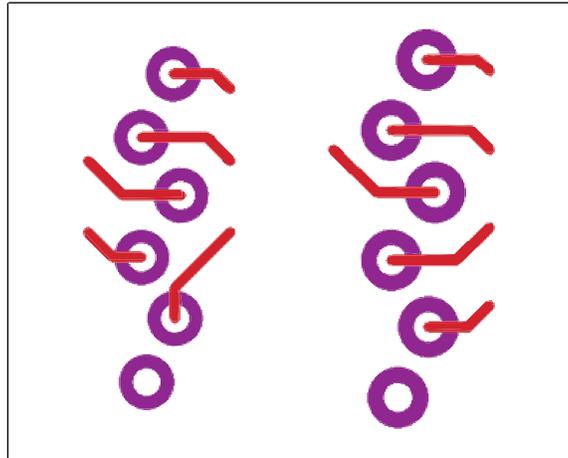
Figure 15. Via Channels 1 and 2: Vias and Clines to be Copied

To complete the top layer routing for this quadrant, two more vias need to be connected; these are shown in blue in Figure 16. Route these signals horizontally between via and the adjacent BGA pin.
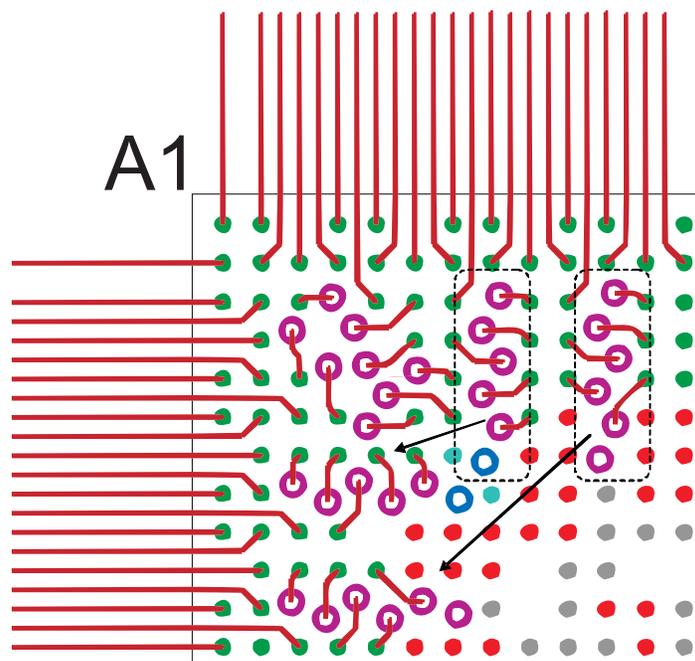
Figure 16. Routed First Quadrant Top Layer

Figure 17 shows the complete top layer of first OMAP3530 first quadrant.
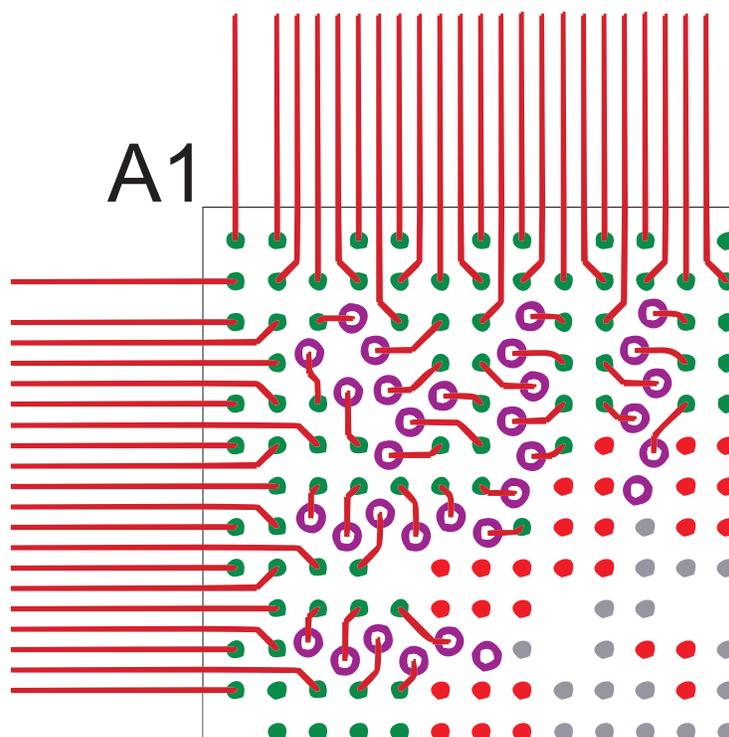
Figure 17. Completed Top layer Routing for Two Outer Rows and Via Channels

1.4   STEP 2: Routing the First Quadrant Bottom Layer

1.4.1   Routing the Bottom Side of the PCB

The next step is what makes this part so unique and desirable from a routing point of view. Turning off the top layer (dimmed in our case) allows a clear view of all the vias connected to the unrouted signals in the first quadrant.

Remember that the bottom vias in via channels 1and 5 (highlighted in red) will not be routed in this step since they are reserved for the power nets.
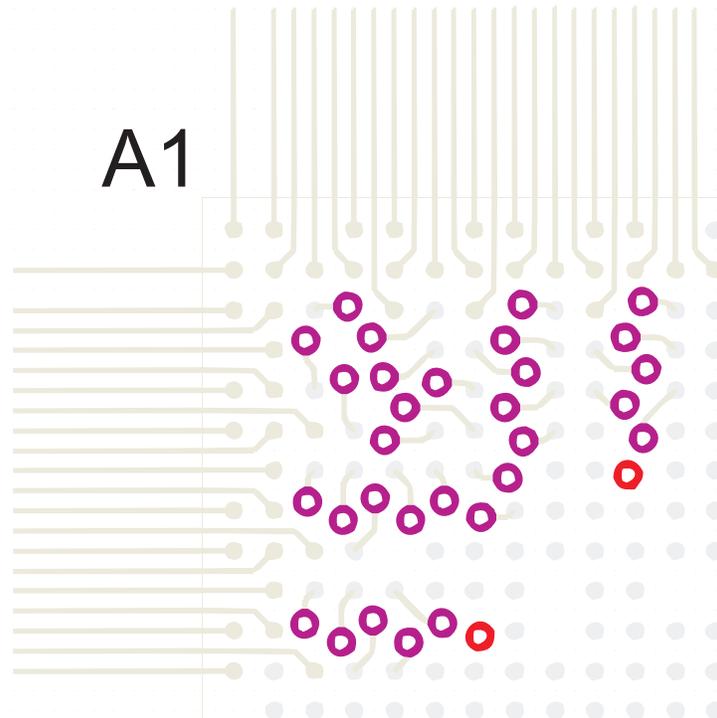
Figure 18. Bottom Layer View of Populated Via Channels

1. Route any one channel, as shown in Figure 19.
2. Copy it to the rest of the channels.
    The result would look like this:
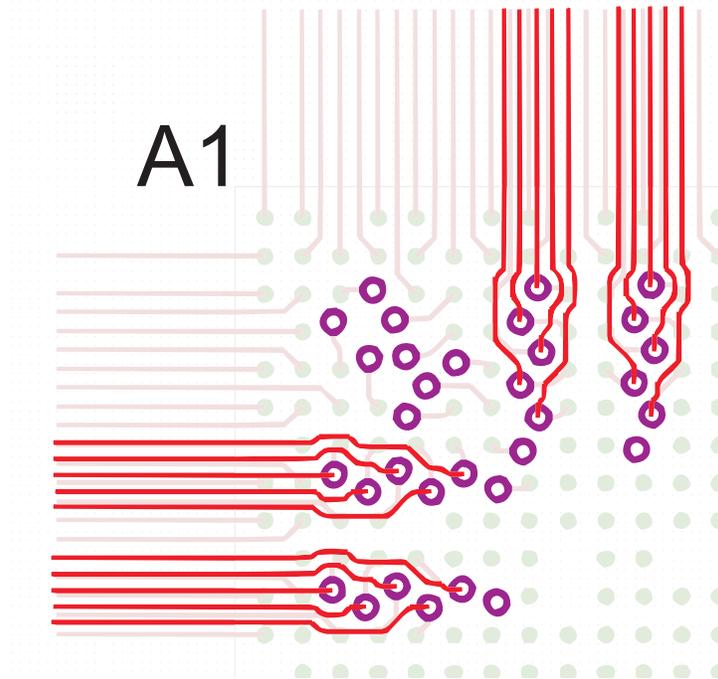
Figure 19. Routing the Via Channels on the Bottom Layer

3. Route corner vias from channel 3.
4. Route the two vias shown by the arrows in Figure 20.
    This completes the bottom side routing of OMAP3530 Quadrant 1.
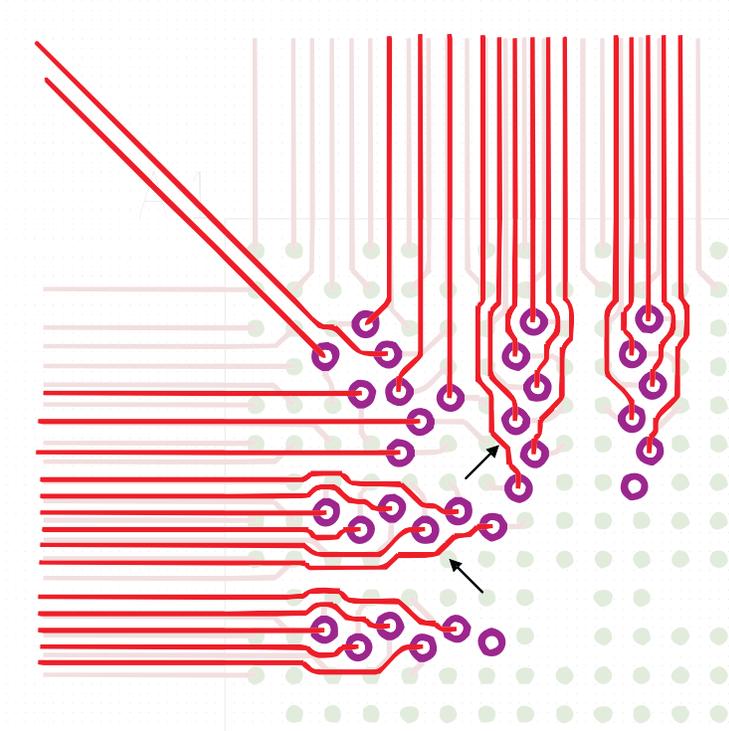
Figure 20. Completed Routing of Quadrant 1

1.5   STEP 3: Copying Quadrant 1 to Quadrants 2-4

1.5.1   Option I – Connecting Lines or Traces (Clines) and Vias Only

1. Turn ON both top and bottom layers to make both sides of the PCB visible.
2. Set your filter Design Object Filter to select Clines and vias .
3. Select both top and bottom layers clines and vias.

Figure 21. Selecting Quadrant 1 Vias and Clines

4. Rotate 90° CCW (or CW) and paste to the next quadrant.
5. Repeat 3 times. The grid set to 0.65mm for correct placement.
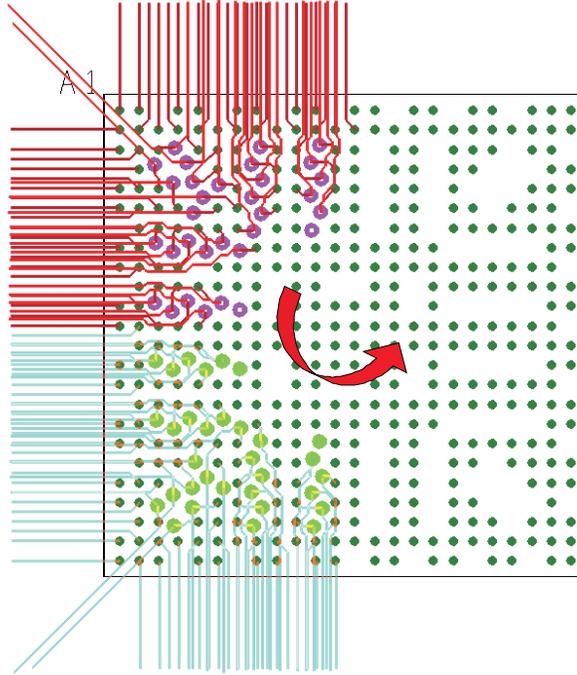
Figure 22. Second Quadrant Routed

Figure 23 shows the completed routed signals. Both layers are turned on and dimmed for clarity. Not only the device is easy to complete, but it is also beautiful layout art!
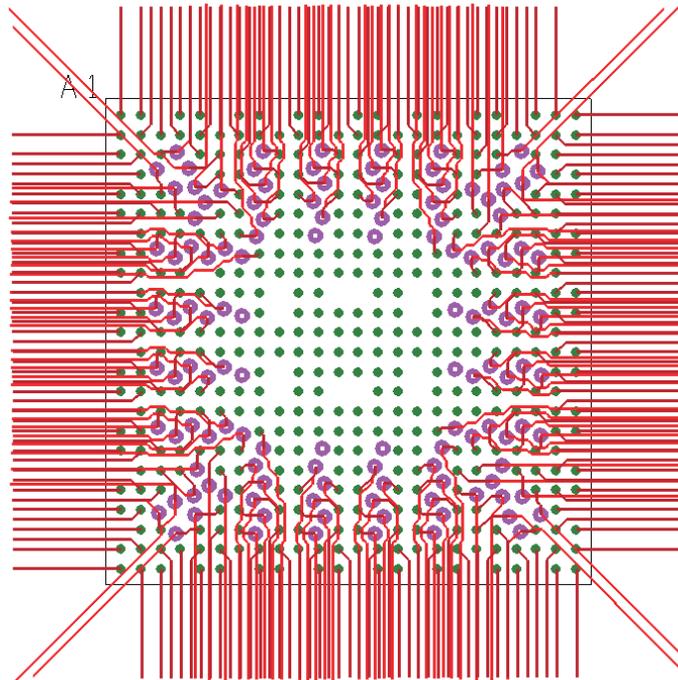
Figure 23. All Signals Routed for the OMAP3530 CUS Package

Figure 24 and Figure 25 show how the escape routes are completed for all the signals on the OMAP3530 CUS package as seen from the top or bottom of the PCB.
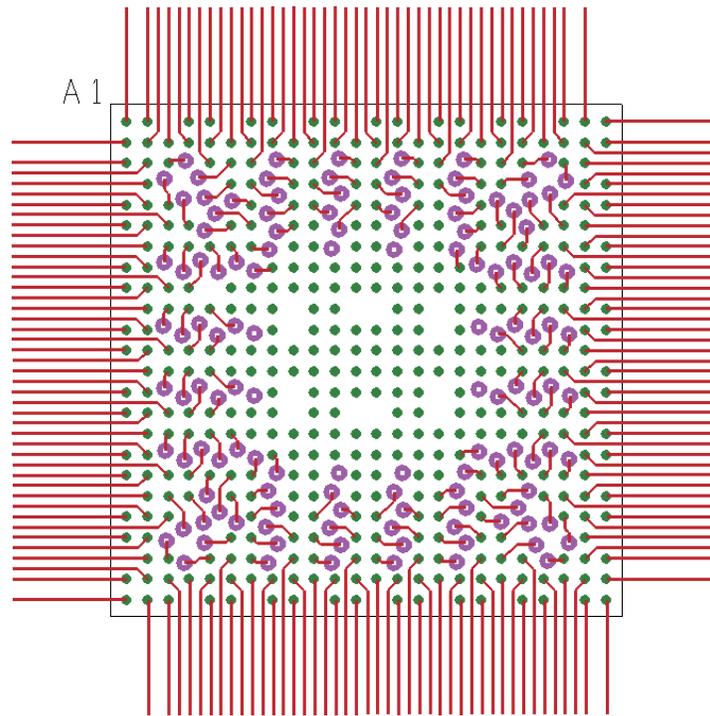
Figure 24. All Signals Routed – Top View
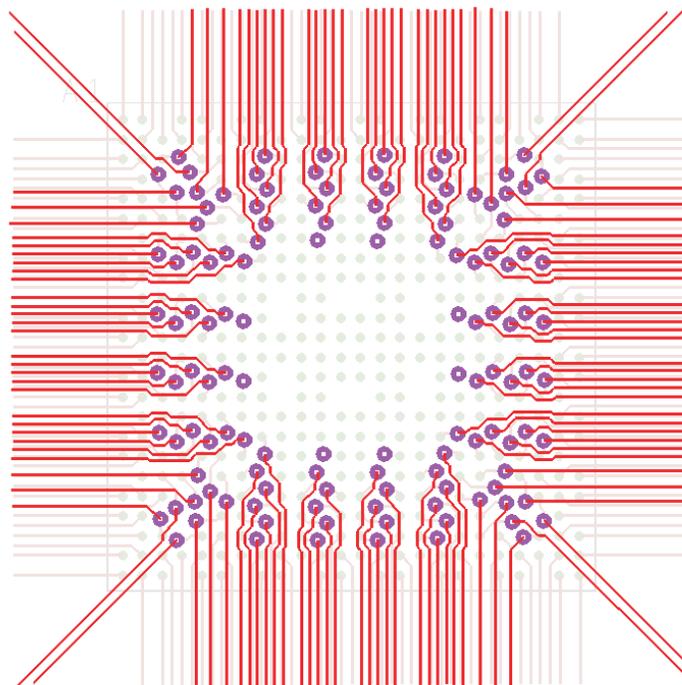
Figure 25. All Signals Routed – Bottom View

1.5.2   Option II – Copy Clines and Vias and Shapes

If the available PCB layout tool allows, the layout for this package can be further simplified by also copying the shapes used as copper fills for the power sections along with the vias and clines of Figure 21. This is a second option to routing the quadrants of the OMAP3530 CUS package. To complete the power routing separately, go to Step 4 in Section 1.6.

The power sections have been highlighted in different colors for each of the three power nets found on the device. The rectangles further highlight these areas.

By observing the arrangement of the power around the CUS package, it is clear that one single shape could be used for almost all of the power sections surrounding the larger ground center. The only exceptions are two red and pink power sections.
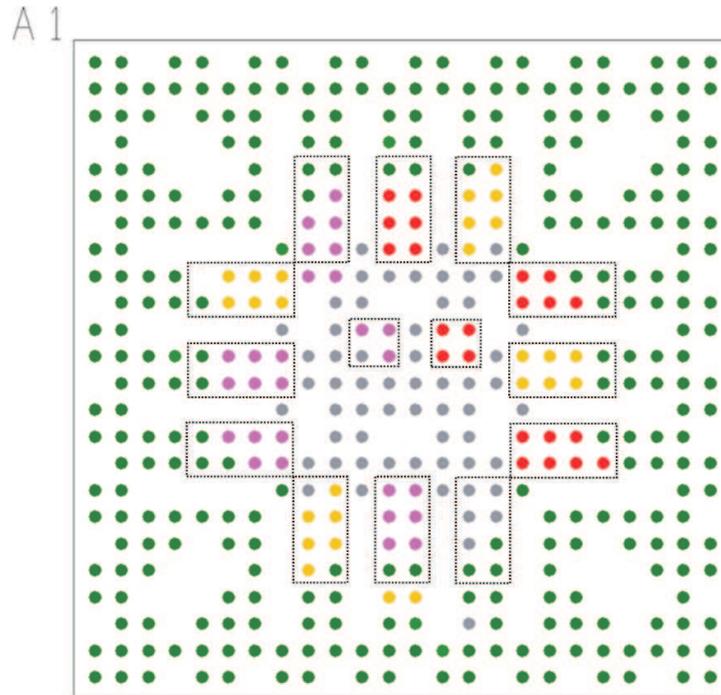
Figure 26. Power Arrangement for the OMAP3530 CUS Package

Noting that these power areas have 3 to 4 rows of power pins, when copied, the shape to be drawn should be such that it completely covers the new power section where it is copied. Figure 27 shows such a shape that could be used around the whole package to route most of the power sections.

Starting at the red power section shown in Figure 27 draw a shape around the three rows of power pins and include the two signal pins.

- Select Shape Add, a menu appears on the Option menu and the option to Assign Net Name gives a list of all the nets in the design.
- Select the net around the shape that will be added. Once the shape is completed, the via connects to the shape and the respective pins.
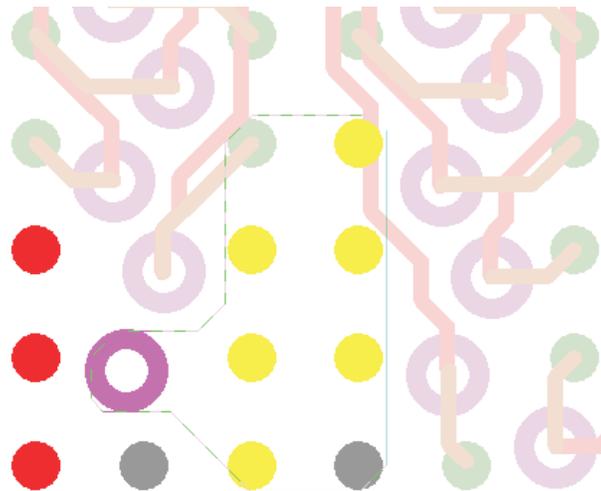
Figure 27. Shape Drawn Around 4 Rows of Pins and Via
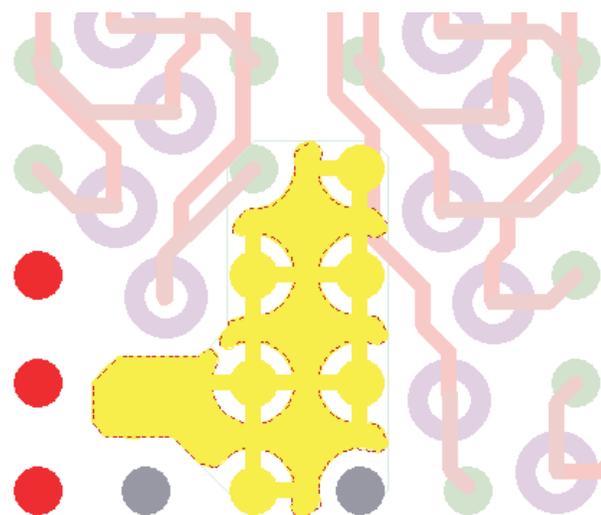
Figure 28. Shape Connected to Pins and Via

To connect each of the following sections to the power plane, at least one via will be needed. The available vias are found at the bottom of each Via Channel - center to the device. These were the vias highlighted in red in Section 1.4.1 of this document.

Because of the symmetrical proprieties of the device, with the exception of some, the vias to the left of each power section can be used to connect these power pins to the power layer.

Figure 29 shows the top layer view of the first complete quadrant, including the power shapes connected to the adjacent available vias. This quadrant can then be copied the same as in step 3.
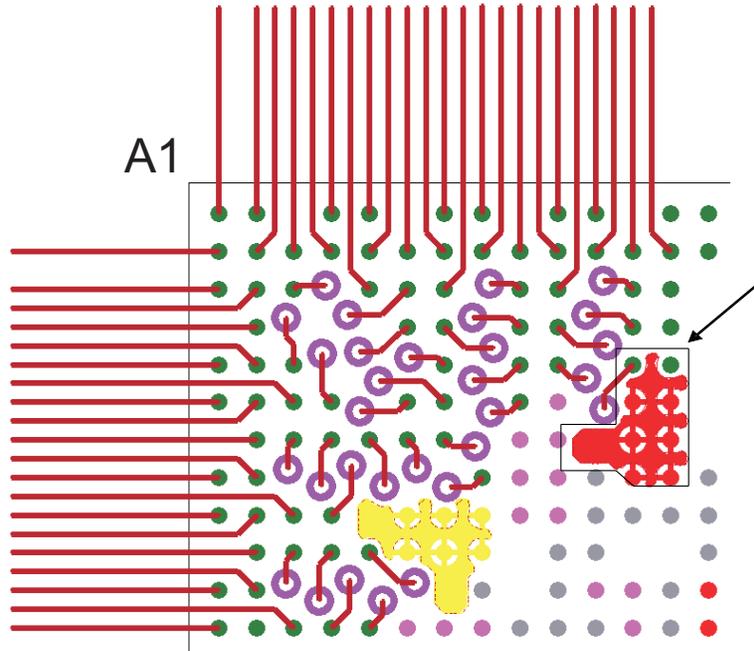
Figure 29. First Quadrant Routing Including Copper Shapes

Figure 30 shows the first copied quadrant that includes the power copper shapes.
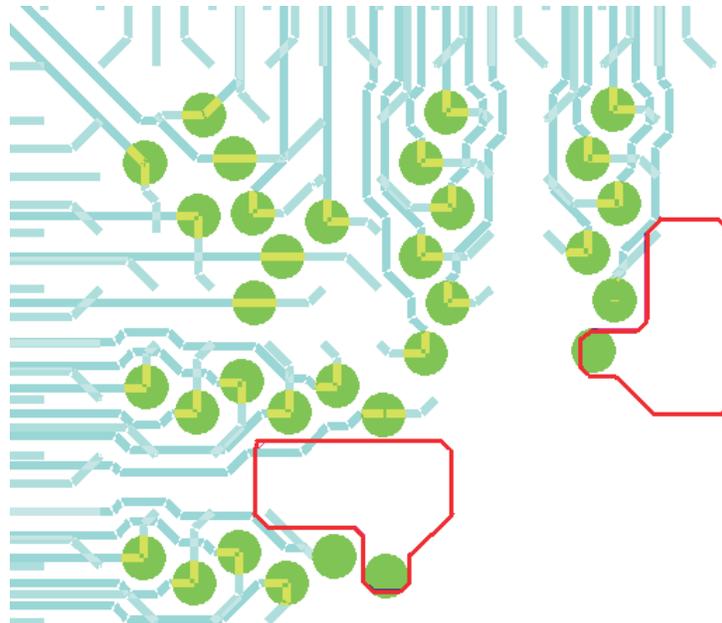
Figure 30. Quadrant Including Power Copper Shapes

Pasting this quadrant around the device three times brings it into the state shown in Figure 31. A few adjustments will connect these power areas to their respective nets.
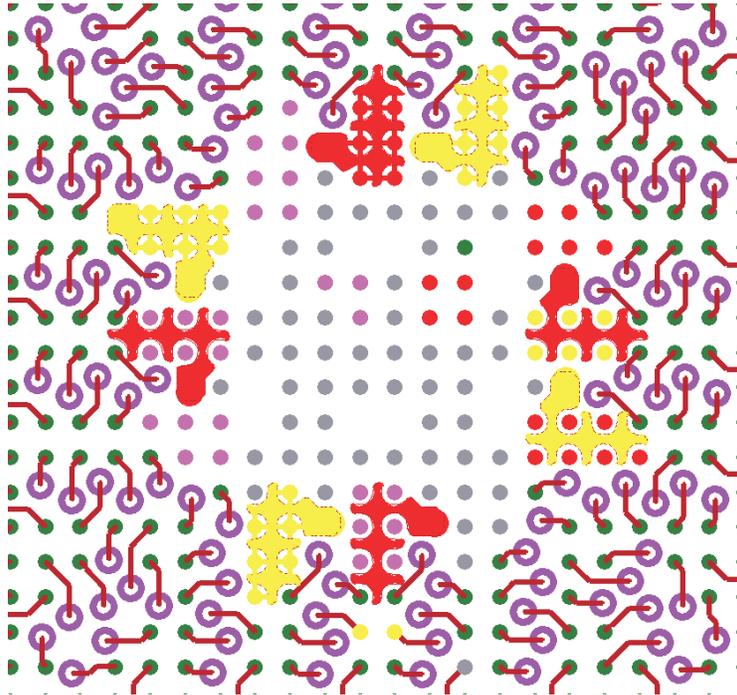
Figure 31. Power Shapes are Copied Along With the First Quadrant

Including these shapes to the first quadrant before copying it to the rest of the CUS device allows almost 60% of the power net routing to be completed. This is shown in Figure 32.

Once copied, these shapes can be manually connected to their respective power pins and vias.
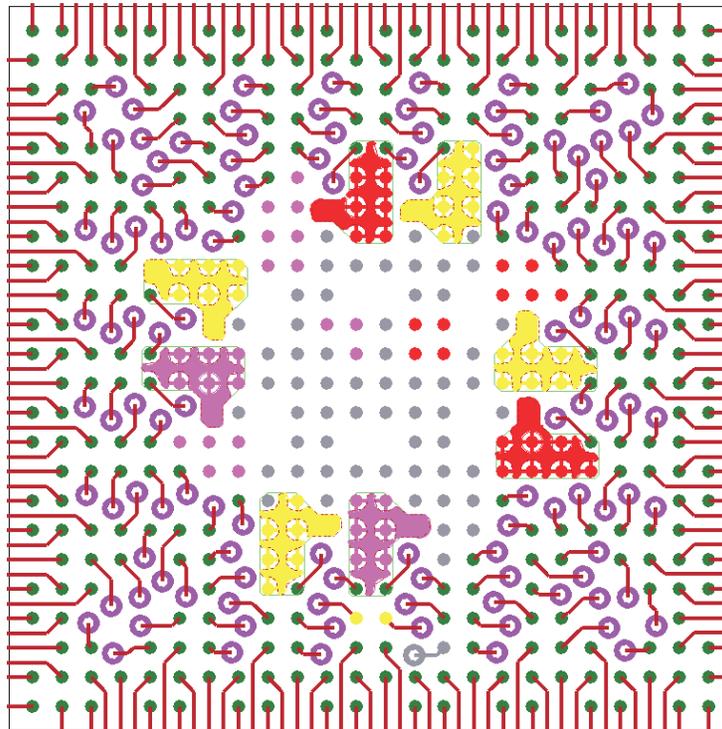
Figure 32. Completed Routing Including 60% of the Power Sections

NOTE: Currently, Allegro does not automatically connect a shape + via that has been copied to a new net. It cannot reconnect the via to the shape if the net name has been changed. Future revisions of the tool may include this capability and other tools may allow it, thus, the inclusion of the option here.

1.6 STEP 4: Adding Power Vias and Copper Areas

1.6.1 Adding Power Vias to Center of CUS PCB Footprint

There are via channels in the center of the CUS package as shown in Figure 33. There are six channels center to the device and each house a maximum of 3 vias. Careful study of the arrangement of the power pins proved that this arrangement is optimal to connect the most pins to a copper area. Add vias to this channel as suggested in Figure 33.

Figure 33. Via Channels for Power and Ground

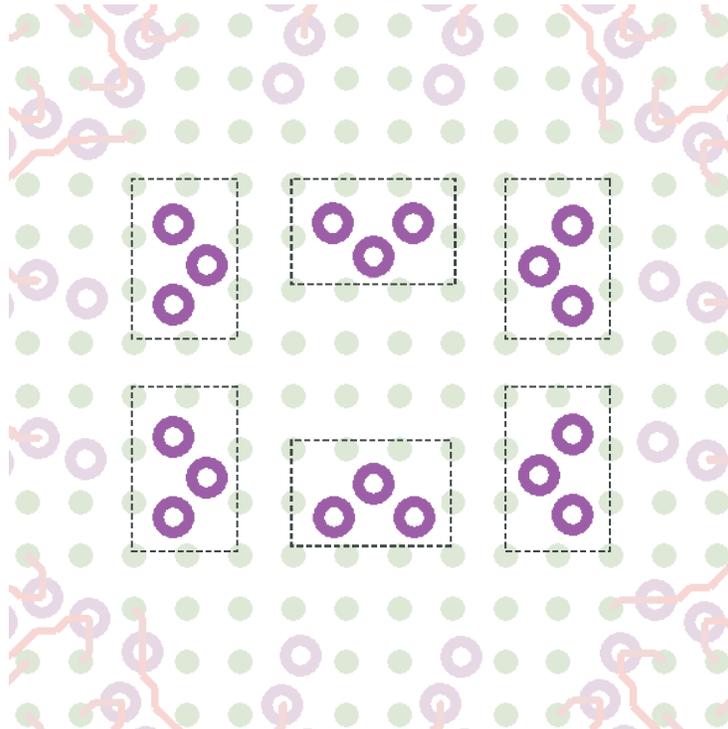### 1.6.2 Route Power and Ground Pins Using Copper Shapes

Once the escape routing is done for the OMAP3530 CUS package, the next step is to complete the power and ground routing.

Form a copper pour area around the power/ground nets being sure to provide thermal reliefs around the BGA ball pads. These are not for thermal issues, but to ensure that the ball solder does not get wicked away (spread too thin) by the copper during reflow. This is a top layer copper pour. The lower power planes should match the same shape somewhat (if not solid) and be routed with heavy traces on the power plane. For signal integrity, it is essential to make the ground layer solid with no cuts. Cut the power plane only in a radial pattern, from the center out, once the pins are grouped. This improves signal integrity as most trace's return currents will not have to cross the gap in the power plane like they would if the cuts were perpendicular to the routing direction, which is typically from the inside of the chip out.

Add the copper shapes over the power and ground pins. At least one via is needed for the different power sections. More vias can be added later as needed and will be discussed later in this document.

The ground pins use most of the vias added in the previous step since the GND net covers most of the center of the CUS package (see Figure 34). However, some of these vias have to be used for the power pins located in the center of the device. Finding the best use of these vias has been done and the next steps show this.
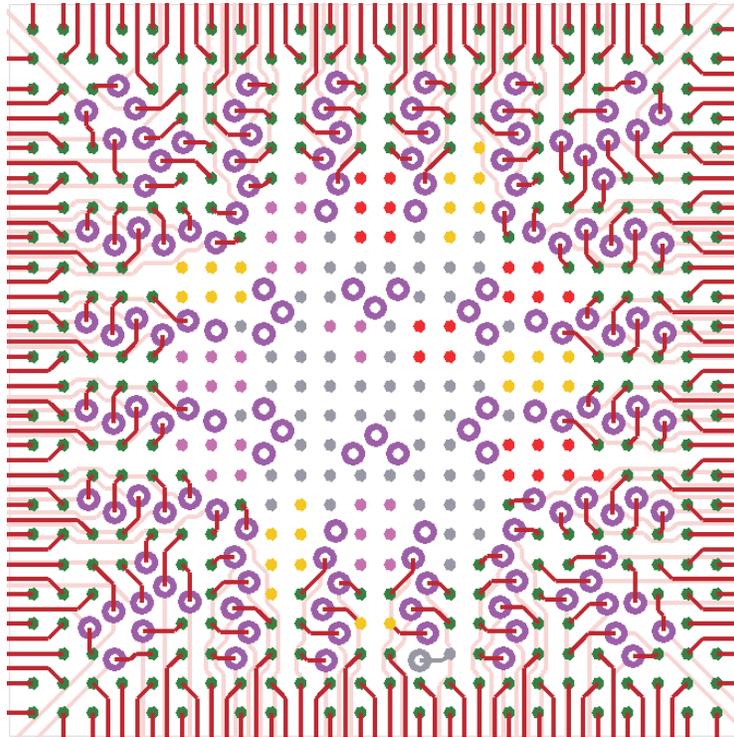
Figure 34. General View of the Power and Ground Nets and Associated Vias

There are many ways to route the power pins, some easier than others, depending on the tool used. One way would be to:

1. Draw one shape over one net and associated via in the channel.
2. Copy the shape to the other power pins/vias on the same net. The result is shown in Figure 35.
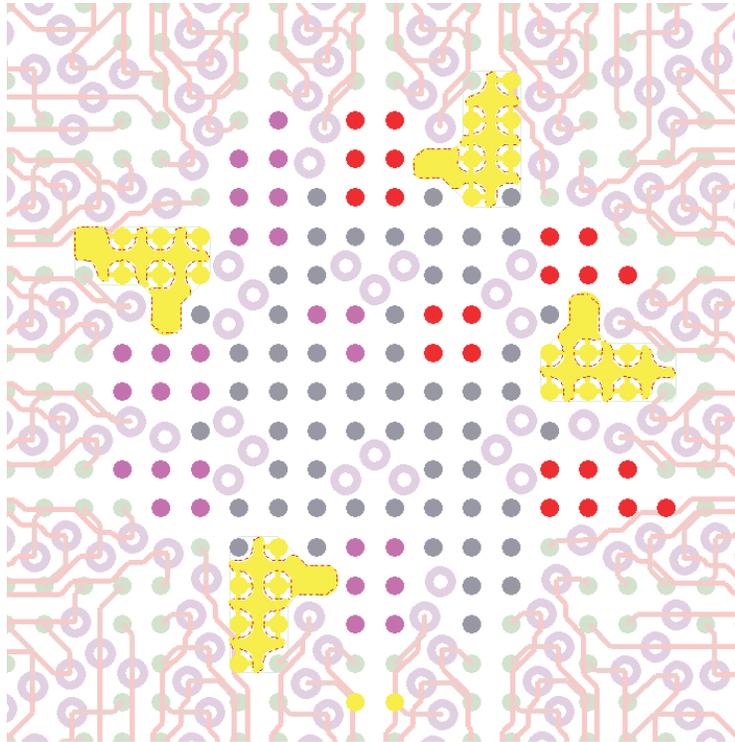
Figure 35. One Shape Drawn and Copied to Entire Net

3. Repeat the same for the remaining nets. The net highlighted in pink for the OMAP3530 CUS package is VOCORE_1V3 net. For the section of this net shown in Figure 36, the same shape can be used to connect all pins.

4. Copy the shape.

5. Rotate it 180°.

6. Paste is as shown in Figure 36.

   Notice how the shape covers all of the remaining pins and the second via? In Allegro, these two shapes can be merged to form one single shape.

7. Go to Shape menu and select Merge Shapes.

8. Click on both shapes and they will become one.
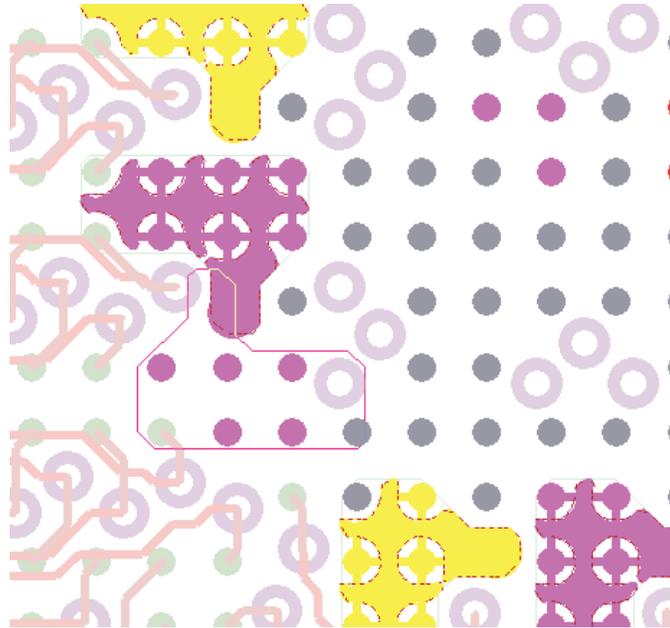
Figure 36. One Shape Does it All

9. Draw shapes around the remaining power pins, as shown in Figure 37.
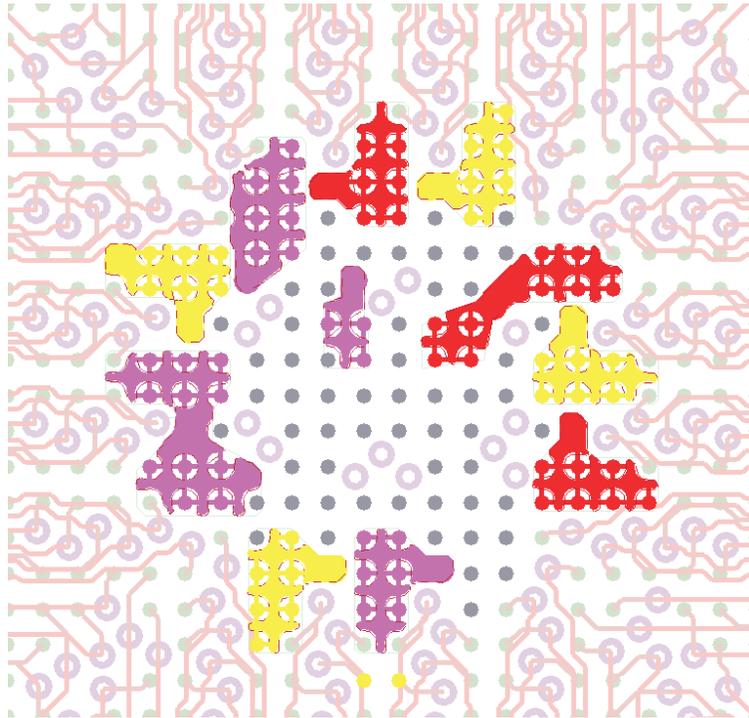
Figure 37. Power Pins Copper Area Distribution

10. Draw a shape around the ground pins, as shown in Figure 38.
11. Optimize any shapes as needed to include all vias and pins with at least two thermals.

Figure 38. All Power and Ground Pins Routed

1.6.3 Custom 16/10 Power and Ground Vias
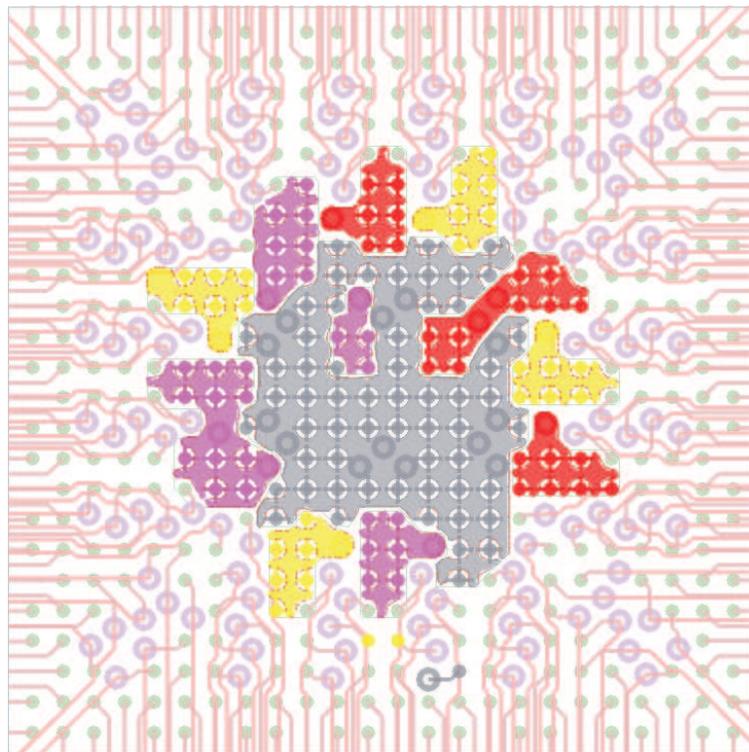
Power sections require multiple 20/10 vias, but this may appear impossible once the via channels are full.

For this reason, a custom via could be generated where the via outer diameter is reduced to 16 mils for the top side. This allows vias to fit between four neighboring power or ground pins. This is not actually a 16 mil via since it is used only as a hole in the middle of a large copper area and, therefore, does not violate the 20 mil minimum via size rule.
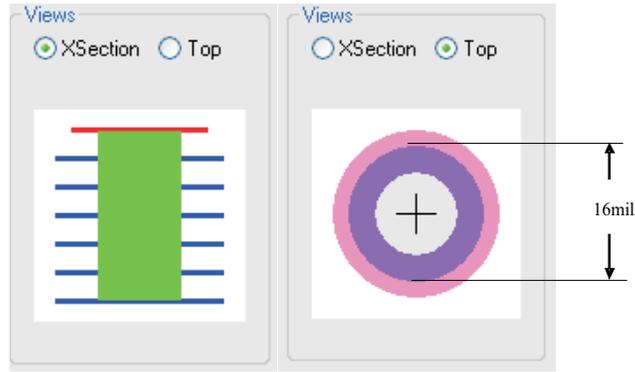
Figure 39. Setting the Via Top Diameter to 16 mils
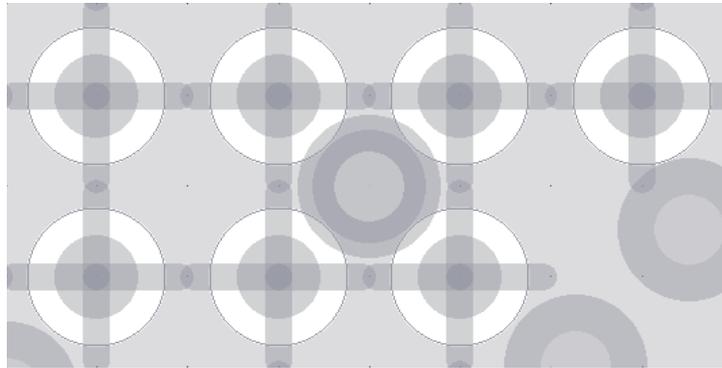
Figure 40. Inserting 16/10 Vias

Place 16/10 vias around the copper areas as needed. See the highlighted vias in Figure 41.
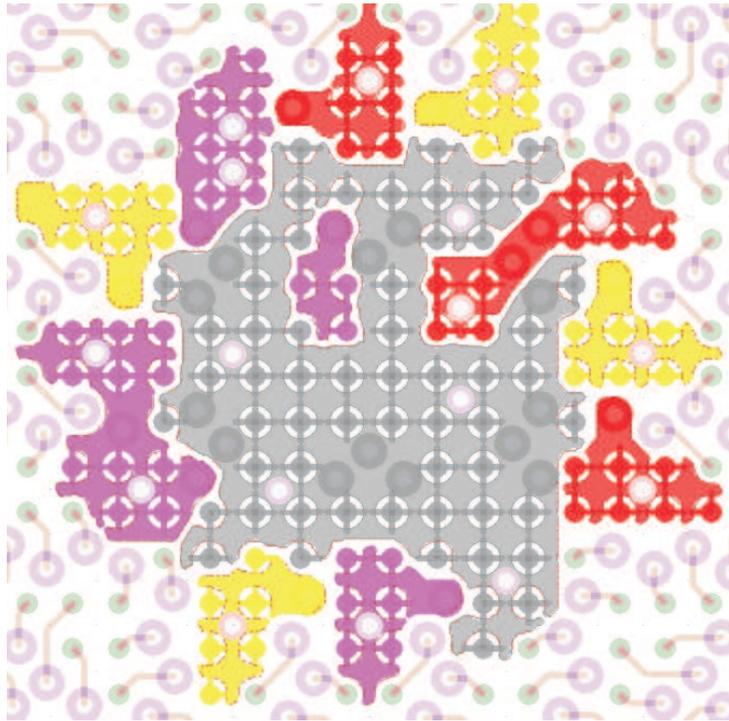
Figure 41. Distributing New Vias Around Power and Ground Copper

1.7   *Conclusion*

These are the results of the BGA escape routing. The Via Channel escape routing for this device is not only less time consuming but also more cost effective than a 0.8mm pitch BGA part of equal pin count .
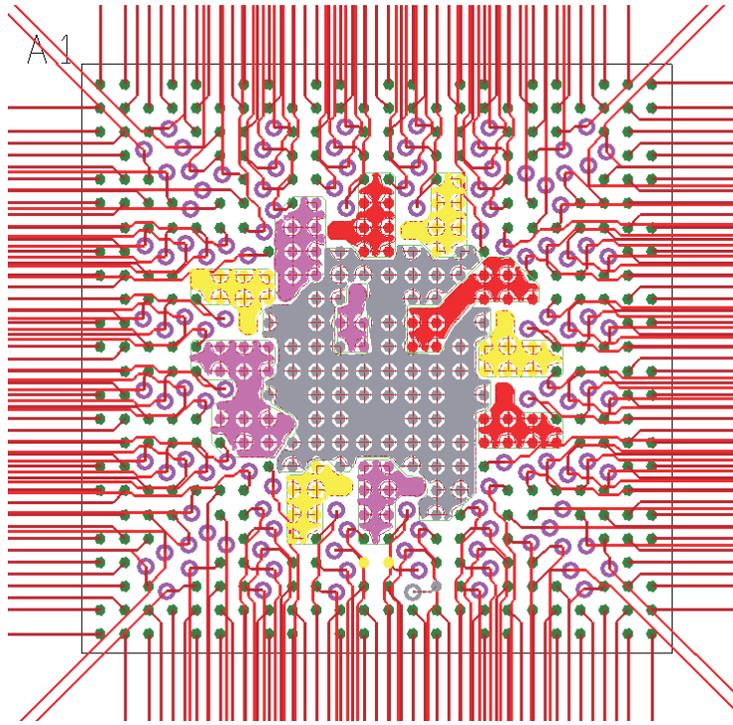
Figure 42. Completed PCB Routing

2   References

OMAP35x 0.65mm Pitch Layout Methods (SPRAAV6)

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