Application Note

Flash Variants Supported by the mmWave Sensor

ABSTRACT

This application note describes the flash variants supported by Texas Instrument's mmWave Sensor.

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Trademarks

1 Introduction

Serial flash devices are one of the most preferred boot media in the embedded system applications. For mmwave sensors as well, the user application components are expected to be stored in the serial data flash which is interfaced with the sensor over the QSPI interface. The sFlash can also be used to store other data based on user's choice. One example would be to store RF-Front end calibration data onto the sFlash and restoring by application during initial calibration cycle of the RF-Front end at every device bootup. This application note lists out verified sFlash devices parts to be working with the mmwave sensors, documents the prerequisites for other sFlash parts, and mentions any known issues.

2 Serial Data FLASH Supported

2.1 AWR1243/xWR1443 ES1.0 and ES2.0 Devices

The AWR1243/xWR1443 ES1.0 and ES2.0 devices work only with Spansion and Macronix devices. In particular, the flash variants tested to work with the ROM bootloader are:

- Spansion S25FL132K0XNFB010
- Macronix MX25L3233F
- Macronix MX25R1635FZNIH0 (wide voltage part variant)

2.2 AWR294x, AWR2544, xWR1642, xWR1843, xWR6843 Devices and AWR1243/xWR1443 ES3.0 Devices

There are several factors that determine if the AWR2xxx/xWR1xxx ROM bootloader can interface and work with the SFLASH on AWR2xxx/xWR1xxx devices.

2.2.1 Prerequisite

Refer to the device data sheet for details on the timing and interfacing requirements with the SFLASH over the QSPI interface.

SFLASH device variants should support 40-MHz operation for all commands (including normal read command). For the xWR6843 device the SFLASH device variants should support 80-MHz operation for all commands.

SFLASH supports the SFDP command and responds with JEDEC-compliant information regarding the capabilities and command set of the flash. The key fields interpreted are listed in Table 2-1.

Table 2-1. Key Fields

Field	Byte Offset
SFDP signature	[3-0]
JEDEC flash parameter offset in bytes	[0xE-0xC]
(1-1-4) Read support	[JEDEC flash parameter offset in bytes + 0x2] – bit6
(1-1-2) Read support	[JEDEC flash parameter offset in bytes + 0x2] – bit0
(1-1-4) Read command code	[JEDEC flash parameter offset in bytes + 0xB]
(1-1-4) Read dummy cycles	[JEDEC flash parameter offset in bytes + 0xA] – bit[4:0]
(1-1-2) Read command code	[JEDEC flash parameter offset in bytes + 0xD]
(1-1-2) Read dummy cycles	[JEDEC flash parameter offset in bytes + 0xC] – bit[4:0]

- The number of address bytes = 3 (always).
- For single data line SPI read – Read Command Code (0xB), Read Dummy cycles (8bit).

2.2.2 ROM-Assisted Download to the FLASH (Device Management Mode - SOP5)

The ROM-assisted download should work with all flash variants that allow for "Memory mapped mode" and "Page program command (0x2)" with 1 dummy byte and 24-bit addressing.

In addition to writing to the flash, the ROM bootloader (RBL) also supports setting the "Quad Enable" bit for Spansion and Macronix variants (certain specific part variants only).

Applicable for AWR294x/AWR2544

AWR294x/AWR2544 ROM Bootloader (RBL) has two step process where an application (flash programmer) is loaded to RAM over UART in SOP5 mode. This application is then responsible to read the actual image (to be flashed) over UART and download that to the Flash.

AWR294x/AWR2544 RBL doesn't support to set the "Quad Enable" bit of sFlash. If SFDP header of Flash variant contains the information of QE bit location (along with Quad-mode) then RBL will go and read that location to enable/disable quad mode option. Else in absence of QE bit location and with Quad-mode support in SFDP header, RBL will assume that QE bit is enabled by customer and move to quad mode.

2.2.3 ROM-Based Load From FLASH (Functional Mode – SOP4)

The ROM bootloader performs the read from the FLASH based on the highest capability mode (quad, dual, or single) as published by the SFLASH in response to the SFDP command. The commands used are as published by the SFDP response. Thus, if the quad read is supported, the expectation is that the Quad Enable (QE) bit is already set in the FLASH. The ROM bootloader uses the quad mode to perform the read.

2.2.4 Recommendation

The flash vendors have an orderable part variant with the Quad Enable (QE) bit set. TI recommends using these variants to work with TI mmWave SOCs.

2.3 Known Issues (xWR1642 ES1.0 and xWR6843 ES1.0 Devices)

The ROM bootloader in XWR1642 pre-production devices is not compatible with SFLASH variants that support extended addressing mode. In particular, the “Number of Address length” field of the SFDP command response being non-zero is not supported. The total SFLASH addressable region in XWR1642 devices is 8 MBytes. Thus, “Number of Address length” = 0 (corresponding to 3 bytes address length) satisfies the addressable range. However, the compatibility issue is with variants that allow for 3 or 4 bytes address length.

This incompatibility will be addressed in the production version of the XWR1642 silicon.

2.4 Flash Variants

2.4.1 Flash Variants

Supported flash parts for xWRL6432, xWRL1432, xWR1642 ES2.0, xWR1842 ES1.0, xWR1443 ES3.0, and xWR6843 ES1.0 & ES2.0 devices. The flash variants that have been tested to work are shown in Table 2-2.

Table 2-2. Tested Flash Variants

Flash Vendor	Variant	Remarks
CYPRESS (SPANSION)	S25FL132K0XNFB01	QE bit set by ROM bootloader in SOP5 while flash programming
	S25FL064LVF01	QE bit set by ROM bootloader in SOP5 while flash programming. This flash variant supports extended addressing mode. All mmWave devices may not be compatible with the extended addressing mode. Refer to Section 2.3.
MACRONIX	MX25L3233F	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25R1635FZNIH0	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25V1635FZNQ	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25U1633FZNQ	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25V8035FM1Q	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25U1633FZUI	Industrial grade 1.8-V flash
ISSI	IS25LP080D	QE bit set
WINBOND	W25Q16DVZPIG	By setting QE bit externally once

Please note for AWR294x and AWR2544 devices, the flash devices in the above table are expected to work. For any flash variant in the above table the QE bit needs to set by the vendor or manually in the sbl_uart_uniflash (flashwriter). Please refer to the MCU Plus SDK readme guide (for AWR294x and AWR2544) for more information on writing a custom flash driver. Additionally, supported flash parts for AWR294X ES1.0, AWR294X ES2.0, and AWR2544 devices that have been tested to work are shown in Table 2-3.

Table 2-3. Tested Flash Variants for AWR294x/AWR2544 Devices

Flash Vendor	Variant	Remarks
GIGADEVICE	GD25B64C	QE bit is set to 1 by default in the device.
MACRONIX	MX25V1635F	QE bit set by the vendor or it needs to be set in the sbl_uart_uniflash (flashwriter) .
	MX25L6433FM2Q-09G	
	MX25L3233FM2Q-08G	
ISSI	IS25LP032D	QE bit set by the vendor or it needs to be set in the sbl_uart_uniflash (flashwriter) .
	IS25LP064D	
WINBOND	W25Q32JV	QE bit set by the vendor or it needs to be set in the sbl_uart_uniflash (flashwriter) .
	W25Q64JV	

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2022) to Revision E (February 2024) **Page**

- Added introduction 2
- Added AWR2544, xWRL6432, and xWRL1432 devices..... 3

Changes from Revision C (November 2021) to Revision D (November 2022) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document..... 2
- Added Tested Flash Variants table to include flash variants tested on the AWR294x device. Changed IWR6843 to xWR6843 to include both all the variants of the device.....3

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