Application Report
SPRACM2–April 2019

Programming PLL Controllers on OMAP-L1x8/C674x/AM18xx

Catalog Processors

ABSTRACT

This document discusses the internal clocking architecture of Texas Instruments OMAPL1x/C674x/AM1x family using a provided clocking spreadsheet. The spreadsheet also provides guidance on max frequency supported by the PLL(s) and its SYSCLKs for a given operating point. This document applies to the following devices: OMAPL138, OMAPL132, C6748/46/42 and AM18x family.

The OMAP-L138, C6748/46/42 and AM18x family have similar internal clocking architecture. For more details on the differences between these devices, see the device-specific data manual.

The spreadsheet discussed in this document can be downloaded from the following URL: http://www.ti.com/lit/zip/spracm2.

Contents

Trademarks

1 Introduction

There are two PLL controllers on the OMAP-L1x8, C674x, and AM18xx devices. Each PLL controller has multiple output clocks and several configurations. The clock outputs of the PLL controllers are used to clock different parts of the device including the ARM, DSP, DDR2 controller, and device peripherals. Furthermore, each input and output clock has a frequency min and max that must be observed. Some of these frequency limits change with the operating voltage of the device.

2 Clocking Check Spreadsheet

The clocking check spreadsheet was created such that you can quickly check for frequency violations. The spreadsheet was created based on the PLL controller information in the OMAP-L138, C6748, AM1808 device-specific data manual (see Figure 1). You can enter several values including PLL multipliers and system clock dividers. The spreadsheet flags any timing violations. The operating core voltage of the device can also be specified. The spreadsheet adjusts the frequency limits based on the operating voltage.

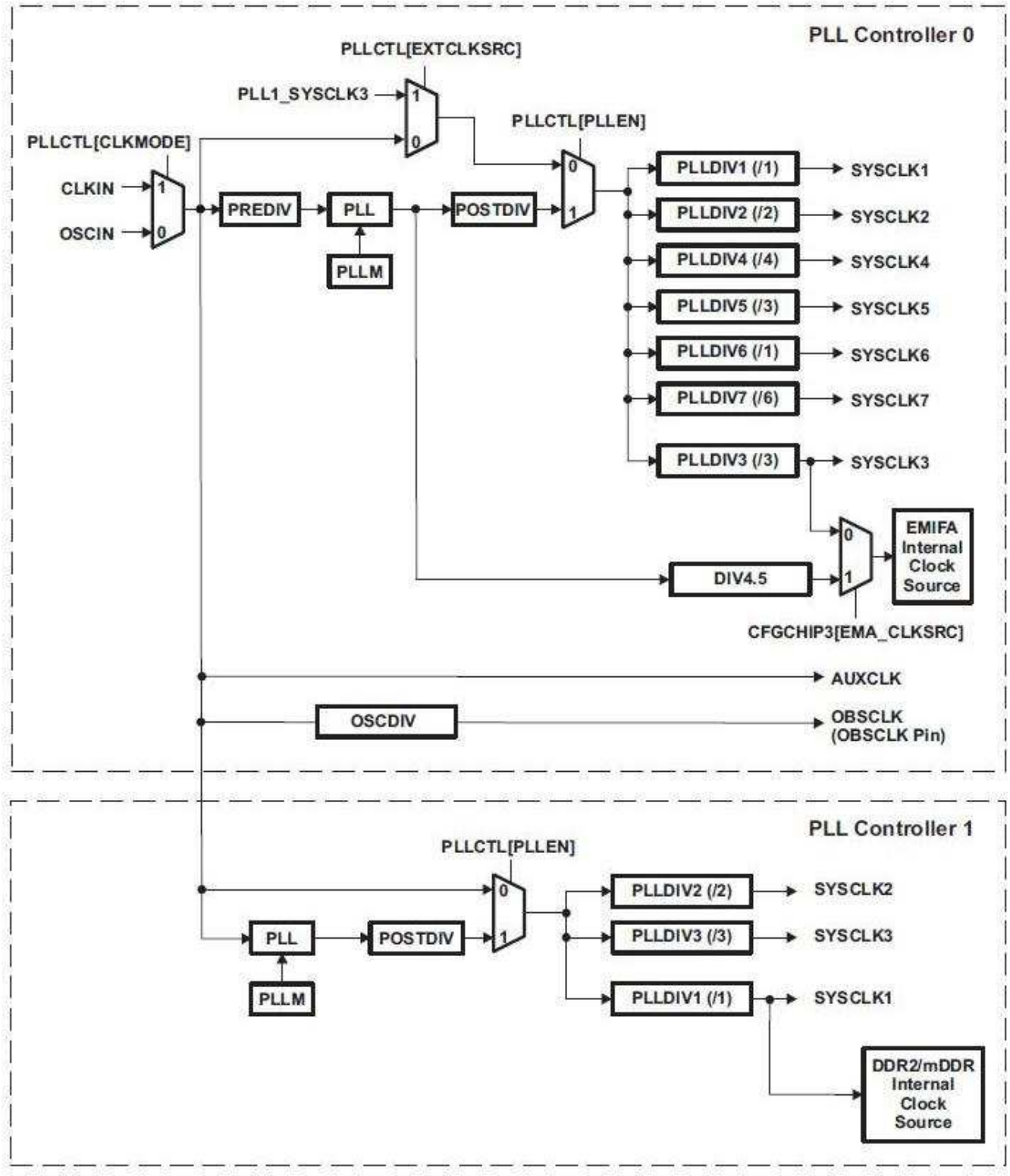

Figure 1. PLL Controller

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