Application Note

Hardware Design Guide for AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Family of Processors

ABSTRACT

This hardware design guide gives an overview of the design considerations to be followed by board designers using any of the AM625, AM623, AM625SIP, AM625-Q1 and AM620-Q1 family of processors. This application note is intended to be used at different stages of board design as a guideline by board designers. Additionally, links are provided for processor product page, related collaterals, E2E FAQs and other commonly referenced documents that could help the board designers optimize the design efforts and schedule during board design.

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1 Introduction

The Hardware Design Guide for AM625, AM623, AM625SIP, AM625-Q1 and AM620-Q1 family of processors provides a starting point for the board designers designing with any processor of the family of processors. This hardware design guide provides an overview of the recommended design flow and design stages, and highlights important design aspects and requirements that must be addressed. Note that this document does not include all of the information required to complete the board design. In many cases, this document refers to the device-specific collaterals and various other user guide as sources for specific information.

This hardware design guide (document) is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the board design, through the selection of key devices, electrical, and thermal requirements. For ensuring a successful board design, issues discussed in each of the section should be resolved before moving to the next section.

Note

The hardware design guide is applicable to ALW, AMC and AMK package processors.

The hardware design guide may not cover every aspect of the board design.

Note

These processor families have capabilities to address safety requirements.

The focus of the hardware design guide is non-safety applications.

1.1 Before Getting Started With the Board Design

The processor family includes wide variety of peripherals and processing capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same processor can vary widely depending on the target application. Board designers are expected to understand the requirements before selecting the processor and determining the board level implementation details. In addition, the board design may require additional circuitry to operate correctly in the target environment. Refer latest collaterals on TI.com including the device-specific data sheet, silicon errata, TRM and SK user's guide for selecting the processor and to determine the following:

- Expected environmental conditions for the processor operation, target boot mode, storage type and interfaces
- Processing (Performance) requirements for each of the cores in the selected processor
- External or Integrated memory, External DDR memory type, speed, size that will be used
- Processor peripherals used for the attached devices

1.2 Processor Selection

Selection of processor is the most important stage of board design. To get an overview of the processor architecture and for selecting the processor variant, features, package (ALW, AMC, AMK) and speed grade, refer the *Functional Block Diagram* and *Device Comparison* sections of the device-specific data sheet.

Select the AM625SIP processor when integrated memory (LPDDR4) is a requirement.

1.2.1 Note on AM625SIP Data Sheet

AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM data sheet references to AM62x Sitara™ Processor data sheet. The recommendation is to refer both the data sheets in combination when using AM625SIP processor.

1.2.2 AM625 and AM625SIP Board Design Compatibility

The AM625SIP processor uses a similar package as the ALW packaged AM6254 processor, where the AM625SIP AMK package has the same footprint as the AM6254 ALW package and most of the AM625SIP AMK package balls have the same signal function assignments as the AM6254 ALW package.

The AM625SIP ball assignment exceptions are listed in the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

Using AM625SIP as a drop-in replacement on an existing AM625 board is NOT recommended. Design changes are required to be made before using the AM625SIP on an AM625 board.

1.3 Technical Documentation

A number of documents relevant to the selected processor are available on the processor product page on TI.com. It is strongly recommended to read through these documents before starting the board design.

The links below summarizes the collaterals that can be referred when starting a custom board design.

[FAQ] AM625 Custom board hardware design – Collaterals to Get started

[FAQ] AM623 Custom board hardware design – Collaterals to Get started

[FAQ] AM625SIP Custom board hardware design – Collaterals to Get started

[FAQ] AM625-Q1 or AM620-Q1 Custom board hardware design – Collaterals to Get started

1.4 Design Documentation

Updating the design documents periodically to capture all the requirements, updates and observations during different stages of the board design is recommended. This updated information provides the foundation for the documentation package, and the design document is required when requesting external review support.

2 Block Diagram

A detailed block diagram, covering all the required functional blocks and interfaces is key to successful board design.

2.1 Constructing the Block Diagram

Preparation of a detailed block diagram is an important stage during the board design. The block diagram should include all major functional blocks, associated devices for processor functioning (Ex: PMIC) and attached devices. The block diagram should illustrate the interfaces and IOs used for interconnecting the processor and attached devices.

The below resources could be used as support documents when constructing the block diagram:

- SK-AM62B-P1 (AM625 / AM623 starter kit EVM with PMIC), SK-AM62-LP (AM625-Q1 / AM620-Q1 starter kit for low-power Sitara™ processors), SK-AM62-SIP (AM62x system-in-package (AM625SIP) starter kit for Sitara™ processors) and any other available SKs are a good source to start with the board design.
- The TI.com processor product folder links referenced below provides device-specific Functional Block Diagrams, Data Sheet, User Guides, Silicon Errata, Application Notes, design considerations, and other related information for different applications. The design and development section include SK information, design tools, simulation models and software information. As part of information related to support and training, links to commonly applicable E2E threads and FAQs are available.
  - AM625 Product Folder
  - AM623 Product Folder
  - AM625SIP Product Folder
  - AM625-Q1 Product Folder
  - AM620-Q1 Product Folder

2.2 Selecting the Boot Mode

It is recommended to indicate the configured boot mode in the block diagram. This includes the primary boot and the backup boot.

The processor family includes multiple peripheral interfaces that support boot mode. Examples include: eMMC, Multi-Media Card/Secure Digital (MMC/SD), QSPI, OSPI, GPMC NAND, GPMC NOR, Ethernet, USB (Device and Host), Serial Flash, xSPI and Inter-Integrated Circuit (I2C). The processor family supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode resistor configurations connected to the processor boot mode input pins provide information on the boot mode to be used by the ROM code during boot. The boot mode pins are sampled at power-on-reset (PORz_OUT), and the inputs must be stable before releasing (deassertion) the reset (MCU_PORz).

Boot mode configurations provide the below information:

PLL Config: BOOTMODE [02:00] – Indicates the system clock (PLL reference clock selection) frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration

Primary Boot Mode: BOOTMODE [06:03] – Select the required boot (primary) mode after POR, that is, the peripheral/memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected

Backup Boot Mode: BOOTMODE [12:10] – Select the required backup boot mode. This is the peripheral/memory to boot from, in case primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – This pin provides additional configuration options (optional - depends on the selected backup boot mode) for the backup boot devices

Reserved: BOOTMODE [15:14] – Reserved pins

Key considerations for boot mode configuration:

- It is recommended to always include provision to configure boot modes used during development, such as USB boot, UART boot or No-boot mode for JTAG debug.

- Boot mode pins have other functions after latching of boot mode configuration. Ensure the board design takes this into account when choosing pullup or pulldown resistors for the boot mode pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the processor is reset (indicated by the PORz_OUT pin) to enable the processor to boot properly.
- Some boot mode pins functionalities are reserved. Any boot mode pins marked as Reserved or not used must be tied high or low with pull resistors. They should not be left floating. For details regarding connection of reserved boot mode pins, refer the *BOOTMODE Pin Mapping* section of the *Initialization* chapter of the device-specific TRM.

For details regarding supported boot modes, refer the *Initialization* chapter of the device-specific TRM.

Note

Board designer is responsible to provide provision to set the required boot mode configuration (using pullups or pulldowns, and optionally jumpers/switches) depending on the required boot configuration.

Note

For updates related to supported boot modes and available boot mode functionality, see the device-specific silicon errata.

2.3 Confirming Pinmux (Multiplexing Compatibility)

The processor includes a number of peripheral interfaces. To optimize size, pin count and package while maximizing functionality, many of the processor pads (pins) provide provision to multiplex up to eight signal functions. Thus, not all peripheral interface instances would be available or can be used simultaneously.

TI provides SysConfig-PinMux Tool that helps board designer configure the required function using pin-multiplexing configuration tool for AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 family of processors.

Note

Recommendation is to save the pinmux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After completion of processor selection and block diagram updates, the next stage of the board design is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architectures that can be considered are listed below:

3.1.1 Integrated Power

The architecture could be based on Multi-channel ICs (PMIC), refer the *Powering the AM62x With the TPS65219 PMIC* application note.

3.1.2 Discrete Power

The architecture could be based on DC-DC converters and LDOs, refer the *Discrete Power Solution for AM62x* application note.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and recommended operating range, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details for some select power rails.

3.2.1 Core Supply

Core supplies VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 (only available on the AMC package) are always recommended to be powered by the same power source and can be operated at 0.75 V or 0.85 V. When these supplies are operating at 0.75 V, it is recommended to ramp-up 0.75 V prior to all 0.85 V supplies.

VDDR_CORE is specified to operate only at 0.85 V. When VDD_CORE is configured to operate at 0.85 V, VDD_CORE and VDDR_CORE are recommended to be powered by the same source to ramp-up together.

VDD_CANUART is recommended to be connected to always on power sources when Partial IO (low power) mode is used. It is recommended to connect VDD_CANUART to the same power source as VDD_CORE when Partial IO mode not used.

For more information, see the *Recommended Operating Conditions* table in the *Specifications* section of the device-specific data sheet.

Note

For selection of core voltage, see the *Operating Performance Points* section of the device-specific data sheet.

3.2.2 Peripheral Power Supply

The processor includes dedicated peripheral supply pins for USB (common for USB0 and USB1), CSIRX0, PLLs, OLDI0. The recommended operating voltage is 1.8 V. An additional 3.3 V analog supply is required for USB.

For more information, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 DDR PHY and SDRAM Power Supply

3.2.3.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

Depending on the memory selected DDR PHY IO (VDDS_DDR) and DDR clock IO (VDDS_DDR_C) supply rails can be 1.1 V (LPDDR4) or 1.2 V (DDR4).

For more information, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3.2 AM625SIP

VDDS_MEM_1P1 (LPDDR4 SDRAM IO supply (Sources the LPDDR4 SDRAM VDD2 and VDDQ power rails)) is recommended to be powered from the same power source as VDDS_DDR (DDR PHY IO supply).

VDDS_MEM_1P1 and VDDS_DDR power rails are connected to 1.1 V (LPDDR4).

VDDS_MEM_1P8 (LPDDR4 SDRAM Core supply (Sources the LPDDR4 SDRAM VDD1 power rail)) is 1.8 V.

For more information, refer the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

3.2.4 Internal LDOs for IO Groups (Processor IO Groups)

The processor includes nine internal LDOs, with the output of each connected to a pin (CAP_VDDSx [x=0-6], CAP_VDDS_CANUART and CAP_VDDS_MCU). A capacitor must be connected close to each of these LDO output pins. For guidance on the capacitor value and connection, refer the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

3.2.5 Dual-Voltage IOs (Processor IOs)

The processor includes nine Dual-voltage IO domains (VDDSHVx [x=0-6], VDDSHV_MCU and VDDSHV_CANUART), where each domain provides power to a fixed set of IOs. Each IO domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of IOs powered by the respective IO domain. All signals (attached devices) connected to these IO domains must be powered from the same power source that is being used to power the respective processor Dual-voltage IO domains (VDDSHVx supply rail). Most of the processor IOs are not fail-safe. For information on fail-safe IOs, see the device-specific data sheet. A valid supply voltage for the VDDSHVx supplies must be present before any input is applied to the associated peripherals or IOs.

IO grouping information is summarized below:

VDDSHV0 – Voltage for the General IO group

VDDSHV1 – Voltage for the Flash IO group

VDDSHV2 – Voltage for the GEMAC IO group

VDDSHV3 – Voltage for the GPMC IO group

VDDSHV4 – Voltage for the MMC0 IO group

VDDSHV5 – Voltage for the MMC1 IO group

VDDSHV6 – Voltage for the MMC2 IO group

VDDSHV_MCU – Voltage for the WKUP_MCU IO group

VDDSHV_CANUART – Voltage for the CANUART IO group

3.2.6 Dual-Voltage Dynamic Switching IOs

VDDSHV4, VDDSHV5 and VDDSHV6 have been designed to support power-up, power-down, or dynamic supply voltage change without any dependency on other supplies. This capability is required to support UHS-I SD Cards.

Integrated LDO required to support SD Card IO supply dynamic voltage switching is not provided internal to the processor. The selected LDO should be able to handle the required voltage transition.

3.2.7 VPP (eFuse ROM programming supply)

VPP power supply can be sourced on-board or externally. VPP pin can be left floating (HiZ) or pulled down to ground through a resistor during processor power-up and power-down sequences and during normal processor operation.

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must applied up after completion of proper processor power-up sequence.
- The VPP power supply has high load current transients and local bulk capacitors are likely required near the VPP pin to assist the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor. A maximum current of 400 mA is specified for programming. It is recommended to use a fixed LDO with higher input supply (2.5 V or 3.3 V) and enable input.
- If an external power supply is used, the supply is recommended to be applied after the processor power supplies are stable.
- When external power supply is applied for VPP, recommend adding bulk capacitor, decoupling capacitor and discharge resistor on-board near to the processor. Add a test point to connect external power supply and provision to connect one of the processor IO to control timing of the external supply.
- It is recommended to disable the VPP supply (left floating (HiZ) or grounded) when not programming the OTP.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application.

For more information, refer the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining Board Power Requirements

The current (maximum and minimum) requirements for each of the power supply rails are not available in the device-specific data sheet. These requirements are highly application dependent and must be estimated using TI provided tools for a specific use case.

3.4 Power Supply Filters

The processor includes multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x=0-2], VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0 and VDDA_1P8_USB. Filtered (ferrite) power supplies are recommended. For more information, see the [FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails. This is a generic FAQ and can also be used for AM625SIP, AM625-Q1 and AM620-Q1 family of processors.

3.5 Power Supply Decoupling and Bulk Capacitors

For general guidance on optimizing and placement of the decoupling and bulk capacitors, refer the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

3.5.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

To properly decouple the processor and attached device supplies from board noise, decoupling and bulk capacitors are recommended. Refer *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP* and other SK schematics for the required decoupling and bulk capacitors.

3.5.2 AM625SIP

To properly decouple the processor and attached device supplies from board noise, decoupling and bulk capacitors are recommended.

Additional bulk and decoupling capacitors are required to be connected to some of the reassigned processor pins due to the integrated LPDDR4 SDRAM. Refer *Starter Kit SK-AM62-SIP* schematic for the required decoupling and bulk capacitors.

3.5.3 Note on PDN target impedance

The PDN target impedance values are provided for the Core and DDR supplies. The PDN target impedance values are not provided for all supply rails since the target impedance calculation includes reference to the maximum current on the supply rails and is dependent on use case.

For updates on the PDN target impedance values, see the [FAQ] AM625 Custom board hardware design – Collaterals to Get started or E2E.

3.6 Power Supply Sequencing

A detailed diagram of the *Power Supply Sequencing* (Power-Up and Power-Down) are available in the device-specific data sheet. All power supplies associated with the processor should allow for controlled supply ramp (supply slew rate) and supply sequencing (using a PMIC-based power supply or using on-board logic when discrete power solution is used).

For more information, refer the *Power Supply Requirements, Power Supply Slew Rate Requirement, Power Supply Sequencing* section of the device-specific data sheet.

3.7 Supply Diagnostics

The processor includes below voltage monitors:

- VMON_VSYS (Recommend provisioning the external resistor voltage divider for early supply failure indication irrespective of the software implementation). For connecting the system voltage (main supply voltage such as 3.3 V, 5 V or other voltage levels) through an external resistor voltage divider, see the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet. It is recommend to implement a noise filter (capacitor) across the voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients.
- VMON_1P8_SOC and VMON_3P3_SOC (Monitoring): These pins are recommended to be connected directly to their respective 1.8 V and 3.3 V supplies. An internal resistor divider with software control is implemented inside the processor for each of these pins. For the allowed supply voltage range, see the *Recommended Operating Conditions* section of the device-specific data sheet.

For connecting the monitoring inputs when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

3.8 Power Supply Monitoring

For optimizing the custom board performance, consider provisioning for external monitoring of supply rails and load currents.

For more information, refer *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP* and *Starter Kit SK-AM62-SIP* schematics.

Now that the power supply architecture and the power supply devices for generating the supply rails have been finalized, update the block diagram to include the power supply rails and interconnection. It is also recommended to create a power supply sequence (Power-Up and Power-Down) diagram.

4 Clocking

The next stage of the board design is proper clocking of processor and attached devices. The processor clock can be generated internally using external crystal or an LVCMOS compatible clock input can be used. Follow the connection recommendations in the device-specific data sheet when using an external clock. This section describes the available processor clock sources and the requirements.

4.1 Processor Clock Inputs

The recommended processor clock inputs and connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25 MHz external main crystal interface pins connected to the internal high frequency oscillator (MCU_HFOSC0), is the default clock source for internal reference clock HFOSC0_CLKOUT.

Very few applications require WKUP_LFOSC0 and is optional. Based on the use case, select a 32.768 kHz crystal as clock source or 1.8 V LVCMOS square-wave digital clock source. For more information, see the [FAQ] AM625: LFOSC usage in the device. This is a generic FAQ and can also be used for AM623, AM625SIP, AM625-Q1 and AM620-Q1 family of processors.

4.1.1 Unused WKUP_LFOSC0

For guidance on the recommended connections for unused clock, refer the *WKUP_LFOSC0 Internal Oscillator Clock Source* section and *WKUP_LFOSC0 Not Used* sub-section in the *Specifications* chapter of the device-specific data sheet.

4.1.2 LVCMOS Digital Clock Source

The MCU_OSC0_XI and WKUP_LFOSC0_XI clock inputs can be sourced from a 1.8 V LVCMOS square-wave digital clock source. For more details, see the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators* section of the device-specific data sheet.

Note

Be sure to connect the MCU_OSC0_XO and WKUP_LFOSC0_XO pins as per the device-specific data sheet recommendation when using an external clock source.

4.1.3 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst case operating environment and expected life expectancy of the board being designed.

Verify the crystal selection with the crystal manufacturer as required.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding Crystal selection.

For more information, see the *MCU_OSC0 Crystal Circuit Requirements* and *WKUP_LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

4.2 Clock Outputs

Processor pins named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for the attached devices (external peripherals). WKUP_CLKOUT0 is a buffered output of the high frequency oscillator (HFOSC0) available during power-up as default.

For more details, refer the device-specific data sheet and TRM.

5 JTAG (Joint Test Action Group)

TI supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, it is recommend to include the JTAG connection in the board design.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires only five standard JTAG signals.
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the processor configuration.

For supported JTAG clocking rates, see the device-specific TRM.

The BSDL model for boundary scan testing can be downloaded from the below sections.

5.1.1.1 AM625 / AM623

- AM62x BSDL Model

5.1.1.2 AM625-Q1 / AM620-Q1

- AM62x AMC BSDL Model

5.1.1.3 AM625SIP

- AM62xSiP BSDL Model

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation signals are in same power domain. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 signals are powered by the VDDSHV_MCU (Dual-voltage IO) supply rail (IO supply for IO group MCU). VDDSHV_MCU can be configured either 1.8 V or 3.3 V.

For proper implementation of the JTAG interface, refer the *Emulation and Trace Headers Technical Reference Manual* and *XDS Target Connection Guide*.

5.1.3 Connection of JTAG Interface Signals

For connecting the JTAG interface signals, refer the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

In case JTAG interface is not used, it is recommended to always provide provision for connecting the JTAG interface signals using test points for development testing and the required pulls as per the *Pin Connectivity Requirements* section of the device-specific data sheet when a JTAG connector is not used.

6 Configuration (Processor) and Initialization (Processor and Device)

It is recommended to deassert (release) the processor cold reset input (MCU_PORz) only after all the supplies ramp and a recommended hold time (in ms) is provided for the crystal to start-up and stabilize (refer device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor includes three external reset input pins (MCU Domain cold reset (MCU_PORz), MCU Domain warm reset (MCU_RESETz) and Main Domain warm reset request (RESET_REQz)). Note the errata related to MCU_RESETz and MCU_RESETSTATz.

Be sure to make the recommended connections in the *Pin Connectivity Requirements* section of the device-specific data sheet.

The reset methods supported by the processor are described in detail in the device-specific data sheet and TRM.

The processor provides three reset status output pins (MCU Domain warm reset status (MCU_RESETSTATz), Main Domain POR (cold reset) status (PORz_OUT) and Main Domain warm reset status (RESETSTATz)). Note the errata related to MCU_RESETz and MCU_RESETSTATz.

Use of Reset status outputs are application dependent. Reset status outputs when not used can be left unconnected. It is recommended to provision for a test point for testing or future enhancements.

3.3 V inputs can be applied to MCU_PORz (3.3 V tolerant, fail-safe input). The input thresholds are a function of the 1.8 V IO supply voltage (VDDS_OSC0).

It is recommended to hold the MCU_PORz low during the supply ramp-up and crystal/oscillator start-up. Follow the recommended MCU_PORz timing requirement in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset modes are available through processor internal registers and emulation.

Note

MCU_RESETz and MCU_RESETSTATz have specific use case recommendation. Refer device-specific silicon errata.

6.2 Latching of Boot Mode Configuration

For more details about the processor boot mode options, see above Section 2.2.

Boot mode configurations for processor and Pin strap configuration for attached devices are latched at the rising edge of PORz_OUT. The device configuration and boot mode input pins have alternate multiplexed functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their alternate functions. The PORz_OUT reset status output indicates latching of boot mode configuration.

6.3 Resetting the Attached Devices

Recommended approach to implement the attached device reset is by using AND gate logic for on-board Media and Data Storage devices, and other peripherals as applicable. One of the AND gate input is the processor general purpose input/output (GPIO) pin and has provision for pullup and 0 Ω to isolate. The other input of the AND gate is the Main Domain POR (cold reset) status output (PORz_OUT) or Main Domain warm reset status output (RESETSTATz) signal. The choice of reset status output is application dependent. Ensure the attached device reset inputs are pulled as per the device recommendations.

In case an ANDing logic is not implemented and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the processor IO voltage level. A level translator is recommended to match the IO voltage level.

The power supply (3.3 V) for the SD Card needs to be connected through a controlled external power switch.

The power switch and power switch reset logic allows power cycling of the SD Card (since this is the only way to reset the SD Card) and place the SD Card back into its default state.

For more information on implementing reset logic for the attached devices and power switch enable logic for SD Card, refer *Starter Kit SK-AM62B-P1*, *Starter Kit SK-AM62-LP*, *Starter Kit SK-AM62-SIP* and other SK schematics.

6.4 Watchdog Timer

Use of watchdog timer is based on the application requirement. Consider using internal or external watchdog timer.

7 Processor Peripherals

This section covers the processor peripherals and modules, and is intended to be used in addition to the information provided in the device-specific Data Sheet, TRM, and relevant Application Notes. The three types of documents could be used as follows:

- Data Sheet: Pin Description, Device operational modes, AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Information regarding registers and configuration
- Application Notes: Board-level understanding and resolving commonly observed issues

7.1 Selecting Peripherals Across Domains

The processor architecture includes multiple domain, each domain includes specific processing cores and peripherals:

- Main Domain
- Microcontroller (MCU) Domain
- Wake-up (WKUP) Domain

For most use cases, peripherals from any of the domain can be used by any of the core. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access most of the peripherals in the MCU Domain. Similarly, MCU can access most of the peripherals in the Main Domain.

7.2 Memory (DDRSS)

7.2.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

DDR Subsystem supports LPDDR4 or DDR4 memory interface. Refer *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter of device-specific data sheet for data bus width, inline ECC support, speed and max addressable range selection.

The allowed memory configurations are 1 X 16-bit or 2 X 8-bit.

1 X 8-bit memory configuration is not a valid configuration.

Based on the application requirements, same memory (LPDDR4) device can be used with the AM625 / AM623 / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3 processors due to the availability of 1 X 16-bit configuration.

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the DDRSS signals when not used.

For more details, refer the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

7.2.1.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and DDR PHY have a large number of parameters to configure. To facilitate the configuration, an online tool (SysConfig tool) is provided that generates an output file that is consumed by the driver.

Choose DDR Subsystem Register Configuration from the Software Product pulldown menu and choose the required processor. This tool takes board information, timing parameters from DDR device data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then kicks off the full training sequence.

The SDK has an integrated configuration file for the memory (DDR4 / LPDDR4) device mounted on the SK. If you need a configuration file for a different memory (DDR4 / LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see the [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration. This is a generic FAQ and can also be used for AM625, AM623, AM625-Q1 and AM620-Q1 family of processors.

7.2.1.2 Calibration Resistor Connection

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations in the device-specific data sheet.

7.2.2 AM625SIP

LPDDR4 SDRAM (512MBytes) is internal (integrated) to AM625SIP. Refer *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter and *Integrated LPDDR4 SDRAM Information* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM) for speed and inline ECC support.

7.2.2.1 Reassigned DDRSS0 Pins on the AMK Package

The AM6254 DDRSS0 signals in the ALW package that would normally connect to an external SDRAM were connected directly to an integrated LPDDR4 SDRAM in the AM625SIP processor, and the pins associated with these signals were reassigned to different power or signal functions.

Refer *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

7.2.2.2 Calibration Resistors Connection

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations in the device-specific data sheet (AM62x Sitara™ Processor).

Follow the DDR_ZQ (LPDDR4 SDRAM Calibration Reference Resistor) connection recommendations in the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

7.3 Media and Data Storage Interfaces

Media and Data Storage interface supports 3 X Multi-Media Card/Secure Digital (MMC/SD/SDIO) ((8b+4b+4b) (8-bit eMMC on MMC0 (Refer *MMC0 - eMMC/SD/SDIO Interface* section of device-specific data sheet for speed), 4-bit SD/SDIO (Refer *MMC0 - eMMC/SD/SDIO Interface* and *MMC1/MMC2 - SD/SDIO Interface* sections of device-specific data sheet for speed))) interfaces, 1 X General-Purpose Memory Controller (GPMC) and 1 X OSPI/QSPI.

For information related to OSPI/QSPI, see the [FAQ] OSPI FAQ for Sitara/Jacinto devices.

For more details, refer the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Ethernet Interface Using Common Platform Ethernet Switch 3-port Gigabit (CPSW3G)

The CPSW3G interface can be configured either as a 3-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having their own MAC address.

CPSW3G supports RMII (10/100) or RGMII (10/100/1000) interface for each of the external Ethernet interface port.

For RMII interface implementation, refer the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G interfaces to EPHY configured for different configurations - external 50 MHz (Buffered External Oscillator or processor clock out) as EPHY clock input or 25 MHz EPHY clock input with 50 MHz clock output from EPHY.

One of the CPSW3G port is an internal CPPI (Communications Port Programming Interface) host port. It is a streaming interface to provide data from DMA to CPSW3G and vice-versa.

CPSW3G allows using mixed RGMII/RMII interface topology for the 2 X external interface ports.

RGMII_ID (internal delay) is not timed, tested, or characterized. RGMII_ID is enabled by default and the register bit is reserved.

For more details on the CPSW3G Ethernet interface, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Programmable Real-Time Unit Subsystem (PRUSS)

The processor provides two PRU subsystems and supports Universal Asynchronous Receiver/Transmitter (UART0), Enhanced Capture (ECAP0), Industrial Ethernet Peripheral (IEP0) modules.

For more details, refer the *Programmable Real-Time Unit Subsystem (PRUSS)* section in the *Processors and Accelerators* chapter of the device-specific TRM.

7.6 Universal Serial Bus (USB) Subsystem

The processor supports up to two USB 2.0 Ports. These Ports can be configured as host or device or Dual-Role Device (DRD). USBn_ID (identification) functionality is supported using any of the processor GPIO.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply connected to the USB interface connector).

VBUS (VBUS supply input including Voltage Divider / Clamp) input is recommended to be connected when the device is configured in device mode. Connection of VBUS (VBUS supply input including Voltage Divider / Clamp) is optional in host mode.

A power switch with OC (over current) output indication is recommended when the USB interface is configured as host. The USB DRVVBUS drives the power switch. It is recommended to connect the OC output to a processor GPIO, when the USB interface is configured as host.

For details related to USB connections and On-The-Go feature support, see the device-specific TRM.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

For connecting the USB pins when USB0 and USB1 are not used or USB0 or USB1 is not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information on USB2.0 interface, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – USB2.0 interface.

7.7 General Connectivity Peripherals

The processor supports multiple instances of UART, Serial Peripheral Interface (SPI), I2C, Multichannel Audio Serial Port (MCASP), Enhanced Pulse Width Modulator (EPWM), Enhanced Quadrature Encoder Pulse (EQEP), ECAP, CAN with CAN-FD support and GPIO modules.

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration. Refer *Pin Connectivity Requirements* section of device-specific data sheet.

When these open-drain output type buffer I2C interfaces are pulled to 3.3 V supply, the inputs have slew rate limit requirements. An RC is recommended to limit the slew rate.

An external pullup is recommended for the I2C interfaces with LVCMOS IOs emulated open-drain outputs. For the available LVCMOS IOs with emulated open-drain output I2C instances, refer the device-specific data sheet.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – I2C interface.

The number of peripheral instances available depends on the processor selection. The required interfaces can be configured using the SysConfig-PinMux tool based on the application.

For more details, refer the *Peripherals* chapter of the device-specific TRM.

7.8 Display Subsystem (DSS)

7.8.1 AM625 / AM623 / AM625SIP / AM625-Q1

The processor supports Dual (OLDI/LVDS (4 lanes - 2x) and 24-bit RGB parallel) display interfaces.

The processors have "Odd/Even" requirements when using OLDI in dual-link mode.

A0 - A3 correspond to the ODD pixels and A4 - A7 correspond to the even pixels.

OLDI/LVDS can be used in single link mode to connect to two displays. However, due to internal hardware configuration, both the displays are mirrored (duplicated).

For more information, refer below FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 Custom board hardware design – OLDI (Open LVDS Display Interface) capabilities

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM62A7 / AM62A3 Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the OLDI signals when not used.

For more details, refer the *Display Subsystem (DSS) and Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

7.8.2 AM620-Q1

Display interfaces (OLDI and DPI) are not supported.

7.9 Camera Subsystem (CSI)

The processor supports one Camera Serial interface (CSI-RX) - 4 Lane with DPHY-RX. Support for 1,2,3 or 4 data lane mode. Refer *Multimedia, Camera Serial interface (CSI-Rx) - 4 Lane with DPHY* section in the *Features* chapter of device-specific data sheet for supported data rate. Provided data rate information is for per lane, this will be updated in the next revision of the device-specific data sheet.

The DPHY-RX supports a single clock lane and all the data lanes are clocked at the same frequency. The frame rate is determined by start-of-frame, end-of-frame signaling and allows handling the input sources with different frame rates per channel.

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting interface pins and supply pins when CSI interface is not used.

For more details, refer the *Camera Subsystem* section in the *Peripherals* chapter of the device-specific TRM.

7.10 Connection of Processor Power Pins, Unused Peripherals and IOs

All the processor power pins must be supplied with the supply voltages specified in *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified.

The processor has pins (package balls) that have specific connectivity requirements and pins (package balls) that are recommended to be left unconnected or can be left unused.

7.10.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

For information on connecting the unused processor peripherals (USB0..1, DDRSS0, CSIRX0 and OLDI0) and IOs, refer the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

7.10.2 AM625SIP

For the AM625SIP processor, the DDRSS0 is internally connected to the LPDDR4 SDRAM device and the pads have alternate external connections. For connecting the reassigned (DDRSS0) pads, refer the *Reassigned DDRSS0 Pins on the AMK Package* table in the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

For information on connecting the unused processor peripherals (USB0..1, CSIRX0 and OLDI0) and IOs, refer the *Pin Connectivity Requirements* section of the *Terminal Configuration and Functions* chapter of the device-specific data sheet (AM62x Sitara™ Processor).

7.10.3 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type buffer, fail-safe IO. It is recommended to connect an external pullup resistor when external input is connected or a PCB trace is connected to the pad.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1/ AM620-Q1 / AM62A7 / AM62A3 Custom board hardware design – EXTINTn pin pullup connection.

7.10.4 Reserved Pins (Signals)

Pins named RSVD are Reserved. RSVD pins must be left unconnected. It is recommended not to connect any PCB trace or test points to the pins.

8 Interfacing of Processor IOs (LVCMOS or Open-Drain or Fail-Safe Type IO Buffers) and Simulations

An important check point during the board design before the schematic design and capture is to confirm electrical compatibility (DC and AC) between the processor and attached devices.

- The device-specific (processor and attached devices) data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, it is recommended to run IBIS simulations using IBIS models provided.

For more information, refer the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

The IBIS model can be downloaded from the below sections.

8.1 AM625 / AM623

- AM62x IBIS Model

8.2 AM625-Q1 / AM620-Q1

- AM62x AMC IBIS Model

8.3 AM625SIP

- AM62xSiP IBIS Model

9 Power Consumption and Thermal Analysis

The board power consumption depends on selected processor, peripherals connected, features implemented, application, operating temperature requirements, and temperature/voltage variations.

9.1 Power Consumption

For estimating the processor power, refer the *AM62x Power Estimation Tool*.

9.2 Maximum Current for Different Supply Rails

For information on the maximum current for different supply rails, refer the *AM62x Maximum Current Ratings*.

9.3 Power Modes

For more details on the available power modes, refer the *Power Modes* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for board designs using Sitara family of processors. This application report provides background information on common terms and methods. Any follow-up design support that may be required will be provided only for board designs that follow thermal design guidelines contained in the application report.

The Thermal Model can be downloaded from the below sections.

9.4.1 AM625 / AM623

- AM62x Thermal Model

9.4.2 AM625-Q1 / AM620-Q1

- AM62x AMC Thermal Model

9.4.3 AM625SIP

Reach out to TI using E2E to check on the availability.

10 Schematic Design, Capture and Review

At this stage of the board design, schematic design and capture can be started.

Refer below FAQ for the documents that could be referenced during schematics design and review of the schematics.

[FAQ] AM64x, AM62x, AM62Ax Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Refer below sections during the schematics design and capture stage:

10.1 Selection of Components and Values

Be sure to use the recommended values including the tolerance in device-specific data sheet as applicable when selecting the passive components.

10.2 Schematic Design and Capture

During the schematic design and capture stage of the board design, the schematics can be drawn newly or SK schematics can be reused.

Refer *Starter Kit SK-AM62B-P1* and *Starter Kit SK-AM62-LP* schematics for ALW and AMC packages and *Starter Kit SK-AM62-SIP* schematic for AMK package.

During schematic design and capture, follow *AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 Schematic Design and Review Checklist* and device-specific silicon errata.

The link below summarizes the considerations board designers are required to be familiar when reusing TI SK design files.

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design - Reusing TI SK (EVM) design files.

Note

When SK schematics are reused, ensure completeness of functionality and change in net name due to redesign are reviewed.

When SK schematics are reused, the DNI settings for the components could be reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality).

10.3 Schematics Review

After completing the schematic design and capture, verify the board design against the *AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 Schematic Design and Review Checklist*.

Plan an schematic review internally to review the schematics with reference to the *Schematic Design and Review Checklist*. Verify circuit implementation for design errors, value or connection inaccuracies, missing net connections, and so forth. Be sure to verify the schematics with *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers and Simulation

After completing the schematic design, capture and review (self, team and external), the recommendation is to perform floor planning of the board to determine the interconnect distances between the different devices, board size and outline.

The next stage in the board design is the layout. Refer below sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

Below application notes describe the recommended PCB escape routing for the processor.

- *AM625 / AM623 (ALW) Escape Routing for PCB Design*
- *AM625-Q1 / AM620-Q1 (AMC) Escape Routing for PCB Design*
- *AM625SIP (AMK) Escape Routing for PCB Design*

11.2 DDR Design and Layout Guidelines

11.2.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

Refer to *AM62x DDR Board Design and Layout Guidelines*. The goal of the guide is to simplify the DDR4 or LPDDR4 implementation. Requirements have been captured as a set of layout (placement and routing) guidelines that allow board designers to successfully implement a robust design for the topologies supported by the processor. Any follow-up design support that may be required will be provided only for board designs using DDR4 or LPDDR4 memories that follow the guidelines.

The target impedance is 40 Ω (single-ended) and 80 Ω (differential) for the DDR4 or LPDDR4 signals.

For the propagation delay, the delay to be considered for DDR4 or LPDDR4 is the delay related to the traces on the board.

In-case package level propagation delay is required, reach-out to the local TI sales representative.

Refer *AM62x DDR Board Design and Layout Guidelines* for DDR4 data rate, device bit width, device count and LPDDR4 Count, Channel Width, Channels, Die, Ranks. Guidelines for bit swapping is also included.

It is highly recommended to perform signal integrity simulations during board schematics design and layout stage.

Note

DDR2 and DDR3 not supported.

11.2.2 AM625SIP

Follow the recommendations in the device-specific data sheet (AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM) to connect the recommended power supplies and ground and DDR_ZQ (LPDDR4 SDRAM Calibration Reference Resistor).

Follow the recommendations in the device-specific data sheet (AM62x Sitara Processor) to connect the recommended DDR0_CAL0 (IO Pad Calibration Resistor).

Follow the *AM62x DDR Board Design and Layout Guidelines* and SK schematics to connect the LPDDR4 reset resistor (DDR0_RESET0_n).

Note

External DDR interface is not supported.

11.3 High-Speed Differential Signal Routing Guidelines

The *High-Speed Interface Layout Guidelines* application note provides guidelines for successful routing of the high-speed differential signals. Guidelines include PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. Any follow-up design support will be required will be provided only for board designs that follow *High-Speed Interface Layout Guidelines*.

Note

Consider using the Starter Kit SK-AM62B-P1 and Starter Kit SK-AM62-LP layouts as reference for ALW and AMC packages.

Consider using the Starter Kit SK-AM62-SIP layout as reference for AMK package.

11.4 Board Layer Count and Stack-up

11.4.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

The main constraint in determining layer count is the number of layers required to implement the high-speed DDR4 / LPDDR4 interface. Memory layout meeting the recommended guidelines typically requires the number of layers used in the Starter Kit (TI recommended). Optimization of layer count could be possible based on the board design and functionalities. Refer to package specific (ALW or AMC) *Escape Routing for PCB Design* guide. Use of TI Via Channel Array (VCA) technology with the ALW package supports further layer optimization.

Refer the *AM62x and AM62Ax DDR Board Design and Layout Guidelines* available on TI.com for further guidance and best practices in implementing the DDR4 / LPDDR4 interface.

11.4.2 AM625SIP

Integrated LPDDR4 optimizes simulation, design and layout efforts. Integrated LPDDR4 provides flexibility in optimizing the layer count.

Refer to the *AM625SIP (AMK) Escape Routing for PCB Design* guide that discusses a 4-layer escape for board design.

11.4.3 Simulation Recommendations

In case the number of layers are optimized, board level simulation is recommended.

11.5 Reference for the Steps to be Followed for Running Simulation

To get an overview of the basic system-level board extraction, simulation, and analysis methodologies to be followed for high-speed LPDDR4 interfaces, refer the *LPDDR4 Board Design Simulations* chapter of the *AM62Ax DDR Board Design and Layout Guidelines*.

12 Device Handling and Assembly

Moisture Sensitivity Level (MSL) rating/Peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, Lead finish/Ball material and the recommended MSL rating/Peak reflow to be followed.

For more information, see the links below:

AM625 Ordering and quality

AM623 Ordering and quality

AM625SIP Ordering and quality

AM625-Q1 Ordering and quality

AM620-Q1 Ordering and quality

12.1 Soldering Recommendations

Note the MSL rating/Peak reflow recommendation on TI.com for the selected processor.

12.1.1 Additional References

For more information on Moisture sensitivity level, refer below:

MSL Ratings and Reflow Profiles

Moisture sensitivity level search.

13 References

13.1 AM625SIP

- Texas Instruments: *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM*
- Texas Instruments: *Starter Kit SK-AM62-SIP*
- Texas Instruments: *AM625SIP (AMK) Escape Routing for PCB Design*
- Texas Instruments: *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*

13.2 AM625 / AM623

- Texas Instruments: *Starter Kit SK-AM62B-P1*
- Texas Instruments: *AM625 / AM623 (ALW) Escape Routing for PCB Design*

13.3 AM625-Q1 / AM620-Q1

- Texas Instruments: *Starter Kit SK-AM62-LP*
- Texas Instruments: *AM625-Q1 / AM620-Q1 (AMC) Escape Routing for PCB Design*

13.4 AM625 / AM623 / AM625-Q1 / AM620-Q1

- Texas Instruments: *AM62x DDR Board Design and Layout Guidelines*

13.5 Common for all AM62x family of processors

- Texas Instruments: *AM62x Sitara™ Processor Data Sheet*
- Texas Instruments: *AM62x Silicon Errata*
- Texas Instruments: *AM62x Sitara Processor Technical Reference Manual*
- Texas Instruments: *AM62x Schematic Design and Review Checklist*
- Texas Instruments: *AM62x Power Consumption Summary*
- Texas Instruments: *AM62x Maximum Current Ratings*
- Texas Instruments: *AM62x Power Estimation Tool*
- Texas Instruments: *Powering the AM62x With the TPS65219 PMIC*
- Texas Instruments: *Discrete Power Solution for AM62x*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto 7 High-Speed Interface Layout Guidelines*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*

14 Terminology

BSDL – Boundary-Scan Description Language

CAN – Controller Area Network

CAN-FD – Controller Area Network Flexible Data-Rate

CPPI – Communications Port Programming Interface

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

CSIRX – Camera Streaming Interface Receiver

DPI – Display Parallel Interface

DRD – Dual-Role Device

E2E – Engineer to Engineer

ECAP – enhanced Capture

ECC – Error-Correcting Code

eMMC – embedded Multi-Media Card

EMU – Emulation Control

EPWM – enhanced Pulse-Width Modulator

EQEP – enhanced Quadrature Encoder Pulse

GEMAC – Gigabit Ethernet Media Access Controller

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High-Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit

IBIS – Input/Output Buffer Information Specification

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

LVDS – Low Voltage Differential Signaling

MCASP – Multichannel Audio Serial Ports

MCU – Micro Controller Unit

MDIO – Management Data Input/Output

MMC – Multi-Media Card

OLDI – Open LVDS Display Interface

OSPI – Octal Serial Peripheral Interface

PCB – Printed Circuit Board

PMIC – Power Management Integrated Circuit

POR – Power-on Reset

PRUSS – Programmable Real-Time Unit Subsystem

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

SD – Secure Digital

SDIO – Secure Digital Input Output

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

VCA – Via Channel Array

WKUP – Wake-up

XDS – eXtended Development System

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2023) to Revision B (December 2023) **Page**

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