*Application Note*

# *AM62 Escape Routing for PCB Design*

**ABSTRACT**

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## Trademarks

# 1 Introduction

AM62x is an extension of the low-power, low-cost Sitara Industrial/Auto grade family of process. AM62x is based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, extensive peripheral and networking options for a variety of embedded applications. AM62x is available in a 13mm x 13mm FBGA package with a 0.5mm ball pitch. The package BGA design is built leveraging TI Via Channel Array Technology (VCA) technology, which enables package miniaturization while still utilizing low cost PCB routing rules. Via Channel Array (VCA) is built with careful considerations on escape routing to avoid costly High-Density Interconnect (HDI) and expensive Via technologies. This document is intended to provide a reference for escape routing on the AM62x device. Care must be taken to route signals with special requirements such as DDR, high speed interfaces. Refer to the High-Speed Interface Layout Guidelines and AM62x DDR Routing Guidelines for more details. Details on Power Delivery Network are provided in AM62x PDN Application note and any routing and layout requirements specified in those documents supersede the generic requirements provided here.

## 2 Via Channel Arrays

Via Channel Array Technology has been successfully used in a variety of TI products that helps in minimizing package dimensions by using smaller ball pitch and utilizing low cost PCB routing. Via Channel technology is a way of enabling routing channels to escape inner most BGA positions. This allows several advantages. First, the via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the BGA's in a tighter pitch, since all the vias are placed in special areas called *via channels*. This makes PCB manufacturing less expensive because larger vias are possible. Second, the vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of vias. The unique outer row routing and the via channel inner routing are two important parts of this technology on the AM62x. The AM62x BGA Via Channel Array is shown in Figure 2-1.

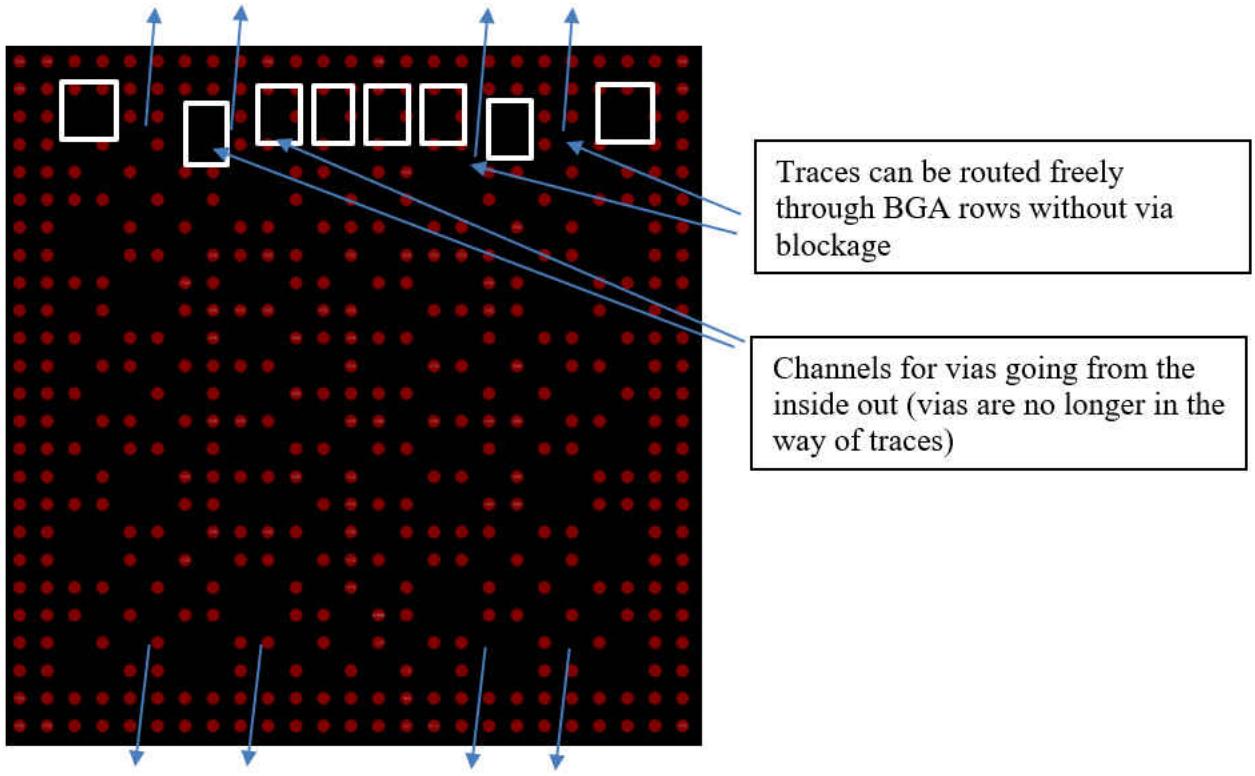


**Figure 2-1. AM62x BGA array with Via Channels**

For the first two rows (from the outside in) of the BGA array, the balls have been arranged to allow wider traces than would otherwise be possible. The first row (the outside row) supports any size trace desired, since the trace simply comes from the PCB ball land and goes out on the PCB. Normally, the second row traces must be routed in between the first row of the PCB ball lands. On this package, the second row traces are routed through an open channel where the BGA ball has been removed to allow wider traces. The AM62x parts allow a 3.2 mil trace/space in all areas, if routed correctly.

Figure 2-2 shows the first two rows of the AM62x package and how it is possible to route large 3.2 mil (mm) traces and spaces in the areas of removed balls.

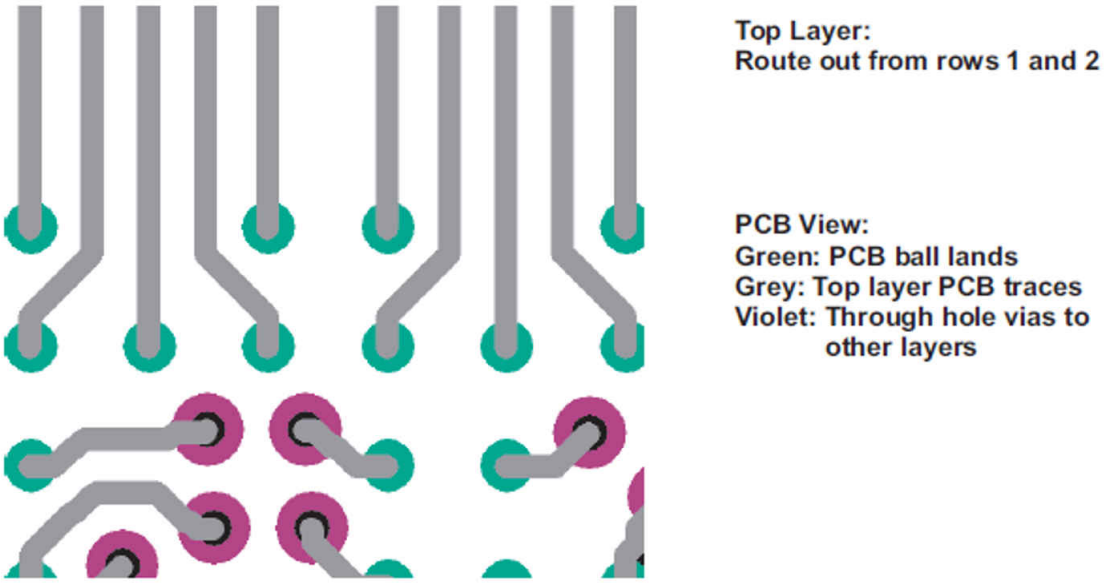


**Figure 2-2. Outer Rows of Traces**

Starting at the third row, as with any BGA package, vias are necessary. As stated before, the vias are gathered in the via channels, so the only vias that need to be placed in between balls are some of the power vias in areas of ground or power copper pour. In this case, they have no regular via ring since they are located in an area of copper pour where all the surrounding balls share the same net. This is elaborated more in the later section with details on via sharing. Since the via ring is larger than one that would normally fit in between these balls with the required clearance, the layout tool may flag a design rule check (DRC) error, however, this is a false warning since there is no risk of shorting to a nearby pad because they are all on the same net. The rest of the vias need to be placed into the via channels as shown below. Figure 2-3 shows how the vias are grouped in the via channels.

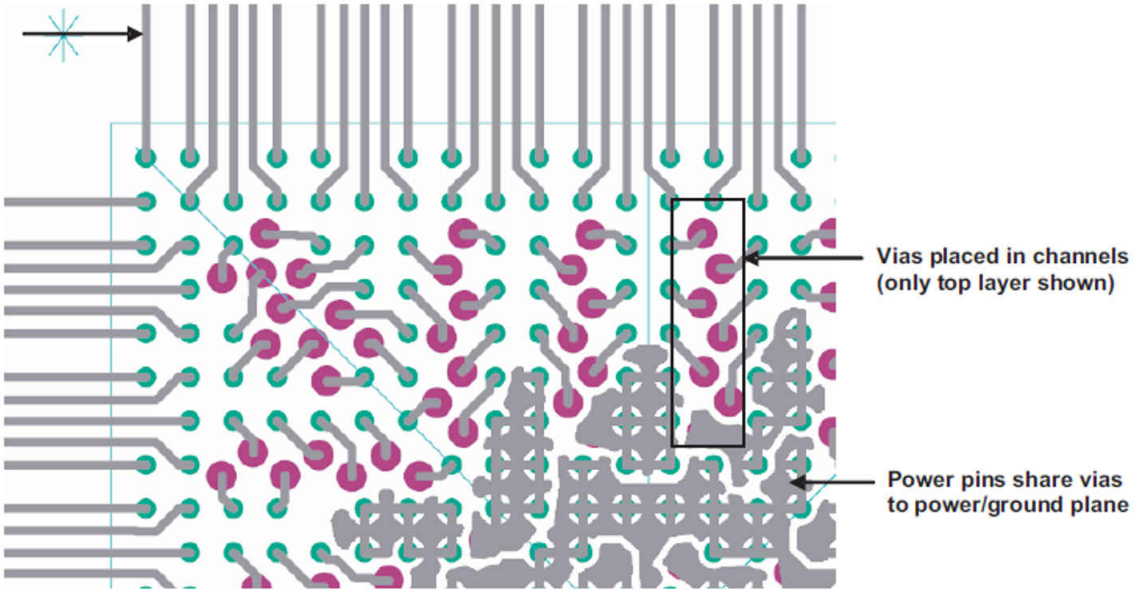


**Figure 2-3. Vias in Via Channels**

# 3 Width/Spacing Proposal for Escapes

The AM62x Via channel array solution has been designed to support the following. AM62x package supports similar feature set as several other competition solutions with approx. 15% smaller package area and ~10% wider line width. This solution therefore, reduces PCB foot print and utilizes lower cost PCB rules enabling compact and low-cost systems.

**Table 3-1. Width/Spacing Proposal for Escapes**

| PCB Feature | PCB Routing Requirements |
|---|---|
| Minimum via diameter | 18 mils |
| Via hole size | 10 mils (0.25mm) |
| Minimum trace width/spacing required in the BGA break out | 3.2mil / 3.2mil |
| Number of layers used for escape | 3 |
| BGA land pad size | 0.25mm via (typical) |
| Package Size | 13mm x 13mm, 0.5mm pitch w/ VCA |
| PCB layers (signal routing, total) recommended | 2, 6 |

# 4 Stackup

PCB stack-up is one of the first and important considerations in realizing a successful PCB. AM62x device supports a BGA array or 25x25 with a 0.5mm pitch and a body size of 13mm. Due to the number of rows of signal balls around the periphery, it is recommended to have two routing layers. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, it is recommended to allocate two layers for power planes. Ground planes will need to be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as DDR, CSI, USB require ground planes for impedance matching. Additionally, to meet the higher DDR interface speeds, ground layers both above and below the DDR signals are strongly recommended. The escapes on the AM62 board design was achieved with 6 layers as shown below.

**Table 4-1. Example PCB Layer Stack-up**

| PCB Layer | Layer Routing, Planes, or Pours |
|---|---|
| Layer 1 | Component pads, Ground and signal escapes |
| Layer 2 | Signal Routing |
| Layer 3 | Ground/Power |
| Layer 4 | Power/Ground |
| Layer 5 | Signal Routing |
| Layer 6 | Ground |
| | |
| | Table 1: Example PCB Layer Stack-up |

The AM62x board design example provided is implemented in a 6-layer stack-up as described above. This board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM62x board is implemented without HDI (High Density Interconnect) and does not use micro vias, which are both intended to save board cost. All vias on the AM62 board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis shall be performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

## 5 Via Sharing

The Via Channel Array BGA pattern implemented on the AM62 design offers several opportunities for via sharing. Vias are shared across BGA pins. Figure 5-1 and Figure 5-2 show the via sharing opportunities for VDDR_CORE and VSS domains, respectively. Figure 5-1 assumes that VDD_CORE and VDDR_CORE domains are separate. If these domains are merged, more via sharing opportunities are presented, as shown in Figure 5-3. Via sharing across BGA pins provides for easier escape routing and also stronger electrical connections by connecting multiple pins.

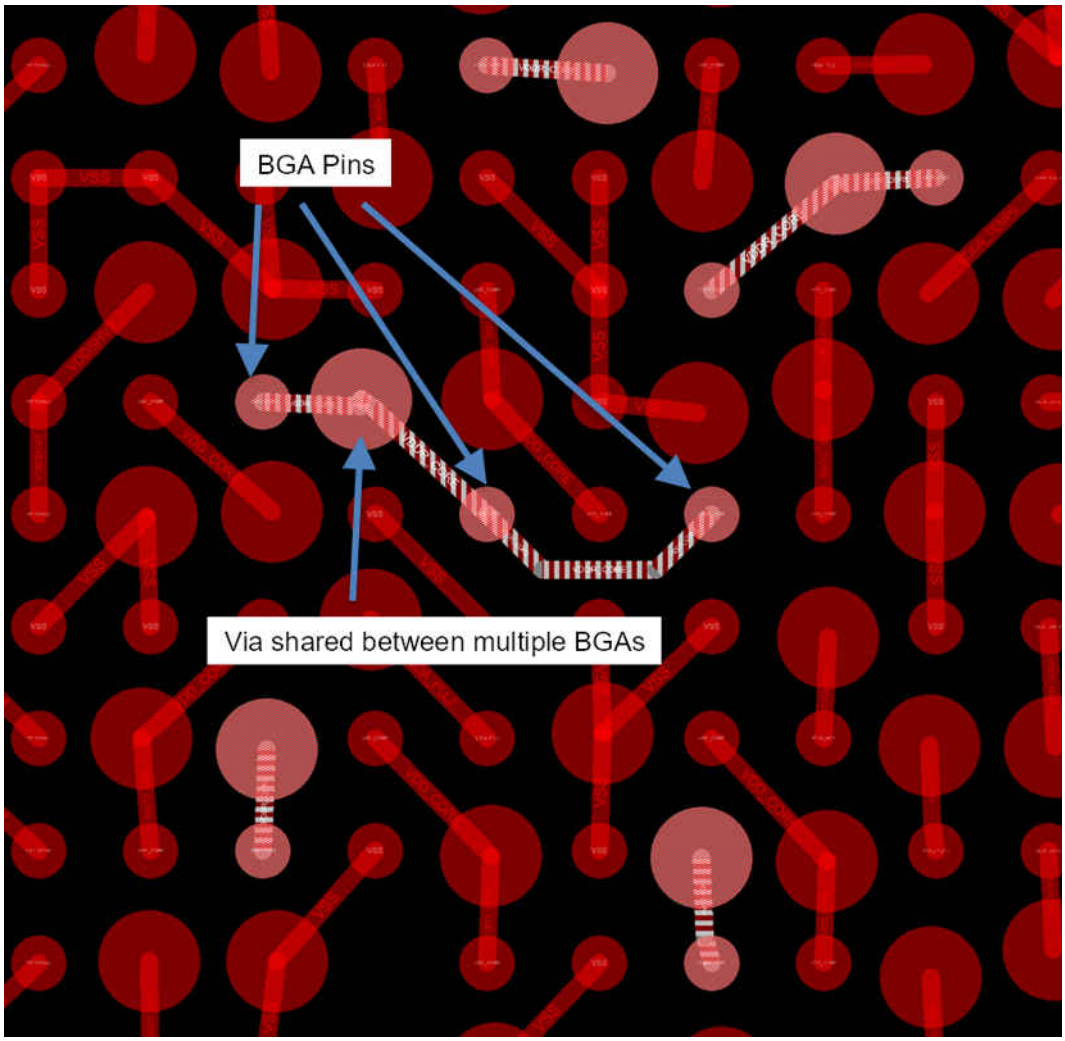


**Figure 5-1. Via Sharing for VDDR_CORE Domain**

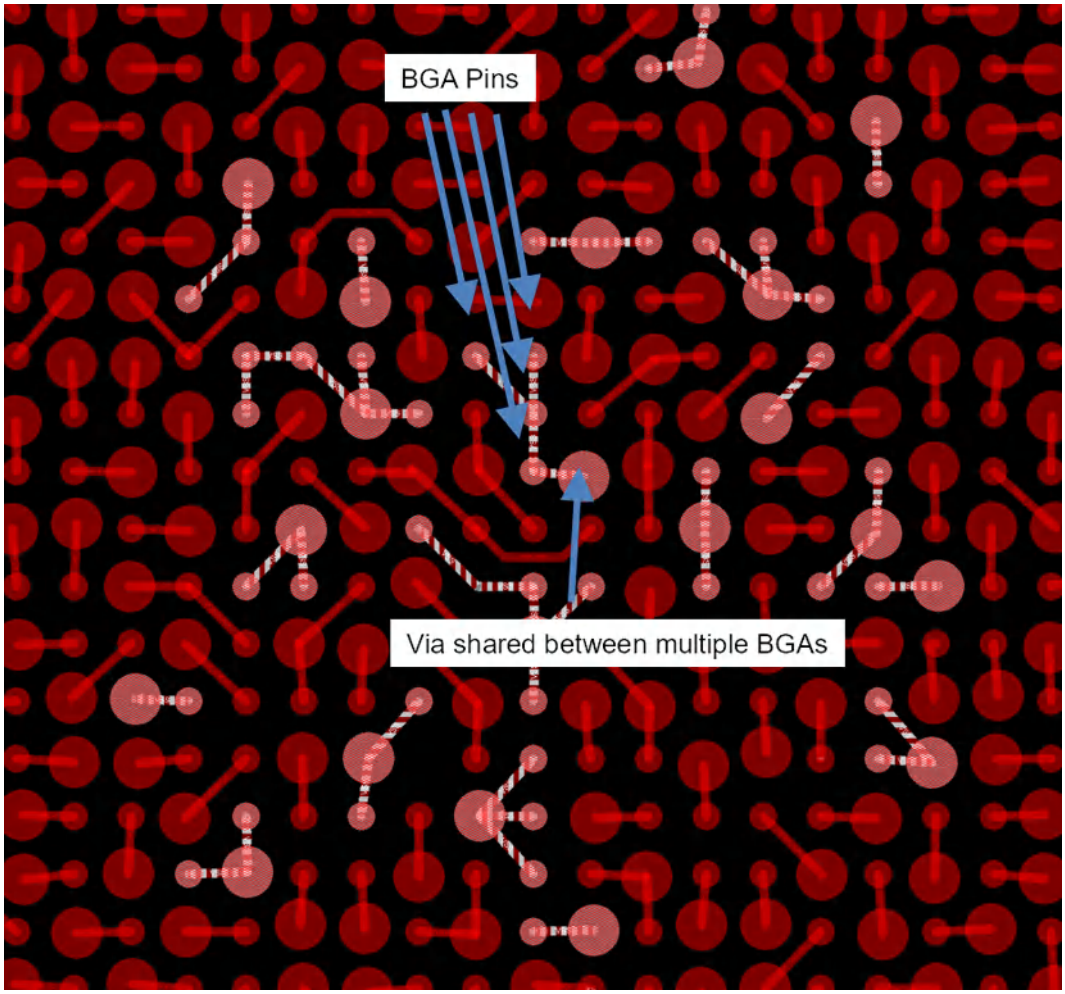


**Figure 5-2. Via Sharing for VSS**

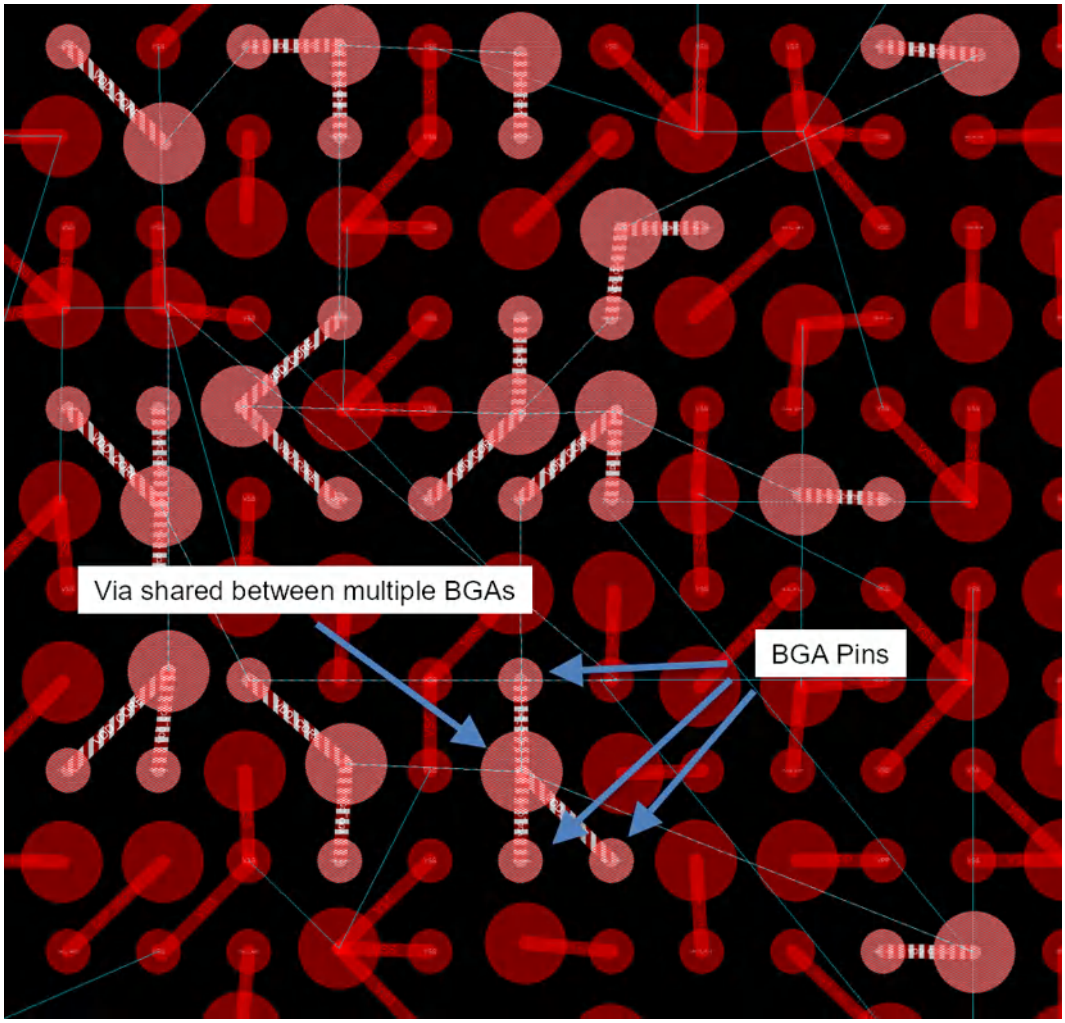


**Figure 5-3. Via Sharing for Merged VDD_CORE and VDDR_CORE Domains**

# 6 Floorplan Component Placement

Careful analysis is required to analyze the locations of the interfaces used on the device and the associated components and connectors. Optimum trace routing will have routes as short as possible with a minimum cross-over. AM62x offers interface selection flexibility through pin-mux choices. Pin-muxing enables a same interface function made available on multiple pins and is selectable through a pin mux option. Favorable pin-mux options that ease PCB routing and component placement can be fully utilized to further optimize the PCB design. The figure below shows the default arrangement of the signal balls as well as the power and ground balls. Priority shall be given to component placements without pin-mux options such as DDR, CSI, USB, OLDI/LVDS, and so forth.


**Figure 6-1. AM62 Floorplan**

# 7 Critical Interfaces Impact Placement

Placement of the AM62 device and some of the component and / or connectors will also be dictated by some of the highest performance interfaces such as DDR, USB etc. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

# 8 Routing Priority

As indicated above, critical interfaces will affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interface with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established.

Table 8-1 lists a recommended priority order for interfaces contained on the AM62 family of devices. Individual design requirements may drive a need for adjustment of the priorities but this serves as a good baseline and has been used for the board example illustrated in this document.

**Table 8-1. Routing Priority**

| Interface | Routing Priority |
|---|---|
| CSI | 10 (Highest Priority) |
| DDR4/LPDDR4 | 9 |
| OLDI | 9 |
| OSC | 8 |
| USB2, OSPI | 8 |
| Power distribution | 7 |
| RGMII | 6 |
| eMMC | 5 |
| Clocks | 5 |
| MII / RMII | 4 |
| SPI | 4 |
| Motor control | 4 |
| Analog | 3 |
| GPMC | 2 |
| GPIO | 1 |
| UART / CANUART | 1 |
| I2C / Temp Diode | 1 (Lowest Priority) |

The multi-gigabit Camera Serial Interfaces (CSI) are the most critical due to their data rate and loss concerns. CSI is at the top of the priority list because it is sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the CSI connector and the AM62 device. CSI signals are found on the outer layers of the BGA footprint, allowing some of the CSI traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. It is often left to last. This then results in poor decoupling performance and/or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling needs to be allocated before routing the middle and low priority interfaces.**

# 9 SerDes Interfaces

The package BGA ball map is also arranged to support routing the highest priority interfaces first. Therefore, the SerDes CSI interfaces are located on the outer two rings. The differential receive pair should be routed away from the SoC on the top layer leaving a gap without blocking vias. The lanes located on inner BGA rows will require vias to escape as a differential pair on the bottom or on an interior layer. The VCA facilitates this for inner rows. See Figure 9-1 for an example of the escape of the SerDes signals on the AM62 board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing Serdes signals refer to the document on High-Speed Interface Layout Guidelines. An example of the routing of CSI signals between the AM62 SoC and a connector on the AM62 SK EVM board is shown in Figure 9-2.

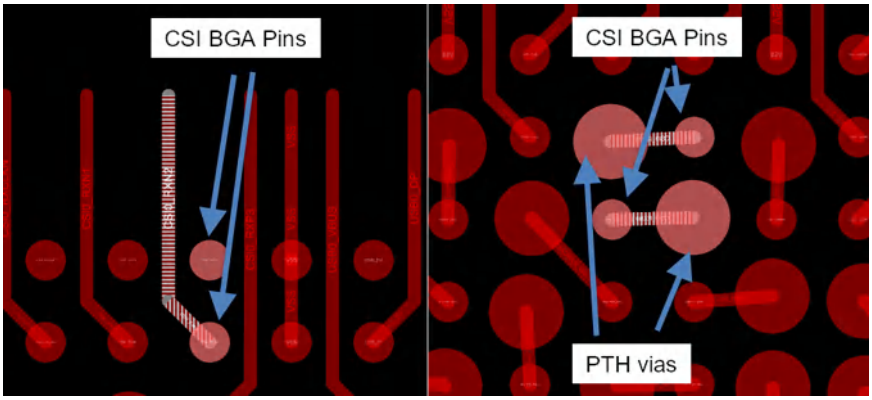


**Figure 9-1. Serdes CSI Escapes for TOP layer (Left) and Inner layer (Right)**

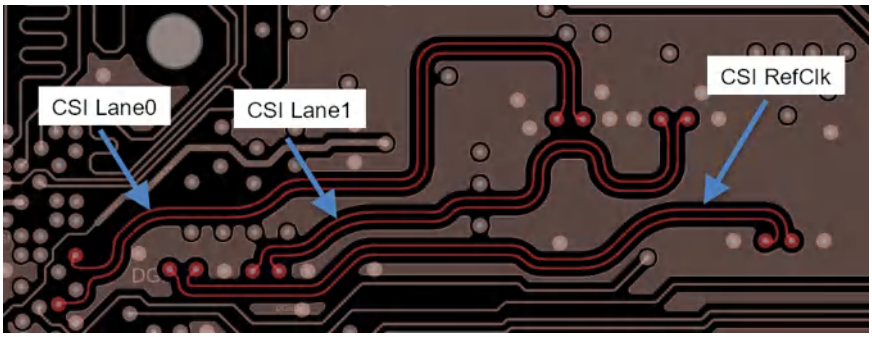


**Figure 9-2. CSI 2-Lane Routing**

# 10 DDR Interfaces

The AM62 supports connection to both DDR4 and LPDDR4 devices. The DDR signals must be routed next. Refer to the DDR Routing Guidelines document for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR interface on the AM62 Board. Routing for both DDR4 and LPDDR4 use a similar escape with LPDDR4 requiring lesser number of signals.

The DDR SDRAM memory devices are normally arranged so that the data group balls are closest to the AM62 device. The Package BGA ball map has been carefully planned to place the DDR address and command signals between data byte lane 1 and data byte lane0.

Figure 10-1 and Figure 10-2 show how to escape the DDR byte lanes 0 and 1, respectively. The use of Plated Through Hole (PTH) vias make the routing of these signals between the SoC and SDRAM possible on any layer. An example routing of the DDR data byte lanes on the AM62 SK EVM board is shown in Figure 10-3.

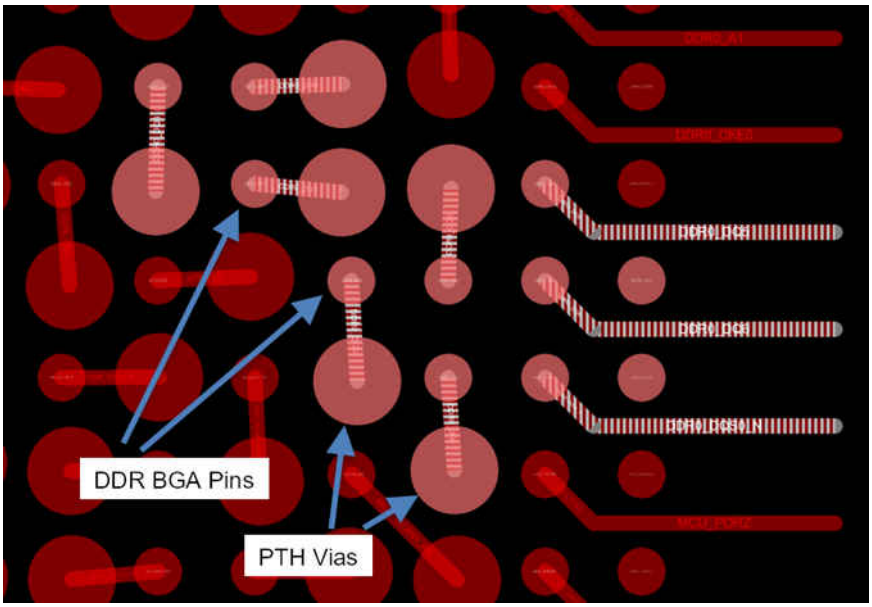


**Figure 10-1. DDR Byte Lane0 Escape**

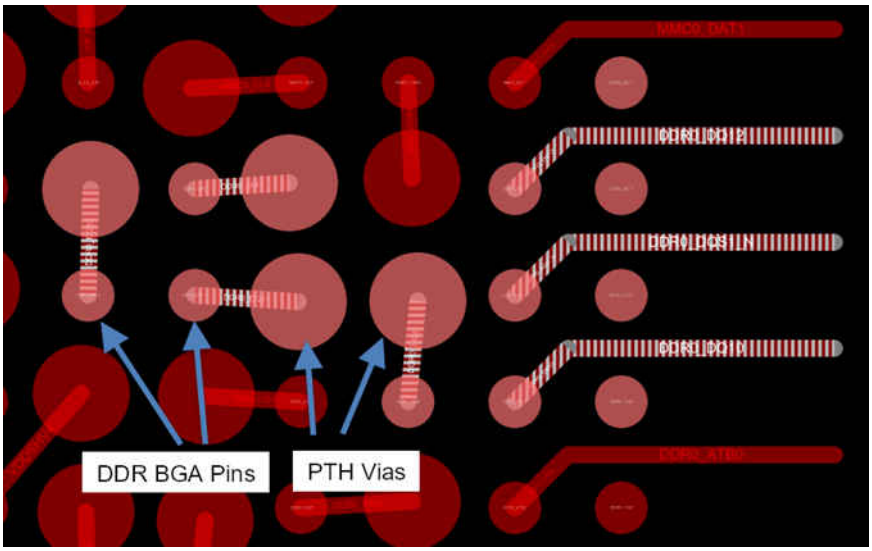


**Figure 10-2. DDR Byte Lane1 Escape**

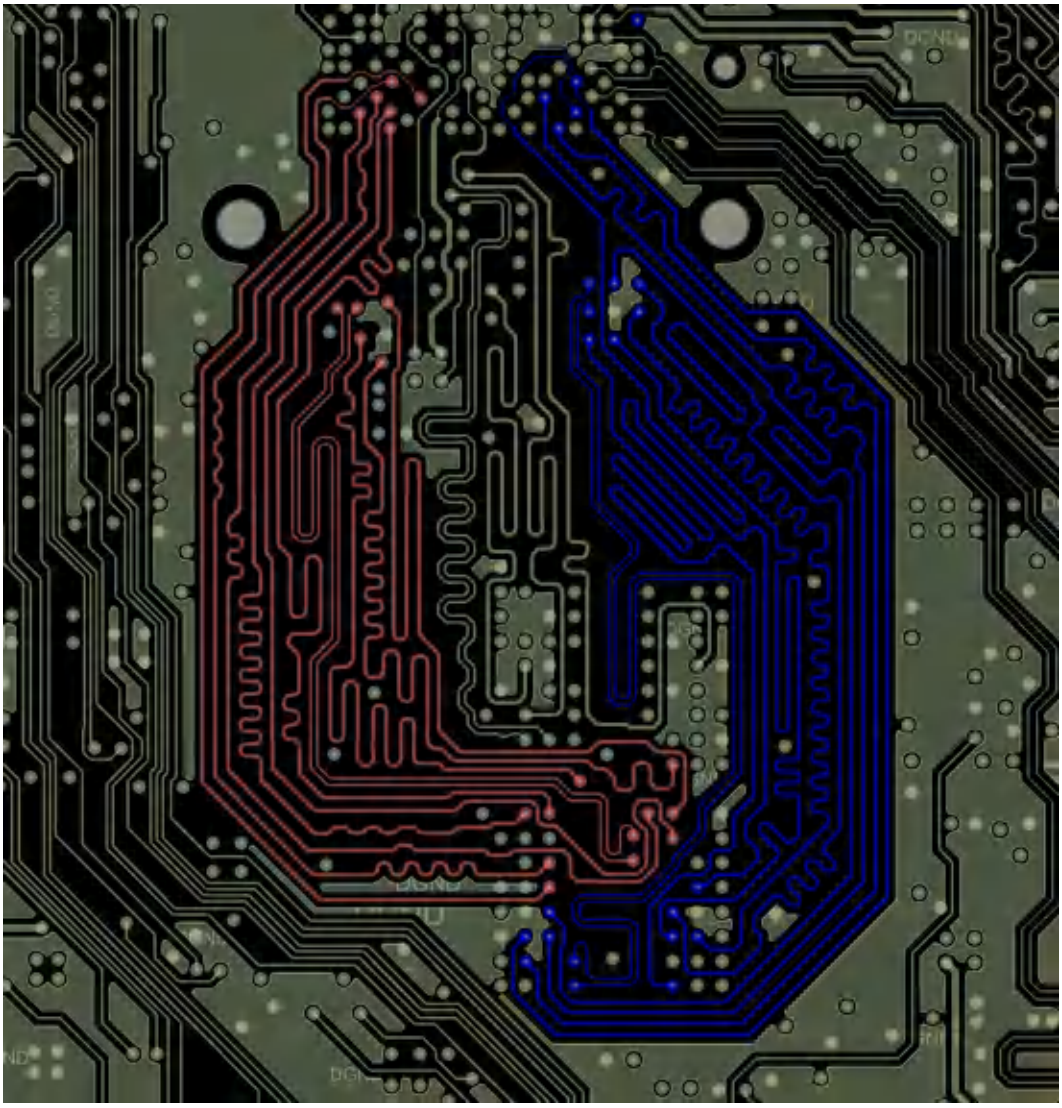

**Figure 10-3. DDR Data Byte Lane Routing (Byte Lane0 – Left; Byte Lane1 – Right)**

The address, command and clock signals are routed directly to the memory device. This design illustrates routing to a x16 DDR4 memory without VTT termination in a point to point topology. If 2 x8 DDR4 memory devices are used the address, command and clock signals should be routed in a fly-by manner with proper VTT termination.

The top and inner layers escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually and must include the stub to the memory pad and all via lengths. Refer to DDR Routing Guidelines for detailed recommendations for DDR routing.

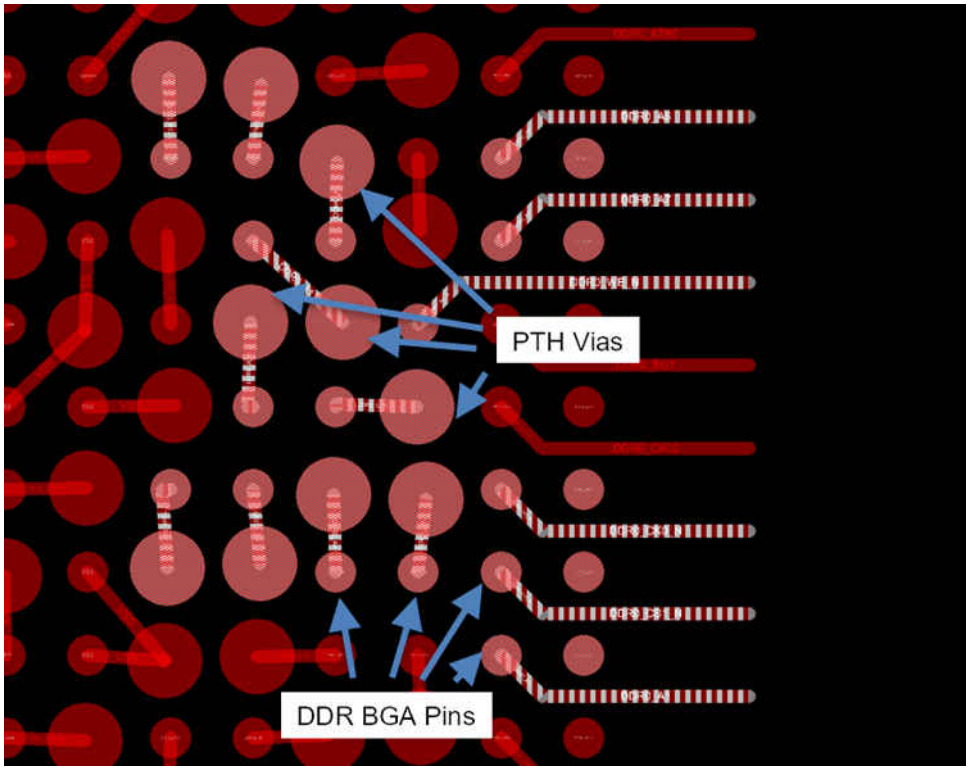


**Figure 10-4. DDR Address/Cmd Escape**

The escapes of the address and command signals on these layers are shown in Figure 10-4.

Address signals were routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. It is required to have the same number of vias for each of the address and command signals. The use of Plated Through Hole (PTH) vias allows the flexibility of routing the address/cmd signals on any layer.

Figure 10-5 shows an example of DDR4 Address, Command, and Clock group routing on the AM62 SK EVM board.

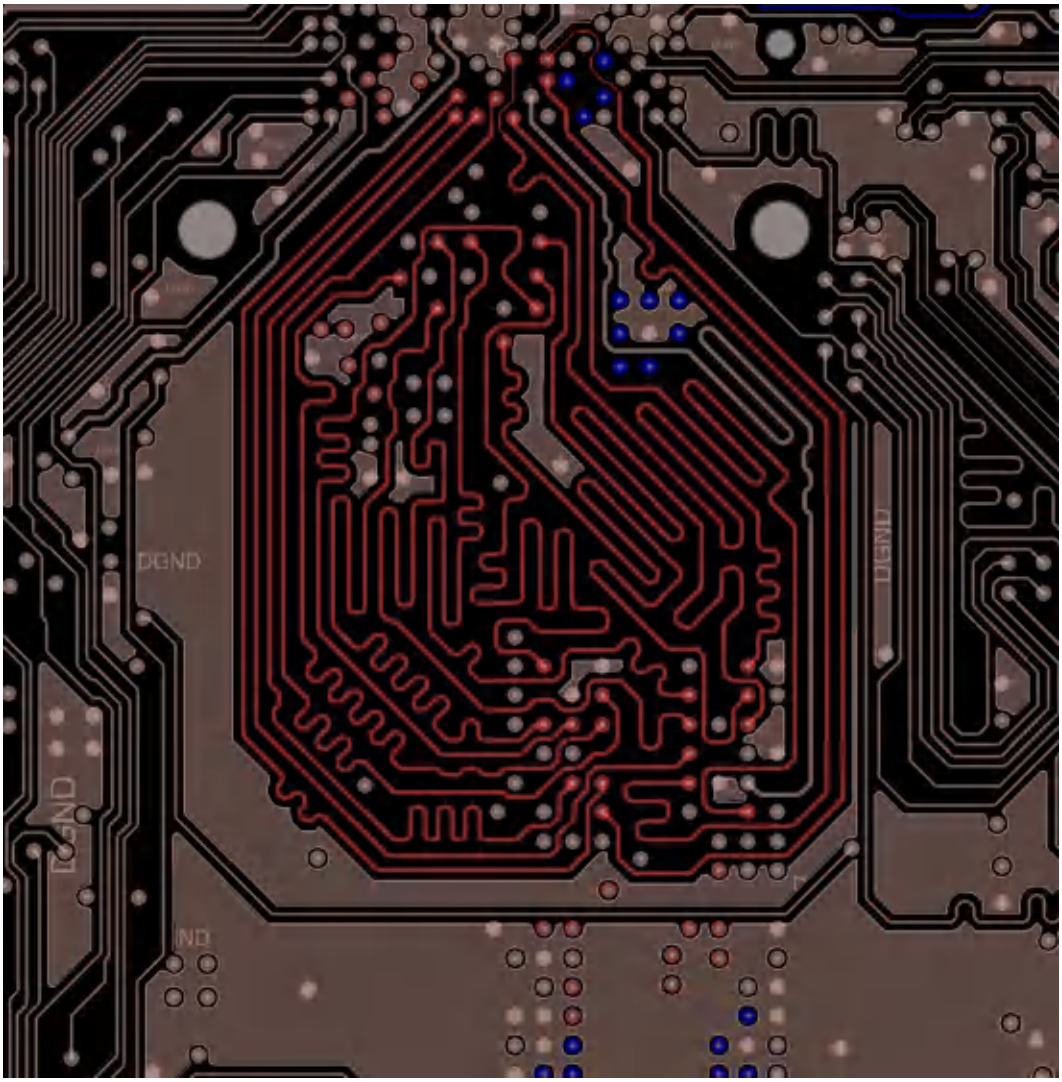


**Figure 10-5. DDR4 Address, Command, and Clock Group Routing**

# 11 Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed next after the SERDES and DDR interfaces. TI recommends completing all SERDES and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SERDES and DDR routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation, thus these also may need to be completed at this time.

Special care is needed for the 1-uF output capacitors connected to the CAP_VDDS* BGA pins on the AM62 device. These capacitors should be placed as close to the pin as possible, and a low inductance path should be present between the CAP_VDDS BGA pin and the supply pad on the capacitor. The layout used on the CAP_VDDS0 net on the AM62 SK EVM is shown in Figure 11-1. Note the sharing of the GND pad of the capacitor with other capacitors in the vicinity, which allows saving routing resources. Also, keep the PTH vias for the capacitor power and GND pad connections as close to each other as possible to minimize the loop inductance.

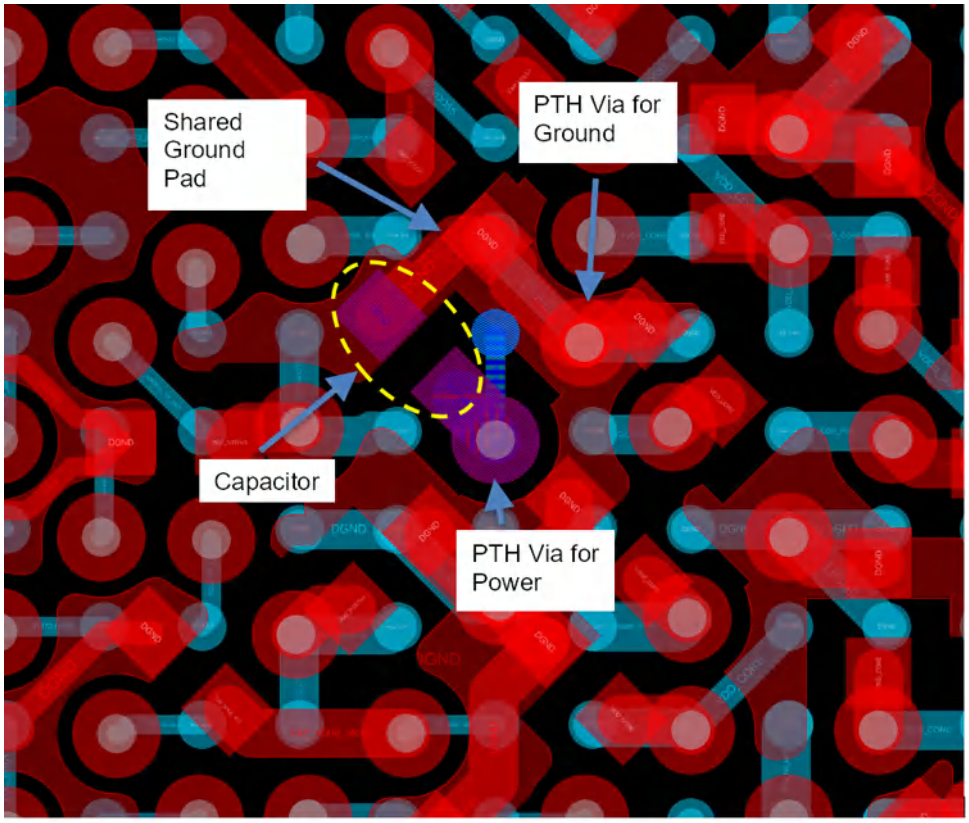


**Figure 11-1. AM62 SK EVM Output Capacitor Placement for CAP_VDDS0**

This placement can be improved if the capacitors can be placed directly under the SoC. The decoupling capacitors for the VDD_CORE and VDDS_DDR supplies should also receive the same priority as those on the CAP_VDDS* pins, and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62 device.

## 12 Route Lowest Priority Interfaces Last

When the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium, then the lower priority interfaces.

# 13 Summary

The via channels have been carefully co-designed to ensure escapes for all signals and power while meeting the respective signal and power integrity goals for each interface. A summary of all via channel arrays and vias for the different signal and power supply nets is shown in Table 13-1.

**Table 13-1. Via Channel Summary**

| Net | #VCA | #Vias | #Pins |
|---|---|---|---|
| Signals | 146 | 146 | 146 |
| VSS | 21 | 20 | 43 |
| VDD_CORE | 11 | 11 | 17 |
| VDDR_CORE | 5 | 5 | 8 |
| VDDS_DDR | 4 | 4 | 4 |
| VDDSHV0 | 1 | 1 | 2 |
| VDDSHV1 | 1 | 1 | 2 |
| VDDSHV2 | 2 | 2 | 2 |
| VDDSHV3 | 2 | 2 | 4 |
| VDDSHV4 | 1 | 1 | 1 |
| VDDSHV5 | 1 | 1 | 1 |
| VDDSHV6 | 1 | 1 | 1 |
| VDDSHV_MCU | 1 | 1 | 2 |
| VDDSHV_CANUART | 1 | 1 | 1 |
| VDD_CANUART | 1 | 1 | 1 |

Notes:

1. Outer two rows are fully fanned-out on top layer with no VCAs or Vias. This includes a handful of VSS balls (in the outer two rows) which are not included in the table.
2. There are a total of 200 VCAs; one is not used (J15 location), one is used for routing (M14 for VSS), all others have a Via.
3. Any net not specifically listed above is either fanned out directly on outer layer, or is counted in the “signals” row with 1 via per 1 pin (this includes VDDA_x and CAP_VDDx nets that are considered as power nets).

A picture showing AM62x with all signals and power escaped is shown in Figure 13-1.

An example layout file for the fully escaped design can be downloaded here.

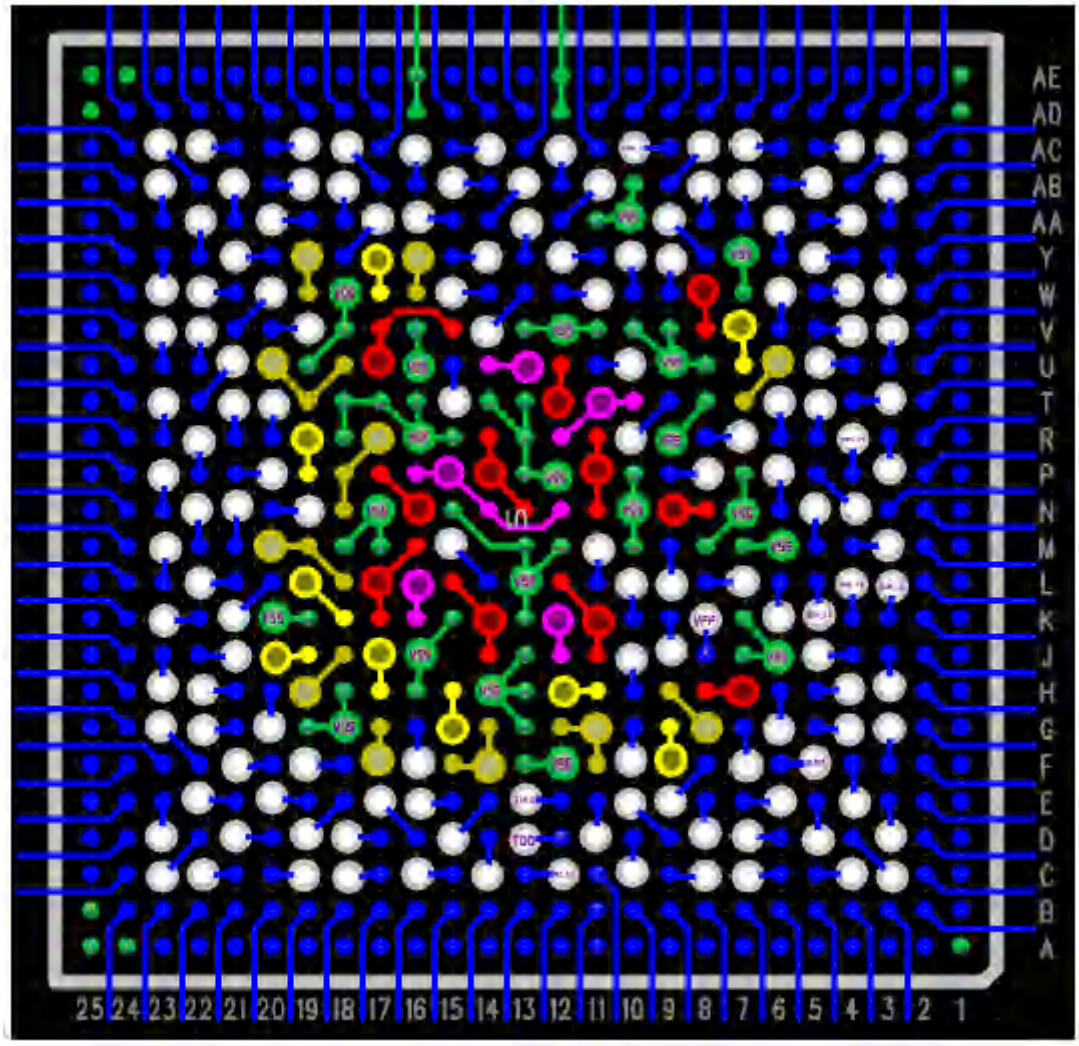


**Figure 13-1. AM62x with Complete Signal and Power Escapes**

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