Application Note

Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)

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ABSTRACT

In many industrial and automotive applications, an increasingly important requirement is the ability to continually monitor systems and enter appropriate fail-safe states. Particularly in real-time control applications, being able to detect potential faults and perform necessary actions within the system can prevent damage to the system and help support functional safety. This application note describes a technical diagnostic application involving a delta-sigma modulator interfaced with a C2000 microcontroller. The configurable logic block (CLB) peripheral in C2000 real-time MCUs can be utilized for test and measurement applications to provide a greater insight into the status of current and voltage feedback systems making use of delta-sigma modulators.

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1 Introduction

Enhanced monitoring and diagnostic features integrated within control systems enable increased system reliability and risk mitigation. In the scheme described within this report, C2000 real-time microcontroller devices' advanced features are used to monitor the status of a delta-sigma modulator. Specifically, the output bitstream, which encodes the digital conversion output of an AMC1306x modulator and is connected to a TMS320F28004x MCU for filtering, is monitored to determine if the high-side of the isolated modulator is powered.

The delta-sigma modulator outputs a bitstream of 1s and 0s, where the density of 1s is proportional to the input analog voltage. A differential input signal of 0 V ideally produces a stream of 1s and 0s that are high 50% of the time and low 50% of the time. A large density of 1s corresponds to a greater input voltage. It features additional fail-safe conditions, described in AMC1306 Bitstream & Fail-Safes, which can be used to identify potential problems in the system. For more information about the AMC1306x device, see the *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI Data Sheet*.

The configurable logic block on C2000 devices is a peripheral composed of various submodules that assist in performing logic operations independent of the CPU. This peripheral can be used in place of an external FPGA or CPLD to execute complex device logic. The clock and bitstream, which are necessary inputs into the SDFM module when in Mode 0 operation, can be routed to the CLB peripheral purely through software, and CLB can diagnose the output bitstream of delta-sigma modulators. For more information about the TMS320F28004x device, see the *TMS320F28004x Data Sheet*.

2 System-Level Application

Delta-sigma modulation is used to measure current and voltage levels in power systems such as the AC motor drive shown in Figure 2-1. Shunt-based isolated delta-sigma modulators are often used for current and voltage sensing in 3-phase inverters due to their high accuracy and high bandwidth, while offering lower system cost.

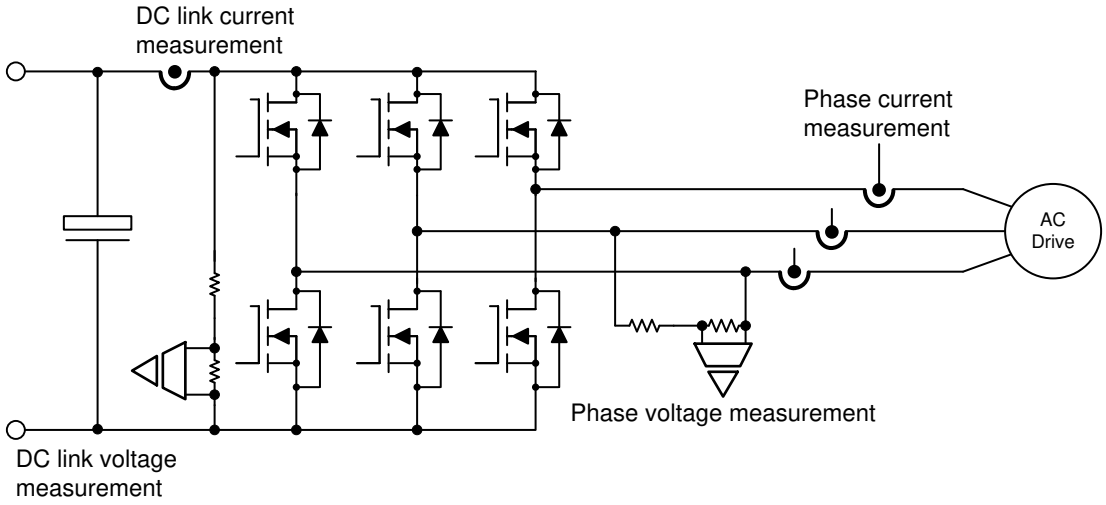

Figure 2-1. Current and Voltage Measurement in Three-Phase Inverters

Delta-sigma modulators are ADCs that allow for continuous oversampling of analog inputs through a delta-sigma modulator and require a digital/decimation filter. The voltage drop across a shunt resistor can be measured by a delta-sigma modulator to enable current sensing. A delta-sigma modulator converts an analog input signal into a high-frequency stream of single bits with out-of-band noise. The advantages of moving the quantization noise to higher frequency bands include simple anti-aliasing filtering, low-cost solution by eliminating cost on drivers, and scalable performance. This leads to reduced overall system cost while providing high performance.

Figure 2-2 shows a block diagram showcasing shunt resistor and delta-sigma modulator for phase current measurement in a three-phase inverter design.

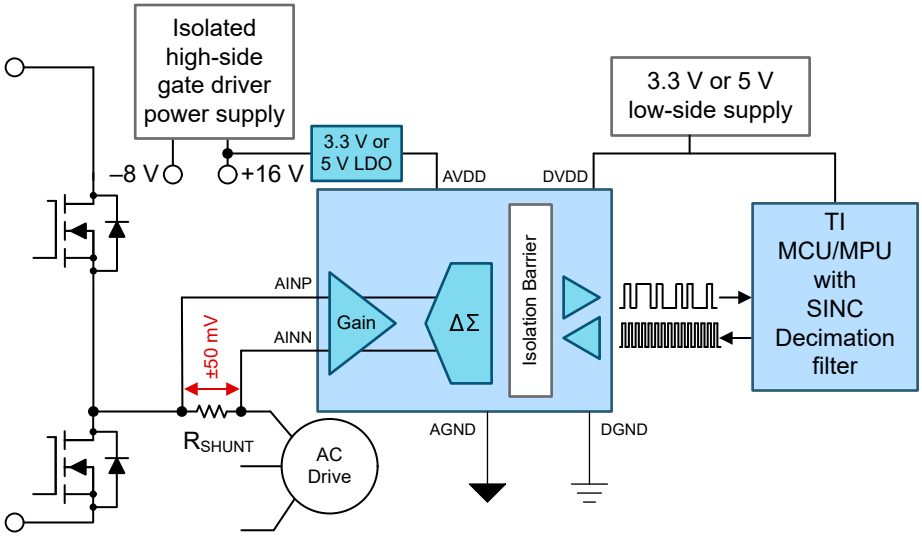

Figure 2-2. Delta-Sigma Modulator in Three-Phase Inverter

The AMC1306 device requires a low-side supply which can be supplied by the 3.3 V rail supplying the C2000 device. The AMC1306 also requires an isolated 3.3 V or 5 V high-side supply (AVDD) which is generated from the isolated high-side gate driver supply by an LDO. The AMC1306 takes as inputs the differential voltage across the shunt resistor on the high-side and the clock supplied by the C2000 device on the low-side. The output of the modulator can be fed into the SDFM peripheral of the C2000 device.

The AMC1306 device's fail-safe conditions, which are described in greater detail throughout this report, provide indication into potential system faults.

One of the fail-safe conditions occurs when the high-side power supplied into the AMC1306 device is not present. Presence of this fail-safe could indicate an issue with the high-side gate driver supplying AVDD. It could also indicate an issue with the LDO used to step-down the voltage into the device.

Another fail-safe condition, known as common mode overvoltage, can be used to indicate a missing or disconnected shunt resistor. If AINN or AINP is disconnected from the shunt resistor, the input bias current of the AMC1306 drives the disconnected terminal towards the positive supply rail, and the common-mode input voltage increases. A similar effect happens when there is no DC current path between AINN, AINP, and AGND. This fail-safe condition is useful to identify interconnect problems on the board.

3 AMC1306 Bitstream and Fail-Safes

The AMC1306 device features four fail-safe conditions depending on different scenarios that could potentially impact the delta-sigma modulator and the system. These fail-safe conditions have predefined effects on the bitstream output produced and therefore can be analyzed by the MCU to detect and distinguish between the different fail-safe conditions.

Figure 3-1 shows the AMC device used requires a 5 V or 3.3 V high-side supply voltage (AVDD). When AVDD is not present, the DOUT output of the modulator remains low for the entire duration that AVDD is missing.

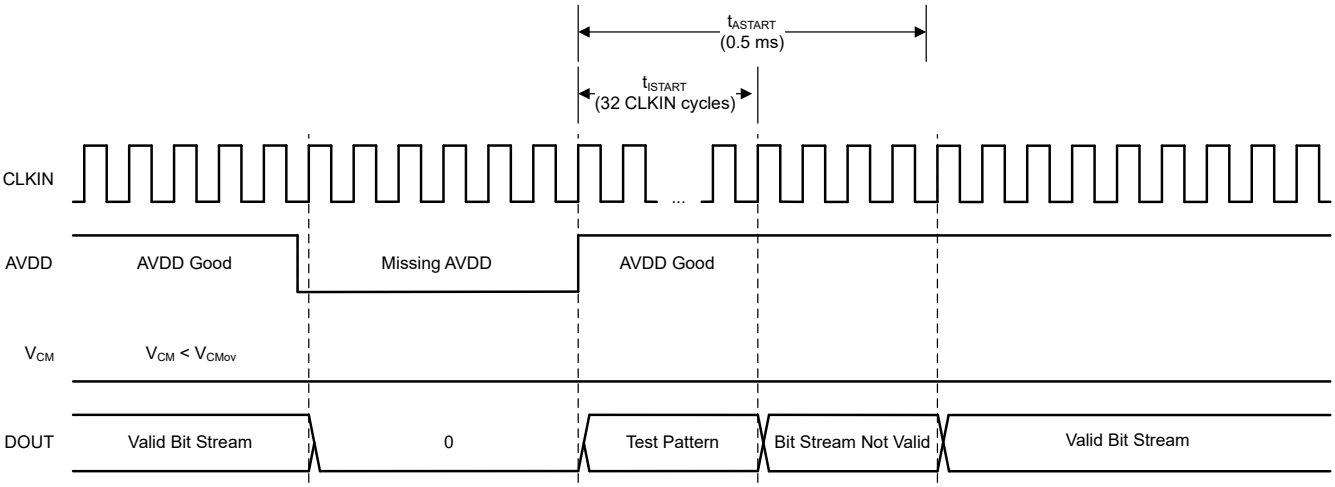

Figure 3-1. Missing High-Side Supply Voltage Fail-Safe

Once the high-side supply voltage returns to correct voltage levels, the device has two startup periods during which the output bitstream are assumed to be invalid. The first startup period is interface startup (ISTART). This interface startup lasts for 32 CLKIN cycles and consists of a test-pattern issued by the device, which consists primarily of alternating 0 and 1 bits. The second startup time is the analog startup (ASTART). This analog startup begins as soon as AVDD returns to a good voltage and lasts for approximately 0.5 ms. To simplify these conditions, it is assumed that the bitstream is invalid for a full 0.5 ms after AVDD returns to the appropriate level.

The next fail-safe occurs when the operating common-mode input voltage, VCM, exceeds the overvoltage limit, VCMov. When this occurs, DOUT will remain at a static value of 1. When VCM is brought back below the overvoltage threshold value, the output of the AMC1306 device will return to a valid bitstream.

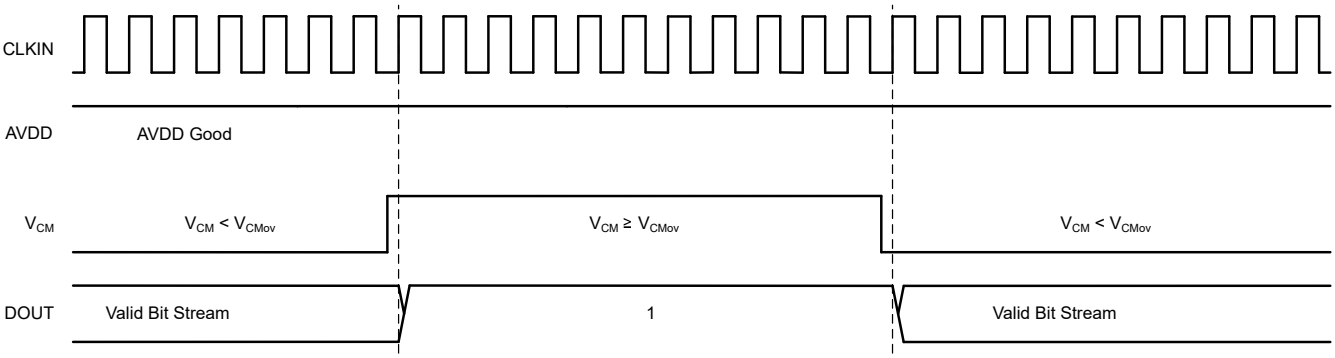

Figure 3-2. Common-Mode Overvoltage Fail-Safe

Examining these two fail-safe conditions in parallel, the missing high-side voltage fail-safe has a higher priority compared to the common-mode overvoltage fail-safe. When both conditions are present, the delta-sigma output bitstream will be low. After AVDD is restored to the device, the 32 CLKIN-cycle interface startup pattern will have priority over the overvoltage condition. After the 32 CLKIN cycles have elapsed and the overvoltage condition is still present, the output DOUT will be high. These conditions and their priority are shown in Figure 3-3.

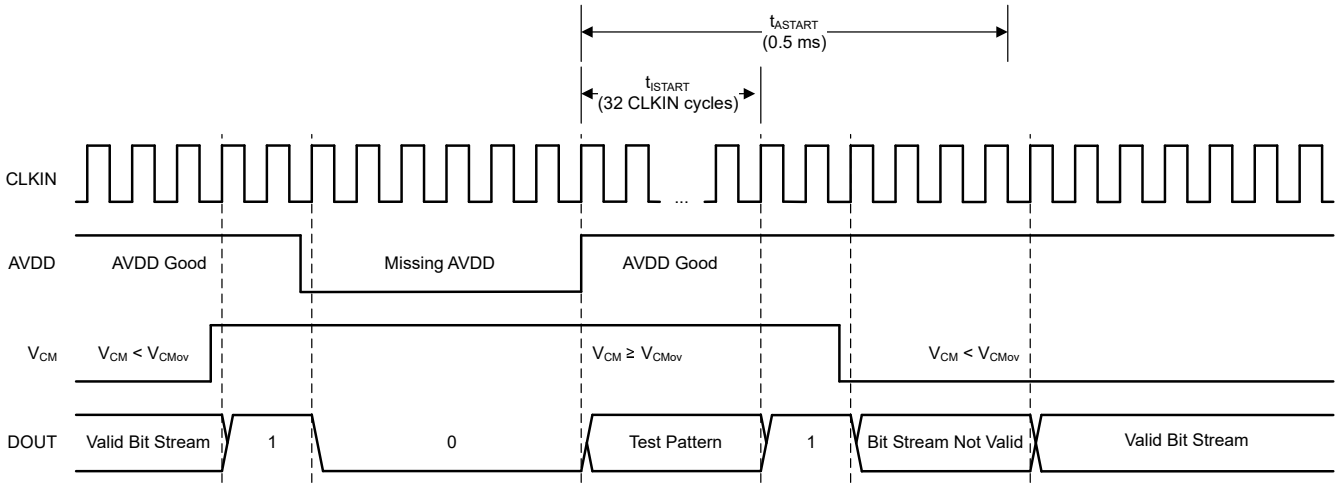

Figure 3-3. Output Bitstream With Fail-Safes

The remaining two fail-safe states are used to detect input-overrange conditions and distinguish these from the missing high-side and common-mode overvoltage conditions. The input voltage clipping ranges differ depending on the device being used. For the AMC1306x25 device, the clipping occurs at +- 320 mV. For a negative full-scale range input, the output bitstream will consist of a pattern of 127 0s followed by a single 1. This pattern continually repeats until the FSR condition is relieved. Depending on the level of overdrive, the single 1 may be extended to two or three 1s. With this unique configuration, it is possible to distinguish the fail-safe condition from a missing AVDD fail-safe.

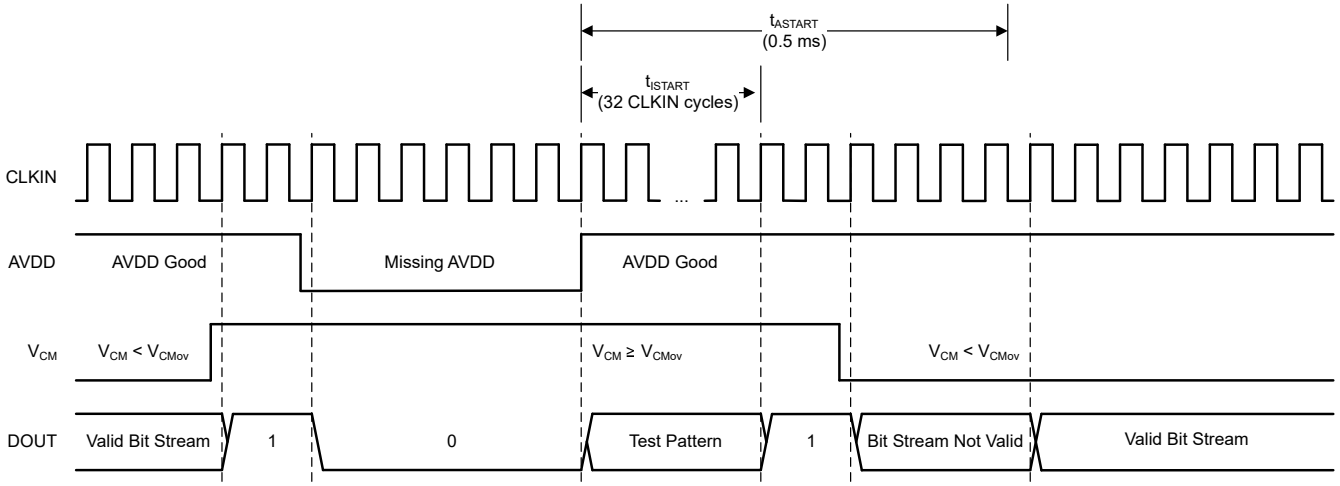

Figure 3-4. Output Bitstream With Fail-Safes

A similar bitstream configuration occurs when a positive full-scale range input is applied to the device. When the input voltage exceeds the positive clipping voltage, DOUT will display a continuous pattern of 127 1s followed by a single 0 bit. Likewise, depending on the level of overdrive, the single 0 may be extended to two or three 0s.

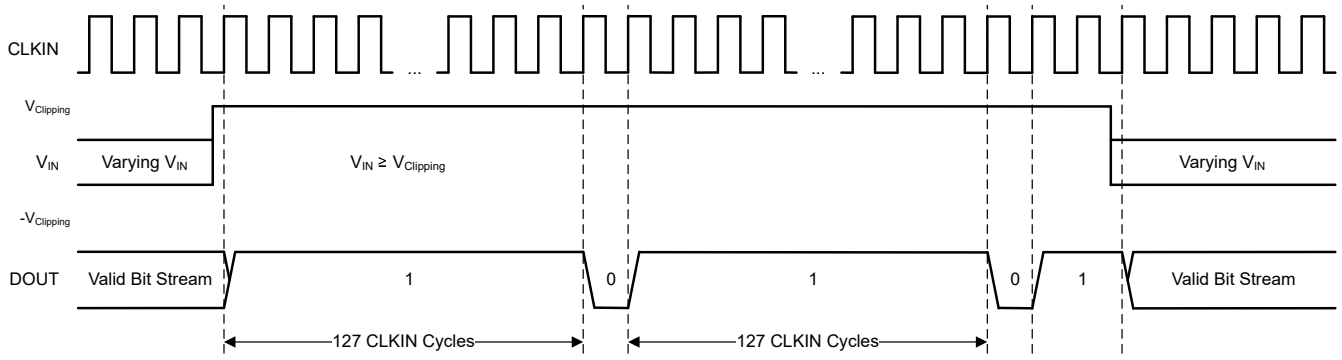

Figure 3-5. Positive Full-Scale Input Fail-Safe

4 Software Implementation

This section describes the software implementation used by the C2000 device to identify fail-safes from the AMC1306 device. The project is available within the C2000Ware SDK at `[C2000Ware_SDK]\examples\demos\clb_amc_failsafe_monitor`. The finite state machine below models the transitions of the states of the delta sigma modulator output depending on the state of the current sensing system. Because the only output signal available externally to the sigma delta modulator is the bitstream itself, a novel software implementation must be used to implement fail-safe monitoring.

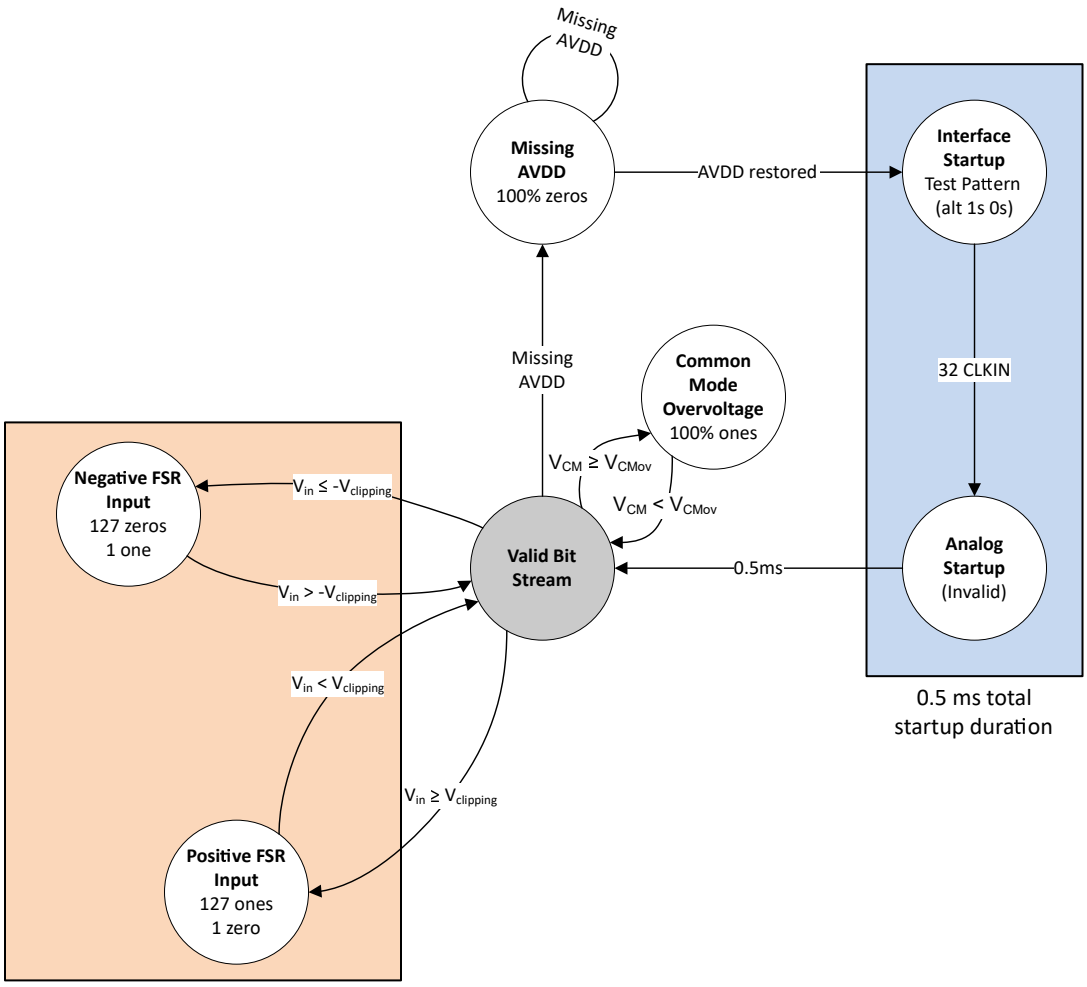

Figure 4-1. AMC1306 Device Fail-Safe Finite State Machine

For this implementation, the specific devices used are the LAUNCHXL-F280049C and AMC1306EVM. The LAUNCHXL-F280049C is an evaluation module featuring a TMS320F280049C microcontroller clocked at 100 MHz. It has four SDFM modules and four CLB tiles in addition to a variety of on-chip control and communication peripherals. The AMC1306EVM device features an AMC1306M25 device which produces an uncoded (non-Manchester encoded) bitstream and allows for an input voltage range of ±250 mV. In the CLB configuration, it is assumed that the delta-sigma bitstream is uncoded and that the SDFM is operated in Mode 0 clock mode. The same signals which are required inputs to the SDFM peripheral are routed to the CLB peripheral within the device using on-chip interconnects. Being a purely software implementation, this does not require any additional soldering or trace connections.

This software application runs the AMC1306 device at 12.5 MHz, though it can be reconfigured to run at any desired frequency within the delta-sigma modulator's allowed operating frequency range, ranging from 5 MHz up to 20 MHz. The C2000 ePWM1A module generates a 12.5 MHz signal with 50% duty cycle, and this clock signal must be connected to three inputs: the CLKIN input of the AMC1306, the clock input of the SDFM module, and the CLB tile. Per typical current sensing designs, the clock signal generated by the ePWM is externally routed to the delta-sigma modulator and SDFM modules. With the C2000's internal interconnects, the C2000's ePWM signals are directly available to the CLB through a global input bus. Each CLB tile has eight individual inputs, and in this software example, the clock signal is configured as BOUNDARY Input 0 of the CLB tile with a rising-edge detect filter.

The DOUT data bitstream output of the AMC1306 device is fed into the SDFM module's DATA input through a muxed GPIO. The input GPIO signal is available in the input X-BAR, and the CLB has access to this signal through the CLB X-BAR. This DOUT signal is fed into BOUNDARY Input 1 of the CLB. The described DOUT and CLK signal connections are displayed in Figure 4-2.

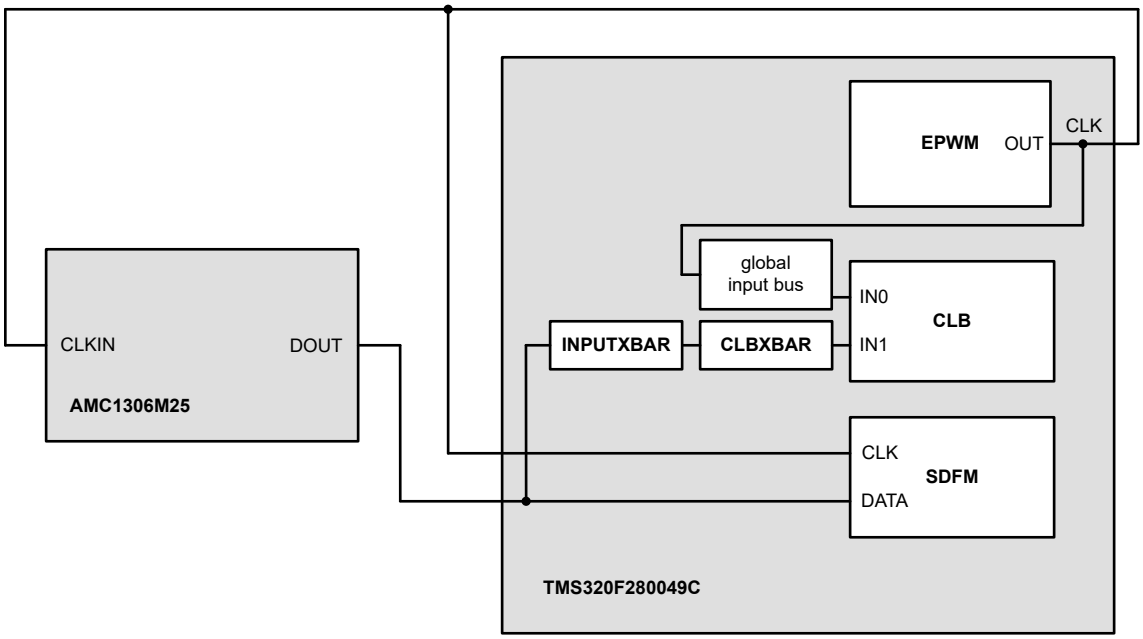

Figure 4-2. DOUT and CLK Signal Connections

With a combination of the CLK and DOUT signals, the CLB module can read the bitstream at the same frequency as is produced by the delta-modulator. To identify any AMC1306 fail-safe states, the CLB analyzes the DOUT bitstream in 128-bit sections. The 128-bit size is chosen to ensure that full-scale range input states can be differentiated between a missing high-side power or common-mode overvoltage state. The CLB decomposes the bitstream into a ratio of zeros and ones. The implementation within the CLB module is given below:

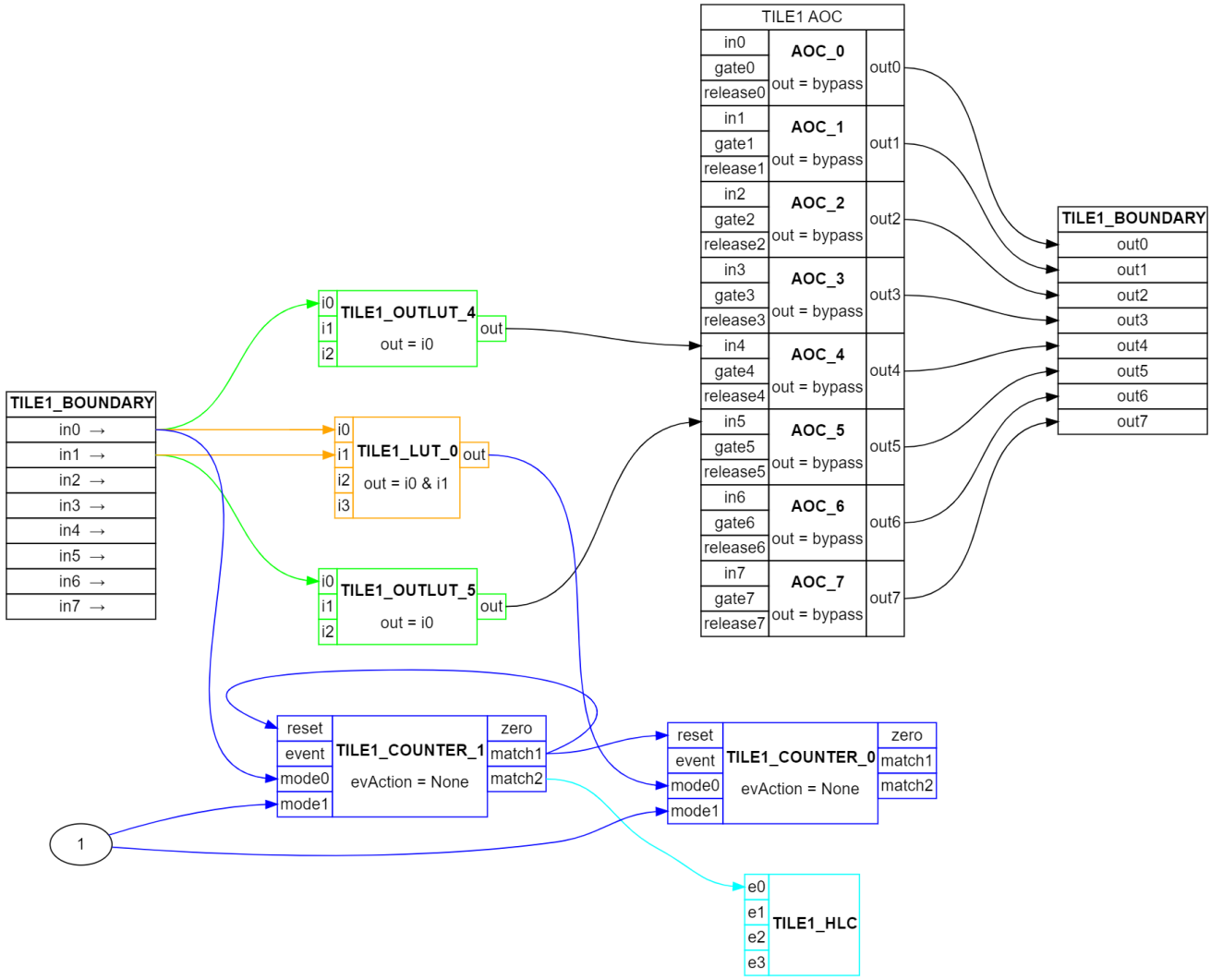

Figure 4-3. CLB Implementation

When the bitstream consists of constant zero, i.e., the analyzed bitstream segment is 128 0-bits, the CLB understands that the delta-sigma modulator is in a missing high-side fail-safe state. The DSModulatorStatus status indicator variable will then display 2. When the analyzed bitstream segment instead consists of 128 1-bits, it is known that the AMC1306 has a common-mode overvoltage condition.

The negative full-scale range input occurs when the analyzed DOUT pattern consists of 127 0-bits to one 1-bit. A buffer of about 3%, equivalent to three total 1-bits, is given to account for the scenario in which the 1-bit persists for a few additional CLKIN cycles. Similarly, a positive full-scale range input occurs when DOUT is a pattern of 127 1-bits to one 0-bit, with a similar 3% buffer for potential substantially out-of-range inputs.

Table 4-1 provides a summary of delta-sigma modulator statuses and their corresponding DSModulator tag.

Table 4-1. DSModulatorStatus Variable Definition

DSModulatorStatus Variable	Delta-Sigma Modulator Status
0	Transition status
1	Normal operation
2	Missing AVDD
3	Common-mode overvoltage
4	Negative full-scale range input
5	Positive full-scale range input

4.1 Running the Software Example

To run this software implementation, import the example project into CCS from its location in the C2000Ware SDK at `[C2000Ware_SDK]\examples\demos\clb_amc_failsafe_monitor`. Table 4-2 shows the required connections for the AMC1306EVM and TMS320F280049C devices.

Table 4-2. Required Connections for the AMC1306EVM and TMS320F280049C Devices

AMC1306EVM Pin	Connect to:
AGND	Ground
AVDD	5 V
AINP	Analog Input
AINN	Ground
DVDD	3.3 V
DGND	Ground
DGND	Ground
CLOCK	EPWM1A, SDFM_C1
DOUT	SDFM_D1

When running the CSS example on the TMS320F280049C device, add the following watch expressions to the CCS debug expressions time and ensure that continuous refresh mode is enabled.

- zeroBits
- oneBits
- ratio
- DSModulatorStatus

An expected bitstream output for the delta-sigma modulator operating in normal operation is given by the below waveform, where Digital I/O 0 represents the CLKIN input and Digital I/O 1 representing the DOUT signal.

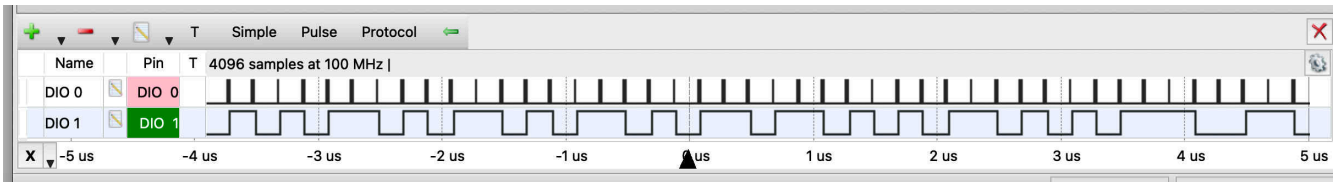

Figure 4-4. Bitstream Waveform for Normal Operation

In the watch expressions view, the zeroBits and oneBits variables describe the number of 0-bits and 1-bits in the most recently analyzed 128-bit-long DOUT section. The ratio describes the percentage of 1-bits within the segment.

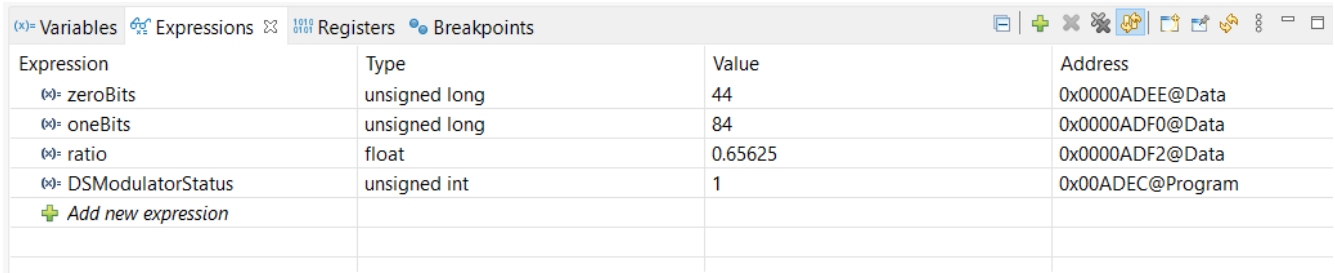

Figure 4-5. CCS Expressions for Normal Operation

For fail-safe states, these conditions will update accordingly. For example, suppose the AMC1306 device has a positive full-scale input. The resulting CLKIN and DOUT waveforms would appear as shown in Figure 4-6.

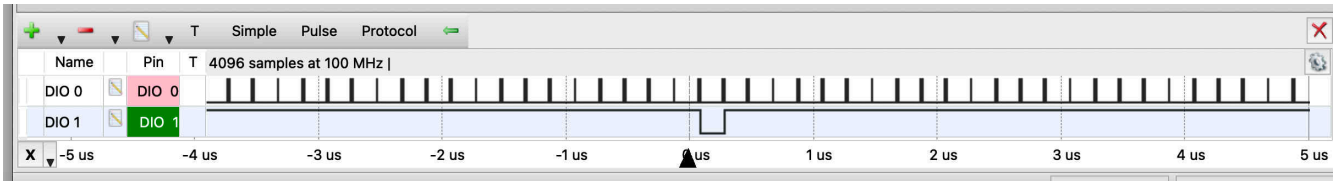

Figure 4-6. Bitstream Waveform for Positive Full-Scale Input

In CCS, the watch expressions would capture this information in the stored variables, and proper action can be taken to relieve the system error.

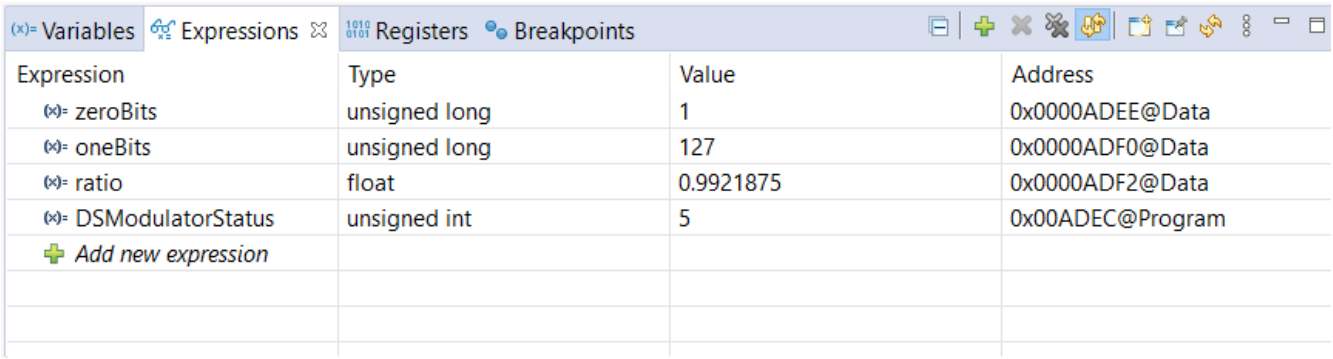

Figure 4-7. CCS Expressions for Positive Full-Scale Input

The state variable which denotes the current fail-safe state of the delta-sigma modulator device can be applied in different ways depending on the desired functional safety outcome. These states can be used to trigger other commands in software. They can also be directly fed back into the device and the CLB using the CLB's GPREG registers.

For applications making use of Manchester-encoded bitstreams, the CLB logic within the C2000 device which handles the input and bitstream realization will need to be adjusted. This can be done by directly altering the logic within the currently implemented CLB tile or using an additional CLB tile to decode the Manchester-encoded bitstream into an uncoded bitstream.

This software example is not limited to only the AMC1306. This project can be adapted to other delta-sigma modulators which feature similar fail-safe detection capabilities.

5 Summary

The configurable logic block within C2000 devices can be interfaced with the output of delta-sigma modulators to understand potential fault scenarios and implement fail-safes. The AMC1306 device being used in this software example has built-in fail-safe conditions which affect the DOUT output bitstream in specific ways. By feeding the DOUT signal into the C2000 device, the CLB can be used to monitor system faults, such as missing AVDD, input voltage out of full-scale range, and input voltage out of common-mode input range. This software implementation is compatible with other types of modulators featuring similar device functional modes, such as AMC1336, and can be applied to any system, like motor drives or solar inverters, where current sensing is an integral function. These monitoring functions can help support functional safety. It can ensure safety-critical operation and has the potential to reduce system costs by performing logical operations on-chip without the need for external logic devices.

6 References

- Texas Instruments: *How delta-sigma ADCs work, Part 1*
- Texas Instruments: *Digital Filter Types in Delta-Sigma ADCs*
- Texas Instruments: *AMC1306x Delta-Sigma Modulators Data Sheet*
- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28004x Real-Time Microcontrollers Technical Reference Manual*
- *C2000 Configurable Logic Block Video Training Series*
- Texas Instruments: *CLB Tool*
- Texas Instruments: *Designing With the C2000™ Configurable Logic Block (CLB)*
- Texas Instruments: *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers*

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