Application Note

Estimating Application Useful Lifetimes for Sitara MPU Products – A Design-Based Methodology

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ABSTRACT

This application note summarizes the Power-on Hours (POH) achievable on AM625 / AM623 family of processors. The application notes provides an overview of the intrinsic reliability capabilities and applied methodologies of the AM62x ARM based processors family

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Trademarks

1 Introduction

This application note applies to the device families mentioned below. Product related documentation is available on the product pages on TI.com.

AM62x Processor Family

AM625

- AM6254
- AM6252
- AM6251

AM623

- AM6234
- AM6232
- AM6231

Note

Content referring to temperatures greater than 105°C junction temperature and up to 125°C, only applies to extended temperature devices as specified in data sheet Recommended Operating Conditions.

This document provides an overview of the intrinsic reliability capabilities and applied methodologies of the AM62x ARM based processors family. TI, along with IP (Intellectual Protocol), Computer-Aided Design (CAD) tool and foundry partners, has developed robust design targets and an advanced design (and design-verification) based approach to meet or exceed market expectations for application mission lifetime profiles. The term mission profile means a table of variable temperature tiers (at fixed voltage and frequency), with each temperature at some fixed duration, with each tier summing to a total lifetime. The lifetime at each tier (and the total) is normally expressed in Power-on Hours (POH). The table is to represent exposure to these various conditions throughout the lifetime of the product. Alternatively, reliability can be represented as a table or graph of POH (dependent variable) as a function of specific temperature and/or voltage or frequency (as the independent variable).

Table 1-1. Example of a Reference Mission Profile (Multi-Temperature Tier) in a TI Data Sheet (AM62Ax Sitara Processors Data Manual)

Power-on Hours (POH)(1) (2) (3)		
Junction Temperature Range (T_J)		**Lifetime (POH)**
Extended	-40°C to 105°C	100000
Automotive	-40°C to 125°C	20000 (4)

(1) This information is provided solely for your convience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature, and time. Usage at higher voltages and temperatures result in a reduction in POH.
(4) Automotive profile is defined as 20000 power on hours with a junction temperature as follows: 5% at -40°C, 65% at 70°C, 20% at 110°C, and 10% at 125°C.

Table 1-2. Example Temerature vs. POH Table (AM243X Data Manual, TI Publication

Temperature Rating	Temperature Range	Junction (T_J) (1)	Estimated Lifetime(2) POH (3)
A	-40°C to 105°C	105°C	100000
I	-40°C to 125°C	105°C	100000
		110°C	64000
		115°C	41000
		120°C	26500
		125°C	17500

(1) Unless specified, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(2) This information is provided solely for your convience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures results in a reduction in POH.

2 Design-Based Approach

HTOL-based testing for the purpose of product lifetime estimation presents some considerable challenges, particularly in terms of practical limitations on sample size and test duration, as well as the difficulty in achieving effective stress conditions for some salient failure mechanisms (notably electro-migration and hot carrier degradation). A fuller account of these issues is provided later in Comparison of Design-Based Approach vs. HTOL Approach for Lifetime Estimates and Appendix A, but a simple summary is provided in Figure 3. TI believes the design-based approach of estimating product lifetime is more accurate and reliable for Embedded Processors than the more typical HTOL approach, which is more common in the industry. The methodology and results of the design-based approach are detailed in this publication.

Table 2-1. High-level Assessment of Reliability Wear-out Mechanisms – HTOL vs. Design (EDA) Tools

Wearout Failure Mechanism	Reliability Robustly Assessed?	
	HTOL	EDA Tools
TDDB (inc. GOI, Drain Stress)	Yes	Yes
Aging- Biased Thermal Instability (BTI)	Maybe (1)	Yes
Aging - Channel Hot Carriers (CHC)	No	Yes
Electromigration - Metal/Via	No	Yes

(1) HTOL stress pattern and ATE program dependent

Note

While the design-based reliability modeling discussed in this document is quantitatively and statistically-oriented, and is based on TI's understanding of how a typical customer would use our products, it cannot predict all possible use scenarios and does not represent any guarantee that extends warranty periods under TI Standard Terms and Conditions of Sale.

While the package option plays a role in overall product reliability, the effects package failure mechanisms can vary substantially depending on the package technology and users' environmental conditions, such as temperature cycling profile and humidity conditions. Such conditions can vary widely. TI product qualification results, including Board-Level Reliability Temperature Cycling, can provide a starting point for the user to estimate package reliability.

3 Background

TI Embedded Processing's overall approach to lifetime (also known as intrinsic) reliability is to embed this into the design and manufacturing process, starting from component-level reliability (transistors, didoes, capacitors, resistors, etc.) through final System-on-Chip (SoC) product release. This process, called Correct by Construction, is illustrated at a high level in Figure 3-1.

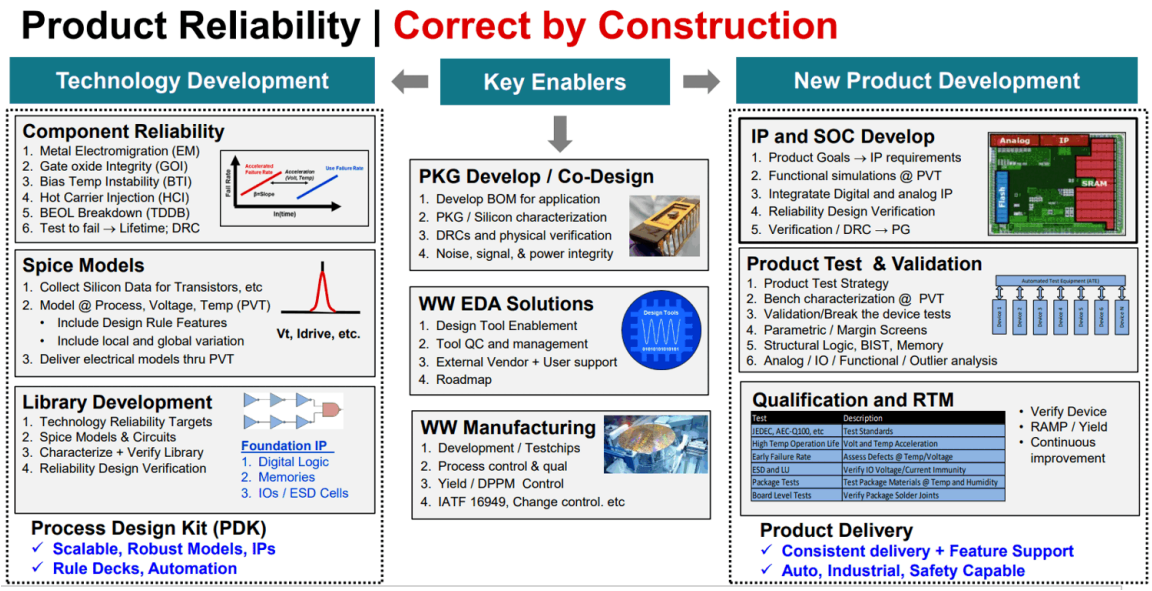

Figure 3-1. Correct by Construction Reliability Approach – From Inception to Product Release

3.1 Process Delivery Kit (PDK)

The backbone of the design process is defined under the umbrella of Process Delivery Kit (PDK) for the technology node. From a reliability perspective, once the silicon wafer manufacturing process baseline flow is defined, component-level reliability is executed by the wafer fab. These tests assess potential intrinsic wear-out mechanisms that can effectively limit the useful lifetime of the final product. Generally, the tests are highly-accelerated, meaning stress conditions are much more aggressive than final product application use conditions, and are tested to failure to enable characterization of reliability models (which can involve testing a multiple stress conditions to define acceleration models.) Each test has defined pass/fail criteria, consistent with the overall reliability targets of the silicon technology. Critically, the component-level tests can be performed at much higher levels of stress than HTOL testing, enabling granular reliability models (necessitating observed failures) and compressed execution times.

3.2 SPICE Models for Circuit Behavior

The next step is generation of SPICE Model libraries integrating the underlying component reliability models (and, critically, aging effects). The output of these electrical models at base component characterized across Process, Voltage, and Temperature (commonly known as PVT). Process means the critical parameters of the elemental components, such as transistor Threshold Voltage, drive (ON state) currents, OFF state currents (sub-threshold leakage), or metal sheet resistances. Statistical modeling simulations also include potential localized variances in parameters that can significantly affect final performance, and builds further robustness into the models.

For digital core logic, memories, (digital) IOs and ESD cells, libraries are constructed of re-usable cells, building on the fundamental components and end-of-life (aged) SPICE models. Analog circuits are not directly constructed from re-usable cell components, but have a separate work flow also leveraging aged SPICE models and maintains operation within safe operating limits. Signal integrity and parameters such as gain, noise, offset, and linearity, must maintain functional and parametric performance within published specifications across specified lifetime profile, which is generally published in data manuals for Embedded Processing products. All digital and analog components, including memories, must furthermore be maintained within physical design-rule

limits encompassed within the PDK, with those limits inherently comprehending reliability. At the IP and SoC development and integration stage, DRCs are once again applied. Design Rule Checkers (DRCs) rigorously enforce these rules prior to Pattern Generation (PG), with any violations requiring action and disposition before mask generation. Figure 3-2 shows a more detailed view of the PDK scope.

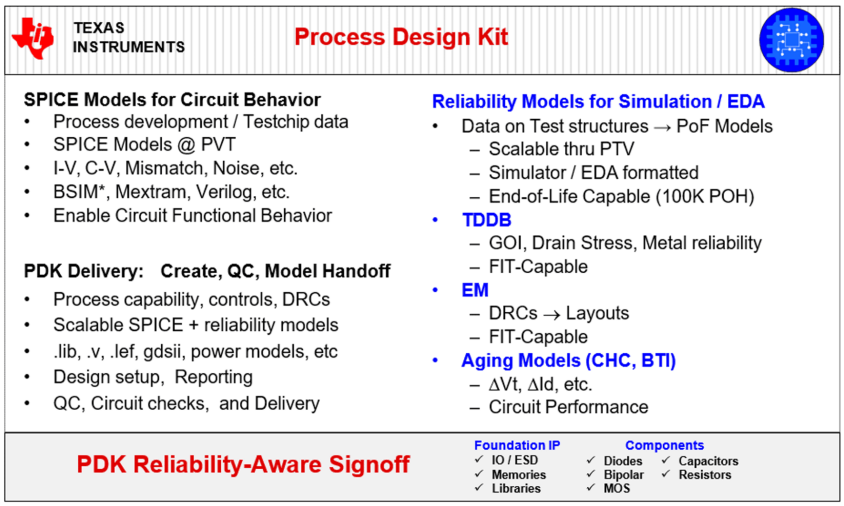

Figure 3-2. Process Design Kit Overview

3.3 Electronic Design Automation (EDA) Tools

Importantly, at the IP and SoC release stages, Electromigration (EM) and Gate Oxide Integrity (GOI) / Time-Dependent Dielectric Breakdown (TDDB) tools TI uses on the most current CMOS technologies (including for AM6*) are FIT-capable through the use of advanced Electronic Design Automation (EDA) tools. This means that FIT (Failures in Time, an expression of failure rate) is reported relative to a “design closure” condition (normally 105°C at 100kPOH, at the specified voltage and frequency conditions published in the product data manual). Furthermore, the EM flow is capable of reporting key by-individual-component average current densities (i.e. for all interconnects and vias) from simulations, enabling accurate quantitative scaling of EM reliability to customer mission profiles or alternative temperature conditions to fixed design closure conditions, an important feature discussed later. In the case of Hard IP (synthesized with physical design layout fixed), the IP are evaluated for FIT as standalone entities. The FIT contributions of Soft IP (re-synthesizable, physical layout not fixed), top-level logic (outside IP boundaries) and memories are summed for the SoC and then combined with the Hard IP (with use at SoC level limited to the bounding operating design conditions of the IP), resulting in total FIT. These FIT values are tallied separately for EM and GOI. The effects of aging on transistor components, by contrast, is generally not associated with FIT calculations, rather the design flow defines and enforces safe operating conditions and margin requirements such that effectively the failure rate within specified mission profile conditions is negligible.

3.4 Package Reliability

Package reliability is partially comprehended within the product design flow through a co-design process, coupled with die (silicon) design. Key considerations are noise minimization and signal and power integrity, as well as thermal effects. In coordination with silicon design, design rules are devised and enforced for the package to holistically affect complete product performance targets. However, package reliability is also dependent on selection of robust materials and manufacturing flows.

Extensive efforts are undertaken during package technology development to identify corner cases of process variation and the effects on manufacturability and reliability. Process limits are then set accordingly and monitoring of process capability on key parameters is performed in production, normally with Statistical Process Control (SPC). With the exception of die Bump Electromigration reliability for Flip-Chip packages, most package long-term reliability failure mechanisms encompassed by thermo-mechanical stress or oxidation/ corrosion reactions. These risks are evaluated during product qualification within defined JEDEC/AEC-Q100

test conditions, but sample sizes are necessarily limited, thus limiting the capabilities of quantitative failure rate assessments. (This issue also applies to HTOL.)

Process development stage activity to build-in margin, as well as robust statistical monitoring through Manufacturing Control Plans in production are both key. However, the solder joint thermo-mechanical reliability for BGAs and bumps can be assessed quantitatively. Board Level Reliability (BLR) Temperature Cycle (T/C) Testing is performed within scope of product qualification (although can be qualified by similarity for any particular product). The BLR stress is generally continued to at least 60-70% of samples failing, enabling a generation of Weibull plots, quantifying reliability performance. (De-rating of BLR stress test conditions to application temperature cycling conditions can be needed. As the application cycling conditions can vary widely, this is typically done on a case-by-case basis.)

4 Comparison of Design-Based Approach vs. HTOL Approach

A well-engineered HTOL stress plan must adequately assess lifetime for TDDB mechanisms (e.g. GOI, ILD failure) in most cases. This can also include detection of extrinsic defects causing premature TDDB failure. In many cases, TDDB mechanisms are not ultimately the limiting factors for lifetime reliability.

Channel Hot Carrier (CHC) and Electromigration are generally not significantly accelerated during HTOL, even under dynamic stress conditions (the norm for processors). In the case of CHC, clock rates and slew conditions during the (dynamic) HTOL stress are not normally conducive to accelerated CHC degradation. Biased Thermal Instability (BTI) can be accelerated in HTOL, largely due to high temperature and voltage, but the dynamic switching activity that occurs during HTOL on the worst-case circuits can not sufficiently represent functional use condition, especially when considering overall aging can combine BTI and CHC components.

Electromigration current densities (also a strong function of clock rate), during HTOL bias are generally not high enough to demonstrate to 10+ years of lifetime when de-rated from a typical 1000-2000hr test duration (even at elevated voltage). Much longer durations are needed. Typically, structural stress patterns (i.e. ATPG-based) are applied with HTOL, along with memory or other applicable BIST, and clocking is normally well below maximum operating frequency.

The focus of HTOL coverage is generally to maximize toggle coverage of nodes. With wear-out mechanisms, know where the relative weak spots are in the design, what operational modes are worst case and target stress pattern conditions to maximize worst case PVT and Frequency corners. Various local weak spots (IP across the die) can have different worst corners. It is very difficult with typical ATPG and BIST patterns applied in HTOL to accelerate all the worst-case functional conditions on targeted circuits. Figure 6 further expands on Figure 3 and summarizes critical aspects of the SoC design flow with a comparison of effectiveness of HTOL coverage vs. EDA tools as Design Verification paths. Applicable reliability failure mechanisms are noted.

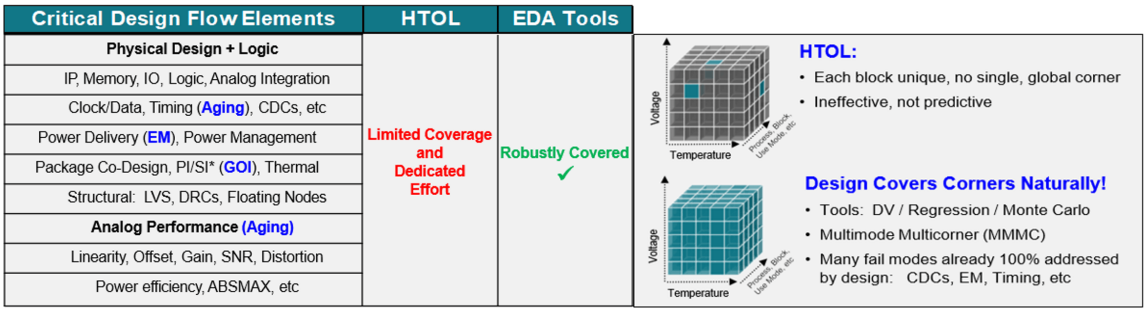

Figure 4-1. Efficacy of HTOL vs. EDA Tools in Design Verification of Critical Design Flow Elements

For a more detailed explanation of the mathematics of HTOL-based product reliability estimates and the shortcomings, see Appendix A. Additionally, the mathematical framework for Electro-migration reliability is described in Appendix B.

5 AM625/623 Lifetime Reliability Analysis Results

TI's design for reliability analysis on AM62x ARM based processors family has so far consistently indicated Electro-migration as the lifetime-limiting failure mechanism. As explained previously, TI does not believe lifetime Electro-migration reliability can be adequately assessed with HTOL testing within reasonable test durations. Furthermore, as an important additional enhancement of the PDK, TI's EDA tool flow for the Sitara AM6* product lines has the capability of integrating and reporting total FIT/Fail Fraction (FF) at our design reference conditions (105°C die junction temperature at 100k POH lifetime). As of early 2024, a software application has been developed outside of the EDA tool flow to accurately scale individual (constituent) metal or via component FF contributions to other specific single temperatures or temperature profiles. These contributions are then tallied across the SoC. Scaling is more complex than a single acceleration factor calculation because simulations show variation in the average current densities relative to the EM design-rule limits. In effect, this means each component has an individual acceleration factor (generally following Black's Law, as explained in Appendix B).

Figure 5-1, Figure 5-2, and Figure 5-3 show POH vs. Temperature plots for AM62X product niche. In Figure 5-1 and Figure 5-2, core voltage is varied from 0.75V to 0.85V (at fixed frequency per data manual). For readability this is broken into two figures. Observe that the POH capability is roughly 25% expanded at 1% fail fraction tolerance vs. a 0.01% fail fraction, largely independent of temperature. For reference, 0.1% fail fraction at 100k POH is equivalent to 10 FIT. Figure 5-3 illustrates the effect of varying fail fraction targets at fixed voltage (and frequency) in the range of 105°C to 125°C junction temperatures. With a baseline of F=0.001 (0.1%), a relaxation to 1% failure tolerance results in roughly 18% increase in POH both at 105°C and 125°C.

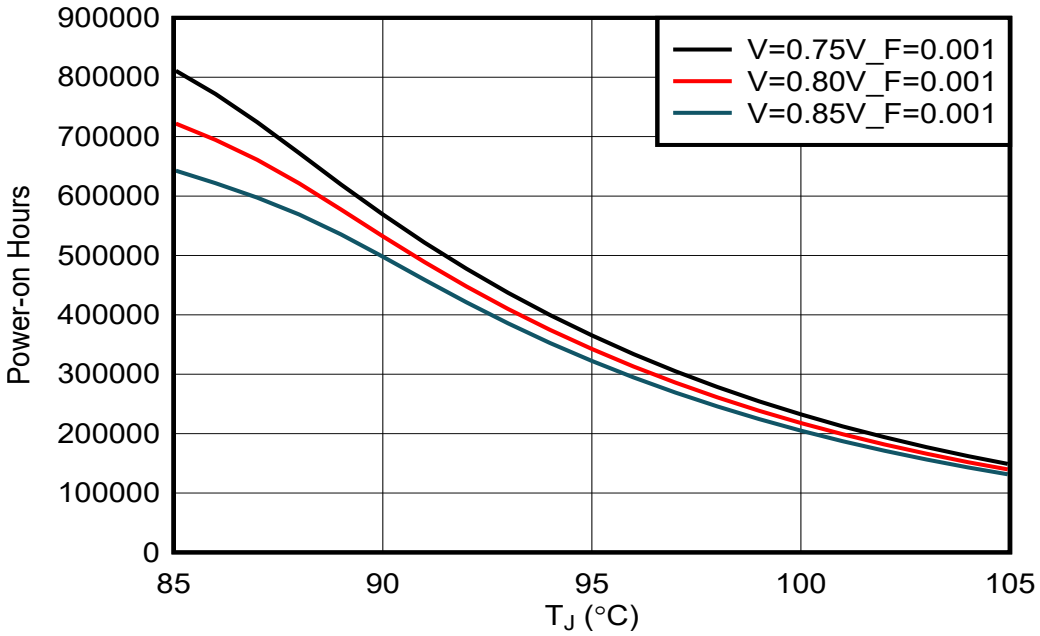

Figure 5-1. AM62X POH vs. Temperature to Fixed Fail Fraction (0.1%), Up to 105°C

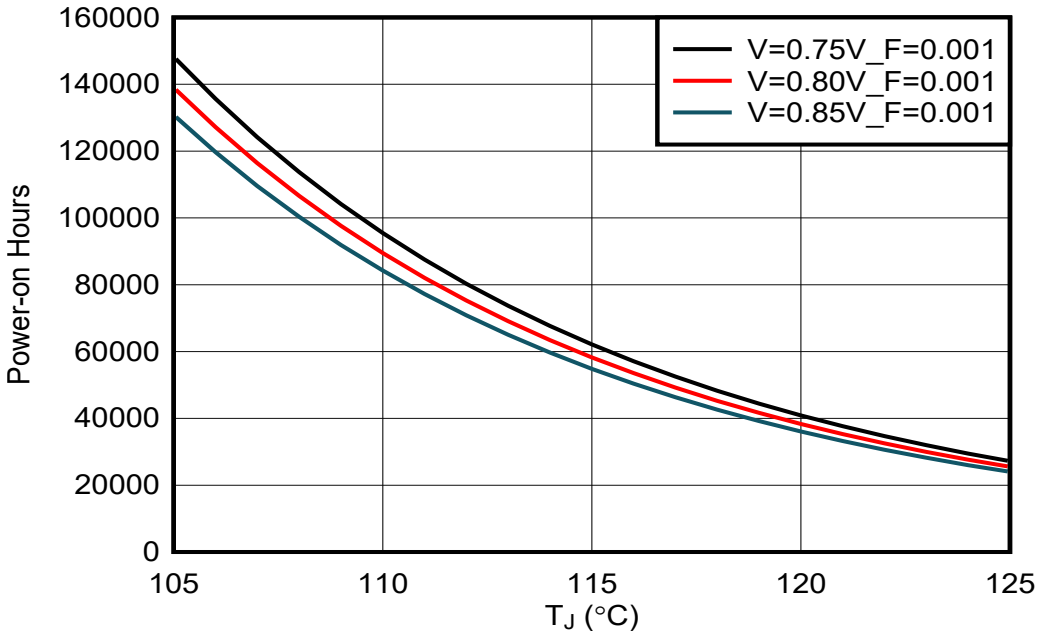

Figure 5-2. AM62X POH vs. Temperature to Fixed Fail Fraction (0.1%), Up to 125°C

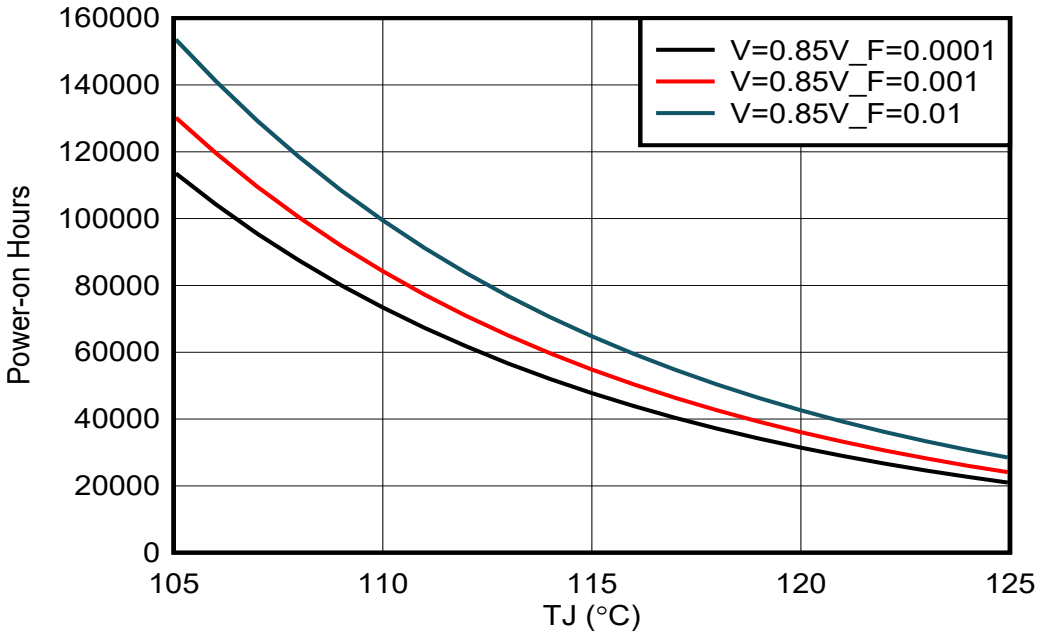

Figure 5-3. POH to Various EM Fail Fractions vs. Tj

Note

All temperatures are expressed as (die) junction, consistent with TI data sheets. Reliability estimates for die-based mechanisms are all performed based on junction temperature. System-level thermal engineering by the user, comprehending package, power dissipation, system board construction and other components on the system board, is therefore critical to managing junction temperature, and, in turn, lifetime reliability.

6 Conclusion

The case for TI's design-based reliability lifetime assessment approach has been presented, along with a comparison to the typical HTOL-based methodology. TI's approach flexibly facilitates variation of temperature and voltage with an output of curves to target fail fractions. The target fail fractions can then be varied, and the effects of variation have been shown. In principle, the effects of frequency can also be comprehended, but these are dependent on where the highest current design components are in the design, which clock domain applies, and whether that particular clock domain is being scaled in frequency. Due to potential complexities introduced by these factors, frequency scaling has been omitted from this publication.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2024	*	Initial Release

A Appendix – The HTOL-Based Approach

HTOL-based models are limited in two ways that do not apply for design-based reliability approach.

Typically, HTOL-based models apply a constant failure rate assumption. This is bottom of the bathtub curve as shown in Figure A-1. Importantly, this paradigm does not credibly represent the useful lifetime of the product, as logically, lifetime coincides with the onset of the wear-out stage, characterized by increasing instantaneous failure rate.

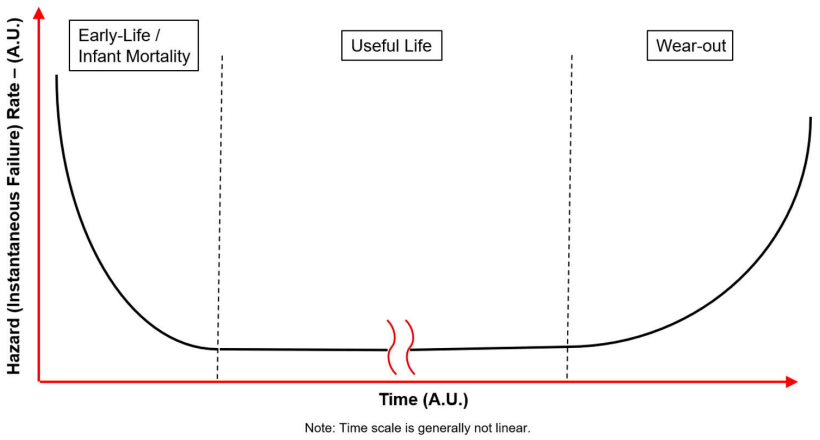

Figure A-1. Bathtub Curve – Mnemonic for Product Reliability Life Cycle

Reliability estimates are limited by fixed HTOL sample size and test duration. Usually one or both of these factors lead to a result of no observed failures. This limits viability of the model to characterize lifetime because no failures means minimal information to asses changes in failure rate vs. time. Mathematically, the case of terminating the test at a fixed duration (usually due to practical reasons) regardless of number of failures is called Type I right censoring. The term right censoring is used because when the test is terminated, it is unknown when the survivors at that point can later fail. The failure rate (in reciprocal time dimension) for Type I right censoring is represented by the following equation as shown in Equation 1.

$$F.R. = \frac{X^2[2 \times f + 2,1 - \alpha]}{2 \times SS\ x\ t_{HTOL} \times AF} \quad (1)$$

Where

$$X^2[2 \times f + 2,1 - \alpha] \quad (2)$$

- = Inverse Chi
- Squared Cumulative Distribution Function (CDF) with f fail count at (1 - a) one-sided confidence level
- SS = HTOL Sample Size
- t_{HTOL} = duration of HTOL test (hours)
- AF = Acceleration Factor (HTOL to application)

To convert the Average Failure Rate (AFR) to CDF (Fail Fraction), use the following general identity:

$$F(t) = 1 - e^{-AFR \times t} \quad (3)$$

In this case, the Average Failure Rate is the same as the Constant Failure Rate. However, more boradly, AFR is a non-constant function of time.

B Appendix – The Mathematic Basis for EM Reliability Estimates

Electro-migration failures are generally recognized to follow the Log-normal statistical reliability distribution with acceleration factors following Black's Law. The parameters are such that the instantaneous failure rate increases with time, reflective of the latest stage of the bathtub curve. It is beneficial to first describe Black's Law in basic form, then proceed to the Lognormal CDF. The fundamental CDF equation for EM Lognormal failures is in Equation 4.

$$t_{failure} = AJ^{-n}e^{-\frac{E_a}{kT}} \tag{4}$$

- *J* is the current density (effectively average current density in practice) through the wire or via.
- *n* is the current density exponent depend on the metallization used. Generally, *n = 1*is applied for Copper (Cu) and *n =2* for Aluminum. In the case of the Sitara products, both Cu and Al metals are used, but the limiting metallization components are typically Cu.
- *A* is a fitting constant that divides away when taking ratios of time to failures at different stress or use conditions, which is the definition of an acceleration factor (AF).
- *k* is Boltzmann's constant, 8.617×10^{-5} eV/°K. *T* in this case is temperature in Kelvin.

$$F(t) = \Phi\left[\sigma^{-1} ln\left(\left[\frac{1}{s^{-n}t_{50-ref}}\right]\sum_{i=1}^{N}\left[\frac{t_i}{\left(\frac{V_i}{V_{ref}}\right)^{-n}\left(\frac{f_i}{f_{ref}}\right)^{-n}e^{-\frac{E_a}{nk}\left(\frac{1}{T_{ref}}-\frac{1}{T_i}\right)}}\right]\right)\right] \tag{5}$$

In Equation 5,

- Φ is the Standard Normal CDF.
- $t_{50\text{-ref}}$ is the Median Time to Failure at a design reference condition.
- σ is the Standard Deviation of the natural logarithims of times to failure, which depends on the technology node, but 0.2 to 0.5 is typical (which is constant with wear-out).
- *s* is a ratio of average current density for the specific wire or via over the allowed maximum current density limit. The maximum limit corresponds to a ceiling for allowed reliability for a single component. As *s* trends lower (i.e. average reducing current density) effect is to scale up the effective t_{50} versus the reference condition. Higher t_{50} implies improved reliability.
- *V* and *f* refer to voltage and frequency respectively.

The terms summed from *i=1 to N* (behind *Σ*) require further explanation. E_a and *n* are are the Black's Law parameters, previously described. The numerator term t_1 refers to time at an application use condition tier in the mission profile. For example, t_1 can represent 20000 POH at 95°C Tj, at some operating some application voltage and frequency (an Operating Performance Point, or OPP, within data sheet specifications).

Another case:

$$t_2 \tag{6}$$

can be 50000 POH at 95°C Tj, and this can be at the same or a different OPP allowed within TI data sheet compared to (T_{ref}, V_{ref}, f_{ref}). The times for each tier must be scaled, either up or down, relative to the equivalent time at the reference condition. Finally, these scaled times must be summed for the entire mission profile (all appliation use tiers).

We have described the (Electro-migration) reliability of a single wire or via (component) up to now. How, then, is the total reliability for the SoC calculated? Mathematically, this is relatively straightforward.

Use the identity for the Reliability function:

$$R = 1 - F \tag{7}$$

where *F* is the CDF, described previously.

If there are *N* total components, then the total Reliability function the overall product of each individual component's Reliability function:

$$R_{tot} = \prod_{i=1}^{N} R_i \tag{8}$$

Finally, the total CDF is 1 minus the total Reliability:

$$F_{tot} = 1 - R_{tot} \tag{9}$$

The Standard Normal CDF also has a convenient mathematical identity that can be used simply translation of *F* to *R* or vice versa. That identity is:

$$\Phi(z) = 1 - \Phi(-z) \tag{10}$$

If

$$F = \Phi(z) \tag{11}$$

then

$$R = \Phi(-z) \tag{12}$$

In Equation 4, the sign of *z* can be changed from positive to negative by taking the reciprocal of the argument of the natural logarithm.

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