TMS320C66x DSP generation of devices

Texas Instruments

Based on TI's innovative KeyStone architecture, the new TMS320C66x DSP core and generation of C66x multicore devices include the industry's first 10-GHz DSP with 320 GMACs and 160 GFLOPs of combined fixed- and floating-point performance on a single device. These devices are designed to maximize the throughput of on-chip data flows and eliminate the possibility of bottlenecks. This enables developers to fully utilize the vast processing power of the DSP cores to design applications in markets such as test and measurement, mission critical, industrial automation, medical and high-end imaging equipment, and high-performance computing.

C66x DSP Core Features:

New C66x CorePac
- New C66x ISA
- Integrated fixed- and floating-point operation
- 8-way VLIW
- SIMD operations for fixed point
- Fully-pipelined instructions
- Up to 32, 8-bit or 16-bit multiplies per cycle
- Up to eight, 32-bit multiplies per cycle
- Up to eight single-precision multiplies per cycle
- Up to two double-precision multiplies per cycle

KeyStone memory architecture
- 32-KB local level-one instruction (L1P) and data (L1D) memories/cache
- Local level-two unified memory/cache (LL2)
- Optimized interface to shared memory with multi-stream prefetching for instructions and data
- Memory protection for read, write, and execute control
- Soft error detection and correction

KeyStone multicore shared memory controller
- Internal shared RAM, configurable as level-two (SL2) or level-three (SL3)
- Up to 8-GB external level-three DDR3 SDRAM
- Memory protection for read, write, and execute control
- Soft error detection and correction

TeraNet switch fabric
- Hierarchical switch fabric with efficient interconnect between masters and endpoints
- High throughput
- Low latency
- Efficient arbitration at endpoints

Multicore Navigator
- Packet transfer engine with 8,096 virtual queues
- Inter-core communication
- Task scheduling/distribution engine
- Data movement

EDMA
- High-bandwidth data paging engine
- Scaled to number of cores and memories
- Efficient throughput and concurrency

Hyperlink
- High-bandwidth, low-overhead port
- Tightly-coupled two devices

Multicore Family Features:

TMS320C6670

Layer 1 coprocessor for wireless
- Turbo encode, decode
- Viterbi decode
- FFT, DFT
- Uplink, downlink chip-rate
- Bit rate coprocessor (BCP)
- Receive accelerator coprocessor (RAC)
- Transmit accelerator coprocessor (TAC)
- Rake search accelerator (RSA)

Layer 2 network coprocessor
- Integrated hardware switch for MAC routing
- IP Network solution for IP v4/6
- 1.5-M packets per sec (1-Gb Ethernet wire-rate)
- IPsec, SRTP, Air Interface Encryption fully offloaded (select devices)

High-bandwidth I/O and memory
- 6x OBSAI/CPRI-compliant antenna interface with up to 6-Gbps lane rate
- x4 Serial RapidIO® v2 with up to 5-Gbps lane rate (splittable to 1, 2, 3, 4 ports)
- x2 PCI Express gen2 with up to 5-Gbps lane rate
- x4 Hyperlink with up to 12.5-Gbps lane rate
- 2x SGMII Ethernet ports with 1.25-Gbps lane rate
- 64-bit DDR3 SRAM + optional ECC

Other I/O and memory
- I^2C, SPI, UART

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- 64-bit DDR3 SRAM + optional ECC

Other I/O and memory
- I^2C
- SPI
- UART
- 2x TSIP for T1/E1 telephony
- 16-bit EMIF for NAND, NOR Flash or (a) sync RAM/FPGA

www.ti.com/c66multicore

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Russian Support	+7 (4) 95 98 10 701

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