Product Overview

J722S/AM67x/TDA4VEN/TDA4AEN Processor Automotive Power Designs using TPS6522312-Q1 PMIC

Abstract

This publication describes recommended power designs to support the *J722S/AM67x/TDA4VEN/TDA4AEN* family of processors as used on J722SXH01EVM - TDA4VEN, TDA4AEN and AM67 evaluation module. A selection guide that reviews system tradeoffs and design benefits is included to assist in power design selection, optimization and feature set comparisons. Power resource and control signal mapping block diagrams are provided to accelerate an end product's design process.

Introduction

The *J722S/AM67x/TDA4VEN/TDA4AEN* processor line provides highly flexible, real-time, and low-latency processing for a broad range of automotive and industrial applications. The *J722S/AM67x/TDA4VEN/TDA4AEN* vision and display processor includes scalable Arm® Cortex®-A53 performance, image signal processor (ISP) up to 600MP/s, Deep Learning AI Accelerators up to 4 tera-operations-per-second (TOPS), Depth and Motion Processing Accelerators (DMPAC), Vision Processing Accelerators (VPAC), along with embedded features such as triple high-definition display support, high-performance 3D-GPU, 4K video acceleration, and many additional peripheral interfaces.

All Power Distribution Network (PDN) schemes described leverage TI Power Management ICs (PMIC) with a mixture of discrete power components to support a *J722S/AM67x/TDA4VEN/TDA4AEN* system. All power components are automotive AEC-Q100 qualified. The PDNs have been designed primarily to support all essential processing components, known as the SoC platform, which includes:

- *J722S/AM67x/TDA4VEN/TDA4AEN* SoC processor
- LPDDR4 SDRAM
- OSI or Octal NAND boot Flash
- eMMC mass storage Flash
- PDN power devices

The functional safety compliant *TPS6522x12-Q1* PMIC and *TPS6287x-Q1* fast transient, high current power stage (HCPS) form the PDN's base power devices for the *J722S/AM67x/TDA4VEN/TDA4AEN* platform. Different PDN schemes can be used to support the SoC platform according to a system's maximum use case and desired features. A selection guide has been created that highlights the value and flexibility of PMIC centric PDN designs that leverages one common PMIC PN along with discrete power devices as needed to add optional features.

PDN Selection Guide

Selecting a *J722S/AM67x/TDA4VEN/TDA4AEN* power design begins with answering a few end product questions:

1. What is the desired processor performance?
2. What is the desired level of core voltage flexibility?
3. What is the desired PDN input voltage?
4. What are the desired optional features?
    a. Low-power modes: (Partial IO Retention only, Partial IO and DDR Retention)
    b. Key functions: (PMIC die temp monitoring, HS SoC eFuse programming, UHS-1 SD card)

c. Target functional safety level: (None or ASIL-B)

Once a system's desired features are determined, then the tables below can be used to optimize a recommended power design that provides:

1. SoC processing peak power demands
2. SoC platform (SoC, LPDDR4, Flash, base power devices) voltages and control signals
3. Flexibility to make design trade-offs: PDN features versus PCB area and BOM cost

Key attributes that define a PDN are: base power devices, processing performance, input voltage, and optional features. For easy reference, a 2-part PDN identification code (for example, PDN-123.456x) defines a PDN's attributes.

The 1st group of characters (-123) is known as the "ID" field and defines base power devices, processing performance and input voltage as follows:

1. Numeric value for base power devices:
   a. 5 = TPS62870/1/2/3-Q1 (HCPS) + TPS65223/112-Q1 (PMIC)
   b. 7 = TPS62874/5/6/7-Q1 (HCPS) + TPS65223/112-Q1 (PMIC)
2. Alphabetic letter for processing performance and resource mapping:
   a. A – D = 1.4GHz clock with 0.85V Core boot voltage
   b. L – P = 1.25GHz clock with 0.75V Core boot voltage
3. Numeric value for PDN input voltage:
   a. "None" = 3.3V default
   b. 5 = 5V

The 2nd group of characters (.456x) is known as the "Variant" field and defines optional features requiring add-on discrete power devices as follows:

D = Partial IO and DDR Retention low power mode (LPM)

E = On-board Efuse programming for high-security SoCs in-the-field

S = UHS-I SD card memory

J722S/AM67x/TDA4VEN/TDA4AEN EVM system (J722SXH01EVM - TDA4VEN, TDA4AEN and AM67 evaluation module) uses the PDN-7D.DES scheme to demonstrate flexible processor performance with all optional features.

Processor Performance

The *J722S/AM67x/TDA4VEN/TDA4AEN* processor can provide 2 basic levels of performance as dictated by the primary clock rate of 1.25 or 1.4GHz which requires 2 different VDD_CORE supply voltage levels of 0.75V or 0.85V, Table 1. A flexible processing PDN scheme has been defined as well that allows the processor to boot up at one performance level (1.4GHz, 0.85V or 1.25GHz, 0.75V) and then transition to a different performance level using system software. The flexibility to operate the processor at a lower clock and VDD_CORE voltage requires the 0.85V fixed input supplies (VDDR_CORE, VDD_MMC0 and VDDA_0P85_xxx) to be independently sourced, see VDD_RAM_0V85 power rail in Table 1. Optional processor low power modes (LPM) can be supported if an independent supply for VDD_CANUART is used to allow all other low voltage supplies to be disabled for SoC power reduction, see VDD_IORET_0V75 power rail in Table 1.

Table 1. Low Voltage Supplies versus Performance and Low Power Mode

Performance Use Cases	PDN-ID	Supply Voltages	Power Rails	SoC Low Voltage Supply Inputs
1.4GHz	PDN-7A, 7B, 7C	0.85V	VDD_CORE	VDD_CORE, VDD_CANUART, VDDR_CORE, VDD_MMC0 VDDA_CORE_xxx,VDDA_0P85_xxx
1,25GHz	PDN-7L, 7N, 7M	0.75 0.85V	VDD_CORE VDD_RAM_0V85	VDD_CORE, VDD_CANUART VDDA_CORE_xxx VDDR_CORE, VDD_MMC0 VDDA_0P85_xxx
Flexible 1.4GHz or 1.25GHz	PDN-7D, 7P	0.85 / 0.75V 0.85V	VDD_CORE VDD_RAM_0V85	VDD_CORE, VDD_CANUARTVDDA_CORE_xxx VDDR_CORE, VDD_MMC0 VDDA_0P85_xxx
Low Power Modes	PDN-7C, 7D PDN-7N, 7P	0.85 / 0.75V 0.85V 0.75V	VDD_CORE VDD_RAM_0V85 VDD_IORET_0V75	VDD_CORE VDDA_CORE_xxx VDDR_CORE, VDD_MMC0 VDDA_0P85_xxx VDD_CANUART

Note

- VDD_CORE supply voltage is set by the HCPS discrete buck's VSEL input setting
- VDD_CORE and VDD_CANUART are independent, dual voltage digital supplies operating at either 0.75V or 0.85V
- VDDA_CORE_xxx are analog supplies that must be derived from VDD_CORE (0.75/0.85V) using in-line supply filtering
- VDDR_CORE and VDD_MMC0 are fixed 0.85V digital supplies
- VDDA_0P85_xxx are fixed 0.85V analog supplies derived from same supply used for VDDR_CORE and VDD_MMC0 (typically VDD_RAM_0V85 power rail) using in-line supply filtering
- VDD_CANUART and VDDSHV_CANUART are the only enabled supplies during Partial IO Retention LPM. Partial IO and DDR Retention LPM needs to enable 2 additional supplies: VDDS_DDR (1.1V) and VDD1_DDR_1V8 (1.8V).

The *J722S/AM67x/TDA4VEN/TDA4AEN* processor has 3 key use cases across automotive and industrial markets, Table 2. Robust PDN designs must be able to support these processor use case operations under peak power conditions when the highest silicon junction temperature causes maximum leakage current and extreme processor resource usage causes peak dynamic currents.

The *J722S/AM67x/TDA4VEN/TDA4AEN* power estimation tool (PET) can be used to estimate a processor's power dissipation for different resource loadings per use case. The PET can provide both a PDN and Thermal power estimate. A PDN estimate gives the peak SoC loads over very short elapsed times (1-10us) during high processor resource demand conditions. The PDN or peak estimate is used for PDN design to ensure sufficient output current is available to support peak loads across all input supplies. A Thermal estimate gives the average sustained power over several minutes during maximum use case conditions. The Thermal or average power estimate is used for designing a processor's thermal management system to avoid exceeding the silicon junction temperature (T_J) maximum.

Table 2. Key Use Case Conditions and Peak Load Currents

Use Case and Clock	SoC T_J [C]	Core Supply [V]	Lkg Load [A]	Load Step [A]	Peak Load [A]
EVM Superset 1.4GHz	+125	0.85	3.7	12.7	16.4
AI Box 1.25GHz	+125	0.75	3.5	10	13.5
Front Camera 1.25GHz	+125	0.75	3.2	9.2	12.4

Note

- Leakage current is derived from PET estimate of the leakage or constant power draw due to applying a supply voltage to SoC's internal transistors.
- Dynamic current is derived from PET estimate of the dynamic or transient power draw due to dynamic switching of SoC's internal transistors.
- Peak load current is the total of the leakage plus dynamic currents over very short elapsed times (1 – 10us).
- Load step is the change in load current from the constant load to peak load current.

Platform Support

PDN designs must support *J722S/AM67x/TDA4VEN/TDA4AEN* processor, SDRAM, boot and storage Flash memories, see Table 3. The base power devices are a functional safety-compliant PMIC (TPS6522312-Q1) and a high-current power stage (HCPS) using functional safety capable, fast transient, stackable buck converter (TPS62875B-Q1) to supply the heaviest processor load drawn by VDD_CORE supply.

Table 3. J722S EVM Platform PNs and Features

Platform Devices	Parameters	PNs and Features
SoC	Processing	TDA4VENx-Q1 / TDA4AENx-Q1 Up to Quad 64-bit Arm® Cortex®-A53 microprocessor up to 1.4GHz for 0.85V and 1.25GHz for 0.75V 3x different Arm® Cortex®-R5F up to 800MHz,to support MCU Channel with FFI to support Device Management to support Run-time Management Two Deep Learning Accelerators (up to 4 TOPS total), each with: C7x floating point and Matrix Multiply Accelerator (MMA) Depth and Motion Processing Accelerators (DMPAC)Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP)
SDRAM Memory	Type and Size	MT53E2G32D4DE-046 AUT:C 1 EMIFs / Dual Banks LPDDR4 (32b, 64Gb, 4000MTs)
Boot Flash Memory	Type and Size	S28HS512TGABHM010 OSPI: 512Mb xSPI or W35N01JWTBAG Octal-NAND: 1Gb
Storage Flash Memory	Type and Size	MTFC32GAZAQHD-AAT eMMC: 32GB
Base Power Devices	PMIC	TPS6522312RAHRQ1 "223" = internal ADC for PMIC T_J monitoring or TPS6522112RAHRQ1 "221" = no ADC
	HCPS	TPS62875B2QWRZVRQ1, Scalable Output Current: "74" = 15A, "75" = 20A, "76" = 25A, "77" = 30A Pkg = WQFN-24 or TPS62873Y1QWRXSRQ1, Scalable Output Current: "70" = 6A, "71" = 9A, "72" = 12A, "73" = 15APkg = VQFN-16

PDN Comparisons

All PDN comparison tables describe designs with the following characteristics:

1. TPS6522312-Q1 PMIC with ADC functionality
2. A 1st stage battery power converter that provides both 3.3V & 5.0V output voltages. The discrete dual voltage LDO (TLV7103318-Q1) used for a few PDN variants to support UHS-I SD cards and some automotive CAN transceivers need 5.0V inputs. If a single 3.3V 1st stage converter is used, then a discrete step-up converter (TPS61240-Q1) could be added as needed.
3. Three PDN scheme pairs have similar PMIC resource assignments with small differences as needed for different processing performance (0.75V or 0.85V) and related power mapping changes:
   a. A and L
   b. B and M
   c. C and N
4. A different buck convert PN can be used within the HCPS for higher performance PDN-7x versus reduced performance PDN-5x schemes in order to realize designs with reduced cost & area.

Table 4. PDN-7A/B and PDN-5L/M Features

PDN Variants										
Features		**7A**	**7A.S**	**7A5**	**7B**	**7B.E**	**5L**	**5L.S**	**5M**	**5M.E**
Safety	ASIL-B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input Voltage	3.3V	Yes	Yes		Yes	Yes	Yes	Yes	Yes	Yes
	5.0V			Yes						
Processor Performance	1.4GHz, 0.85V	Yes TPS62875 B2-Q1	Yes TPS62875 B2-Q1	Yes TPS62875 B2-Q1	Yes TPS62875 B2-Q1	Yes TPS62875 B2-Q1				
	1.25GHz, 0.75V						Yes TPS62873 -Q1	Yes TPS62873 -Q1	Yes TPS62873 -Q1	Yes TPS62873 -Q1
Flexible	1.4GHz or 1.25GHz									
PMIC	Available Resources	Buck3, Buck4, GPIO2, GPIO4	Buck3, Buck4, GPIO2, GPIO4	Buck3, GPIO2, GPIO4,	Buck3, Buck4, GPIO2, GPIO4	Buck3, Buck4, GPIO2, GPIO4	Buck4, GPIO2, GPIO4	Buck4, GPIO2, GPIO4	Buck4, GPIO2, GPIO4	Buck4, GPIO2, GPIO4
Optional Features										
Low Power Modes	Partial IO Retention Only									
	Partial IO and DDR Retention									
Security	Efuse Prgm on-board	Yes	Yes	Yes		Yes TPS7A21 P-Q1	Yes	Yes		Yes TPS7A21 P-Q1
Portable Storage	UHS-I SD card		Yes TLV71033 18-Q1		Yes	Yes		Yes TLV71033 18-Q1	Yes	Yes
Pwr IC Cost Ratio vs EVM		0.88	0.91	0.88	0.88	0.91	0.78	0.81	0.78	0.81
Pwr IC Area Ratio vs EVM		0.63	0.66	0.63	0.63	0.77	0.58	0.61	0.63	0.72
Pwr IC Area [mm**2**]		42.4	44.8	42.4	42.4	52.0	39.1	41.5	39.1	48.7

Table 5. PDN-7C Features

PDN Variants									
Features		**7C**	**7C.E**	**7C.S**	**7C.ES**	**7C.D**	**7C.DE**	**7C.DS**	**7C.DES**
Safety	ASIL-B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input Voltage	3.3V	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	5.0V								
Processor Performance	1.4GHz, 0.85V	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1
	1.25GHz, 0.75V								
Flexible	1.4GHz or 1.25GHz								
PMIC	Available Resources	Buck3 GPIO2	Buck3 GPIO	Buck3 GPIO	Buck3 GPIO	Buck3 GPIO	Buck3 GPIO	Buck3 GPIO	Buck3 GPIO
Optional Features and Part Numbers									
Low Power Modes	Partial IO Retention Only	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1
	Partial IO & DDR Retention					Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1
Security	Efuse Prgm on-board		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1
Portable Storage	UHS-I SD card			Yes TLV7103318-Q1	Yes TLV7103318-Q1			Yes TLV7103318-Q1	Yes TLV7103318-Q1
Pwr IC Cost Ratio vs EVM		0.92	0.95	0.96	0.99	0.94	0.97	0.97	1.00
Pwr IC Area Ratio vs EVM		0.69	0.83	0.72	0.86	0.82	0.96	0.86	1.00
Pwr IC Area [mm**2**]		46.4	56.0	48.8	58.4	55.5	65.1	57.9	67.5

Table 6. PDN-5N Features

PDN Variants									
Features		**5N**	**5N.E**	**5N.S**	**5N.ES**	**5N.D**	**5N.DE**	**5N.DS**	**5N.DES**
Safety	ASIL-B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input Voltage	3.3V	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	5.0V								
Processor Performance	1.4GHz, 0.85V								
	1.25GHz, 0.75V	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1	Yes TPS62873-Q1
Flexible	1.4GHz or 1.25GHz								
PMIC	Available Resources	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2
Optional Features and Part Numbers									
Low Power Modes	Partial IO Retention Only	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1
	Partial IO & DDR Retention					Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1
Security	Efuse Prgm on-board		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1
Portable Storage	UHS-I SD card			Yes TLV7103318-Q1	Yes TLV7103318-Q1			Yes TLV7103318-Q1	Yes TLV7103318-Q1
Pwr IC Cost Ratio vs EVM		0.83	0.86	0.86	0.89	0.84	0.87	0.87	0.90
Pwr IC Area Ratio vs EVM		0.64	0.78	0.67	0.82	0.77	0.92	0.81	0.95
Pwr IC Area [mm**2**]		43.1	52.7	45.5	55.1	52.2	61.8	54.6	64.2

Table 7. PDN-7D Features

PDN Variants									
Features		**7D**	**7D.E**	**7D.S**	**7D.ES**	**7D.D**	**7D.DE**	**7D.DS**	**7D.DES (EVM)**
Safety	ASIL-B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input Voltage	3.3V	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	5.0V								
Processor Performance	1.4GHz, 0.85V								
	1.25GHz, 0.75V								
Flexible	1.4GHz (Boot) or 1.25GHz	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1
PMIC	Available Resources	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2	GPIO2
Optional Features and Part Numbers									
Low Power Modes	Partial IO Retention Only	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1	Yes TPS22965-Q1
	Partial IO & DDR Retention					Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1	Yes TLV73318P-Q1
Security	Efuse Prgm on-board		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1		Yes TPS7A21P-Q1
Portable Storage	UHS-I SD card			Yes TLV7103318-Q1	Yes TLV7103318-Q1			Yes TLV7103318-Q1	Yes TLV7103318-Q1
Pwr IC Cost Ratio vs EVM		0.92	0.95	0.96	0.99	0.94	0.97	0.97	1.00
Pwr IC Area Ratio vs EVM		0.69	0.83	0.72	0.86	0.82	0.96	0.86	1.00
Pwr IC Area [mm**2**]		46.4	56.0	48.8	58.4	55.5	65.1	57.9	67.5

Table 8. PDN-7M Features

PDN Variants			
Features		**7M**	**7M.E**
Safety	ASIL-B	Yes	Yes
Input Voltage	3.3V	Yes	Yes
	5.0V		
Processor Performance	1.4GHz, 0.85V		
	1.25GHz, 0.75V		
Flexible	1.4GHz or 1.25GHz (Boot)	Yes TPS62875B2-Q1	Yes TPS62875B2-Q1
PMIC	Available Resources	Buck4 GPIO2, GPIO4	Buck4 GPIO2, GPIO4
Optional Features and Part Numbers			
Low Power Modes	Partial IO Retention Only		
	Partial IO & DDR Retention		
Security	Efuse Prgm on-board		Yes TPS7A21P-Q1
Portable Storage	UHS-I SD card	Yes	Yes
Pwr IC Cost Ratio vs EVM		0.88	0.91
Pwr IC Area Ratio vs EVM		0.63	0.77
Pwr IC Area [mm**2**]		42.4	52.0

Base Power Devices

All PDN designs are supported by a *TPS6522x12-Q1* PMIC that has been optimized for *J722S/AM67x/TDA4VEN/TDA4AEN* processors and a fast transient, discrete buck converter within the TPS6287x-Q1 family that forms the high-current power stage (HCPS) to supply the heaviest VDD_CORE load.

PMIC TPS6522x12-Q1

The common *TPS6522x12-Q1* PMIC can use 1 of 2 variant PNs: 1) *TPS6522312X-Q1* that has an internal ADC to monitor either the PMIC T_J or on-board net voltage connected to a dedicated PMIC GPIO input by I2C. 2) *TPS6522112-Q1* that does not have an ADC. The PMIC internal NVM settings (identified by the PN characters “12”) and pre-configurable finite state machine (PFSM) use four Resource Selection (RS) control signals to direct PMIC power and GPIO resource assignments as needed for implementing different PDN schemes. The optimized *TPS6522x12-Q1* PMIC simplifies the design process, supports multiple PDN schemes, enables recommended power designs and reduces time to market. Table 9 provides an overview of the PMIC's basic features.

Table 9. TPS6522x12-Q1 Basic Features

Features	Characteristics
Junction Temp Range	-40 to +150C
Input Voltage Range	3.0 to 5.5V
Total Number of Regulators	7
DC-DC step-down converters	Qty = 4, 2x Bucks, Single phase: Vo = 0.5 – 3.3V, 3.5A up to 1.2V, 2.5A above 1.2V Dual phase: Vo = 0.5 – 1.2V, Current = 7A max 2x Bucks, Single phase: Vo = 0.5 – 3.3V, Current = 2A max Switching Freq: 2.2 to 4.4MHz Remote voltage sense OV/UV VMON
LDOs	Qty = 3, 2x LDOs, Regulator: Vo = 0.6 – 3.3V, Current = 400mA max Load Switch: Vo = 1.5 – 3.3V, Ron = 200 – 250mohm 1x Low Noise LDO, Regulator: Vo = 1.2 – 3.3V, Current = 300mA max Load Switch: Vo = 2.2 – 3.6V, Ron = 1ohm
Additional Features	AEC-Q100 qualified Functional safety-compliant targeted • Developed for functional safety applications • Documentation to aid ISO26262 and IEC61508 system design available upon product release • Systematic capability and hardware integrity up to ASIL-B and SIL-2 targeted • Undervoltage and overvoltage monitors and current limit on all output supply rails • Undervoltage and overvoltage monitors for two external supply rails and for input supply • Watchdog (trigger or Q&A) • Error signal monitor (level or PWM) • Temperature warning and thermal shutdown • Built-in self-test on voltage monitors Configurable power sequence and GPIO control in non-volatile memory (NVM) 6 configurable GPIOs, reset, interrupt and enable signals One 12-bit ADC function mappable to GPIO (PN: TPS6522312-Q1) I2C serial interface control Interrupt function with programmable masking Output short-circuit and overload protection Overtemperature warning and protection 4 Resource Selection control signals to direct power and GPIO resource assignments

The PMIC Resource Selection (RS[3:0]) signals direct the PMIC power and GPIO resource assignments to support different PDN variants along with add-on discrete power resources as needed for optional features. All four RS control signals are captured during each PMIC cold boot power up sequence. The RS3 and RS2 bits are set automatically when the PMIC’s Pre-configurable Finite State Machine (PFSM) executes two sequences that leverage internal voltage comparators connected to VCCA and VMON1 inputs to determine the PDN input

voltage and VDD_CORE supply levels respectfully. RS1 and RS0 bits are latched logic levels on PMIC's GPIO1 and GPIO2 inputs. The logic levels are set based upon the output voltage of a resistor divider network formed by the combination of PMIC weak, internal pull-up resistors (Rpu about 400k) to VIO supply and any on-board, pull-down resistors (Rpd = 10k) to ground. Table 10 summarizes the PMIC RS[3:0] operations and assignments.

Table 10. PMIC Resource Selection

RS[3:0]	Method	Sensitivity	Logic	Power Assignments	GPIO Assignments
RS3	VCCA internal voltage comparator determines level during pwr up seq	Vin = 5V Vin = 3.3V	1 0	Buck4 Vo = 3.3V Buck4 Vo = 0.75V per PDN	
RS2	VMON1 internal voltage comparator determines level during pwr up seq	VDD_CORE = 0.85V VDD_CORE = 0.75V	1 0	VMON1 V_{THRSH} for 0.85V VMON1 V_{THRSH} for 0.75V	
RS1	GPIO pulled up to 3.3V GPIO pulled down to 0V	No board Rpd Install board 10k Rpd	1 0	Buck4 Vo = 0.75V for LPM Buck4 = Disabled	GPIO1 = GPI / PMIC_nLPM_EN GPIO4 = VMON2 / VDD_IO_3V3
RS0	GPIO pulled up to 3.3V GPIO pulled down to 0V	No board Rpd Install board 10k Rpd	1 0	LDO2 Vo for Efuse Prgm LDO2 Vo for SD Card	GPIO1 = GPI / EN_EFUSE_VPP GPIO1 = GPI / VSEL_SD_VIO

Note

- GPIO# = NVM function / PDN board net connection.
- RS1=1 and RS0=1 state enables flexible VDD_CORE performance with Buck3 set to a fixed 0.85V for supplying VDD_RAM_0V85 power rail.

In addition, TPS6522x12-Q1 PMIC supports a HW option to disable watchdog timer before a system cold boot which is useful during product development and debugging. The PMIC latches the logic level on GPIO6 pin during the execution of an SoC power up sequence.

The logic level dedicates watchdog timer operation as follows:

a) High level disables the Watch-Dog Timer by setting WD_PWRHOLD bit to disable timer's long-window time-out.

b) Low level enables Watch-Dog Timer by setting WD_PWRHOLD bit to enable timer's long-window time-out.

After the PMIC's VCCA input supply is energized and completes NVM initialization, the GPIO6 pin is configured as an input with a weak pull-down resistance and set to nERR_MCU function to monitor SoC processing errors. The J722SXH01EVM - TDA4VEN, TDA4AEN and AM67 evaluation module schematic demonstrates how to connect the SoC's ERRORn output signal through a tri-stateable buffer to isolate the SoC's output from the GPIO6 input pin during the early portion of a power up sequence. This allows the GPIO6 input to be pulled up to PMIC's VCCA supply (either 3.3 or 5V) to disable the watchdog timer or the PMIC's internal, weak pull-down resistor sets a low logic level to enable the watchdog timer. The tri-stateable buffer is required to avoid current bleeding into an unenergized SoC output pin whenever disabling watchdog timer is desired at system cold boot. The latching of GPIO6 level occurs before the PMIC enables the VDD_IO_1V8 supply at 2.5ms time step. Once VDD_IO_1V8 is energized, the tri-state buffer is enabled to connect the SoC's ERRORn output signal to GPIO6 as desired for active system operation.

HCPS TPS6287x-Q1

The HCPS uses a high current, fast transit discrete buck converter *TPS6287x-Q1* PN series capable of supplying output currents ranging from 6 to 30A in a single phase configuration. Two similar buck converters families are available with excellent fast transient performance, stack-able for multi-phase operation, different output current ranges, power optimized package types and similar register maps. An end product's peak load

during very demanding high processor resource use determines which buck PN should be used, Table 11. The buck PN selected and whether to use a multi-phase configuration is dependent upon the total output current capacity needed to provide a positive current margin vs peak load. A good power design practice is to design for +15% current margin for each power rail to enable potential processor resource increases or use case feature growth during development.

Table 11. HCPS Buck PN Options and Settings

PDN-ID	Buck PN	Max Output Currents [A]	Pkg: Types, Pin #, HxWxL [mm2]	Output Voltage [V]	I2C Addr	VSEL Connection
PDN-7x	TPS62874 TPS62875 TPS62876 TPS62877	15 20 25 30	WQFN- FCRLF 24-pins 0.65 x 3.05 x 4.05	0.85	0x44	6.2k to Gnd
				0.75	0x45	0-ohm to Gnd
PDN-5x	TPS62870 TPS62871 TPS62872 TPS62873	6 9 12 15	VQFN- FCRLF 16-pins 1.0 x 2.55 x 3.55	0.85	0x40	6.2k to Gnd
				0.75	0x41	0-ohm to Gnd

Table 12 shows PMIC and HCPS output voltages with start-up enabling and shut-down disabling sequence delays per TPS6522x12X-Q1 NVM elapsed time step settings. For more information on PMIC registers and NVM settings, see TPS6522x12X-Q1 user's guide.

Table 12. Base Power Voltage and Sequencing

PDN	HCPS	PMIC		
Power Rail / Net Name	**Resource**	**Resource**	**Output Voltage [V]**	**Startup / Shutdown Delay [ms]**
EN_3V3_VIO		LDO2	Bypass mode, Vin = 3.3	0 / 2.5
VDD_IO_1V8		Buck1	1.8	2.5 / 2.0
VDA_PLL_1V8		LDO1	1.8	2.5 / 2.0
VDA_PHY_1V8		LDO3	1.8	2.5 / 2.0
VDD_DDR_1V1		Buck2	1.1	4.8 / 1.5
VDD_IORET_0V75		Buck4	0.75	5.4 / 1.0
EN_CORE_BUCK		GPIO5	Push-Pull, VSYS_3V3 reference	5.95 / 1.0
VDD_CORE	Buck-A		0.75 / 0.85 (VSEL R setting)	5.95 / 1.0
VDD_RAM_0V85		Buck3	0.85	7.45 / 0.5
MCU_PORz		nRSTOUT	Open-Drain, Rpu to VDD_IO_1V8 (1)	14.8 / 0

Note

GPIO5 and nRSTOUT control signals have NVM settings that select either Push-Pull (PP) buffer type referenced to PMIC's VIO input supply or Open-Drain (OD) buffer type with external pull-up resistor (Rpu) to desired voltage. Buck3 and Buck4 operation and inclusion in the power sequencing is dependent on PMIC RS[3:0] settings.

Example Power Maps

Power resource and control signal mapping diagrams for several PDN-7x variants have been captured to demonstrate *J722S/AM67x/TDA4VEN/TDA4AEN* platform (SoC, LPDDR4 and Flash memories, power resources) support for 1.4 or 1.25GHz processing performance with optional PDN features.

All PDN schemes that apply a 3.3V voltage sourced from the 1st stage battery power converter to an SoC interface input supply (VDDSHV_CANUART, VDDSHV5) must enable the PMIC to begin a complete SoC power up sequence upon applying 3.3V. This avoids subjecting the SoC to a partial power condition.

All PDN schemes support a HW option to disable watchdog timer before a system cold boot which can be useful during product development and debugging. The PMIC latches the logic level on GPIO6 pin during the execution of an SoC power up sequence, see PMIC TPS6522x12-Q1 section above for details.

All PDN-5x schemes support the similar feature sets as the PDN-7x examples shown below. A key difference is the HCPS uses a buck converter PN that supports smaller output currents, see HCPS TPS6287x-Q1 section above for details.

A few PDN schemes may show a 1st stage battery power converter that provides both 3.3V & 5.0V output voltages. The discrete dual voltage LDO (TLV7103318-Q1) used for a few PDN variants to support UHS-I SD cards and some automotive CAN transceivers need 5.0V inputs to provide regulated 3.3V outputs. If a single 3.3V 1st stage converter is used, then a discrete step-up converter (TPS61240-Q1) could be added as needed.

J722S PDN-7A with 3.3V input

PDN-7A uses 3.3V input voltage with only the base power devices to enable 1.4GHz processing for *J722S/AM67x/TDA4VEN/TDA4AEN* platform that supports in-field Efuse programming optional feature, Table 13.

Table 13. 1.4GHz, 3.3Vin, PDN-7A Features and PMIC Resource Selection Settings

PDN Features	PDN-7A (Base only)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.4GHz, 0.85V	TPS62875B2-Q1 20A Buck	Vin/VCCA auto detect	Core/ VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1 PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75V or 0.85V
Platform Support	Yes						
HS SoC Efuse prgm	Yes		0	1	0	0	

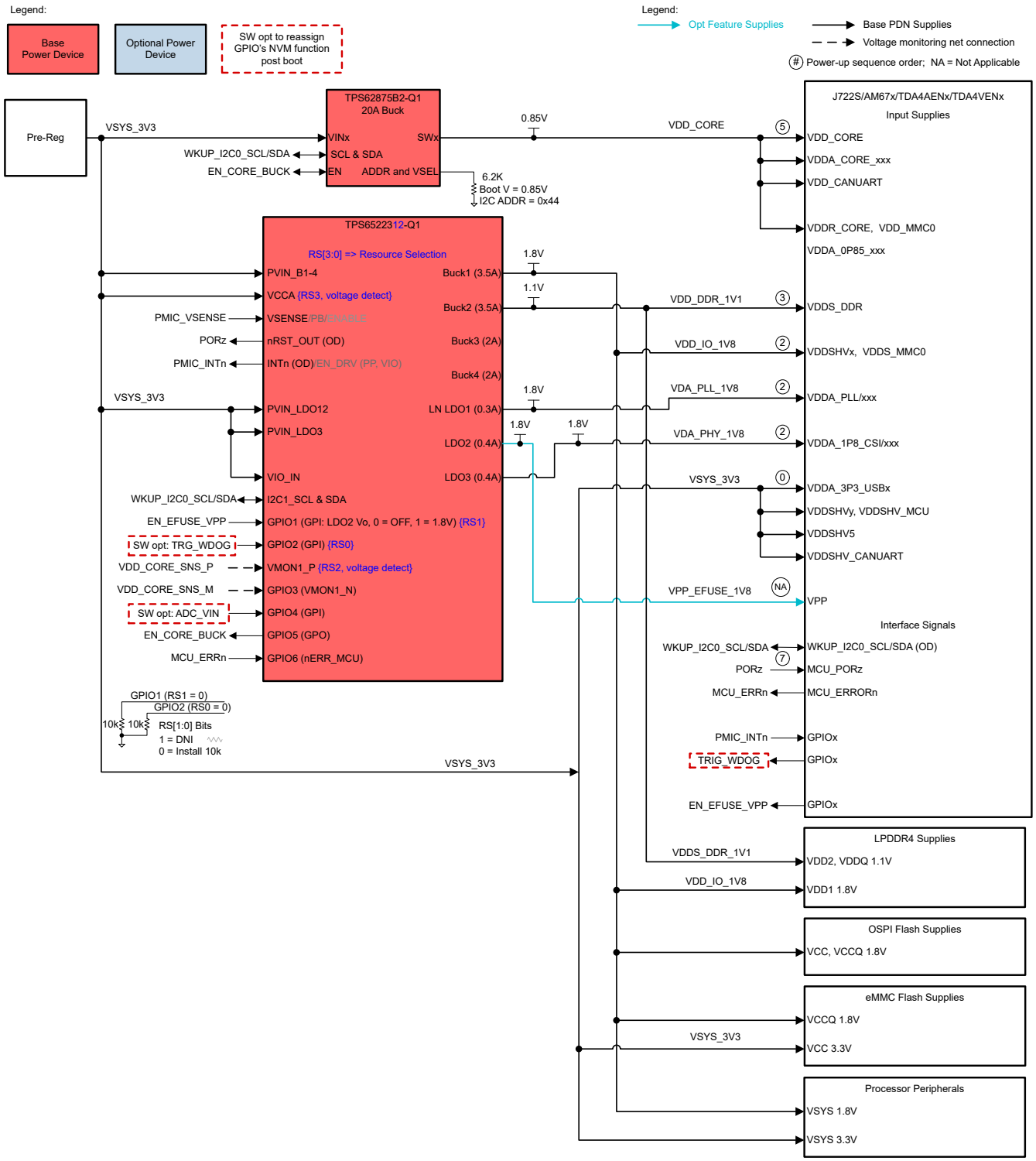

Figure 1. 1.4GHz, 3.3Vin, PDN-7A with Optional eFuse Programming

J722S PDN-7A.S with 3.3V input

PDN-7A.S uses 3.3V input voltage with base power devices to provide 1.4GHz processing for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 1 discrete device to enable UHS-I SD card optional feature, Table 14.

Table 14. 1.4GHz, 3.3Vin, PDN-7A.S Variant Features and PMIC Resource Selection Settings

PDN Features	PDN-7A.S (Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.4GHz, 0.85V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
HS SoC Efuse prgm	Yes		0	1	0	0	
Optional Feature needs add-on discrete power device							
UHS-I SD card	Yes	TLV7103318-Q1, 200mA dual Vo LDO					

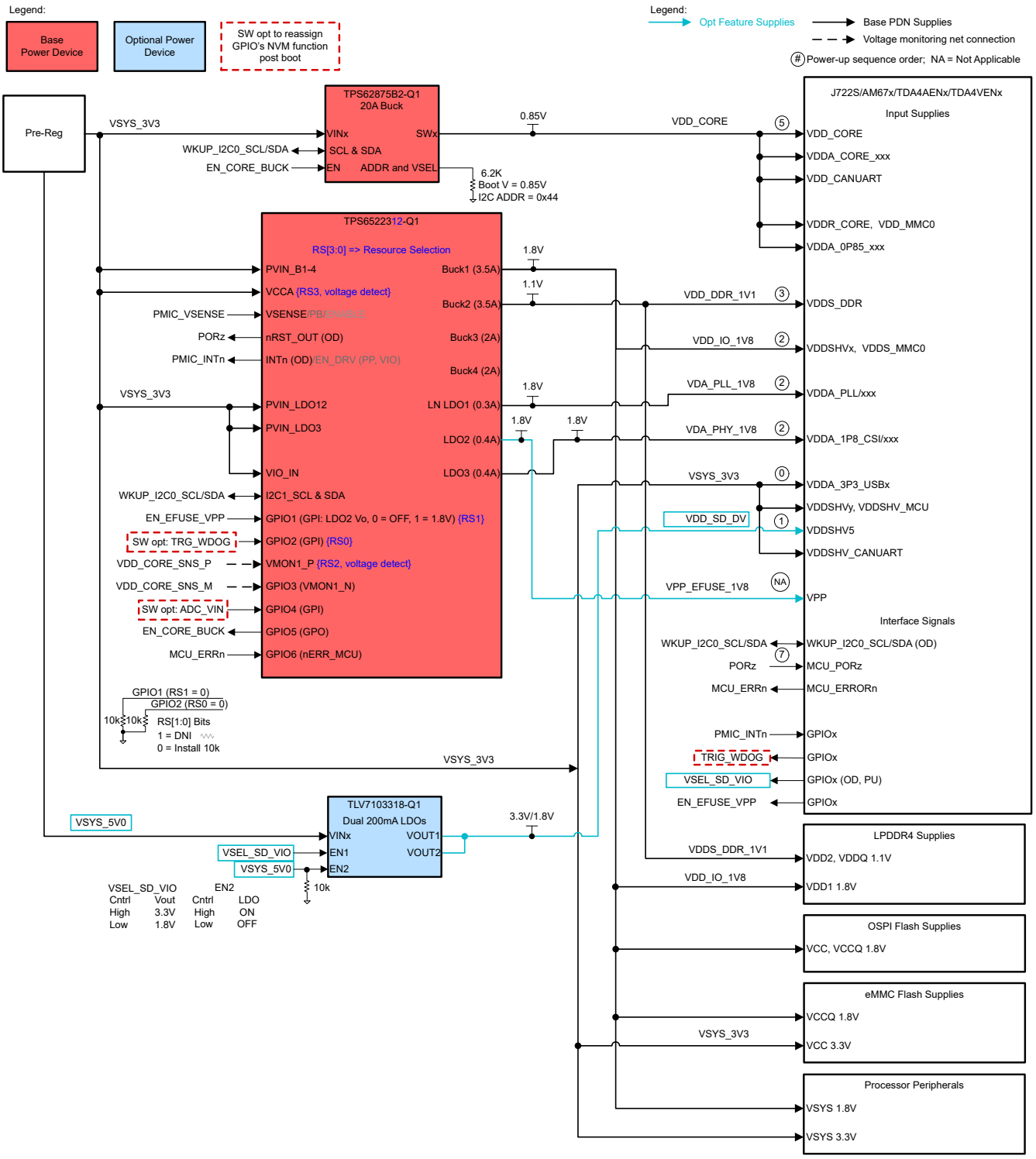

Figure 2. 1.4GHz, 3.3Vin, PDN-7A.S variant adds Optional UHS-I SD Card

J722S PDN-7B with 3.3V input

PDN-7B uses 3.3V input voltage with only the base power devices to provide 1.4GHz processing for*J722S/AM67x/TDA4VEN/TDA4AEN* platform that supports UHS-I SD card optional feature, Table 15.

Table 15. 1.4GHz, 3.3Vin, PDN-7B Features and PMIC Resource Selection Settings

PDN Features	PDN-7B (Base only)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.4GHz, 0.85V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
UHS-I SD Card	Yes		0	1	0	1	

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram

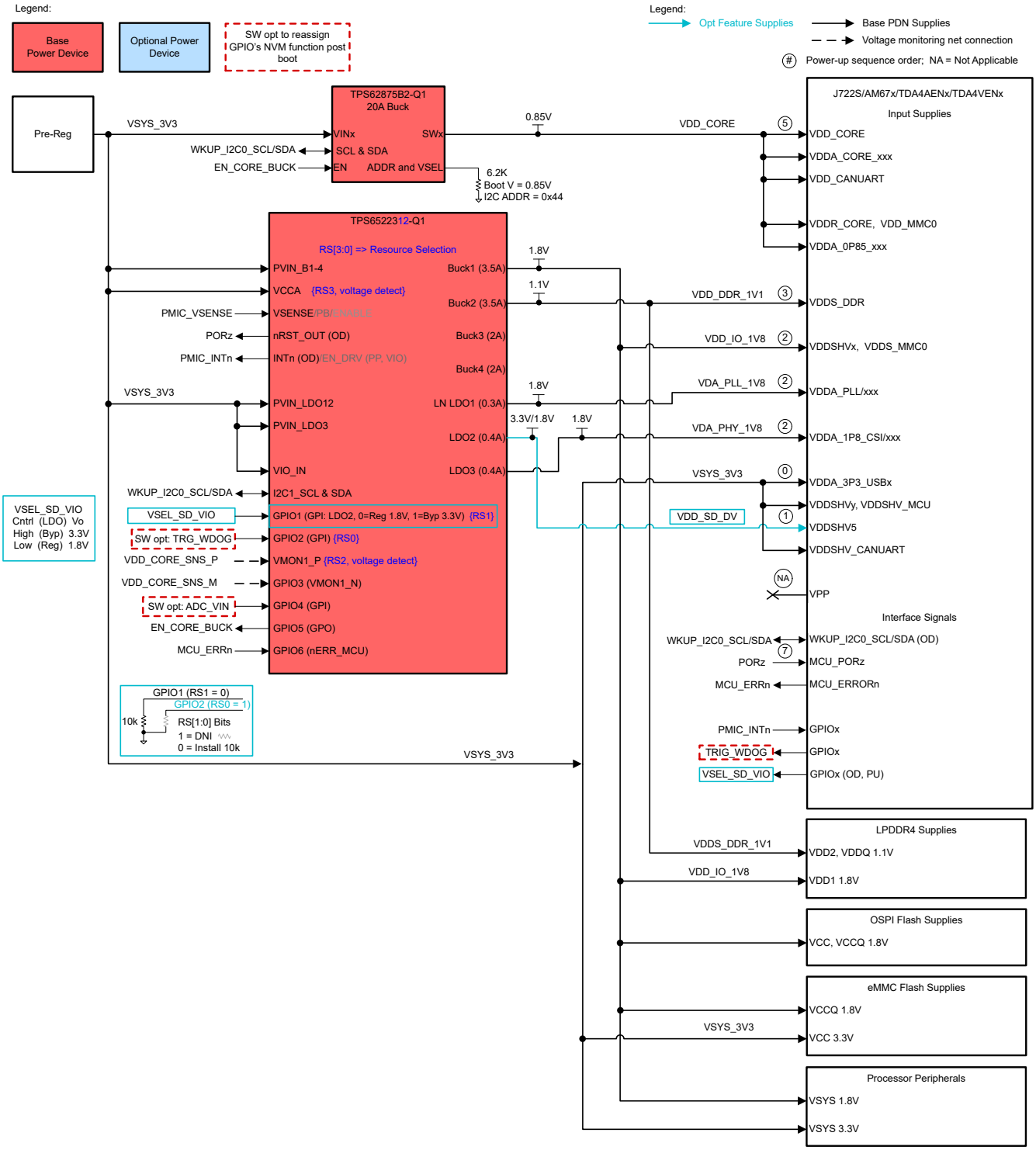

Figure 3. 1.4GHz, 3.3Vin, PDN-7B with Optional UHS-I SD Card

J722S PDN-7B.E with 3.3V input

PDN-7B.E uses 3.3V input voltage with base power devices to provide 1.4GHz processing for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 1 discrete device to enable in-field HS Efuse Programming optional feature, Table 16.

Table 16. 1.4GHz, 3.3Vin, PDN-7B.E Variant Features and PMIC Resource Selection Settings

PDN Features	PDN-7B.E(Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.4GHz, 0.85V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
UHS-I SD Card	Yes		0	1	0	1	
Optional Feature needs add-on discrete power device							
HS SoC Efuse prgm	Yes	TPS7A21P-Q1, 500mA LDO					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram

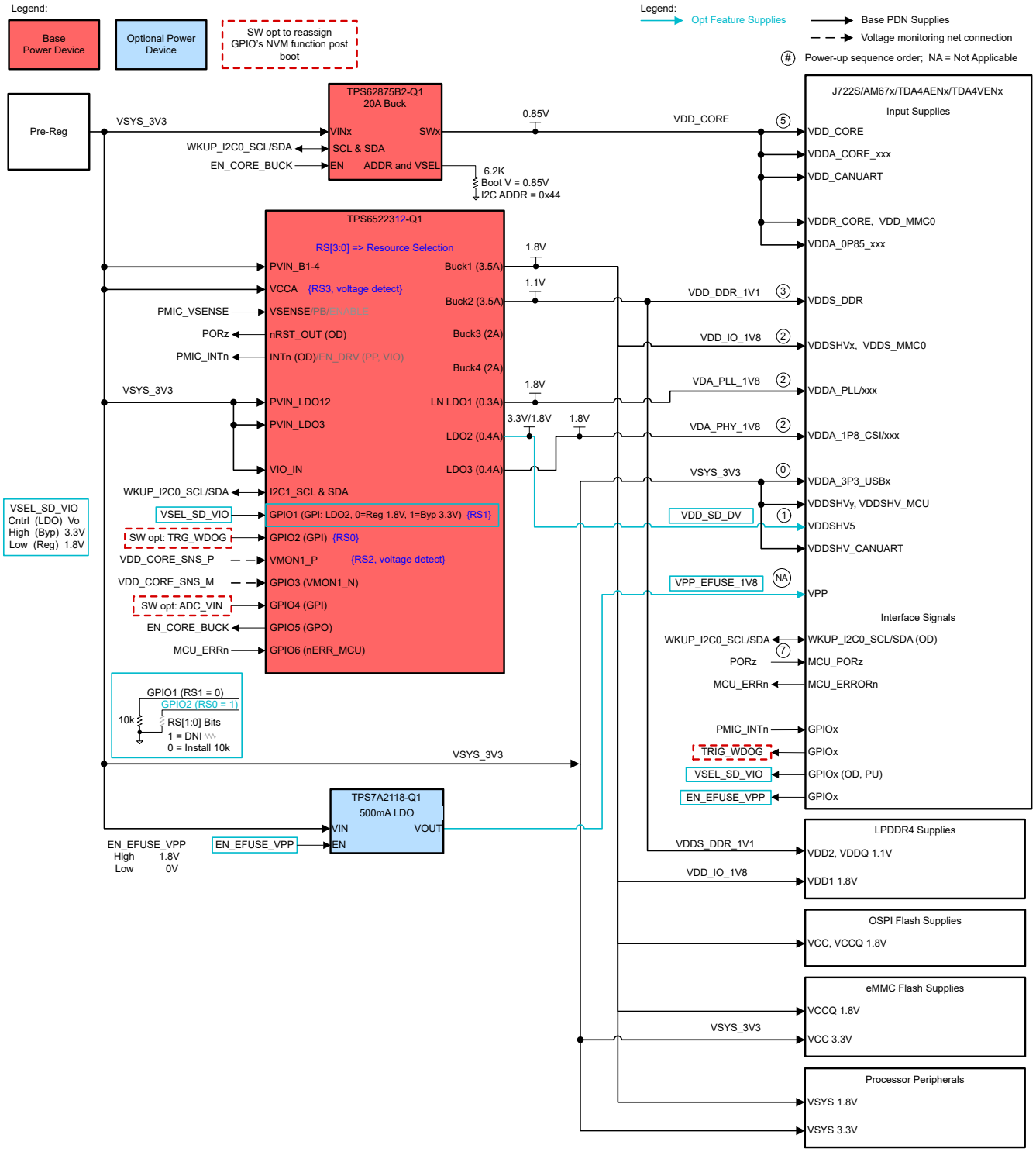

Figure 4. 1.4GHz, 3.3Vin, PDN-7B.E variant adds Optional Efuse Programming

J722S PDN-7C with 3.3V input

PDN-7C uses 3.3V input voltage with base power devices to provide 1.4GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 1 discrete device to enable the Partial IO LPM optional feature, Table 17.

Table 17. 1.4GHz, 3.3Vin, PDN-7C Features and PMIC Resource Selection Settings

PDN Features	PDN-7C (Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Flex Per	1.4GHz, 0.85V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes		0	1	1		0
Optional Feature needs add-on discrete power device							
Partial IO Retention	Yes	TPS22965-Q1, 4A Load Switch					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference versus baseline PDN-7A scheme as shown in diagram

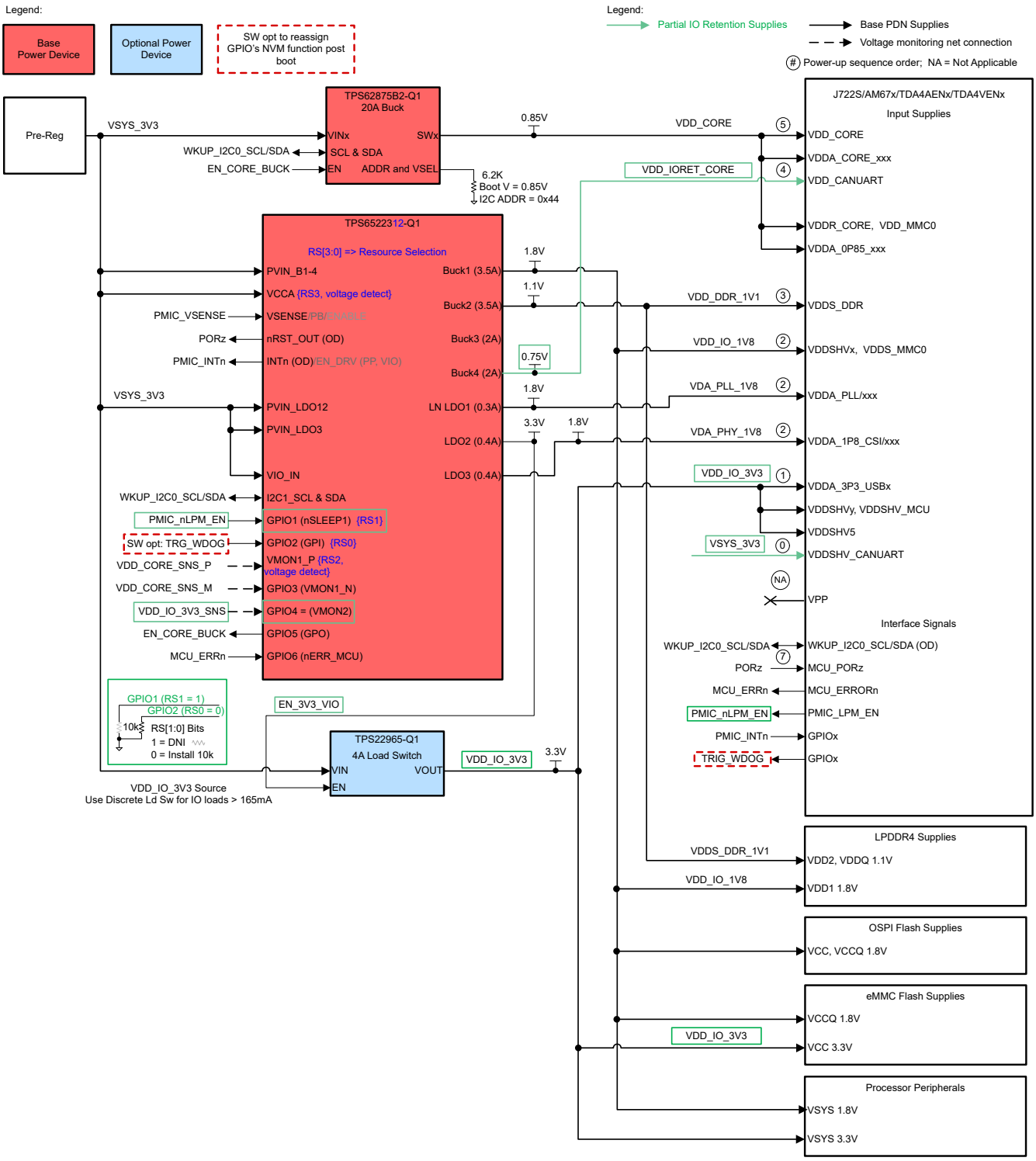

Figure 5. 1.4GHz, 3.3Vin, PDN-7C with Partial IO Retention LPM

J722S PDN-7D with 3.3V input

PDN-7D uses 3.3V input voltage with base power devices to provide flexible 1.4GHz boot and run-time adjustable to 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 1 discrete device to enable the Partial IO LPM optional feature, Table 18.

Table 18. 1.4GHz, 3.3Vin, Flexible PDN-7D Features and PMIC Resource Selection Settings

PDN Features	PDN-7D (Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Flex Perf Boot SW Adjusted	1.4GHz, 0.85V 1.25GHz, 0.75V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes		0	1	1		1
Optional Feature needs add-on discrete power device							
Partial IO Retention	Yes	TPS22965-Q1, 4A Load Switch					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram

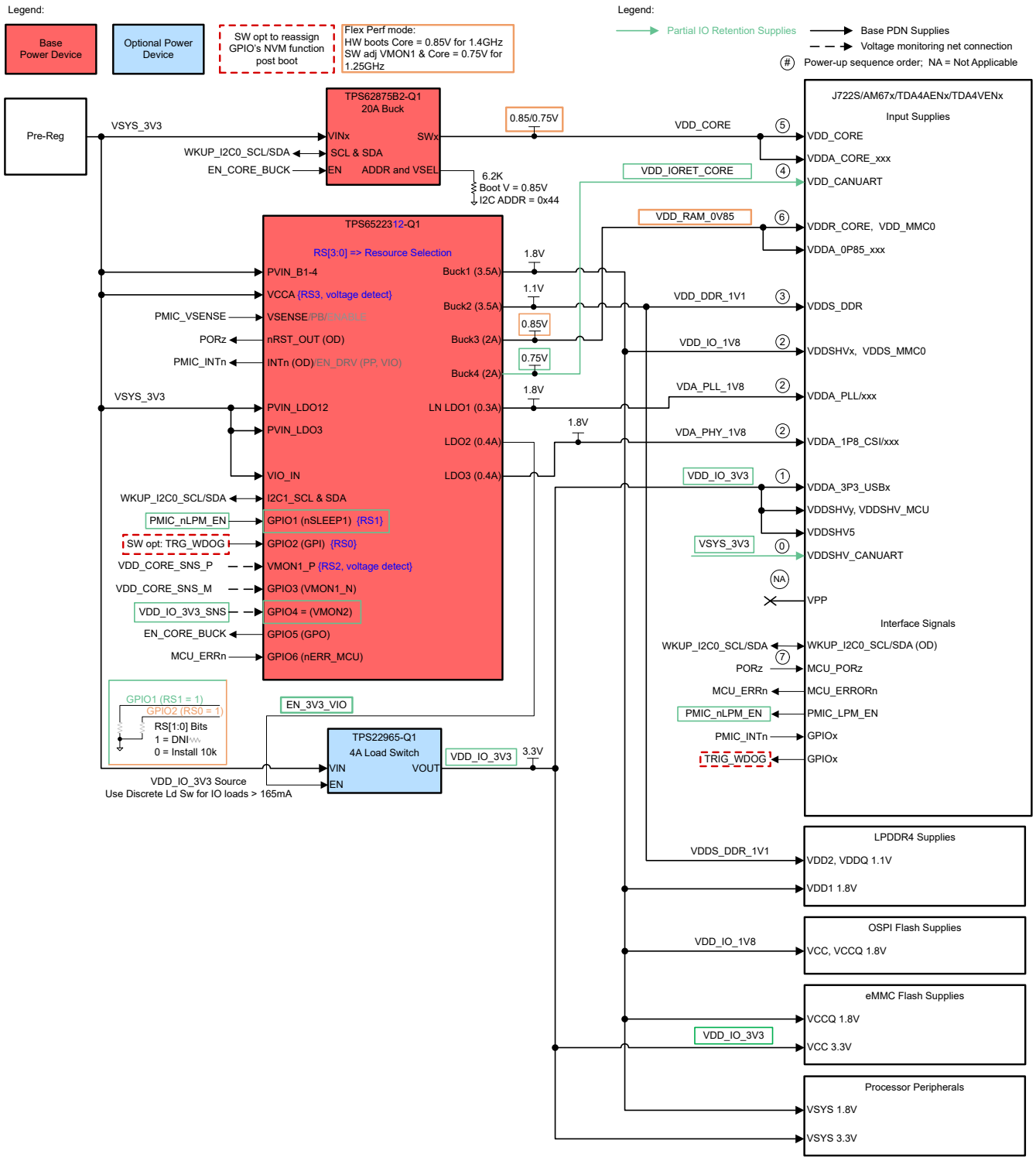

Figure 6. 1.4GHz, 3.3Vin, Flexible PDN-7D with Partial IO Retention LPM

J722S PDN-7D.DES with 3.3V input (EVM)

PDN-7D.DES uses 3.3V input voltage with base power devices to provide flexible 1.4GHz boot and run-time adjustable to 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform. PDN-7D.DES adds 4 discrete devices to enable Partial IO and DDR Retention LPM, HS SOC Efuse programming and UHS-I SD card optional features, Table 19. The TI EVM demonstrates this PDN scheme.

Table 19. 1.4GHz, 3.3Vin, Flexible PDN-7D.DES Variant Features and PMIC Resource Selection Settings Diagram

PDN Features	PDN-7D.DES (Base + add)	Power Resource	PMIC Resource Selection RS [3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Flex Perf Boot SW Adjusted	1.4GHz, 0.85V 1.25GHz, 0.75V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes		0	1	1		1
Optional Feature needs add-on discrete power device							
Partial IO Retention	Yes	TPS22965-Q1, 4A Load Switch					
and DDR Retention	Yes	TPS73318P-Q1, 300mA LDO					
HS SoC Efuse prgm	Yes	TPS7A21P-Q1, 500mA LDO					
UHS-I SD Card	Yes	TLV7103318-Q1, Dual Vo LDO					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram.

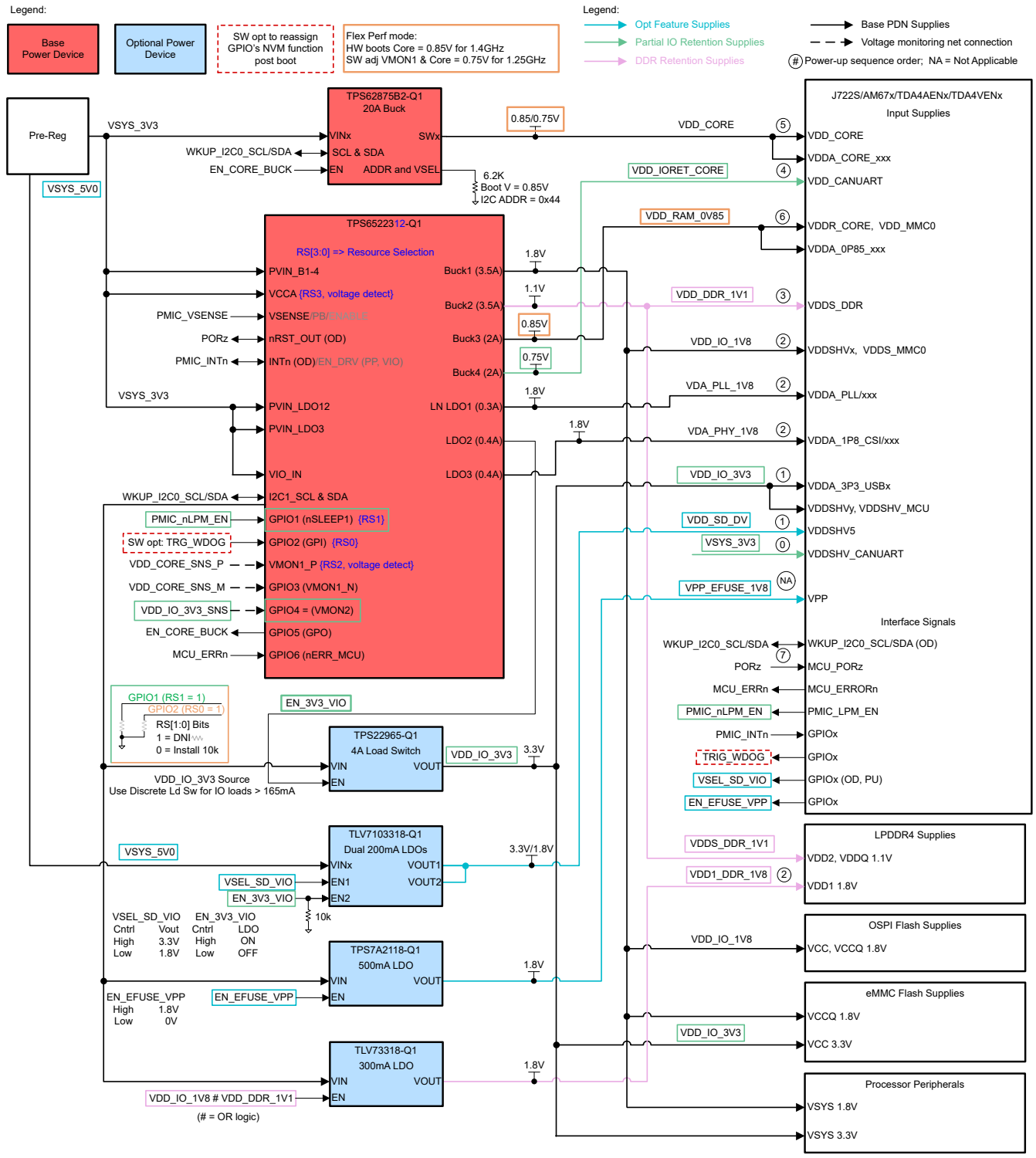

Figure 7. 1.4GHz, 3.3Vin, Flexible PDN-7D.DES variant adds Optional Partial IO and DDR Retention LPM, Efuse Programming and UHS-I SD Card

J722S PDN-5L with 3.3V input

PDN-5L uses 3.3V input voltage with only the base power devices to provide 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform that support in-field Efuse programming optional feature, Table 20.

Table 20. 1.25GHz, 3.3Vin, PDN-5L Features and PMIC Resource Selection Settings

PDN Features	PDN-5L (Base only)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.25GHz	TPS62873-Q1, 15A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
HS SoC Efuse prgm	Yes		0	0	0	0	

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference versus baseline PDN-7A scheme as shown in diagram

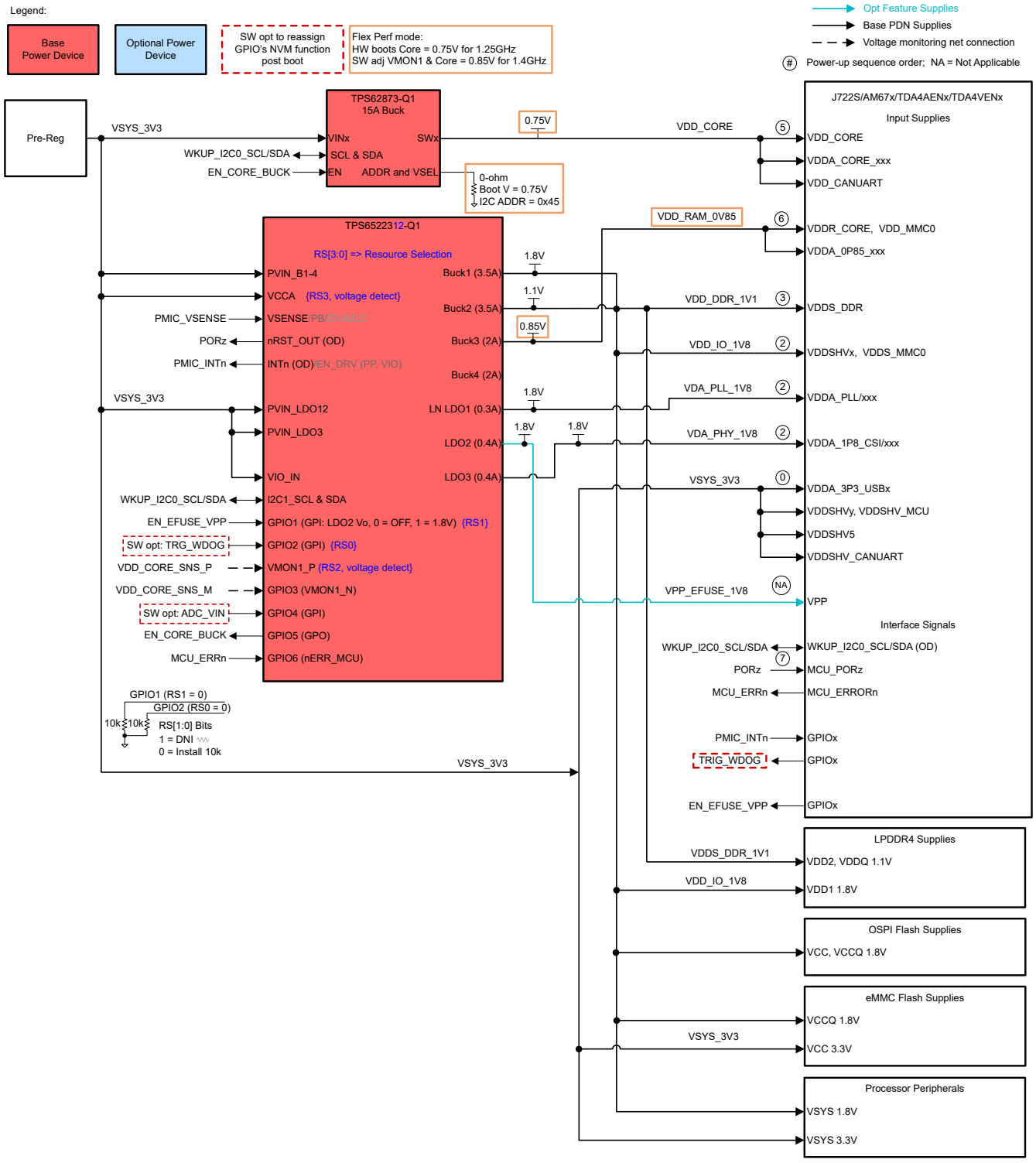

Figure 8. 1.25GHz, 3.3Vin, PDN-5L with Optional eFuse Programming

J722S PDN-5M with 3.3V input

PDN-5M uses 3.3V input voltage with only the base power devices to provide 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN*platform that support UHS-I SD card optional feature, Table 21.

Table 21. 1.25GHz, 3.3Vin, PDN-5M Features and PMIC Resource Selection Settings

PDN Features	PDN-5M (Base only)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.25GHz	TPS62873-Q1, 15A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
HS SoC Efuse prgm	Yes		0	0	0	1	

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram.

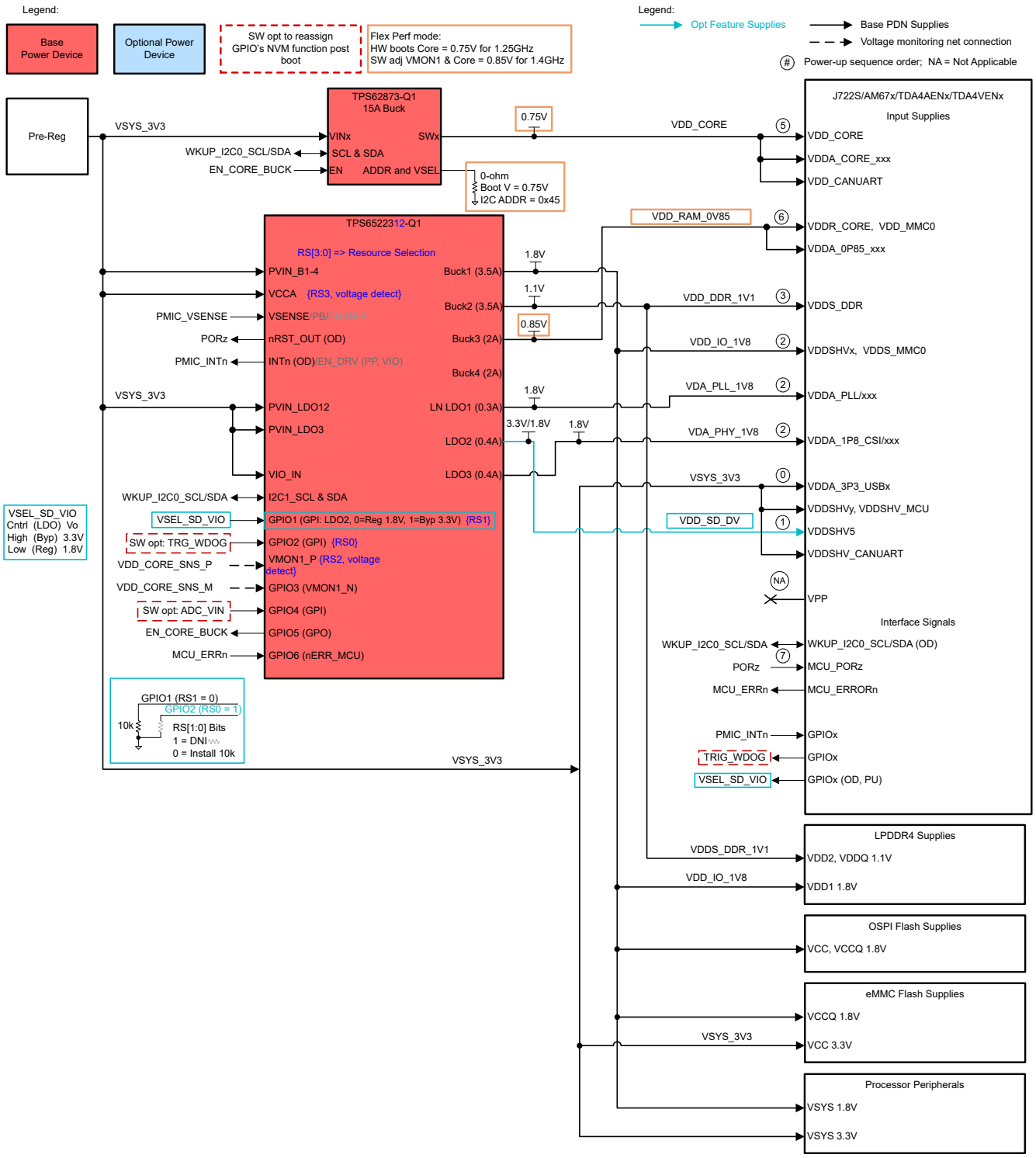

Figure 9. 1.25GHz, 3.3Vin, PDN-5M with Optional UHS-I SD Card

J722S PDN-5N with 3.3V input

PDN-5N uses 3.3V input voltage with base power devices to provide 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 1 discrete device to enable the Partial IO LPM optional feature, Table 22.

Table 22. 1.25GHz, 3.3Vin, PDN-5N Features and PMIC Resource Selection Settings

PDN Features	PDN-5N (Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.25GHz, 0.75V	TPS62873-Q1, 15A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes		0	0	1		0
Optional Feature needs add-on discrete power device							
Partial IO Retention	Yes	TPS22965-Q1, 4A Load Switch					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram.

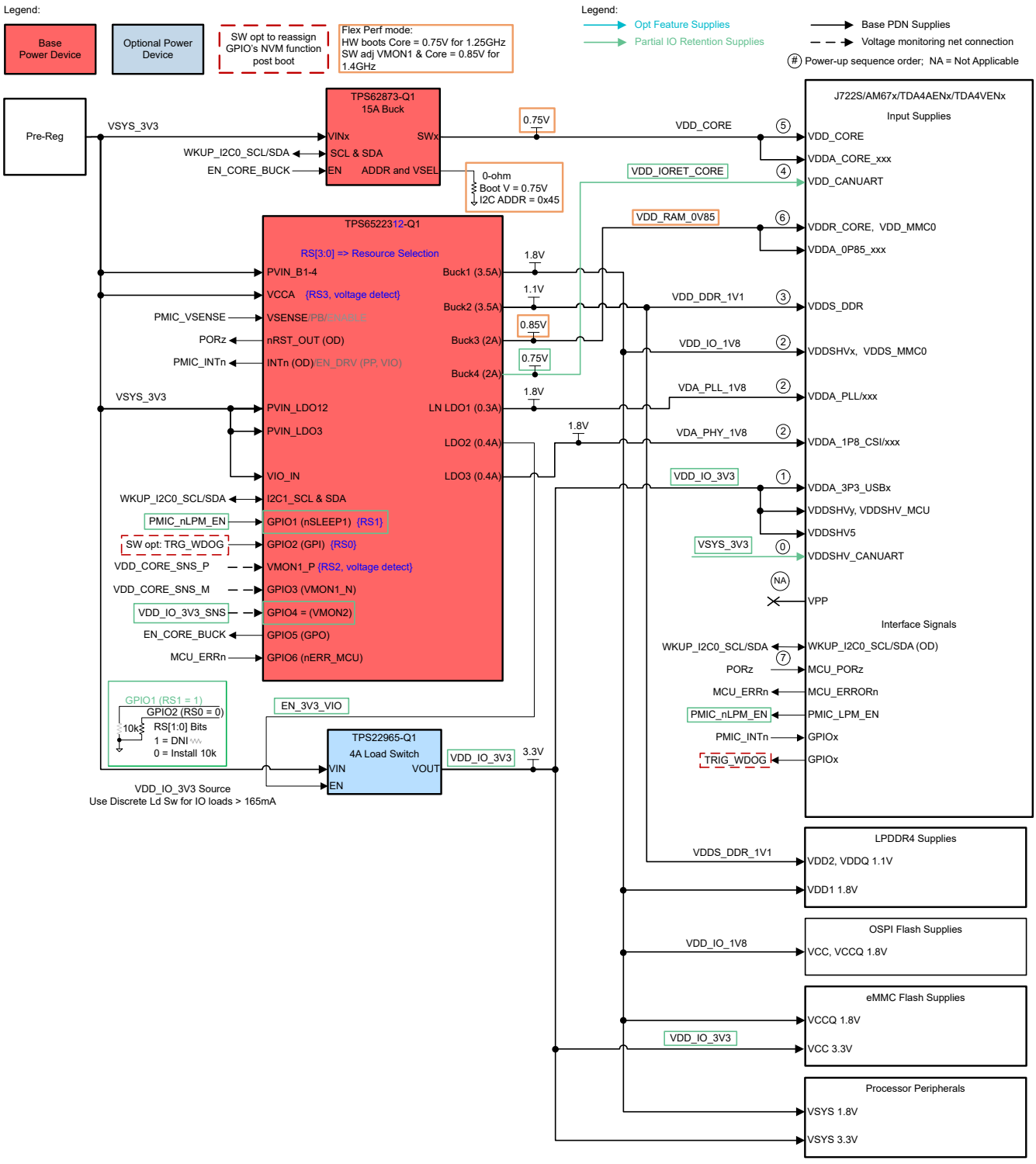

Figure 10. 1.25GHz, 3.3Vin, PDN-5N With Partial IO Retention LPM

J722S PDN-5N.DES with 3.3V input

PDN-5N.DES uses 3.3V input voltage with base power devices to provide 1.25GHz performance for *J722S/AM67x/TDA4VEN/TDA4AEN* platform plus 4 discrete devices to enable Partial IO and DDR Retention LPM, HS SOC Efuse programming and UHS-I SD card features, Table 23.

Table 23. 1.25GHz, 3.3Vin, PDN-5N.DES Variant Features and PMIC Resource Selection Settings

PDN Features	PDN-5N.DES (Base + add)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Flex Perf Boot SW Adjusted	1.25GHz, 0.75V 1.4GHz, 0.85V	TPS62873-Q1, 15A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	3.3V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes		0	0	1		0
Optional Feature needs add-on discrete power device							
Partial IO Retention	Yes	TPS22965-Q1, 4A Load Switch					
and DDR Retention	Yes	TPS73318P-Q1, 300mA LDO					
HS SoC Efuse prgm	Yes	TPS7A21P-Q1, 500mA LDO					
UHS-I SD Card	Yes	TLV7103318-Q1, Dual Vo LDO					

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram.

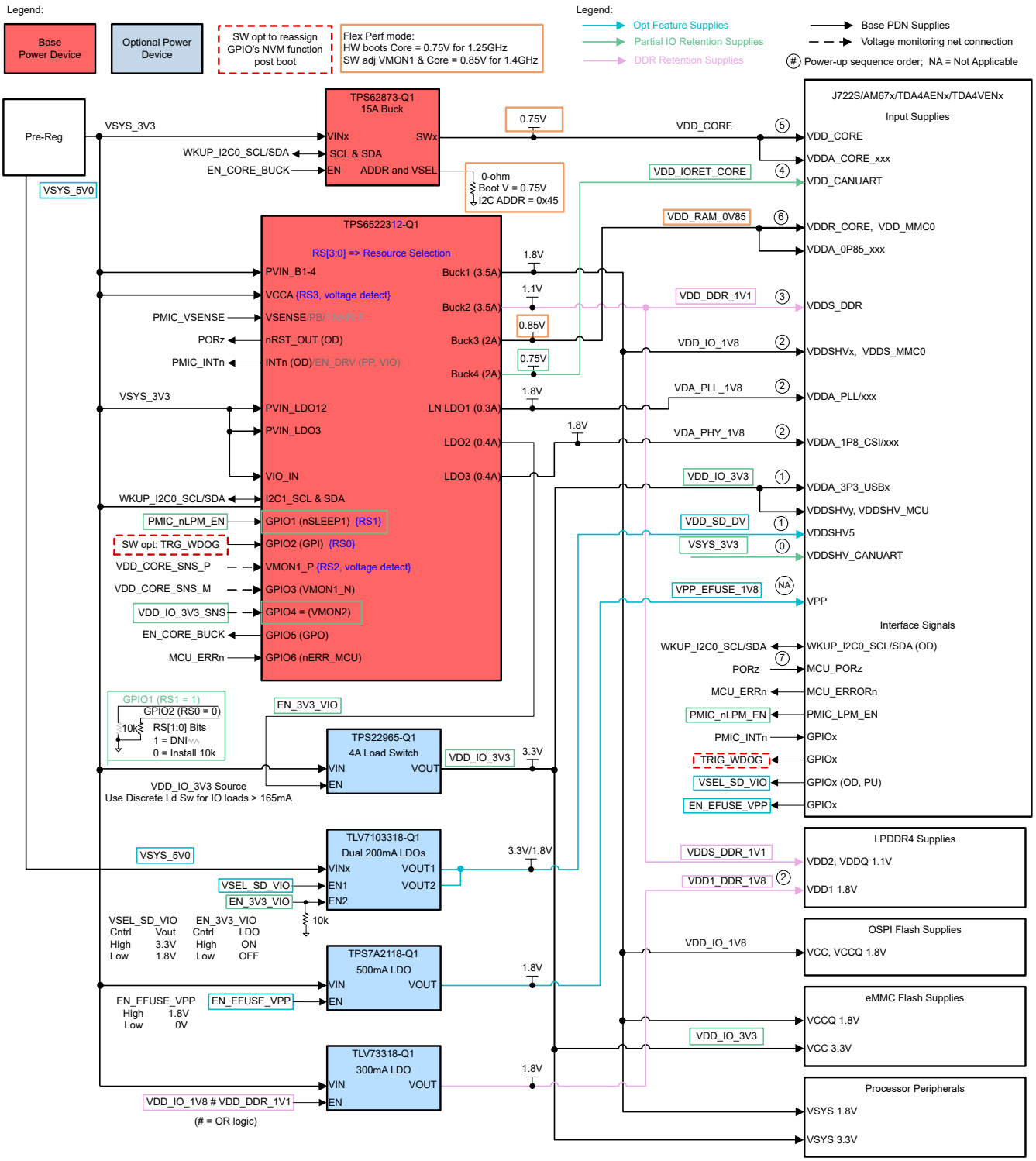

Figure 11. 1.25GHz, 3.3Vin, PDN-5N.DES Variant Adds Partial IO and DDR Retention LPM, Efuse Programming and UHS-I SD Card

J722S PDN-7A5 with 5.0V input

PDN-7A5 uses 5.0V input voltage with only the base power devices with 5.0V input voltage to enable 1.4GHz processing for *J722S/AM67x/TDA4VEN/TDA4AEN* platform that supports in-field Efuse programming optional feature, Table 24.

Table 24. 1.4GHz, 5Vin, PDN-7A5 Features and PMIC Resource Selection Settings

PDN Features	PDN-7A5 (Base only)	Power Resource	PMIC Resource Selection RS[3:0]				
			RS3	RS2	RS1	RS0 when RS1 = 0	RS0 when RS1 = 1
Processing Perf	1.4GHz, 0.85V	TPS62875B2-Q1, 20A Buck	Vin/VCCA auto detect	Core/VMON1 auto detect	GPIO1 LPM status	GPIO2 LDO2 use	GPIO2 Flex Core V
ASIL-B	Yes	TPS6522312X-Q1, PMIC	0 = 3.3V	0 = 0.75V	0 = No	0 = Efuse	0 = Fixed V
3.3V or 5V Input	5.0V		1 = 5V	1 = 0.85V	1 = Yes	1 = SD card	1 = 0.75/0.85V
Platform Support	Yes						
HS SoC Efuse prgm	Yes		1	1	0	0	

Note

"Gray" cell for an RS bit logic level high-lights a PMIC resource difference vs. baseline PDN-7A scheme as shown in diagram.

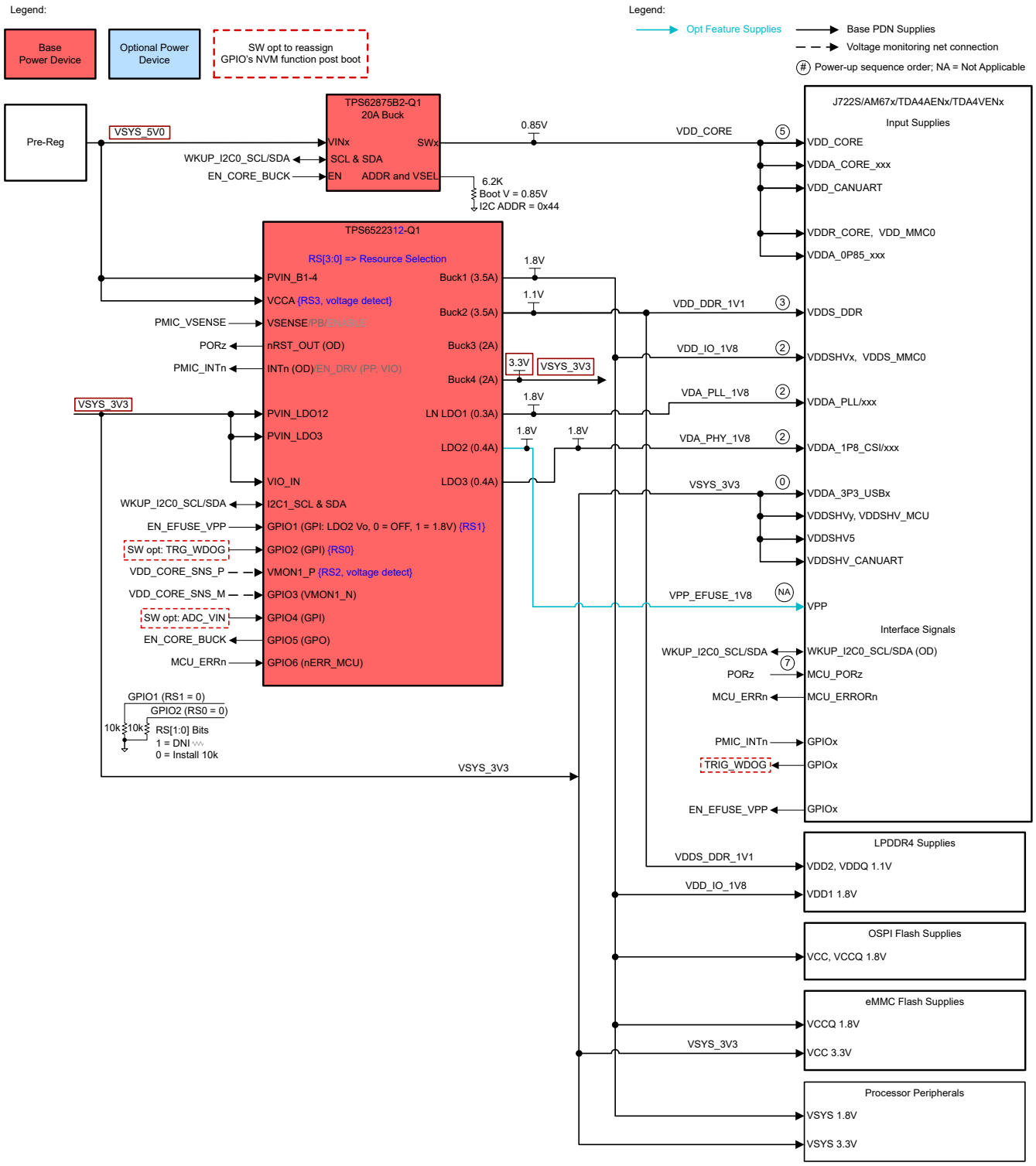

Figure 12. 1.4GHz, 5Vin, PDN-7A5 with Optional eFuse Programming

Conclusion

Multiple recommended power designs that provide peak processing power for the *J722S/AM67x/TDA4VEN/TDA4AEN* platform have been described. A resource configurable *TPS6522x12-Q1* PMIC has been defined as the central power device with a flexible HCPS that scales to meet peak loads across various maximum use cases for low cost, small area PDN schemes. The functional safety compliant *TPS6522x12-Q1* PMIC and *TPS6287x-Q1* fast transient, high current buck converter used within the HCPS form base power devices for automotive *J722S/AM67x/TDA4VEN/TDA4AEN* products. A PDN selection guide enables optimizing *J722S/AM67x/TDA4VEN/TDA4AEN* processor use cases with different peak loads and optional end product features. Example power maps for several PDN variants were provided to clarify different power designs, demonstrate flexibility and help accelerate the design process.

References

Automotive Components

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- Texas Instruments, *TPS65224-Q1 Power Management IC (PMIC) with 4 BUCKs and 3 LDOs for Safety-Relevant Automotive Applications data sheet*
- Texas Instruments, *TPS6287x-Q1, 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Stackable, Synchronous Step-Down Converters with Fast Transient Response data sheet*
- Texas Instruments, *TPS6287x-Q1, 2.7-V to 6-V Input, 15-A, 20-A, 25-A,and 30-A AutomotiveFast Transient Synchronous Step-Down Converter with I2C Interface data sheet*
- Texas Instruments, *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Automotive Load Switch data sheet*
- Texas Instruments, *TLV733P-Q1 Capacitor-Free, 300-mA, Low Dropout (LDO) Linear Regulator data sheet*
- Texas Instruments, *TLV7103318-Q1 Dual, 200mA, Low-I_Q, Low-Dropout Regulator for Portable Devices datasheet*
- Texas Instruments, *TPS7A21-Q1 Automotive, 500mA, Low-Noise, Low-IQ , High-PSRR LDO data sheet*
- Texas Instruments, *TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter data sheet*

Industrial Components

- Texas Instruments, *AM67x Processors data sheet*
- Texas Instruments, *TPS6287x, 2.7 to 6V Input, 6-A, 9-A, 12-A, 15-A, Stackable, Synchronous Step-Down Converters with Fast Transient Response data sheet*
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- Texas Instruments, *TPS7A21 500mA, Low-Noise, Low-IQ, High-PSRR LDO data sheet*
- Texas Instruments, *TPS6124x 3.5-MHz High Efficiency Step-Up Converter Data Sheet*

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