OMAP5912 Multimedia Processor Initialization Reference Guide

Literature Number: SPRU752C
February 2006

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Preface

Read This First

About This Manual

This document describes the reset architecture, the configuration, and the initialization of the OMAP5912 multimedia processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

Trademarks

OMAP and the OMAP symbol are trademarks of Texas Instruments.

This page is intentionally left blank.

Contents

Tables

This page is intentionally left blank.

Initialization

This document describes the reset architecture, the configuration, and the initialization of the OMAP5912 multimedia processor. All references to device package ball number in this document refer to the ZZG package. Please see the data manual (SPRS231) for complete pinout information for both the ZZG and ZDY packages.

1 Reset Architecture

The reset architecture describes the reset signal distribution to the peripherals.

1.1 Reset Modes and Clocking Options

Reset mode 0 has several clocking options while reset mode 1 is much more restrictive. It is important to examine Table 1 when determining which reset mode to use.

Table 1. Clocking Options with respect to Reset Modes

Reset Mode = 0	12 MHz	13 MHz	19.2 MHz
OSC1_IN support via crystal?	Yes	Yes	Yes
OSC1_IN support w/external clock source?	Yes	Yes	Yes
SYS_CLK_IN support w/external clock source?	No	No	No
Reset Mode = 1	**12 MHz**	**13 MHz**	**19.2 MHz**
OSC1_IN support via crystal?	No	No	No
OSC1_IN support w/external clock source?	No	No	No
SYS_CLK_IN support w/external clock source?	No	No	Yes

CAUTION

It is critical to understand that certain systems and functionalities may not be available in both reset modes. The selection between reset modes should be made at an early stage in the development cycle. Generally, reset mode 0 is flexible while reset mode 1 is more restrictive. Reset mode is based on the value of the RESET_MODE pin (sampled on the rising edge of $\overline{\text{PWRON\_RESET}}$).

In addition to affecting the clocking options, reset mode affects many other features such as pin multiplexing at reset time, I/O direction and impedance at reset time, and more. Throughout this document, the reset mode will be specified when it is relevant to the discussion.

1.2 Resets

This processor has up to three external reset pins depending on the reset mode. PWRON_RESET is the cold reset for the entire chip. MPU_RST is the MPU subsystem reset (this pin has special setup requirements in reset mode 1). RTC_ON_NOFF is a software controlled, power-on reset (unavailable in reset mode 1).

Table 2. External Reset

External Reset	Description	Notes
	Reset Mode = 0	
PWRON_RESET	Power-up reset	If RTC is used, must be considered as battery power-up reset. Pulse duration must be two periods of 32 kHz.
	Reset Mode = 0 (Continued)	
RTC_ON_NOFF	Power-up reset	Gated by bit 7 of RTC_CTRL_REG. RTC_ON_NOFF is gated (i.e. disabled) at PWRON_RESET.
MPU_RST	MPU reset	Cold reset of MPU subsystem. Does not reset on chip DPLL.
	Reset Mode = 1	
PWRON_RESET	Power-up reset	Cold reset. Pulse duration must be 2 periods of 32 kHz.
RTC_ON_NOFF	Not used	Gated by reset mode 1.
MPU_RST	MPU reset	Proper pin functionality must be configured (this pin defaults to MPUIO4).

In reset mode 1, the RTC split-power functionality cannot be used, since the RTC_ON_NOFF pin is inactive. The real-time clock functionality of the RTC works correctly in both modes.

In the following sections:

- Table 3 summarizes sources and status bits for global resets.
- Table 4 covers the resets specific to OMAP3.2 (MPU subsystem).
- Table 5 summarizes the peripheral resets for both the MPU and the DSP.

1.2.1 RTC Split Power

RTC split power is available with reset mode 0 only. The RTC power domain is split from the core power domain so that the real-time clock and its associated oscillator can continue to run off of the battery while the MPU subsystem is completely powered off. With RTC split power, $\overline{\text{PWRON\_RESET}}$ acts as a battery power-on reset while RTC_ON_OFF is used to subsequently reset the MPU subsystem without disrupting the time stored in the RTC.

1.2.2 Global Reset

Table 3 summarizes sources and status bits for global resets. The table groups some peripherals into general classes. Peripheral classes group peripherals based on the source of the reset input. For example, a Class-1 module resets directly from the cold, power-on reset while a Class-2 peripheral (module) resets from the MPU subsystem. See Figure 1 and Table 5 for more information on peripheral classes.

Table 3. Global Resets

Reset	Source	Event	Reset Description	Status Bit
Cold reset	External PWRON_RESET	Low on PWRON_RESET	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller DSP MMU MPU TIPB bridge and peripherals Shared peripherals	POR (bit 5) MPU clock reset status register (ARM_SYSST)
				EXT_RST (bit 4) MPU clock reset status register (ARM_SYSST)
			In RESET_MODE 1 sole reset source for Class1 modules: boot ROM, ULPD, OMAP5912 conf, sync counter. Sole reset source for RTC.	GLOB_SWRST (bit1) MPU clock reset status register (ARM_SYSST)
	External RTC_ON_NOFF	Low on RTC_ON_NOFF if RTC split power set to 1 (bit 6 of RTC_CTRL_REG)	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller DSP MMU MPU TIPB bridge and peripherals Shared peripherals	POR (bit5 5) MPU clock reset status register (ARM_SYSST)
				EXT_RST (bit 4) MPU clock reset status register (ARM_SYSST)
			Reset source for Class 1 modules boot ROM,ULPD, OMAP5912 conf, sync counter in RESET_MODE 1. In RESET_MODE 0, does not reset RTC.	GLOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)
Warm reset	External MPU_RST	Low on MPU_RST	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller DSP MMU MPU TIPB bridge and peripherals Shared peripherals	EXT_RST (bit 4) MPU clock reset status register (ARM_SYSST)
			Class 2 and class 3 modules. SDRAM refresh mode switched to self-refresh if previously set to autorefresh state. Not applicable in RESET_MODE 1.	GLOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)

Table 3. Global Resets (Continued)

Reset	Source	Event	Reset Description	Status Bit
	Production eFuse	eFuse programmed value to BAD	Warm reset permanently asserted by ULPD	EXT_RST (bit 4) MPU clock reset status register (ARM_SYSST)
				GLOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)
Warm reset (continued)	32-kHz WD reset	32-kHz WD time-out default configuration leads to 32s time-out with 32-kHz input frequency.	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller SDRAM refresh mode switched to self-refresh if previously set to autorefresh state, DSP MMU, MPU TIPB bridge and peripherals, shared peripherals Class 2 and class 3 modules.	EXT_RST (bit 4) MPU clock reset status register (ARM_SYSST)
				Reset Done (bit 0) in 32K watchdog system status register (WD_SYSSTATUS)
				GOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)
				EXTERNAL_RESET_ SOURCE_3 (bit 3) of ULPD status register

Table 3. Global Resets (Continued)

Reset	Source	Event	Reset Description	Status Bit
Warm reset (continued)	Global system reset (software)	SW_RST (bit 3) in ARM_ RSTCT1 is set to 1 or set ARM_RST (bit 0) in ARM_RSTC1 and clear DSP_EN (bit 1) in ARM_RSTC1	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller DSP MMU MPU TIPB bridge and peripherals Shared peripherals SDRAM refresh mode switched to self-refresh if previously set to autorefresh state. Class 2 and class 3 modules.	GLOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)
	MPU WD reset	MPU WD underflow	Reset LCD controller System DMA MPU port interface L3 OCP initiator L4 controller Traffic controller DSP MMU MPU TIPB bridge and peripherals Shared peripherals SDRAM refresh mode switched to self-refresh if previously set to autorefresh state. Class 2 and class 3 modules.	ARM_WDRST (bit 2) in MPU clock reset status register (ARM_SYSST) GLOB_SWRST (bit 1) MPU clock reset status register (ARM_SYSST)
DSP WD reset	DSP WD timeout	DSP WD Underflow	Reset DSP system and peripheral modules wrapper switches. Reset WD_PER_EN (bit 1) in DSP_RSTCT2.	DSP_WDRST (bit 0) in MPU clock reset status register (ARM_SYSST)
MPU software reset	Software	ARM_RST (bit 0) in ARM_RSTC1 is set to 1	Reset the MPU.	ARM_MCRST (bit 3) in MPU clock reset status register (ARM_SYSST)
MPU peripheral reset	Software	PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.	Reset peripheral class 2 modules and peripheral modules wrapper switches.	

Table 3. Global Resets (Continued)

Reset	Source	Event	Reset Description	Status Bit
DSP core software reset	Software	DSP_EN (bit 1) in ARM_RSTC1 is cleared to 0.	Reset the DSP, excluding the configuration settings (config registers of EMIF internal to DSP and the MPUI control logic internal to DSP).	
DSP peripheral reset	Software	DSP_PEREN (bit 0) in DSP_RSTC2 is cleared to 0.	Reset peripheral Class 3 modules.	
DSP Software Reset	Software	DSP_RST (bit 2) in ARM_RSTC1 is set to 1.	Reset the priority registers (TIPB) module, EMIF configuration register, and the MPUI control logic in the DSP.	

In conjunction with the reset status register in OMAP3.2, the user can poll the ULPD reset status register to determine whether the reset was caused by a 32K watchdog time-out. See Table 3.

1.2.3 OMAP 3.2 Resets

Table 4 shows how OMAP3.2 components are affected by various reset sources. The MPU and DSP peripheral resets are not included in this table as they are not part of OMAP3.2 (see Table 5 for peripheral resets).

Table 4. OMAP 3.2 Resets

Components	Type	Cold Resets	Warm Resets	DSP WD Reset	MPU Software Reset	DSP Core Software Reset	DSP Software Reset
CLKM_1	MPU	Yes	Yes	No	No	No	No
CLKM_2	DSP	Yes	Yes	No	No	No	No
CLKM_3	MPU	Yes	Yes	No	No	No	No
DPLL_1		Yes	See Note	No	No	No	No
ARM926EJS	MPU	Yes	Yes	No	Yes	No	No

† DSP-MMU SW reset bit in CNTL_REG of DSP-MMU module must also be set correctly for DSP-MMU to be reset.
‡ SDRAM is in self-refresh; some of the registers controlled by SDRAM FSM do not reset.
§ See Table 3 for a listing of all cold/warm resets.

Note: DPLL is reset by $\overline{\text{MPU\_RST}}$ or 32-kHz WD. Other warm resets do not reset the DPLL.

Table 4. OMAP 3.2 Resets (Continued)

Components	Type	Cold Resets	Warm Resets	DSP WD Reset	MPU Software Reset	DSP Core Software Reset	DSP Software Reset
ETM	MPU	Yes	Yes	No	No	No	No
MPU timer 1	MPU	Yes	Yes	No	No	No	No
MPU timer 2	MPU	Yes	Yes	No	No	No	No
MPU timer 3	MPU	Yes	Yes	No	No	No	No
MPU WD timer	MPU	Yes	Yes	No	No	No	No
MPU INTH	MPU	Yes	Yes	No	No	No	No
LCD controller	MPU	Yes	Yes	No	No	No	No
DSP	DSP	Yes	Yes	Yes	No	Yes DSP core only, not EMIF config regs and MPUI control logic	Yes Only EMIF config regs and MPUI control logic in DSP, not DSP core
DSP MMU	DSP	Yes †	Yes †	No	No	No	No
DSP timer 1	DSP	Yes	Yes	Yes	No	No	No
DSP timer 2	DSP	Yes	Yes	Yes	No	No	No
DSP timer 3	DSP	Yes	Yes	Yes	No	No	No
DSP WD timer	DSP	Yes	Yes	Yes	No	No	No
DSP INTIF	DSP	Yes	Yes	Yes	No	No	No
DSP INTH	DSP	Yes	Yes	Yes	No	No	No
Mailbox		Yes	Yes	No	No	No	No
MPUI		Yes	Yes	No	No	No	No
System DMA controller	MPU	Yes	Yes	No	No	No	No

† DSP-MMU SW reset bit in CNTL_REG of DSP-MMU module must also be set correctly for DSP-MMU to be reset.
‡ SDRAM is in self-refresh; some of the registers controlled by SDRAM FSM do not reset.
§ See Table 3 for a listing of all cold/warm resets.

Note: DPLL is reset by $\overline{\text{MPU\_RST}}$ or 32-kHz WD. Other warm resets do not reset the DPLL.

Table 4. OMAP 3.2 Resets (Continued)

Components	Type	Cold Resets	Warm Resets	DSP WD Reset	MPU Software Reset	DSP Core Software Reset	DSP Software Reset
TIPB bridge	MPU	Yes	Yes	No	No	No	No
EMIFF	MPU	Yes	Self-Ref ‡	No	No	No	No
EMIFS	MPU	Yes	Yes	No	No	No	No
L3/OCP/T1 (target)	MPU	Yes	Yes	No	No	No	No
L3/OCP/T2 (target)	MPU	Yes	Yes	No	No	No	No
L3/OCP(initiator)	MPU	Yes	Yes	No	No	No	No
WT	MPU	Yes	No	No	No	No	No

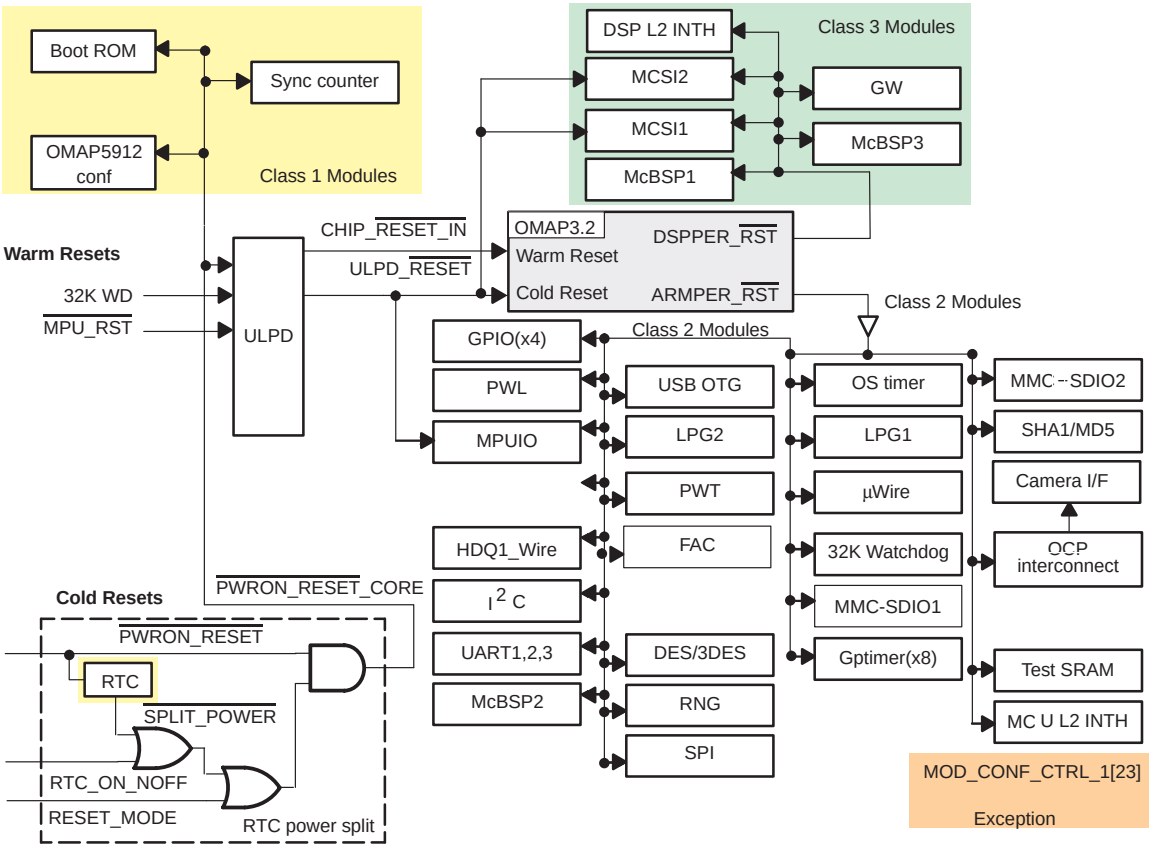
† DSP-MMU SW reset bit in CNTL_REG of DSP-MMU module must also be set correctly for DSP-MMU to be reset.
‡ SDRAM is in self-refresh; some of the registers controlled by SDRAM FSM do not reset.
§ See Table 3 for a listing of all cold/warm resets.

Note: DPLL is reset by $\overline{\text{MPU\_RST}}$ or 32-kHz WD. Other warm resets do not reset the DPLL.

1.2.4 Peripheral Resets

Figure 1 shows how the resets are distributed to the peripherals. See Table 5 for a description of the different peripheral classes.

Figure 1. Reset Distribution to Peripherals



Note that in Figure 1, peripheral classes group peripherals based on the source of the reset input.

The ULPD is in charge of generating two functional reset signals to the MPU subsystem (OMAP3.2 core): cold reset (PIPORN) and warm reset (PICHIPNRST). It is then the task of the MPU subsystem to reset processors and peripherals. In addition, there are three input resets to the ULPD. Two of these resets are external pins: PWRON_RESET (cold reset on ball R12) and MPU_RST (warm reset on ball U20). The 32-kHz watchdog timer reset is a warm reset.

1.2.5 Peripheral Reset Table

Table 5 shows the various reset sources for each peripheral. Many of the OMAP peripherals (external to the MPU subsystem) have module wrappers or switches that facilitate conversion between different bus protocols (wrapper) or control DSP and MPU access to that peripheral (switch).

For example, the UART1 peripheral is on the TIPB, but the internal bus protocol for UART1 is OCP. UART1 has a wrapper that converts between the TIBP and OCP bus protocols. The *wrapper* must be released from reset before access to the UART1 peripheral is possible. This wrapper also acts as a *switch* that determines whether the DSP or MPU has control over the UART1.

For peripherals with wrappers/switches, functionality is gated by the reset for the wrapper/switch. Consequently, the wrapper/switch must be released from reset before the peripheral becomes available. Table 5 details which peripherals have wrappers or switches. In addition, the Multimedia Processor Peripheral Interconnects Reference Guide (SPRU758) discusses the specific types of wrappers and switches for those peripherals. It is also important to understand that there are two types of switches, each with distinct default behaviors when released from reset. SPRU758 details such behaviors.

Table 5. Reset Sources for Peripherals

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 1 Modules				
Real-time clock (RTC)	Cold reset	No	No	No
OMAP5912configuration	Cold reset	No	No	No
Boot ROM	Cold reset	No	No	No
32-kHz synchro counter	Cold reset	No	Dynamic switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3#/ SWRST2/SWRST1

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
|| SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
		Class 2 Modules		
µWire ‖	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
HDQ/1-Wire	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
PWT	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
PWL	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
LPG1	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
LPG2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
OCP interconnect ‖	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
Frame Buffer	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	No	
RNG	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 2 Modules (Continued)				
GPIO1	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Dynamic switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/ SWRST2/SWRST1
GPIO2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Dynamic switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/ SWRST2/SWRST1
GPIO3	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Dynamic switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/ SWRST2/SWRST1
GPIO4	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Dynamic switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/ SWRST2/SWRST1
USB On-the-Go	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP MPU	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1
UART1	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
UART2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 2 Modules (Continued)				
UART3	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
I^2C multi-master/slave	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
SPI master/ slave	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
MMC/SDIO2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 1	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 3	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 2 Modules (Continued)				
General-purpose timer 4	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 5	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 6	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 7 (sleep timer)	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
General-purpose timer 8 (32K DSP)	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
McBSP2	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	Partial	Static switch	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2/SWRST1
MPU level 2 interrupt handler	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 2 Modules (Continued)				
MMC/SDIO1	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1
32-kHz watchdog	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1
SHA-1/MD5	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1
DES/3DES	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1
FAC	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	pvci2rhea	
OS Timer ‖	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1	No	TIPB	
MPUIO‖	Cold reset/Warm reset/ARM_WD/SWRST2/SWRST1/ 32-kHz WD	No	No	

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Table 5. Reset Sources for Peripherals (Continued)

Peripheral Name	HW Reset	SW Reset	Wrapper/ Switch	Wrapper/Switch Reset
Class 3 Modules				
DSP Interrupt handler 2.1	Cold reset/Warm reset/ARM_WD/SWRST3/SWRST2	OCP SWRST	OCP wrapper	Cold reset/Warm reset/ARM_WD/ DSP_WD/SWRST3/SWRST2
McBSP1	Cold reset/Warm reset/ARM_WD/SWRST3/SWRST2	Partial	OCP wrapper	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2
McBSP3	Cold reset/Warm reset/ARM_WD/SWRST3/SWRST2	Partial	OCP wrapper	Cold reset/Warm reset/ARM_WD/DSP_WD/SWRST3/SWRST2
MCSI1	Cold reset/Warm reset/ARM_WD/SWRST3/ SWRST2/ 32-kHz WD/ SEC WD /SEC FSM	Partial	TIPB	
MCSI2	Cold reset/Warm reset/ARM_WD/SWRST3/SWRST2/ 32-kHz WD/SEC WD/ SEC FSM	Partial	TIPB	

† OCP SWRST: Reset software done in corresponding module.
‡ SWRST1: PER_EN (bit 0) in ARM_RSTC2 is cleared to 0.
§ SWRST2: Set ARM_RST (bit 0) in ARM_RSTCT1 and clear DSP_EN (bit 1) in ARM_RSTCT1.
¶ SWRST3: DSP_PEREN (bit 0) in DSP_RSTCT2 is cleared to 0.
# Warm reset: Source can be MPU_RST, global software reset, or 32-kHz watchdog time-out.
‖ SW control via RESET_CONTROL register (see Table 51).
☆ SW control via MOD_CONF_CTRL_1[23].

Note: DSP_WD is controlled by the DSP_RSTCT2.WD_PER_EN.

1.3 Input/Output

Table 6 lists all I/Os that are related to the clock and reset module.

Table 6. Input/Output for Clock and Reset

Pin Name	Dir.	Ball	Description	Default Mode in RESET_MODE 0	Default Mode in RESET_MODE 1	Notes
RESET_ MODE	In	P12	Reset_ mode	Yes	Yes	Sampled at power-up reset.
$\overline{\text{PWRON\_ RESET}}$	IN	R12	Power-up reset	Yes	Yes	Is battery asserted only once when RTC split power backup is used. See the Multimedia Processor Power Management Reference Guide (SPRU753).
RTC_ON_ NOFF	IN	Y12	Power-up reset	Yes	No	Bit 7 of RTC_ CTRL_REG must be set to 1.
$\overline{\text{MPU\_RST}}$	IN	U20	Warm reset	Yes	No	
$\overline{\text{RST\_OUT}}$	OUT	AA20		Yes		
OSC32K_IN	IN	V13	32-kHz oscillator	Yes	Yes	If external 32-kHz clock is used, must be tied high.
OSC32K_OUT	OUT	AA13	32-kHz oscillator	Yes	Yes	If external 32-kHz clock is used, must be tied low.
CLK32K_IN	IN	P13	32-kHz clock In	Yes	Yes	Must be tied low if on-chip 32-kHz oscillator is used.
OSC1_IN	IN	Y2	12-MHz oscillator	Yes	Yes	If external SYS_CLK_IN is used, must be tied low.
OSC1_OUT	OUT	W3	12-MHz oscillator	Yes	Yes	

† See SPRU763

Table 6. Input/Output for Clock and Reset (Continued)

Pin Name	Dir.	Ball	Description	Default Mode in RESET_MODE 0	Default Mode in RESET_MODE 1	Notes
SYS_CLK_IN	IN	Y4	12-MHz to 19.2-MHz clock in	No	Yes	Must be tied low if on-chip oscillator is used. Must select mode 110 for Ball Y4 with software.
EXT_CLK	IN	N18	External clock for GP timers	No	No	
EXT_48M	IN	N21	Backup 48-MHz clock in	No	No	Through GPIO14 input pin. Used if on-chip APLL is disabled.
BCLKREQ	IN	W15	Request for BCLK	Yes	Yes	
MCLKREQ	IN	R10	Request for MCLK	Yes	Yes	
CLK32K_OUT	OUT	R13	32-kHz clock out	Yes	No	
EXT_MASTER_REQ	OUT	R10	Request for external clock	No	No	
RST_HOST_OUT	OUT	W13	Modem shut down if battery fails	No	No	Can be controlled by software (POWER_CTRL_REG[3] if POWER_CTRL_REG[2]=0)
BCLK	OUT	Y15	System clock or derived from APLL clock	Yes	Yes	Can be divided further by setting SDW_CLK_DIV_CTRL_SEL[7:2]
MCLK	OUT	V5	System clock or derived from APLL clock	Yes		When 48MHz, can be divided further by setting COM_RATIO_SEL[7:2]

† See SPRU763

Table 6. Input/Output for Clock and Reset (Continued)

Pin Name	Dir.	Ball	Description	Default Mode in RESET_MODE 0	Default Mode in RESET_MODE 1	Notes
USB.CLK0	OUT	W4	Derived from APLL clock	No	No	96-MHz APLL clock divided by 16
SYS_CLK_ OUT	OUT	B15	System clock output	No		Same frequency as DPLL1 input (ARMPER_CK/ TC2_CK)
CAM.EXCLK	OUT	H19	Derived from ARMPER_CK /TC2_CK†	Yes		Camera clock output
ULPD_ DPLL48M	OUT	J18	Output from APLL	No	No	In test/ observability mode only
LOW_PWR	OUT	T20	Low-voltage mode	No	No	High in deep sleep or can be set high by software (POWER_CTRL_R EG[1] if POWER_CTRL_ REG[0]=1)
$\overline{\text{LOW\_PWR}}$	OUT	W4	Low-voltage mode	No	Yes	Low in deep sleep mode

† See SPRU763

2 Configuration

The configuration module allows software to control the various static modes supported by the device. This module is the primary point of control for the following areas of the device:

- ❏ Functional I/O multiplexing
- ❏ Debug and observation I/O multiplexing
- ❏ I/O gating and inhibiting for power-down modes
- ❏ Pullup and pulldown enable and selection
- ❏ Interface voltage selection
- ❏ Static module configuration
- ❏ Control of clock multiplexing
- ❏ Multiplexing mode status
- ❏ Control of USB integrated transceivers
- ❏ LDO bypassing control
- ❏ Reset control

2.1 Configuration Register Capabilities

The configuration module is a bank of 32-bit registers that can be read and written by software. The module is reset only with a cold reset. This bank of registers can be broken down into the following sections:

Table 7. Configuration Registers

Legacy configuration registers	FUNC_MUX_CTRL(0-2)
I/O multiplex enable register	COMP_MODE_CTRL_0
Generic multiplexing registers	FUNC_MUX_CTRL(3-12)
Pullup/pulldown enable registers	PULL_DWN_CTRL(0-4)
Pullup/pulldown select registers	PU_PD_SEL(0-4)
Gating and inhibiting registers	GATE_INH_CTRL_0
Voltage control registers	VOLTAGE_CTRL_0
Test and debug registers	TEST_DBG_CTRL_0
Configuration module version number	CONF_REV
Module configuration registers	MOD_CONF_CTRL(0-1)
DSP DMA request multiplex registers	FUNC_MUX_DSP_DMA(A-D)

Table 7. Configuration Registers (Continued)

MPU DMA request multiplex registers	FUNC_MUX_ARM_DMA(A-G)
Status register	CONF_STATUS
LDO bypassing control register	LDO_PWRDN_CTRL
USB Transceivers control register	USB_TRANSCEIVER_CTRL
Reset control register	RESET_CONTROL
OMAP5912 control register	CONF_5912_CTRL

2.2 Pin Multiplexing and Pullups/Pulldowns

Each pin that has a multiplexing function is assigned a 3-bit field in the register set FUNC_MUX_CTRL(3-12), thus creating up to eight possible multiplexing options per pin. At reset ($\overline{\text{PWRON\_RESET}}$ is low), the multiplexing of each pin is asynchronously forced by the RESET_MODE pin, regardless of the value written to the FUNC_MUX_CTRL(3-12) registers.

Most of the pins can be configured either as a pullup or a pulldown. The PULL_DWN_CTRL (0–4) registers control whether the pullup or the pulldown is enabled. The pulls (up and down) are disabled by setting a 1 in the corresponding field.

The PU_PD_SEL(0-4) registers configure pin-by-pin whether a pullup or a pulldown is selected. At reset, the pin-for-pin, pullup/pulldown state is forced to be consistent with reset state. The pullups and pulldowns remain in this forced state until 0x0000EAEF is written to the COMP_MODE_CTRL_0 register.

2.2.1 Pin Multiplexing Considerations with Respect to RESET_MODE and GPIO1

The RESET_MODE pin is sampled on the rising edge of $\overline{\text{PWRON\_RESET}}$. When $\overline{\text{PWRON\_RESET}}$ is low, RESET_MODE affects the impedance state or direction of some of the pins because the intended use of these pins differs between reset modes. The RESET_MODE affects the initial mulitplexing state of some pins irrespective of the FUNC_MUX_CTRL registers and it affects the initial state of the EMIFS interface.

Note: Choosing between reset modes

It is critical to understand that by changing the RESET_MODE, certain systems and functionalities may not be available in both modes. The decision to choose between reset mode 0 or 1 should be made at an early stage of the development cycle. Generally, reset mode 0 is flexible while reset mode 1 is more restrictive.

It is important to distinguish between pin functionalities before and after writing 0x0000EAEF to COMP_MODE_CTRL_0:

- Prior to writing 0x0000EAEF, pin multiplexing for all pins depends solely on:
  - RESET_MODE latched by the rising edge of $\overline{\text{PWRON\_RESET}}$.
  - GPIO1 latched by the rising edge of $\overline{\text{PWRON\_RESET}}$ if RESET_MODE = 0.
- After writing 0x0000EAEF, pin multiplexing depends on the FUNC_MUX_CTRL registers for all pins.

CAUTION

Even though all FUNC_MUX_CTRL registers reset to 0x0000, reset mode 1 causes some pins to default to a pin mux mode other than 000. To maintain the same mux mode on such pins, the appropriate FUNC_MUX_CTRL register must be programmed prior to writing 0x0000EAEF to COMP_MODE_CTRL_0.

For example, in reset mode 1, pin Y4 defaults to SYS_CLK_IN (or mux mode 6) rather than UART2.BCLK (mux mode 0). However, FUNC_MUX_CTRL_D(2:0) bits are at their reset value of 000. The FUNC_MUX_CTRL_D(2:0) bits must be set to 110 (mux mode 6) prior to writing 0x0000EAEF to COMP_MODE_CTRL_0 in order for SYS_CLK_IN to maintain its functionality. Otherwise, the system clock is killed when 0x0000EAEF is written to COMP_MODE_CTRL_0 (because the default mux mode 0, UART2.BCLK, takes effect).

In a similar manner, the reset mode determines how the pullup/pulldown configuration is set.

Finally, it is important to note that GPIO1 affects the default pin multiplexing for some of the EMIFS pins if reset mode is 0. The pins are K7, H3, H4, K8, G2, G3, G4, F3, J7, E3, F4, D2, E4, C1, D3 and J8.

2.2.2 Multiplexing Exceptions with USB Host Client

The pin muxing for USB can be overridden by a JTAG sequence. USB host client multiplexing is an exception to the previously described pin multiplexing and pullup-/pulldown-enable generation. For more information contact your TI representative.

2.2.3 Configuration of USB Ports 0, 1, and 2

USB port 0 has an integrated USB transceiver cell able to operate UART or I^2C transactions (3-V mode). It also can be programmed to enable an external pullup.

The default mode is USB mode.

Programming of the UART, I^2C modes, and control of the external pullup are done in the USB_TRANSCEIVER_CTRL register.

The USB ports 1 or 2 can be configured to operate with USB IC transceivers, whose interfaces are either bidirectional or unidirectional. Configuration is done with the USB_TRANSCEIVER_CTRL[8:7] register bits.

See the Multimedia Processor Universal Serial Bus (USB) Reference Guide (SPRU761) for additional information.

2.2.4 Procedure for Setting the Pin Multiplexing

The value of the RESET_MODE pin can be read in the CONF_RESET_MODE_STAT_R bit field of the CONF_STATUS register:

- All mux mode registers (FUNC_MUX_CTRL(3-12)) reset to 000, regardless of RESET_MODE input pin status.
- All pullup/pulldown enable registers (PULL_DWN_CTRL(0-4)) reset to 0, regardless of the RESET_MODE input pin status. However, the actual states of the pulldowns does not depend on the values in the PULL_DWN_CTRL(0−4) registers until programming 0x0000EAEF in the COMP_MODE_CTRL_0 register.
- All pullup/pulldown select registers (PU_PD_SEL(0-4)) reset to 0, regardless of the RESET_MODE input pin status.

See the Application Processor Data Manual (SPRS231) for default states for pin multiplexing and pulls.

Note:

Register values are ignored until 0x0000EAEF is written to the COMP_MODE_CTRL_0 register.

When configuring the pinout of the device:

1) Determine the desired values for each FUNC_MUX_CTRL (3–12), PU_PD_SEL(0-4), and PULL_DWN_CTRL (0–4) configuration register.
2) Program the desired values by writing to the appropriate register.

3) Program the COMP_MODE_CTRL_0 register to 0x0000EAEF.

This procedure allows the user to make all of the multiplex configuration settings and enable all of the modes at once. The bit values as they correspond to pin multiplexing modes are shown in Table 8.

The desired pin multiplexing and the pullup/pulldown modes are then activated. Once 0x0000EAEF is written to COMP_MODE_CTRL_0, it must not be changed because the device will revert to the original multiplexing and pullup/down states.

Table 8. Functional Multiplexing Modes

FUNC_MUX_CTRL 3-Bit Value	Corresponding Multiplexing Mode for Pin Configuration
000	Default configuration/functional multiplexing 0
001	Functional pin multiplexing mode 1
010	Functional pin multiplexing mode 2
011	Functional pin multiplexing mode 3
100	Functional pin multiplexing mode 4
101	Functional pin multiplexing mode 5
110	Functional pin multiplexing mode 6
111	Functional pin multiplexing mode 7

For a given interface, the values of the FUNC_MUX_CTRL bits may vary from pin to pin. For example, the USB1_HOST port is split between functional multiplexing 1 and functional multiplexing 2 columns. In this case, four of the pins have a mode value of 001, and the other four have a mode value of 010.

Note:

The programming of a pin in a mux mode that is not defined in the pinout section of the Application Processor Data Manual (SPRS231) leads to undefined operation of the pin, and thus must be strictly avoided.

2.3 Parallel Observability During Functional Mode

For debug purposes, various internal signals can be brought to the boundary during functional mode. The software procedure for enabling observability of internal signals is as follows:

- Set FUNC_MUX_CTRL_2.CONF_OBS_MUX_SEL_R, depending on the signal that must be observed (see Table 9).
- Set FUNC_MUX_CTRL_0.OBS_288_1 bit to 1.

There is no need to write 0xEAEF to COMP_MODE_CTRL_0 to set observability mode. Table 9 gives the observable signals, and their locations on the boundary, depending on CONF_OBS_MUX_SEL_R.

Table 9. Parallel Observability Multiplexing Signals

	CONF_OBS_MUX_SEL_R Value			
Ball	**0**	**1**	**2**	**3**
J18	Reserved	ARMXOR_CK	LDO_SLEEP	ULPD_DPLL48M
J19	Reserved	DSPXOR_CK	LDO_STEADY	ULPD_ USBW2FCCLK12M
Ball	**0**	**1**	**2**	**3**
J14	USB RXD	ARMPER_CK	LDO_PWRDN	OMAP3.2 functional clock
K18	USB RXDP	DSPPER_CK	UART3 functional clock	Reserved
K19	USB RXDM	Reserved	UART2 functional clock	Reserved
K15	Reserved	Reserved	UART1 functional clock	Reserved
Ball	**0**	**1**	**2**	**3**
K14	Reserved	Reserved	MMC2 functional clock	Reserved
L19	Reserved	Reserved	MMC1 functional clock	Reserved
	4	**5**	**6**	**7**
J18	MCLK	DPLL2 clock	LDO sleep	APLL PWRDN

Table 9. Parallel Observability Multiplexing Signals (Continued)

	CONF_OBS_MUX_SEL_R Value			
J19	BCLK	Reserved	MPU DMA REQ observable	APLL SYNC
J14	BCLK	Reserved	DSP DMA REQ observable	OMAP3.2 MPU warmreset
K18	USB OTG functional clock	Reserved	MPU interrupt observable	CLK12M STABLE
K19	USB host functional clock	DPLL1 clock	DSP interrupt observable	APLL output clock
K15	Camera functional clock	Lv2 INTH functional clock	BIST FAIL	WKUP_NREQ
K14	CAM.OUTCLK	OMAP3.2 Idle	BIST DONE	APLL LOCK
L19	SYS_CLK_OUT	OMAP3.2 DPLL enable	BIST GO	CHIP_NWAKEUP
	8	**9**	**10**	
J18	DLL_PMT_DCB[7]	ULPD clock switch status	RNG functional clock	
J19	DLL_PMT_DCB[6]	UART2 functional clock (from system clock)	Reserved	
	8	**9**	**10**	
J14	DLL_PMT_DCB[5]	Internal 32k clock (distributed to peripherals)	Reserved	
K18	DLL_PMT_DCB[4]	Internal system clock	Reserved	
K19	DLL_PMT_DCB[3]	Internal 32k clock (feeding ULPD)	Reserved	
K15	DLL_PMT_DCB[2]	32k oscillator PWRDN	Reserved	
K14	DLL_PMT_DCB[1]	12-MHz oscillator GZ	Reserved	
L19	DLL_PMT_DCB[0]	12-MHz oscillator PWRDN	Reserved	

2.4 OMAP5912/5910 Software and Hardware Compatibility

The device resets based on the RESET_MODE pin are forced either to the functional multiplexing mode 000, with the appropriate pullups or pulldowns configured and enabled to preserve the OMAP5910 pinout reset condition, or to the new reset mode 1. The multiplexing per pin remains software compatible with OMAP5910 and is controlled by the same 3-bit field (eight mux modes possible).

Pullup and pulldown control has changed from OMAP5910 to OMAP5912. As applicable, the OMAP5910 device has either a pullup or a pulldown per pin, and a 1-bit register per pin enables or disables the pullup or pulldown. The OMAP5912 device, however, has both a pullup and a pulldown available on each pin. Thus, a new OMAP5912 register set is implemented (PU_PD_SEL (0-4)) to allow the software to select between the use of a pullup or a pulldown on each pin. The reset condition of PU_PD_SEL(0-4) is determined, to keep compatibility with the OMAP5910 reset condition. The OMAP5910 pullup/pulldown enable register set remains (PULL_DWN_CTRL (0-3). The reset state, however, is changed to match what the pinout requires at reset.

In the OMAP5910, programming of the following registers does not take effect until the COMP_MODE_CTRL_0 register is written with 0x0000EAEF. For OMAP5912, however, these registers do not have this restriction, and programming the register takes effect immediately, regardless of the state of the COMP_MODE_CTRL_0 register.

- GATE_INH_CTRL_0
- VOLTAGE_CTRL_0
- TEST_DBG_CTRL_0
- MOD_CONF_CTRL_0

For OMAP5912, all I/O power supplies have a low- and a high-voltage mode VS. In OMAP5910, only the EMIFS, EMIFF, and communication processor interface have dual voltage interfaces. For OMAP5912 at reset, the voltage mode has changed to default to low-voltage mode, whereas in OMAP5910 it is high-voltage mode.

The OMAP5912 software/hardware compatibility summary for I/O multiplexing and configuration is as follows:

- The device resets to functional multiplexing mode 000 with appropriate pullups or pulldowns configured and enabled to preserve the OMAP5910 pinout reset condition if RESET_MODE pin is set to 0.

- Multiplexing-per-pin stays the same as in the OMAP5910 mode. More pins are multiplexed in OMAP5912, so that there are additional FUNC_MUX_CTRL registers.
- The PULL_DWN_CTRL register set remains unchanged. It is responsible for pullup or pulldown enable, as determined by the state of the newly created PU_PD_SEL register set. Because there are additional pins requiring pullup/pulldown capability, extra PULL_DWN_CTRL registers have been added. Because not all pins need a pullup or pulldown function, see the OMAP5912 Application Processor Data Manual (SPRS231) to determine whether a pullup/pulldown is implemented.

Table 10 lists the configuration registers. Table 11 through Table 52 describe the register bits.

2.5 Configuration Registers

Table 10. Configuration Registers

Base Address = 0xFFFE 1000			
Name	**Description**	**R/W**	**Offset**
FUNC_MUX_CTRL_0	Functional multiplexing control 0	R/W	0x00
FUNC_MUX_CTRL_1	Functional multiplexing control 1	R/W	0x04
FUNC_MUX_CTRL_2	Functional multiplexing control 2	R/W	0x08
COMP_MODE_CTRL_0	Compatibility mode control 0	R/W	0x0C
FUNC_MUX_CTRL_3	Functional multiplexing control 3	R/W	0x10
FUNC_MUX_CTRL_4	Functional multiplexing control 4	R/W	0x14
FUNC_MUX_CTRL_5	Functional multiplexing control 5	R/W	0x18
FUNC_MUX_CTRL_6	Functional multiplexing control 6	R/W	0x1C
FUNC_MUX_CTRL_7	Functional multiplexing control 7	R/W	0x20
FUNC_MUX_CTRL_8	Functional multiplexing control 8	R/W	0x24
FUNC_MUX_CTRL_9	Functional multiplexing control 9	R/W	0x28
FUNC_MUX_CTRL_A	Functional multiplexing control	R/W	0x2C
FUNC_MUX_CTRL_B	Functional multiplexing control	R/W	0x30
FUNC_MUX_CTRL_C	Functional multiplexing control	R/W	0x34
FUNC_MUX_CTRL_D	Functional multiplexing control	R/W	0x38

Table 10. Configuration Registers (Continued)

Base Address = 0xFFFE 1000			
Name	**Description**	**R/W**	**Offset**
PULL_DWN_CTRL_0	Pulldown control 0	R/W	0x40
PULL_DWN_CTRL_1	Pulldown control 1	R/W	0x44
PULL_DWN_CTRL_2	Pulldown control 2	R/W	0x48
PULL_DWN_CTRL_3	Pulldown control 3	R/W	0x4C
GATE_INH_CTRL_0	Gate and inhibit control 0	R/W	0x50
CONF_REV	Configuration revision	R	0x58
VOLTAGE_CTRL_0	Voltage control	R/W	0x60
USB_TRANSCEIVER_CTRL	USB transceiver control	R/W	0x64
LDO_PWRDN_CBTRK	LDO powerdown control	R/W	0x68
TEST_DBG_CTRL_0	Test debug control 0	R/W	0x70
MOD_CONF_CTRL_0	Module configuration control 0	R/W	0x80
FUNC_MUX_CTRL_E	Functional multiplexing control	R/W	0x90
FUNC_MUX_CTRL_F	Functional multiplexing control	R/W	0x94
FUNC_MUX_CTRL_10	Functional multiplexing control	R/W	0x98
FUNC_MUX_CTRL11	Functional multiplexing control	R/W	0x9C
FUNC_MUX_CTRL_12	Functional multiplexing control	R/W	0xA0
PULL_DWN_CTRL_4	Pulldown control 4	R/W	0xAC
PU_PD_SEL_0	Pullup/pulldown selection 0	R/W	0xB4
PU_PD_SEL_1	Pullup/pulldown selection 1	R/W	0xB8
PU_PD_SEL_2	Pullup/pulldown selection 2	R/W	0xBC
PU_PD_SEL_3	Pullup/pulldown selection 3	R/W	0xC0
PU_PD_SEL_4	Pullup/pulldown selection 4	R/W	0xC4
FUNC_MUX_DSP_DMA_A	Functional multiplexing DSP DMA A	R/W	0xD0*
FUNC_MUX_DSP_DMA_B	Functional multiplexing DSP DMA B	R/W	0xD4*
FUNC_MUX_DSP_DMA_C	Functional multiplexing DSP DMA C	R/W	0xD8*

Table 10. Configuration Registers (Continued)

Base Address = 0xFFFE 1000			
Name	**Description**	**R/W**	**Offset**
FUNC_MUX_DSP_DMA_D	Functional multiplexing DSP DMA D	R/W	0xDC*
FUNC_MUX_ARM_DMA_A	Functional multiplexing MPU DMA A	R/W	0xEC*
FUNC_MUX_ARM_DMA_B	Functional multiplexing MPU DMA B	R/W	0xF0*
FUNC_MUX_ARM_DMA_C	Functional multiplexing MPU DMA C	R/W	0xF4*
FUNC_MUX_ARM_DMA_D	Functional multiplexing MPU DMA D	R/W	0xF8*
FUNC_MUX_ARM_DMA_E	Functional multiplexing MPU DMA E	R/W	0xFC*
FUNC_MUX_ARM_DMA_F	Functional multiplexing MPU DMA F	R/W	0x100*
FUNC_MUX_ARM_DMA_G	Functional multiplexing MPU DMA G	R/W	0x104*
MOD_CONF_CTRL_1	Module configuration control 1	R/W	0x110
CONF_STATUS	Configuration status		0x130
RESET_CONTROL	Reset control register	R/W	0x140
CONF_5912_CTRL	OMAP5912 configuration control	R/W	0x150

Note: Register descriptions for DMA functional mux registers are in the Multimedia Processor Direct Memory Access (DMA) Support Reference Guide (SPRU755).

Table 11. Functional Multiplexing Control O Register (FUNC_MUX_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CTRL_288_1	This bit configures the control mode 288_1, which enables the control of the OMAP CHIP_NWAKEUP signal from the RTCK pad. 0: Functional mode. ULPD controls the OMAP CHIP_NWAKEUP signal. 1: Debug. The RTCK pad controls the OMAP CHIP_NWAKEUP signal.	R/W	0x0
30	OBS_288_2	See Note 1	R/W	0x0
29	OBS_600_1	See Note 1	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 11. Functional Multiplexing Control O Register (FUNC_MUX_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
28	OBS_288_1	Configures observation mode multiplexing on the camera interface (See Section 2.3). 0: Observation mode is disabled and camera interface is in functional mode. 1: Enables the observation mode. Programming sequence: 1) Configure CONF_OBS_MUX_CTRL_R (see Section 2.3 for details). 2) Enable the observability multiplexing by programming OBS_288_1 to 1.	R/W	0x0
27	UWIRE_HIZ_DISABLE	See Note 1	R/W	0x0
26	GIGA_UART_GATING	See Note 1	R/W	0x0
25	BT_UART_GATING	See Note 1	R/W	0x0
24	COM_UART_GATING	See Note 1	R/W	0x0
23	USB_TRANS_MUX	See Note 1	R/W	0x0
22	LB_RESET_DISABLE	See Note 1	R/W	0x0
21	HSAB_RESET_DISABLE	See Note 1	R/W	0x0
20	LRU_SEL	This field configures the OMAP traffic controller arbitration algorithm. 0: LRU priority scheme is used for arbitration. 1: Fixed priority scheme is used for arbitration. This bit can be changed only when the DSP is in reset.	R/W	0x0
19	VBUS_CTRL	See Note 1	R/W	0x0
18	VBUS_MODE	See Note 1	R/W	0x0
17:16	UWIRE_DCD	See Note 1	R/W	0x0
15	OS_TYPE	Reserved	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 11. Functional Multiplexing Control O Register (FUNC_MUX_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
14	NRESET_ENABLE	Allows AND gating of outputs with the OMAP CHIP_NRESET_OUT 0: Disabled 1: Enabled	R/W	0x0
13	PWR_MASK_IN	This register enables the Inhibit2 function. Depending on the status of GPIO(9) and ARMIO(3), subject inputs are gated to low internally when this function is enabled. 1: Enable the gating of inputs by the combination of COM_PWR_REQ (GPIO(9)) and COM_STS (MPUIO(3)) input pins. 0: Disable the gating of inputs by the combination of COM_PWR_REQ (GPIO(9)) and COM_STS (MPUIO(3)) input pins. This is the control for the function called Inhibit2 in SPRS231.	R/W	0x0
12	PWR_MASK_OUT	This register enables the Gated2 function. Depending on the status of GPIO(9) and ARMIO(3), the subject outputs are gated to low when this function is enabled. 1: Enable AND gating of outputs with COM_PWR_REQ (GPIO(9)) and COM_STS (MPUIO(3)) input pins. 0: Disables AND gating of outputs with COM_PWR_REQ (GPIO(9)) and COM_STS (MPUIO(3)) input pins. This function is called Gated2 in the SPRS231 document.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 11. Functional Multiplexing Control O Register (FUNC_MUX_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x00				
Bit	**Name**	**Function**	**R/W**	**Reset**
11	BVLZ_MASK_IN	This register enables the Inhibit1 function. Depending on the status of BVLZ input pin, subject inputs are gated to low internally when this function is enabled. 1: Enables AND gating of inputs with BVLZ input pin. 0: Disables AND gating of inputs with BVLZ input pin. This function is called Inhibit1 in SPRS231.	R/W	0x0
10	BVLZ_MASK_OUT	This register enables the Gated1 function. Depending on the status of BVLZ, subject outputs are gated to low when this function is enabled. 1: Enables AND gating of outputs with BVLZ input pin. 0: Disables AND gating of outputs with BVLZ input pin. This function is called Gated1 in SPRS231.	R/W	0x0
9	BLUETOOTH	See Note 1	R/W	0x0
8	CAMERA	See Note 1	R/W	0x0
7	USB.CLK0	See Note 1	R/W	0x0
6	COM_SHUT	See Note 1	R/W	0x0
5	GIGA_UART	See Note 1	R/W	0x0
4	MEDIA_HIZ_DISABLE	See Note 1	R/W	0x0
3	LCD	See Note 1	R/W	0x0
2	NFCS2	See Note 1	R/W	0x0
1:0	LB_HSAB_RHEA	See Note 1	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

This register primarily controls legacy functional multiplexing. Many mux modes have been removed and made more generic. When a function has been removed, it is noted in the register description.

Table 12. Functional Multiplexing Control 1 Register (FUNC_MUX_CTRL_1)

Base Address = 0xFFFE 1000, Offset Address = 0x04				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:0	RESERVED	Reserved †	R/W	0x0000

† The register functions have been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 13. Functional Multiplexing Control 2 Register (FUNC_MUX_CTRL_2)

Base Address = 0xFFFE 1000, Offset Address = 0x08				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:28	RESERVED	Reserved	R/W	0x0
27:24	CONF_OBS_MUX_SEL_R	Sets the parallel observation multiplexing mode. These bits determine which of the 10 observation multiplexing modes is selected (See Section 2.3 for details).	R/W	0x0
23:19	CONF_DSP_DMA_REQ_19	Maps DSP DMA_REQUEST for observability. The pin configuration for each observation mode is specified (See Section 2.3). Observability of the DSP DMA request(i) is done before the crossbar.	R/W	0x00
18:13	CONF_ARM_DMA_SEL_REQ31	Maps MPU DMA_REQUEST for observability. The pin configuration for each observation mode is specified (See Section 2.3). Observability of the MPU DMA request(i) is done before the crossbar.	R/W	0x00

Table 13. Functional Multiplexing Control 2 Register (FUNC_MUX_CTRL_2)

Base Address = 0xFFFE 1000, Offset Address = 0x08				
Bit	**Name**	**Function**	**R/W**	**Reset**
12:7	CONF_DSP_INT_SEL_R	Select the DSP level 2 interrupts to be observed. The pin configuration for each observation mode is specified (See Section 2.3). Observing interrupts is done after multiplexers that select between level and edge activity.	R/W	0x00
6:0	CONF_ARM_INT_SEL_R	Select the MPU level 2 interrupts to be observed. The pin configuration for each observation mode is specified (See Section 2.3). Observing interrupts is done after multiplexers that select between level and edge activity.	R/W	0x00

Table 14. Compatibility Mode Control 0 Register (COMP_MODE_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x0C				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:16	CONF_COMP_ RESERVED_R	Reserved for future expansion. These bits must be written to 0x0000h	R/W	0x0000
15:0	CONF_MUX_EN_R	A value of 0xEAEF must be written to this register to enable the pin multiplexing controlled by the registers FUNC_MUX_CTRL (3-12), PU_PD_SEL(0-4), and PULL_DWN_CTRL (0-4). The boot code must configure all the pin multiplexing registers FUNC_MUX_CTRL (3-12), PU_PD_SEL(0-4), and PULL_DWN_CTRL (0-4) first. Writing 0xEAEF enables all the pin multiplexing to take effect simultaneously.	R/W	0x0000

This is the I/O multiplex enable register. At reset, any value written to the registers FUNC_MUX_CTRL (3-12), PU_PD_SEL(0-4), and PULL_DWN_CTRL (0-4) does not change the configuration of the pins. However, setting the COMP_MODE_CTRL_0 register to 0x0000EAEF activates:

- Generic multiplexing registers: FUNC_MUX_CTRL_x, $x \in \{3..12\}$
- Pullup/pulldown enable registers: PULL_DWN_CTRL_y, $y \in \{0..4\}$
- Pullup/pulldown select registers: PU_PD_SEL_z, $z \in \{0..4\}$

Table 15. Functional Multiplexing Control 3 Register (FUNC_MUX_CTRL_3)

Base Address = 0xFFFE 1000, Offset Address = 0x10				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_F19	Controls the multiplexing on F19. Formerly, CONF_KBR_1_R.	R/W	000
26:24	CONF_H14	Controls the multiplexing on H14. Formerly, CONF_KBR_2_R.	R/W	000
23:21	CONF_E20	Controls the multiplexing on E20. Formerly, CONF_KBR_3_R.	R/W	000
20:18	CONF_E19	Controls the multiplexing on E19. Formerly, CONF_KBR_4_R.	R/W	000
17:15	CONF_F18	Controls the multiplexing on F18. Formerly, CONF_KBC_0_R.	R/W	000
14:12	CONF_D20	Controls the multiplexing on D20. Formerly, CONF_KBC_1_R.	R/W	000
11:9	CONF_D19	Controls the multiplexing on D19. Formerly, CONF_KBC_2_R.	R/W	000
8:6	CONF_E18	Controls the multiplexing on E18. Formerly, CONF_KBC_3_R.	R/W	000
5:3	CONF_C21	Controls the multiplexing on C21. Formerly, CONF_KBC_4_R.	R/W	000
2:0	CONF_G19	Controls the multiplexing on G19. Formerly, CONF_KBC_5_R.	R/W	000

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit−field values.

Table 16. Functional Multiplexing Control 4 Register (FUNC_MUX_CTRL_4)

Base Address = 0xFFFE 1000, Offset Address = 0x14				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_J18	Controls multiplexing on J18. Formerly CON_CAM_D_7_R.	R/W	000
26:24	CONF_J15	Controls multiplexing on J15. Formerly CONF_CAM_LCLK_R.	R/W	000
23:21	CONF_H19	Controls multiplexing on H19. Formerly CONF_CAMEXCLK_R.	R/W	000
20:18	CONF_H20	Controls multiplexing on H20. Formerly CONF_MCBSP1_DIN_R.	R/W	000
17:15	CONF_H18	Controls multiplexing on H18. Formerly CONF_MCBSP1_DOUT_R.	R/W	000
14:12	CONF_H15	Controls multiplexing on H15. Formerly CONF_MCBSP1_SYNC_R.	R/W	000

Table 16. Functional Multiplexing Control 4 Register (FUNC_MUX_CTRL_4) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x14				
Bit	**Name**	**Function**	**R/W**	**Reset**
11:9	CONF_G21	Controls multiplexing on G21. Formerly CONF_MCBSP1_BCLK_R.	R/W	000
8:6	CONF_G20	Controls multiplexing on G20. Formerly CONF_MCBSP1_CLKS_R.	R/W	000
5:3	RESERVED	Reserved for future expansion	R/W	000
2:0	CONF_G18	Controls multiplexing on G18. Formerly CONF_KBR_0_R.	R/W	000

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 17. Functional Multiplexing Control 5 Register (FUNC_MUX_CTRL_5)

Base Address = 0xFFFE 1000, Offset Address = 0x18				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_M19	Controls multiplexing on M19. Formerly, CONF_CAM_RSTZ_R.	R/W	0x0
26:24	CONF_L15	Controls multiplexing on L15. Formerly, CONF_CAM_HS_R.	R/W	0x0
23:21	CONF_L18	Controls multiplexing on L18. Formerly, CONF_CAM_VS_R.	R/W	0x0
20:18	CONF_L19	Controls multiplexing on L19. Formerly, CONF_CAM_D_0_R.	R/W	0x0
17:15	CONF_K14	Controls multiplexing on K14. Formerly, CONF_CAM_D_1_R.	R/W	0x0
14:12	CONF_K15	Controls multiplexing on K15. Formerly, CONF_CAM_D_2_R.	R/W	0x0
11:9	CONF_K19	Controls multiplexing on K19. Formerly, CONF_CAM_D_3_R.	R/W	0x0
8:6	CONF_K18	Controls multiplexing on K18. Formerly, CONF_CAM_D_4_R.	R/W	0x0
5:3	CONF_J14	Controls multiplexing on J14. Formerly, CONF_CAM_D_5_R.	R/W	0x0
2:0	CONF_J19	Controls multiplexing on J19. Formerly, CONF_CAM_D_6_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 18. Functional Multiplexing Control 6 Register (FUNC_MUX_CTRL_6)

Base Address = 0xFFFE 1000, Offset Address = 0x1C				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_P20	Controls multiplexing on P20. Formerly, CONF_GPIO_4_R.	R/W	0x0
26:24	CONF_P19	Controls multiplexing on P19. Formerly, CONF_GPIO_6_R.	R/W	0x0
23:21	CONF_M15	Controls multiplexing on M15. Formerly, CONF_GPIO_7_R.	R/W	0x0
20:18	CONF_N20	Controls multiplexing on N20. Formerly, CONF_GPIO_11_R.	R/W	0x0
17:15	CONF_N18	Controls multiplexing on N18. Formerly, CONF_GPIO_11_R.	R/W	0x0
14:12	CONF_N19	Controls multiplexing on N19. Formerly, CONF_GPIO_11_R.	R/W	0x0
11:9	CONF_N21	Controls multiplexing on N21. Formerly, CONF_GPIO_11_R.	R/W	0x0
8:6	CONF_M20	Controls multiplexing on M20. Formerly, CONF_GPIO_11_R.	R/W	0x0
5:3	CONF_L14	Controls multiplexing on L14. Formerly, CONF_RX3_R.	R/W	0x0
2:0	CONF_M18	Controls multiplexing on M18. Formerly, CONF_TX3_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 19. Functional Multiplexing Control 7 Register (FUNC_MUX_CTRL_7)

Base Address = 0xFFFE 1000, Offset Address = 0x20				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_V20	Controls multiplexing on V20. Formerly, CONF_SDA_R.	R/W	0x0
26:24	CONF_T18	Controls multiplexing on T18. Formerly, CONF_SCL_R.	R/W	0x0
23:21	CONF_U19	Controls multiplexing on U19. Formerly, CONF_ARMIO_1_R.	R/W	0x0
20:18	CONF_N15	Controls multiplexing on N15. Formerly, CONF_ARMIO_2_R.	R/W	0x0
17:15	CONF_T19	Controls multiplexing on T19. Formerly, CONF_ARMIO_4_R.	R/W	0x0
14:12	CONF_T20	Controls multiplexing on T20. Formerly, CONF_ARMIO_5_R.	R/W	0x0

Table 19. Functional Multiplexing Control 7 Register (FUNC_MUX_CTRL_7) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x20				
Bit	**Name**	**Function**	**R/W**	**Reset**
11:9	CONF_R18	Controls multiplexing on R18. Formerly, CONF_GPIO_0_R.	R/W	0x0
8:6	CONF_R19	Controls multiplexing on R19. Formerly, CONF_GPIO_1_R.	R/W	0x0
5:3	CONF_M14	Controls multiplexing on M14. Formerly, CONF_GPIO_2_R.	R/W	0x0
2:0	CONF_P18	Controls multiplexing on P18. Formerly, CONF_GPIO_3_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 20. Functional Multiplexing Control 8 Register (FUNC_MUX_CTRL_8)

Base Address = 0xFFFE 1000, Offset Address = 0x24				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_J20	Controls multiplexing on J20. Formerly, CONF_ARM_BOOT_R.	R/W	0x0
26:24	CONF_W17	Controls multiplexing on W17. Formerly, CONF_NEMU1_R.	R/W	0x0
23:21	CONF_V16	Controls multiplexing on V16. Formerly, CONF_NEMU0_R.	R/W	0x0
20:18	CONF_Y12	Controls multiplexing on Y12. Formerly, CONF_ON_OFF_R.	R/W	0x0
17:15	CONF_W19	Controls multiplexing on W19. Formerly, CONF_BVLZ_R.	R/W	0x0
14:12	CONF_P15	Controls multiplexing on P15. Formerly, CONF_WIRE_NSCS3_R.	R/W	0x0
11:9	CONF_N14	Controls multiplexing on N14. Formerly, CONF_WIRE_NSCS0_R.	R/W	0x0
8:6	CONF_V19	Controls multiplexing on V19. Formerly, CONF_WIRE_SCLK_R.	R/W	0x0
5:3	CONF_W21	Controls multiplexing on W21. Formerly, CONF_WIRE_SDO_R.	R/W	0x0
2:0	CONF_U18	Controls multiplexing on U18. Formerly, CONF_WIRE_SDI_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 21. Functional Multiplexing Control 9 Register (FUNC_MUX_CTRL_9)

Base Address = 0xFFFE 1000, Offset Address = 0x28				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_W15	Controls multiplexing on W15. Formerly CONF_UARTS_CLKREQ_R.	R/W	0x0
26:24	CONF_W14	Controls multiplexing on W14. Formerly CONF_MCSI1_DOUT_R.	R/W	0x0
23:21	CONF_Y14	Controls multiplexing on Y14. Formerly CONF_TX1_R.	R/W	0x0
20:18	CONF_V14	Controls multiplexing on V14. Formerly CONF_RX1_R.	R/W	0x0
17:15	CONF_R14	Controls multiplexing on R14. Formerly CONF_CTS1_R.	R/W	0x0
14:12	CONF_AA15	Controls multiplexing on AA15. Formerly CONF_RTS1_R.	R/W	0x0
11:9	CONF_AA20	Controls multiplexing on AA20. Formerly CONF_NRESET_OUT_R.	R/W	0x0
8:6	CONF_U20	Controls multiplexing on U20. Formerly CONF_MPU_NRESET_R.	R/W	0x0
5:3	CONF_W16	Controls multiplexing on W16. Formerly CONF_MCBSP3_CLK_R.	R/W	0x0
2:0	CONF_W13	Controls multiplexing on W13. Formerly CONF_WAKEUP_INT_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 22. Functional Multiplexing Control A Register (FUNC_MUX_CTRL_A)

Base Address = 0xFFFE 1000, Offset Address = 0x2C				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_P11	Controls multiplexing on P11. Formerly CONF_MMC_CMD_R.	R/W	0x0
26:24	CONF_V10	Controls multiplexing on V10. Formerly CONF_MMC_DAT1_R.	R/W	0x0
23:21	CONF_V11	Controls multiplexing on V11. Formerly CONF_MMC_CLK_R.	R/W	0x0

Table 22. Functional Multiplexing Control A Register (FUNC_MUX_CTRL_A) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x2C				
Bit	**Name**	**Function**	**R/W**	**Reset**
20:18	CONF_W10	Controls multiplexing on W10. Formerly CONF_MMC_DAT2_R.	R/W	0x0
17:15	CONF_P13	Controls multiplexing on P13. Formerly CONF_CLK32K_IN_R.	R/W	0x0
14:12	CONF_R13	Controls multiplexing on R13. Formerly CONF_CLK32K_OUT_R.	R/W	0x0
11:9	CONF_V15	Controls multiplexing on V15. Formerly CONF_MCSI1_DIN_R.	R/W	0x0
8:6	CONF_P14	Controls multiplexing on P14. Formerly CONF_MCSI1_BCLK_R.	R/W	0x0
5:3	CONF_AA17	Controls multiplexing on AA17. Formerly CONF_MCSI1_SYNC_R.	R/W	0x0
2:0	CONF_Y15	Controls multiplexing on Y15. Formerly CONF_BCLK_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 23. Functional Multiplexing Control B Register (FUNC_MUX_CTRL_B)

Base Address = 0xFFFE 1000, Offset Address = 0x30				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_V8	Controls multiplexing on V8. Formerly CONF_ARMIO_3_R.	R/W	0x0
26:24	CONF_Y8	Controls multiplexing on Y8. Formerly CONF_GPIO_8_R.	R/W	0x0
23:21	CONF_W8	Controls multiplexing on W8. Formerly CONF_GPIO_9_R.	R/W	0x0
20:18	CONF_R10	Controls multiplexing on R10. Formerly CONF_COM_MCLK_REQ_R.	R/W	0x0
17:15	CONF_V5	Controls multiplexing on V5. Formerly CONF_COM_MCLK_OUT_R.	R/W	0x0
14:12	CONF_V9	Controls multiplexing on V9. Formerly CONF_MCSI2_SYNC_R.	R/W	0x0
11:9	CONF_W9	Controls multiplexing on W9 Formerly CONF_MCSI2_DOUT_R.	R/W	0x0
8:6	CONF_AA9	Controls multiplexing on AA9. Formerly CONF_MCSI2_DIN_R.	R/W	0x0
5:3	CONF_Y10	Controls multiplexing on Y10. Formerly CONF_MCSI2_CLK_R.	R/W	0x0
2:0	CONF_R11	Controls multiplexing on R11. Formerly CONF_MMC_DAT0_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 24. Functional Multiplexing Control C Register (FUNC_MUX_CTRL_C)

Base Address = 0xFFFE 1000, Offset Address = 0x34				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_V6	Controls multiplexing on V6. Formerly CONF_TX2_R.	R/W	0x0
26:24	CONF_W5	Controls multiplexing on W5. Formerly CONF_RTS2_R.	R/W	0x0
23:21	CONF_Y5	Controls multiplexing on Y5. Formerly CONF_CTS2_R.	R/W	0x0
20:18	CONF_R9	Controls multiplexing on R9. Formerly CONF_RX2_R.	R/W	0x0
17:15	CONF_AA5	Controls multiplexing on AA5. Formerly CONF_MCBSP2_DOUT_R.	R/W	0x0
14:12	CONF_W6	Controls multiplexing on W6. Formerly CONF_MCBSP2_RSYNC_R.	R/W	0x0
11:9	CONF_Y6	Controls multiplexing on Y6. Formerly CONF_MCBSP2_CLKX_R.	R/W	0x0
8:6	CONF_V7	Controls multiplexing on V7. Formerly CONF_MCBSP2_CLKR_R.	R/W	0x0
5:3	CONF_W7	Controls multiplexing on W7. Formerly CONF_MCBSP2_XSYNC_R.	R/W	0x0
2:0	CONF_P10	Controls multiplexing on P10. Formerly CONF_MCBSP2_DIN_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 25. Functional Multiplexing Control D Register (FUNC_MUX_CTRL_D)

Base Address = 0xFFFE 1000, Offset Address = 0x38				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_G13	Controls multiplexing on G13. Formerly CONF_LCD_PIXEL_12_R.	R/W	0x0
26:24	CONF_A17	Controls multiplexing on A17. Formerly CONF_LCD_PIXEL_13_R.	R/W	0x0
23:21	CONF_C16	Controls multiplexing on C16. Formerly CONF_LCD_PIXEL_14_R.	R/W	0x0

Table 25. Functional Multiplexing Control D Register (FUNC_MUX_CTRL_D)

Base Address = 0xFFFE 1000, Offset Address = 0x38				
Bit	**Name**	**Function**	**R/W**	**Reset**
20:18	CONF_D15	Controls multiplexing on D15. Formerly CONF_LCD_PIXEL_15_R.	R/W	0x0
17:15	CONF_C15	Controls multiplexing on C15. Formerly CONF_LCD_PCLK_R.	R/W	0x0
14:12	CONF_C20	Controls multiplexing on C20. Formerly CONF_LDC_HSYNC_R.	R/W	0x0
11:9	CONF_B15	Controls multiplexing on B15. Formerly CONF_LCD_AC_R.	R/W	0x0
8:6	CONF_M4	Controls multiplexing on M4. Formerly CONF_NFCS2_R.	R/W	0x0
5:3	CONF_W4	Controls multiplexing on W4. Formerly CONF_USB_PUEN_R.	R/W	0x0
2:0	CONF_Y4	Controls multiplexing on Y4. Formerly CONF_BDCLK2_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEFh for this register to control functional multiplexing. See Table 8 for bit field values.

Table 26. Pulldown Control 0 Register (PULL_DWN_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x40				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PDEN_L14	Enables (0) pullup or pulldown on L14.	R/W	0x0
30	CONF_PDEN_M18	Enables (0) pullup or pulldown on M18.	R/W	0x0
29	CONF_PDEN_M19	Enables (0) pullup or pulldown on M19.	R/W	0x0
28	CONF_PDEN_L15	Enables (0) pullup or pulldown on L15.	R/W	0x0
27	CONF_PDEN_L18	Enables (0) pullup or pulldown on L18.	R/W	0x0
26	CONF_PDEN_L19	Enables (0) pullup or pulldown on L19.	R/W	0x0
25	CONF_PDEN_K14	Enables (0) pullup or pulldown on K14.	R/W	0x0
24	CONF_PDEN_K15	Enables (0) pullup or pulldown on K15.	R/W	0x0
23	CONF_PDEN_K19	Enables (0) pullup or pulldown on K19.	R/W	0x0
22	CONF_PDEN_K18	Enables (0) pullup or pulldown on K18.	R/W	0x0
21	CONF_PDEN_J14	Enables (0) pullup or pulldown on J14.	R/W	0x0
20	CONF_PDEN_J19	Enables (0) pullup or pulldown on J19.	R/W	0x0
19	CONF_PDEN_J18	Enables (0) pullup or pulldown on J18.	R/W	0x0

Table 26. Pulldown Control 0 Register (PULL_DWN_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x40				
Bit	**Name**	**Function**	**R/W**	**Reset**
18	CONF_PDEN_J15	Enables (0) pullup or pulldown on J15.	R/W	0x0
17	CONF_PDEN_H19	Enables (0) pullup or pulldown on H19.	R/W	0x0
16	CONF_PDEN_H20	Enables (0) pullup or pulldown on H20.	R/W	0x0
15	CONF_PDEN_H18	Enables (0) pullup or pulldown on H18.	R/W	0x0
14	CONF_PDEN_H15	Enables (0) pullup or pulldown on H15.	R/W	0x0
13	CONF_PDEN_G21	Enables (0) pullup or pulldown on G21.	R/W	0x0
12	CONF_PDEN_G20	Enables (0) pullup or pulldown on G20.	R/W	0x0
11	RESERVED	Reserved for future expansion.	R/W	0x0
10	CONF_PDEN_G18	Enables (0) pullup or pulldown on G18.	R/W	0x0
9	CONF_PDEN_F19	Enables (0) pullup or pulldown on F19.	R/W	0x0
8	CONF_PDEN_H14	Enables (0) pullup or pulldown on H14.	R/W	0x0
7	CONF_PDEN_E20	Enables (0) pullup or pulldown on E20.	R/W	0x0
6	CONF_PDEN_E19	Enables (0) pullup or pulldown on E19.	R/W	0x0
5	CONF_PDEN_F18	Enables (0) pullup or pulldown on F18.	R/W	0x0
4	CONF_PDEN_D20	Enables (0) pullup or pulldown on D20.	R/W	0x0
3	CONF_PDEN_D19	Enables (0) pullup or pulldown on D19.	R/W	0x0
2	CONF_PDEN_E18	Enables (0) pullup or pulldown on E18.	R/W	0x0
1	CONF_PDEN_C21	Enables (0) pullup or pulldown on C21.	R/W	0x0
0	CONF_PDEN_G19	Enables (0) pullup or pulldown on G19.	R/W	0x0

This register controls the enable or disable of the combined pullup/pulldown cell (0 = enabled, 1 = disabled). When enabling the cell, the user must set the corresponding bit in PU_PD_SEL_0 to select either a pullup or a pulldown. The pinout documentation in SPRS231 must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF, so that the programming is taken into account in the corresponding tactical cell.

Table 27. Pulldown Control 1 Register (PULL_DWN_CTRL_1)

Base Address = 0xFFFE 1000, Offset Address = 0x44				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PDEN_AA20	Enables (0) pullup or pulldown on AA20.	R/W	0x0
30	CONF_PDEN_U20	Enables (0) pullup or pulldown on U20.	R/W	0x0
29	CONF_PDEN_W16	Enables (0) pullup or pulldown on W16.	R/W	0x0
28	CONF_PDEN_W13	Enables (0) pullup or pulldown on W13.	R/W	0x0
27	CONF_PDEN_J20	Enables (0) pullup or pulldown on J20.	R/W	0x0
26	CONF_PDEN_W17	Enables (0) pullup or pulldown on W17.	R/W	0x0
25	CONF_PDEN_V16	Enables (0) pullup or pulldown on V16.	R/W	0x0
24	CONF_PDEN_Y12	Enables (0) pullup or pulldown on Y12.	R/W	0x0
23	CONF_PDEN_W19	Enables (0) pullup or pulldown on W19.	R/W	0x0
22	CONF_PDEN_P15	Enables (0) pullup or pulldown on P15.	R/W	0x0
21	CONF_PDEN_N14	Enables (0) pullup or pulldown on N14.	R/W	0x0
20	CONF_PDEN_V19	Enables (0) pullup or pulldown on V19.	R/W	0x0
19	CONF_PDEN_W21	Enables (0) pullup or pulldown on W21.	R/W	0x0
18	CONF_PDEN_U18	Enables (0) pullup or pulldown on U18.	R/W	0x0
17	Reserved	Reserved.	R/W	0x0
16	Reserved	Reserved.	R/W	0x0
15	CONF_PDEN_U19	Enables (0) pullup or pulldown on U19.	R/W	0x0
14	CONF_PDEN_N15	Enables (0) pullup or pulldown on N15.	R/W	0x0
13	CONF_PDEN_T19	Enables (0) pullup or pulldown on T19.	R/W	0x0
12	CONF_PDEN_T20	Enables (0) pullup or pulldown on T20.	R/W	0x0
11	CONF_PDEN_R18	Enables (0) pullup or pulldown on R18.	R/W	0x0
10	CONF_PDEN_R19	Enables (0) pullup or pulldown on R19.	R/W	0x0
9	CONF_PDEN_M14	Enables (0) pullup or pulldown on M14.	R/W	0x0
8	CONF_PDEN_P18	Enables (0) pullup or pulldown on P18.	R/W	0x0
7	CONF_PDEN_P20	Enables (0) pullup or pulldown on P20.	R/W	0x0

Table 27. Pulldown Control 1 Register (PULL_DWN_CTRL_1) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x44				
Bit	**Name**	**Function**	**R/W**	**Reset**
6	CONF_PDEN_P19	Enables (0) pullup or pulldown on P19.	R/W	0x0
5	CONF_PDEN_M15	Enables (0) pullup or pulldown on M15.	R/W	0x0
4	CONF_PDEN_N20	Enables (0) pullup or pulldown on N20.	R/W	0x0
3	CONF_PDEN_N18	Enables (0) pullup or pulldown on N18.	R/W	0x0
2	CONF_PDEN_N19	Enables (0) pullup or pulldown on N19.	R/W	0x0
1	CONF_PDEN_N21	Enables (0) pullup or pulldown on N21.	R/W	0x0
0	CONF_PDEN_M20	Enables (0) pullup or pulldown on M20.	R/W	0x0

This register controls the enable or disable of the combined pullup/pulldown cell (0 = enabled, 1 = disabled). When enabling the cell, the user must set the corresponding bit in PU_PD_SEL_1 to select either a pullup or a pulldown. The pinout documentation in SPRS231 must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF, so that the programming is taken into account in the corresponding tactical cell.

Table 28. Pulldown Control 2 Register (PULL_DWN_CTRL_2)

Base Address = 0xFFFE 1000, Offset Address = 0x48				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PDEN_AA5	Enables (0) pullup or pulldown on AA5.	R/W	0x0
30	CONF_PDEN_W6	Enables (0) pullup or pulldown on W6.	R/W	0x0
29	CONF_PDEN_Y6	Enables (0) pullup or pulldown on Y6.	R/W	0x0
28	CONF_PDEN_V7	Enables (0) pullup or pulldown on V7.	R/W	0x0
27	CONF_PDEN_W7	Enables (0) pullup or pulldown on W7.	R/W	0x0
26	CONF_PDEN_P10	Enables (0) pullup or pulldown on P10.	R/W	0x0
25	CONF_PDEN_V8	Enables (0) pullup or pulldown on V8.	R/W	0x0
24	CONF_PDEN_Y8	Enables (0) pullup or pulldown on Y8.	R/W	0x0
23	CONF_PDEN_W8	Enables (0) pullup or pulldown on W8.	R/W	0x0
22	CONF_PDEN_R10	Enables (0) pullup or pulldown on R10.	R/W	0x0

Table 28. Pulldown Control 2 Register (PULL_DWN_CTRL_2) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x48				
Bit	**Name**	**Function**	**R/W**	**Reset**
21	CONF_PDEN_V5	Enables (0) pullup or pulldown on V5.	R/W	0x0
20	CONF_PDEN_V9	Enables (0) pullup or pulldown on V9.	R/W	0x0
19	CONF_PDEN_W9	Enables (0) pullup or pulldown on W9.	R/W	0x0
18	CONF_PDEN_AA9	Enables (0) pullup or pulldown on AA9.	R/W	0x0
17	CONF_PDEN_Y10	Enables (0) pullup or pulldown on Y10.	R/W	0x0
16	CONF_PDEN_R11	Enables (0) pullup or pulldown on R11.	R/W	0x0
15	CONF_PDEN_P11	Enables (0) pullup or pulldown on P11.	R/W	0x0
14	CONF_PDEN_V10	Enables (0) pullup or pulldown on V10.	R/W	0x0
13	CONF_PDEN_V11	Enables (0) pullup or pulldown on V11.	R/W	0x0
12	CONF_PDEN_W10	Enables (0) pullup or pulldown on W10.	R/W	0x0
11	CONF_PDEN_P13	Enables (0) pullup or pulldown on P13.	R/W	0x0
10	CONF_PDEN_R13	Enables (0) pullup or pulldown on R13.	R/W	0x0
9	CONF_PDEN_V15	Enables (0) pullup or pulldown on V15.	R/W	0x0
8	CONF_PDEN_P14	Enables (0) pullup or pulldown on P14.	R/W	0x0
7	CONF_PDEN_AA17	Enables (0) pullup or pulldown on AA17.	R/W	0x0
6	CONF_PDEN_Y15	Enables (0) pullup or pulldown on Y15.	R/W	0x0
5	CONF_PDEN_W15	Enables (0) pullup or pulldown on W15.	R/W	0x0
4	CONF_PDEN_W14	Enables (0) pullup or pulldown on W14.	R/W	0x0
3	CONF_PDEN_Y14	Enables (0) pullup or pulldown on Y14.	R/W	0x0
2	CONF_PDEN_V14	Enables (0) pullup or pulldown on V14.	R/W	0x0
1	CONF_PDEN_R14	Enables (0) pullup or pulldown on R14.	R/W	0x0
0	CONF_PDEN_AA15	Enables (0) pullup or pulldown on AA15.	R/W	0x0

This register controls the enable or disable of the combined pullup/pulldown cell (0 = enabled, 1 = disabled). When enabling the cell, the user must set the corresponding bit in PU_PD_SEL_2 to select either a pullup or a pulldown. The pinout documentation in SPRS231 must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF, so that the programming is taken into account in the corresponding tactical cell.

Table 29. Pulldown Control 3 Register (PULL_DWN_CTRL_3)

Base Address = 0xFFFE 1000, Offset Address = 0x4C				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PDEN_W2	Enables (0) pullup or pulldown on W2.	R/W	0X0
30	CONF_PDEN_V4	Enables (0) pullup or pulldown on V4.	R/W	0X0
29	CONF_PDEN_Y1	Enables (0) pullup or pulldown on Y1.	R/W	0X0
28	CONF_PDEN_Y17	Enables (0) pullup or pulldown on Y17.	R/W	0X0
27	CONF_PDEN_D18	Enables (0) pullup or pulldown on D18.	R/W	0X0
26	CONF_PDEN_B21	Enables (0) pullup or pulldown on B21.	R/W	0X0
25	CONF_PDEN_C19	Enables (0) pullup or pulldown on C19.	R/W	0X0
24	CONF_PDEN_G14	Enables (0) pullup or pulldown on G14.	R/W	0X0
23	CONF_PDEN_H13	Enables (0) pullup or pulldown on H13.	R/W	0X0
22	CONF_PDEN_A20	Enables (0) pullup or pulldown on A20.	R/W	0X0
21	CONF_PDEN_B19	Enables (0) pullup or pulldown on B19.	R/W	0X0
20	CONF_PDEN_C18	Enables (0) pullup or pulldown on C18.	R/W	0X0
19	Reserved	Reserved.	R/W	0X0
18	CONF_PDEN_D17	Enables (0) pullup or pulldown on D17.	R/W	0X0
17	CONF_PDEN_D16	Enables (0) pullup or pulldown on D16.	R/W	0X0
16	CONF_PDEN_C17	Enables (0) pullup or pulldown on C17.	R/W	0X0
15	CONF_PDEN_B17	Enables (0) pullup or pulldown on B17.	R/W	0X0
14	CONF_PDEN_G13	Enables (0) pullup or pulldown on G13.	R/W	0X0
13	CONF_PDEN_A17	Enables (0) pullup or pulldown on A17.	R/W	0X0
12	CONF_PDEN_C16	Enables (0) pullup or pulldown on C16.	R/W	0X0

Table 29. Pulldown Control 3 Register (PULL_DWN_CTRL_3) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x4C				
Bit	**Name**	**Function**	**R/W**	**Reset**
11	CONF_PDEN_D15	Enables (0) pullup or pulldown on D15.	R/W	0X0
10	Reserved	Reserved.	R/W	0X0
9	Reserved	Reserved.	R/W	0X0
8	CONF_PDEN_W11	Enables (0) pullup or pulldown on W11.	R/W	0x0
7	Reserved	Reserved.	R/W	0x0
6	CONF_PDEN_M4	Enables (0) pullup or pulldown on M4.	R/W	0x0
5	CONF_PDEN_W4	Enables (0) pullup or pulldown on W4.	R/W	0x0
4	CONF_PDEN_Y4	Enables (0) pullup or pulldown on Y4.	R/W	0x0
3	CONF_PDEN_V6	Enables (0) pullup or pulldown on V6.	R/W	0x0
2	CONF_PDEN_W5	Enables (0) pullup or pulldown on W5.	R/W	0x0
1	CONF_PDEN_Y5	Enables (0) pullup or pulldown on Y5.	R/W	0x0
0	CONF_PDEN_R9	Enables (0) pullup or pulldown on R9.	R/W	0x0

This register controls the enable or disable of the combined pullup/pulldown cell (0 = enabled, 1 = disabled). When enabling the cell, it is assumed that the user has cleared or set the corresponding bit in PU_PD_SEL_3 to select a pullup or a pulldown. The pinout section in the Application Processor Data Manual (SPRS231) should be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF, so that the programming is taken into account in the corresponding tactical cell.

Table 30. Gate and Inhibit Control Register (GATE_INH_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x50				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:6	CONF_GATE_INH_ RESERVED	Reserved for future expansion.	R/W	0x0000000
5	RESERVED1	Reserved for future expansion.	R/W	0x0
4	RESERVED	Reserved for future expansion.	R/W	0x0
3	CONF_HIGH_IMP3	Controls high impedance on MCSI1.DOUT. 0: Normal function 1: Hi-Z	R/W	0x0
2	CONF_SOFTWARE_PWR _R	Controls software gating and inhibiting of the I/O, which is gated or inhibited by COM_PWR status. If the gating and inhibiting logic is enabled by FUNC_MUX_CTRL_0 (10−13 bits) and CONF_SOFTWARE_GATE_ENA_R is set to 1, this bit controls the com_pwr gating and inhibiting, instead of device pins.	R/W	0x0
1	CONF_SOFTWARE_BVLZ _R	This bit controls software gating and inhibiting of the I/O, which is gated or inhibited by the BFAIL/EXT_FIQ signal. If the gating and inhibiting logic is enabled by FUNC_MUX_CTRL_0(10−13)bits and CONF_SOFTWARE_GATE_ENA_R is set to 1, this bit controls the BFAIL/EXT_FIQ gating and inhibiting, instead of device pins.	R/W	0x0
0	CONF_SOFTWARE_GATE _ENA_R	This bit controls software gating of the I/O, which is gated or inhibited. If the gating and inhibiting logic is enabled by FUNC_MUX_CTRL_0(10−13) bits, the software is enabled to control the gating and inhibiting, instead of device pins.	R/W	0x0

This register controls the software gating and inhibiting functionality for the device. The pinout section of the Application Processor Data Manual (SPRS231) should be consulted to understand which pins are affected by the Gated1, Gated2, Inhibit1, and Inhibit2 functions of the device.

Table 31. Configuration Revision Register (CONF_REV)

Base Address = 0xFFFE 1000, Offset Address = 0x58				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:8	CONF_REV_RESERVED	Reserved for future expansion.	R	0x000000
7:0	CONF_REV_R	This 8-bit field indicates the revision number of the current module. This value is fixed by hardware. The 4-bit LSBs indicate a minor revision. The 4-bit MSBs indicate a major revision. Example: 0x10 => Version 1.0 Reset has no effect on the value returned.	R	0x10

This is a read-only register that contains the revision number of the module. A write to this register has no effect.

Table 32. Voltage Control 0 Register (VOLTAGE_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x60				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:14	CONF_VOLTAGE_ RESERVED	Reserved for future expansion.	R/W	0x00000
13	RESERVED	This bit should be set as 0.	R/W	0X0
12	CONF_VOLTAGE_RTC_R	This bit controls the drive strength of the DVDD10 RTC voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0

† For EMIFS and EMIFF 3.0-V and 3.3-V operation, use the 2.75V setting.
Note: For a description of 1.8-V and 2.75-V nominal voltage ranges, see the Data Manual (SPRS231).

Table 32. Voltage Control 0 Register (VOLTAGE_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x60				
Bit	**Name**	**Function**	**R/W**	**Reset**
11	CONF_VOLTAGE_ VDDSHV9_R	This bit controls the drive strength of the DVDD9 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
10	CONF_VOLTAGE_ VDDSHV8_R	This bit controls the drive strength of the DVDD8 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
9	CONF_VOLTAGE_ VDDHSV7_R	This bit controls the drive strength of the DVDD7 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
8	CONF_VOLTAGE_ VDDHSV6_R	This bit controls the drive strength of the DVDD6 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0

† For EMIFS and EMIFF 3.0-V and 3.3-V operation, use the 2.75V setting.
Note: For a description of 1.8-V and 2.75-V nominal voltage ranges, see the Data Manual (SPRS231).

Table 32. Voltage Control 0 Register (VOLTAGE_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x60				
Bit	**Name**	**Function**	**R/W**	**Reset**
7	CONF_VOLTAGE_ VDDSHV2_R	This bit controls the drive strength of the DVDD2 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
6	CONF_VOLTAGE_ VDDSHV1_R	This bit controls the drive strength of the DVDD1 voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
5	RESERVED1	Reserved for potential low-power operation control	R/W	0x0
4	RESERVED2	Reserved for potential low-power operation control	R/W	0x0
3	RESERVED	Reserved for potential low-power operation control	R/W	0x0

† For EMIFS and EMIFF 3.0-V and 3.3-V operation, use the 2.75V setting.
Note: For a description of 1.8-V and 2.75-V nominal voltage ranges, see the Data Manual (SPRS231).

Table 32. Voltage Control 0 Register (VOLTAGE_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x60				
Bit	**Name**	**Function**	**R/W**	**Reset**
2	CONF_VOLTAGE_ COMIF_R	This bit controls the drive strength of the DVDD3 communication processor interface voltage domain. The bit controls the low/high voltage mode. The voltage range is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range).	R/W	0x0
1	CONF_VOLTAGE_ SDRAM_R	This bit controls the drive strength of the DVDD4 SDRAM interface voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range)†.	R/W	0x0
0	CONF_VOLTAGE_ FLASH_R	This bit controls the drive strength of the DVDD5 flash interface voltage domain. The bit controls the low/high voltage mode. The voltage range supported is defined in the SPRS231 document. 0: Low-voltage mode drive strength of nominal (nominal 1.80-V range). 1: Interface in high-voltage mode drive strength (nominal 2.75-V range)†.	R/W	0x0

† For EMIFS and EMIFF 3.0-V and 3.3-V operation, use the 2.75V setting.
Note: For a description of 1.8-V and 2.75-V nominal voltage ranges, see the Data Manual (SPRS231).

This register controls the low- or high-voltage mode for each I/O power supply domain. Low-voltage mode is defined as 1.8-V range, and high-voltage mode is defined as 2.75-V range. The exact I/O voltage ranges supported by the interfaces of the device are specified in the Data Manual (SPRS231). After reset, the device interfaces are configured in low-voltage mode, and the software must adjust the programming of this register to match the actual voltages applied to each I/O power supply domain. The effect of applying 2.75 V while the interface is in low-voltage mode, for example, is simply that it is faster and more powerful than is usually required.

Table 33. USB Transceiver Control Register (USB_TRANSCEIVER_CTRL)

Base Address = 0xFFFE 1000, Offset Address = 0x64				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:9	UNUSED	These bits are not implemented.	R	0x000000
8	CONF_USB2_UNI_R	This bit configures the way USB port 2 interfaces with external USB transceiver. 0: Bidirectional mode USB2.SE0 is a bidirectional I/O, rather than an output only. Input of the USB2.SE0 bidirectional I/O is connected to usb2_vm port of the USB OTG module. USB2.TXD is a bidirectional I/O, rather than an output only. Input of the USB2.TXD bidirectional I/O is connected to USB2.VP port of the USB OTG module. 1: Unidirectional mode	R/W	0x0
7	CONF_USB1_UNI_R	This bit configures the way USB port 1 interfaces with external USB transceiver. 0: Bidirectional mode USB1.SE0 is a bidirectional I/O, rather than an output only. Input of the USB1.SE0 bidirectional I/O is connected to USB1.VM port of the USB OTG module. USB1.TXD is a bidirectional I/O, rather than an output only. Input of the USB1.TXD bidirectional I/O is connected to USB1.VP port of the USB OTG module. 1: Unidirectional mode	R/W	0x0

Table 33. USB Transceiver Control Register (USB_TRANSCEIVER_CTRL) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x64				
Bit	**Name**	**Function**	**R/W**	**Reset**
6:4	CONF_USB_PORT0_R	These bits control the multiplexing on the I/O, which defaults to USB.DP and USB.DM at reset. These 3 bits configure USB port 0 for alternate operation. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. 000: USB.DP/USB.DM 100: I2C.SDA/I2C.SCl 101: UART1.RX/UART1.TX 111: USB2.PUEN/HI-Z Other values are not allowed. Programming this field on some other value produces unpredictable results.	R/W	0x0
3	CONF_USB0_ISOLATE_R	Isolates the USB port 0 controller from the integrated USB transceiver. 0: Normal mode 1: Isolation mode	R/W	0x0
2	CONF_USB_PWRDN_DM_R	Enable/disable of pulldown on USB DM pin. 0: Enable of pulldown on DM 1: Disable of pulldown on DM	R/W	0x1
1	CONF_USB_PWRDN_DP_R	Enable/disable of pulldown on USB DP pin. 0: Enable of pulldown on DP 1: Disable of pulldown on DP	R/W	0x1
0	RESERVED	Reserved for future expansion.	R/W	0x0

Table 34. LDO Powerdown Control Register (LDO_PWRDN_CNTRL)

Base Address = 0xFFFE 1000, Offset Address = 0x68				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:1	UNUSED	These bits are not implemented.	R	0x00000000
0	CONF_LDO_PWRDN_ CNTRL_R	If the user sets LDO_PWRDN to 1, the LDO can be powered-down and bypassed.	R/W	0x0

This 1-bit register bypasses the LDO.

Table 35. Test Debug Control 0 Register (TEST_DBG_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x70				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:22	CONF_TEST_DBG_ RESERVED	Reserved for future expansion.	R/W	0x0000
21	CONF_RNG_TEST_OSC	Ring oscillator divider enable.	R/W	0x0
20	CONF_RNG_SELECT_ OSC	Ring oscillator selection for characterization Active high.	R/W	0x0
19	CONF_DSP_BRTE_ WRITE_R	DFT WRITE signal to control DSP BRTE memories.	R/W	0x1
18	CONF_DSP_BRTE_ READ_R	DFT READ signal to control DSP BRTE memories.	R/W	0x1
17:8	CONF_TDBG_RESERVED _R	These are reserved test and debug bits for the device. They must be set to 0 at all times to avoid errant behavior.	R/W	0x000
7:5	CONF_TEST_DBG_ RESERVED1	Reserved for future expansion.	R/W	0x0
4	CONF_TEST_VBUS_CELL	This bit tests the UIS480 VBUS detect cell. When set to 1, the output of the VBUS detect logic outputs a 0.	R/W	0x0
3	CONF_DPLL_EXT_SEL	This bit selects between the internal 48-MHz clock generated by the APLL and an external 48-MHz clock source. When this bit is set to 1, GPIO14 becomes the source of 48 MHz for the device.	R/W	0x0

Table 35. Test Debug Control 0 Register (TEST_DBG_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x70				
Bit	**Name**	**Function**	**R/W**	**Reset**
2	CONF_VBOX_EN	OMAP VBOX SW test enable. This register must be set to 1 to enable writing to the bit fields CONF_VBOX1 CONF_VBOX2, CONF_DSP_BRTE_READ_R, and CONF_DSP_BRTE_WRITE_R.	R/W	0x0
1	CONF_VBOX2	OMAP VBOX − DFT WRITE signal to control MPU BRTE memories.	R/W	0x1
0	CONF_VBOX1	OMAP VBOX 1 − DFT READ signal to control MPU BRTE memories.	R/W	0x1

Table 36. Module Configuration Control 0 Register (MOD_CONF_CTRL_0)

Base Address = 0xFFFE 1000, Offset Address = 0x80				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_MOD_UART3_CLK_MODE_R	This bit determines the 48-MHz clock request for UART3. 0: 48-MHz clock request is inactive. 1: 48-MHz clock request is active.	R/W	0x0
30	CONF_MOD_UART2_CLK_MODE_R	This bit determines the clock source of UART2. 0: UART_MCLKO from ULPD that can be either the system clock or 32 kHz, depending on system state and ULPD register programming. 1: 48 MHz.	R/W	0x0
29	CONF_MOD_UART1_CLK_MODE_R	This bit determines whether 48-MHz clock request for UART1 is active. 0: 48-MHz clock request is inactive. 1: 48-MHz clock request is active.	R/W	0x0
28	RESERVED	See Note 1.	R/W	0x0
27:24	MOD_32KOSC_SW_R	See Note 1.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 36. Module Configuration Control 0 Register (MOD_CONF_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x80				
Bit	**Name**	**Function**	**R/W**	**Reset**
23	CONF_MOD_MMC_SD_ CLK_REQ_R	This is the functional 48-MHz clock request for the MMCSDIO1 interface. This bit resets to 0. This corresponds to the MMCSDIO1 clock *not* being requested. The user must set the bit to 1 to request the clock for the MMCSDIO1 interface.	R/W	0x0
22	CONF_MOD_DPRAM_ ENABLE_R	See Note 1.	R/W	0x0
21	CONF_MOD_MSMMC_ VSS_HIZ_OVERRIDE	See Note 1.	R/W	0x0
20	CONF_MOD_MMC_SD2_ CLK_REQ_R	This is the functional 48-MHz clock request for the device MMC/SD 2 interface. This bit resets to 0. This corresponds to the MMC/SD clock *not* being requested. The user must set the bit to 1 to request the clock for the MMC/SD interface.	R/W	0x0
19	CONF_MOD_MCBSP3_ CLK_SEL_R	This bit determines the method of frame sync wrap-around used on MCBSP3. 0: Wrap-around done in hardware external to the McBSP (3 pins mode). 1: Wrap-around disabled. Wrap-around can be performed within the McBSP module (4 pins mode). This bit also selects the Interface clock used for the McBSP3 module: 0: DSPXOR_CLK is selected. 1: DSPPER_CLK is selected.	R/W	0x0
18	CONF_MOD_MCBSP1_ CLKS_SEL_R	This register selects the clock used for the McBSP1 clocks input: 0: McBSP1.CLKS pin of the device. 1: OMAP DPLL1 clockout.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 36. Module Configuration Control 0 Register (MOD_CONF_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x80				
Bit	**Name**	**Function**	**R/W**	**Reset**
17	CONF_MOD_USB_W2FC_VBUS_MODE_R	This bit determines the method used for USB VBUS detection. 0: The VBUS detection is controlled by GPIO_0 state (if in muxed mode 2). 1: The VBUS detection is controlled by DVDD2 detection on the line.	R/W	0x0
16	CONF_MOD_I2C_SELECT_R	See Note 1.	R/W	0x0
15	CONF_MOD_UART3_IRDA_MODE_R	See Note 1.	R/W	0x0
14	CONF_MOD_MCBSP1_CLK_SEL_R	This register selects the clock used for the McBSP1 module: 0: DSPXOR_CLK is selected. 1: DSPPER_CLK is selected.	R/W	0x0
13	CONF_MOD_MMC2_CLK_SEL_R	This register selects the clock used for the MMC/SD2 module: 0: 48-MHz MMC2_DPLL_CLK from the ULPD. 1: ARM_XOR_CLK from OMAP clock module	R/W	0x0
12	CONF_MOD_COM_MCLK_12_48_SEL_R	This bit determines whether MCLK of the device outputs the system clock or the 48-MHz clock (selection must be in accordance in ULPD and IO_CTRL). 0: MCLK is system clock. 1: MCLK is 48-MHz clock (or divided down).	R/W	0x0
11	CONF_MOD_USB_HOST_UART_SELECT_R	0: Disables UART multiplexing on USB port 1. 1: Enables UART multiplexing on USB port 1.	R/W	0x0
10	CONF_MOD_USB_HOST_LB_ARB_EN_R	Not currently used.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 36. Module Configuration Control 0 Register (MOD_CONF_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x80				
Bit	**Name**	**Function**	**R/W**	**Reset**
9	CONF_MOD_USB_HOST_HHC_UHOST_EN_R	Enable input for functional-mode clocking of USB_HHC. 0: Internal functional mode 48-MHz and 12-MHz clocks are disabled. USB_HHC cannot function as a USB host. 1: Internal functional mode 48-MHz and 12-MHz clocks are enabled.	R/W	0x0
8	CONF_MOD_USB_HOST_HMC_TLL_SPEED_R	Transceiverless link logic (TLL) USB speed control. For HMC modes (as defined by HMC_MODE_I and HMC_JTAG_EN_I) where the TLL is used, this bit determines whether the modeling of the device pullup resistor is on the internal D+ or the internal D− signal. The pullup is modeled only when HMC_TLL_ATTACH_I is active. This signal is ignored when either device is driving USB data, and whenever HMC_MODE or HMC_JTAG_EN_I specify that the TLL is not being used. 0: When HMC_TLL_ATTACH_I is high and the TLL is enabled and neither the USB host nor the external USB device attempts to drive, the pullup is modeled on the D− signal to indicate a low-speed device. 1: When HMC_TLL_ATTACH_I is high and the TLL is enabled and neither the USB host nor the external USB device attempts to drive, the pullup is modeled on the D− signal to indicate a full-speed device.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 36. Module Configuration Control 0 Register (MOD_CONF_CTRL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x80				
Bit	**Name**	**Function**	**R/W**	**Reset**
7	CONF_MOD_USB_HOST_HMC_TLL_ATTACH_R	Transceiverless link logic (TLL) USB attach control. For HMC modes (as defined by HMC_MODE_I and HMC_JTAG_EN_I) where the TLL is used, this bit determines whether or not the TLL models its internal representation of USB differential data signals with or without a pullup when neither the internal USB host nor the external USB device is attempting to drive the signals. This signal is ignored when either device is driving USB data. 0: When neither the USB host nor the external USB device attempts to drive, no pullup is modeled. The associated USB host port interprets this as no device attached. 1: When neither the USB host nor the external USB device attempts to drive, a pullup is modeled on either the internal representation of D+ or D−. The associated USB host port interprets this as an attached device with the bus in an idle condition.	R/W	0x0
6:1	CONF_MOD_USB_HOST_HMC_MODE_R	USB_HHC port multiplexing control. This resets to the following configuration. 000000b: USB port 0 is controlled by the USB_W2FC, and USB ports 1 and 2 are held in benign states.	R/W	0x0
0	CONF_MOD_USB_HOST_EXTCLKENI_R	See Note 1.	R/W	0x0

Notes: 1) This function has been removed. Writing a 1 or a 0 to this register is acceptable. However, it is recommended to write a 0, in case functions are added to this register space in the future.

Table 37. Functional Multiplexing Control E Register (FUNC_MUX_CTRL_E)

Base Address = 0xFFFE 1000, Offset Address = 0x90				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0x0
29:27	CONF_G14	Controls multiplexing on G14. Formerly CONF_LCD_PIXEL_3_R.	R/W	0x0
26:24	CONF_H13	Controls multiplexing on H13. Formerly CONF_LCD_PIXEL_4_R.	R/W	0x0
23:21	CONF_A20	Controls multiplexing on A20. Formerly CONF_LCD_PIXEL_5_R.	R/W	0x0
20:18	CONF_B19	Controls multiplexing on B19. Formerly CONF_LCD_PIXEL_6_R.	R/W	0x0
17:15	CONF_C18	Controls multiplexing on C18. Formerly CONF_LCD_PIXEL_7_R.	R/W	0x0
14:12	CONF_D17	Controls multiplexing on D17. Formerly CONF_LCD_PIXEL_8_R.	R/W	0x0
11:9	CONF_B18	Controls multiplexing on B18. Formerly CONF_LCD_VSYNC_R.	R/W	0X0
8:6	CONF_D16	Controls multiplexing on D16. Formerly CONF_LCD_PIXEL_9_R.	R/W	0x0
5:3	CONF_C17	Controls multiplexing on C17. Formerly CONF_LCD_ PIXEL_10_R.	R/W	0X0
2:0	CONF_B17	Controls multiplexing on B17. Formerly CONF_LCD_ PIXEL_11_R.	R/W	0X0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. See Table 8 for bit-field values.

Table 38. Functional Multiplexing Control F Register (FUNC_MUX_CTRL_F)

Base Address = 0xFFFE 1000, Offset Address = 0x94				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0X0
29:27	CONF_V2	Controls multiplexing on V2. Formerly CONF_FRDY_R.	R/W	0x0
26:24	CONF_U4	Controls multiplexing on U4. Formerly CONF_NFOE_R.	R/W	0X0
23:21	CONF_W1	Controls multiplexing on W1. Formerly CONF_NFRP_R.	R/W	0X0
20:18	CONF_W2	Controls multiplexing on W2. Formerly CONF_NFWE_R.	R/W	0X0
17:15	CONF_V4	Controls multiplexing on V4. Formerly CONF_NFWP_R.	R/W	0X0
14:12	CONF_Y1	Controls multiplexing on Y1. Formerly CONF_NFCS_1B_R.	R/W	0X0
11:9	CONF_Y17	Controls multiplexing on Y17. Formerly CONF_RTCK_R.	R/W	0x0
8:6	CONF_D18	Controls multiplexing on D18. Formerly CONF_LCD_PIXEL_0_R.	R/W	0x0
5:3	CONF_B21	Controls multiplexing on B21. Formerly CONF_LCD_PIXEL_1_R.	R/W	0x0
2:0	CONF_C19	Controls multiplexing on C19. Formerly CONF_LCD_PIXEL_2_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. See Table 8 for bit-field values.

Table 39. Functional Multiplexing Control 10 Register (FUNC_MUX_CTRL_10)

Base Address = 0xFFFE 1000, Offset Address = 0x98				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0X0
29:27	CONF_M3	Controls multiplexing on M3. Formerly CONF_NFCS_1_R.	R/W	0X0
26:24	CONF_N8	Controls multiplexing on N8. Formerly CONF_NFCS_3_R.	R/W	0X0
23:21	CONF_N3	Controls multiplexing on N3. Formerly CONF_FCLK_R.	R/W	0X0
20:18	CONF_P3	Controls multiplexing on P3. Formerly CONF_NFCS_2B_R.	R/W	0X0
17:15	CONF_W11	Controls multiplexing on W11. Formerly CONF_MMC_DAT3_R.	R/W	0X0
14:12	RESERVED 1	Reserved for future expansion.	R/W	0X0

Table 39. Functional Multiplexing Control 10 Register (FUNC_MUX_CTRL_10) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x98				
Bit	**Name**	**Function**	**R/W**	**Reset**
11:9	CONF_L4	Controls multiplexing on L4. Formerly CONF_NFADV_R.	R/W	0X0
8:6	CONF_L3	Controls multiplexing on L3. Formerly CONF_NFBE_0_R.	R/W	0x0
5:3	CONF_M8	Controls multiplexing on M8. Formerly CONF_NFBE_1_R.	R/W	0x0
2:0	CONF_M7	Controls multiplexing on M7. Formerly CONF_GPIO_1_R.	R/W	0x0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. See Table 8 for bit-field values.

Table 40. Functional Multiplexing Control 11 Register (FUNC_MUX_CTRL_11)

Base Address = 0xFFFE 1000, Offset Address = 0x9C				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0X0
29:27	RESERVED	Reserved for future expansion.	R/W	0X0
26:24	CONF_F3	Controls multiplexing on F3. Formerly CONF_FADD_9_R.	R/W	0X0
23:21	CONF_G4	Controls multiplexing on G4. Formerly CONF_FADD_10_R.	R/W	0X0
20:18	CONF_G3	Controls multiplexing on G3. Formerly CONF_FADD_11_R.	R/W	0X0
17:15	CONF_G2	Controls multiplexing on G2. Formerly CONF_FADD_12_R.	R/W	0X0
14:12	CONF_K8	Controls multiplexing on K8. Formerly CONF_FADD_13_R.	R/W	0X0
11:9	CONF_H4	Controls multiplexing on H4. Formerly CONF_FADD_14_R.	R/W	0X0
8:6	CONF_H3	Controls multiplexing on H3. Formerly CONF_FADD_15_R.	R/W	0X0
5:3	CONF_K7	Controls multiplexing on K7. Formerly CONF_FADD_16_R.	R/W	0X0
2:0	RESERVED	Reserved for future expansion.	R/W	0X0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. See Table 8 for bit−field values.

Table 41. Functional Multiplexing Control 12 Register (FUNC_MUX_CTRL_12)

Base Address = 0xFFFE 1000, Offset Address = 0xA0				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	RESERVED	Reserved for future expansion.	R/W	0X0
29:27	RESERVED	Reserved for future expansion.	R/W	0x0
26:24	CONF_J8	Controls multiplexing on J8. Formerly CONF_FADD_1_R.	R/W	0X0
23:21	CONF_D3	Controls multiplexing on D3. Formerly CONF_FADD_2_R.	R/W	0X0
20:18	CONF_C1	Controls multiplexing on C1. Formerly CONF_FADD_3_R.	R/W	0X0
17:15	CONF_E4	Controls multiplexing on E4. Formerly CONF_FADD_4_R.	R/W	0X0
14:12	CONF_D2	Controls multiplexing on D2. Formerly CONF_FADD_5_R.	R/W	0X0
11:9	CONF_F4	Controls multiplexing on F4. Formerly CONF_FADD_6_R.	R/W	0X0
8:6	CONF_E3	Controls multiplexing on E3. Formerly CONF_FADD_7_R.	R/W	0X0
5:3	CONF_J7	Controls multiplexing on J7. Formerly CONF_FADD_8_R.	R/W	0X0
2:0	RESERVED	Reserved for future expansion.	R/W	0X0

This register controls functional multiplexing. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control functional multiplexing. See Table 8 for bit-field values.

Table 42. Pulldown Control 4 Register (PULL_DWN_CTRL_4)

Base Address = 0xFFFE 1000, Offset Address = 0xAC				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PDEN_Y18	Enables (0) pullup or pulldown on Y18.	R/W	0X0
30	CONF_PDEN_W18	Enables (0) pullup or pulldown on W18.	R/W	0X0
29	CONF_PDEN_V17	Enables (0) pullup or pulldown on V17.	R/W	0X0
28	CONF_PDEN_Y19	Enables (0) pullup or pulldown on Y19.	R/W	0X0
27	CONF_PDEN_V18	Enables (0) pullup or pulldown on V18.	R/W	0X0
26	CONF_PDEN_L3	Enables (0) pullup or pulldown on L3.	R/W	0x0
25	CONF_PDEN_M8	Enables (0) pullup or pulldown on M8.	R/W	0x0
24	CONF_PDEN_M7	Enables (0) pullup or pulldown on M7.	R/W	0x0
23	CONF_PDEN_M3	Enables (0) pullup or pulldown on M3.	R/W	0x0

Table 42. Pulldown Control 4 Register (PULL_DWN_CTRL_4) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xAC				
Bit	**Name**	**Function**	**R/W**	**Reset**
22	CONF_PDEN_N8	Enables (0) pullup or pulldown on N8.	R/W	0x0
21	CONF_PDEN_N3	Enables (0) pullup or pulldown on N3.	R/W	0X0
20	CONF_PDEN_J8	Enables (0) pullup or pulldown on J8.	R/W	0x0
19	CONF_PDEN_D3	Enables (0) pullup or pulldown on D3.	R/W	0x0
18	CONF_PDEN_C1	Enables (0) pullup or pulldown on C1.	R/W	0x0
17	CONF_PDEN_E4	Enables (0) pullup or pulldown on E4.	R/W	0x0
16	CONF_PDEN_D2	Enables (0) pullup or pulldown on D2.	R/W	0x0
15	CONF_PDEN_F4	Enables (0) pullup or pulldown on F4.	R/W	0x0
14	CONF_PDEN_E3	Enables (0) pullup or pulldown on E3.	R/W	0x0
13	CONF_PDEN_J7	Enables (0) pullup or pulldown on J7.	R/W	0x0
12	CONF_PDEN_F3	Enables (0) pullup or pulldown on F3.	R/W	0x0
11	CONF_PDEN_G4	Enables (0) pullup or pulldown on G4.	R/W	0x0
10	CONF_PDEN_G3	Enables (0) pullup or pulldown on G3.	R/W	0X0
9	CONF_PDEN_G2	Enables (0) pullup or pulldown on G2.	R/W	0X0
8	CONF_PDEN_K8	Enables (0) pullup or pulldown on K8.	R/W	0X0
7	CONF_PDEN_H4	Enables (0) pullup or pulldown on H4.	R/W	0X0
6	CONF_PDEN_H3	Enables (0) pullup or pulldown on H3.	R/W	0X0
5	CONF_PDEN_K7	Enables (0) pullup or pulldown on K7.	R/W	0X0
4	CONF_PDEN_L4	Enables (0) pullup or pulldown on L4.	R/W	0X0
3	CONF_PDEN_V2	Enables (0) pullup or pulldown on V2.	R/W	0X0
2	CONF_PDEN_P3	Enables (0) pullup or pulldown on P3.	R/W	0X0
1	CONF_PDEN_U4	Enables (0) pullup or pulldown on U4.	R/W	0X0
0	CONF_PDEN_W1	Enables (0) pullup or pulldown on W1.	R/W	0X0

This register controls the enable or disable of the combined pullup/pulldown cell (0 = enabled, 1 = disabled). When enabling the cell, the user must set the corresponding bit in PU_PD_SEL_4 to select either a pullup or a pulldown. The pinout documentation (Application Processor Data Manual (SPRS231)) must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF, so that the programming is taken into account in the corresponding tactical cell.

Table 43. Pullup/Pulldown Selection 0 Register (PU_PD_SEL_0)

Base Address = 0xFFFE 1000, Offset Address = 0xB4				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PU_PD_L14	Configure pullup (=1) or pulldown (=0) on L14.	R/W	0x0
30	CONF_PU_PD_M18	Configure pullup (=1) or pulldown (=0) on M18.	R/W	0x0
29	CONF_PU_PD_M19	Configure pullup (=1) or pulldown (=0) on M19.	R/W	0x0
28	CONF_PU_PD_L15	Configure pullup (=1) or pulldown (=0) on L15.	R/W	0x0
27	CONF_PU_PD_L18	Configure pullup (=1) or pulldown (=0) on L18.	R/W	0x0
26	CONF_PU_PD_L19	Configure pullup (=1) or pulldown (=0) on L19.	R/W	0x0
25	CONF_PU_PD_K14	Configure pullup (=1) or pulldown (=0) on K14.	R/W	0x0
24	CONF_PU_PD_K15	Configure pullup (=1) or pulldown (=0) on K15.	R/W	0x0
23	CONF_PU_PD_K19	Configure pullup (=1) or pulldown (=0) on K19.	R/W	0x0
22	CONF_PU_PD_K18	Configure pullup (=1) or pulldown (=0) on K18.	R/W	0x0
21	CONF_PU_PD_J14	Configure pullup (=1) or pulldown (=0) on J14.	R/W	0x0
20	CONF_PU_PD_J19	Configure pullup (=1) or pulldown (=0) on J19.	R/W	0x0
19	CONF_PU_PD_J18	Configure pullup (=1) or pulldown (=0) on J18.	R/W	0x0
18	CONF_PU_PD_J15	Configure pullup (=1) or pulldown (=0) on J15.	R/W	0x0
17	CONF_PU_PD_H19	Configure pullup (=1) or pulldown (=0) on H19.	R/W	0x0
16	CONF_PU_PD_H20	Configure pullup (=1) or pulldown (=0) on H20.	R/W	0x0
15	CONF_PU_PD_H18	Configure pullup (=1) or pulldown (=0) on H18.	R/W	0x0
14	CONF_PU_PD_H15	Configure pullup (=1) or pulldown (=0) on H15.	R/W	0x0
13	CONF_PU_PD_G21	Configure pullup (=1) or pulldown (=0) on G21.	R/W	0x0
12	CONF_PU_PD_G20	Configure pullup (=1) or pulldown (=0) on G20.	R/W	0x0

Table 43. Pullup/Pulldown Selection 0 Register (PU_PD_SEL_0) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xB4				
Bit	**Name**	**Function**	**R/W**	**Reset**
11	RESERVED	Reserved for future expansion.	R/W	0x0
10	CONF_PU_PD_G18	Configure pullup (=1) or pulldown (=0) on G18.	R/W	0x0
9	CONF_PU_PD_F19	Configure pullup (=1) or pulldown (=0) on F19.	R/W	0x0
8	CONF_PU_PD_H14	Configure pullup (=1) or pulldown (=0) on H14.	R/W	0x0
7	CONF_PU_PD_E20	Configure pullup (=1) or pulldown (=0) on E20.	R/W	0x0
6	CONF_PU_PD_E19	Configure pullup (=1) or pulldown (=0) on E19.	R/W	0x0
5	CONF_PU_PD_F18	Configure pullup (=1) or pulldown (=0) on F18.	R/W	0x0
4	CONF_PU_PD_D20	Configure pullup (=1) or pulldown (=0) on D20.	R/W	0x0
3	CONF_PU_PD_D19	Configure pullup (=1) or pulldown (=0) on D19.	R/W	0x0
2	CONF_PU_PD_E18	Configure pullup (=1) or pulldown (=0) on E18.	R/W	0x0
1	CONF_PU_PD_C21	Configure pullup (=1) or pulldown (=0) on C21.	R/W	0x0
0	CONF_PU_PD_G19	Configure pullup (=1) or pulldown (=0) on G19.	R/W	0x0

This register controls the selection of the pullup or pulldown (0 = pulldown, 1 = pullup). The pinout documentation (SPRS231) must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control the selection.

Table 44. Pullup/Pulldown Selection 1 Register (PU_PD_SEL_1)

Base Address = 0xFFFE 1000, Offset Address = 0xB8				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PU_PD_AA20	Configure pullup (=1) or pulldown (=0) on AA20.	R/W	0x0
30	CONF_PU_PD_U20	Configure pullup (=1) or pulldown (=0) on U20.	R/W	0x0
29	CONF_PU_PD_W16	Configure pullup (=1) or pulldown (=0) on W16.	R/W	0x0
28	CONF_PU_PD_W13	Configure pullup (=1) or pulldown (=0) on W13.	R/W	0x0
27	CONF_PU_PD_J20	Configure pullup (=1) or pulldown (=0) on J20.	R/W	0x0
26	CONF_PU_PD_W17	Configure pullup (=1) or pulldown (=0) on W17.	R/W	0x0
25	CONF_PU_PD_V16	Configure pullup (=1) or pulldown (=0) on V16.	R/W	0x0

Table 44. Pullup/Pulldown Selection 1 Register (PU_PD_SEL_1) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xB8				
Bit	**Name**	**Function**	**R/W**	**Reset**
24	CONF_PU_PD_Y12	Configure pullup (=1) or pulldown (=0) on Y12.	R/W	0x0
23	CONF_PU_PD_W19	Configure pullup (=1) or pulldown (=0) on W19.	R/W	0x0
22	CONF_PU_PD_P15	Configure pullup (=1) or pulldown (=0) on P15.	R/W	0x0
21	CONF_PU_PD_N14	Configure pullup (=1) or pulldown (=0) on N14.	R/W	0x0
20	CONF_PU_PD_V19	Configure pullup (=1) or pulldown (=0) on V19.	R/W	0x0
19	CONF_PU_PD_W21	Configure pullup (=1) or pulldown (=0) on W21.	R/W	0x0
18	CONF_PU_PD_U18	Configure pullup (=1) or pulldown (=0) on U18.	R/W	0x0
17	Reserved	Reserved.	R/W	0x0
16	Reserved	Reserved.	R/W	0x0
15	CONF_PU_PD_U19	Configure pullup (=1) or pulldown (=0) on U19.	R/W	0x0
14	CONF_PU_PD_N15	Configure pullup (=1) or pulldown (=0) on N15.	R/W	0x0
13	CONF_PU_PD_T19	Configure pullup (=1) or pulldown (=0) on T19.	R/W	0x0
12	CONF_PU_PD_T20	Configure pullup (=1) or pulldown (=0) on T20.	R/W	0x0
11	CONF_PU_PD_R18	Configure pullup (=1) or pulldown (=0) on R18.	R/W	0x0
10	CONF_PU_PD_R19	Configure pullup (=1) or pulldown (=0) on R19.	R/W	0x0
9	CONF_PU_PD_M14	Configure pullup (=1) or pulldown (=0) on M14.	R/W	0x0
8	CONF_PU_PD_P18	Configure pullup (=1) or pulldown (=0) on P18.	R/W	0x0
7	CONF_PU_PD_P20	Configure pullup (=1) or pulldown (=0) on P20.	R/W	0x0
6	CONF_PU_PD_P19	Configure pullup (=1) or pulldown (=0) on P19.	R/W	0x0
5	CONF_PU_PD_M15	Configure pullup (=1) or pulldown (=0) on M15.	R/W	0x0
4	CONF_PU_PD_N20	Configure pullup (=1) or pulldown (=0) on N20.	R/W	0x0
3	CONF_PU_PD_N18	Configure pullup (=1) or pulldown (=0) on N18.	R/W	0x0
2	CONF_PU_PD_N19	Configure pullup (=1) or pulldown (=0) on N19.	R/W	0x0
1	CONF_PU_PD_N21	Configure pullup (=1) or pulldown (=0) on N21.	R/W	0x0
0	CONF_PU_PD_M20	Configure pullup (=1) or pulldown (=0) on M20.	R/W	0x0

This register controls the selection of the pullup or pulldown (0 = pulldown, 1 = pullup). The pinout documentation must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control the selection.

Table 45. Pullup/Pulldown Selection 2 Register (PU_PD_SEL_2)

Base Address = 0xFFFE 1000, Offset Address = 0xBC				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PU_PD_AA5	Configure pullup (=1) or pulldown (=0) on AA5.	R/W	0x0
30	CONF_PU_PD_W6	Configure pullup (=1) or pulldown (=0) on W6.	R/W	0x0
29	CONF_PU_PD_Y6	Configure pullup (=1) or pulldown (=0) on Y6.	R/W	0x0
28	CONF_PU_PD_V7	Configure pullup (=1) or pulldown (=0) on V7.	R/W	0x0
27	CONF_PU_PD_W7	Configure pullup (=1) or pulldown (=0) on W7.	R/W	0x0
26	CONF_PU_PD_P10	Configure pullup (=1) or pulldown (=0) on P10.	R/W	0x0
25	CONF_PU_PD_V8	Configure pullup (=1) or pulldown (=0) on V8.	R/W	0x0
24	CONF_PU_PD_Y8	Configure pullup (=1) or pulldown (=0) on Y8.	R/W	0x0
23	CONF_PU_PD_W8	Configure pullup (=1) or pulldown (=0) on W8.	R/W	0x0
22	CONF_PU_PD_R10	Configure pullup (=1) or pulldown (=0) on R10.	R/W	0x0
21	CONF_PU_PD_V5	Configure pullup (=1) or pulldown (=0) on V5.	R/W	0x0
20	CONF_PU_PD_V9	Configure pullup (=1) or pulldown (=0) on V9.	R/W	0x0
19	CONF_PU_PD_W9	Configure pullup (=1) or pulldown (=0) on W9.	R/W	0x0
18	CONF_PU_PD_AA9	Configure pullup (=1) or pulldown (=0) on AA9.	R/W	0x0
17	CONF_PU_PD_Y10	Configure pullup (=1) or pulldown (=0) on Y10.	R/W	0x0
16	CONF_PU_PD_R11	Configure pullup (=1) or pulldown (=0) on R11.	R/W	0x0
15	CONF_PU_PD_P11	Configure pullup (=1) or pulldown (=0) on P11.	R/W	0x0
14	CONF_PU_PD_V10	Configure pullup (=1) or pulldown (=0) on V10.	R/W	0x0
13	CONF_PU_PD_V11	Configure pullup (=1) or pulldown (=0) on V11.	R/W	0x0
12	CONF_PU_PD_W10	Configure pullup (=1) or pulldown (=0) on W10.	R/W	0x0
11	CONF_PU_PD_P13	Configure pullup (=1) or pulldown (=0) on P13.	R/W	0x0
10	CONF_PU_PD_R13	Configure pullup (=1) or pulldown (=0) on R13.	R/W	0x0

Table 45. Pullup/Pulldown Selection 2 Register (PU_PD_SEL_2) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xBC				
Bit	**Name**	**Function**	**R/W**	**Reset**
9	CONF_PU_PD_V15	Configure pullup (=1) or pulldown (=0) on V15.	R/W	0x0
8	CONF_PU_PD_P14	Configure pullup (=1) or pulldown (=0) on P14.	R/W	0x0
7	CONF_PU_PD_AA17	Configure pullup (=1) or pulldown (=0) on AA17.	R/W	0x0
6	CONF_PU_PD_Y15	Configure pullup (=1) or pulldown (=0) on Y15.	R/W	0x0
5	CONF_PU_PD_W15	Configure pullup (=1) or pulldown (=0) on W15.	R/W	0x0
4	CONF_PU_PD_W14	Configure pullup (=1) or pulldown (=0) on W14.	R/W	0x0
3	CONF_PU_PD_Y14	Configure pullup (=1) or pulldown (=0) on Y14.	R/W	0x0
2	CONF_PU_PD_V14	Configure pullup (=1) or pulldown (=0) on V14.	R/W	0x0
1	CONF_PU_PD_R14	Configure pullup (=1) or pulldown (=0) on R14.	R/W	0x0
0	CONF_PU_PD_AA15	Configure pullup (=1) or pulldown (=0) on AA15.	R/W	0x0

This register controls the selection of the pullup or pulldown (0 = pulldown, 1 = pullup). The pinout documentation (Application Processor Data Manual (SPRS231)) must be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control the selection.

Table 46. Pullup/Pulldown Selection 3 Register (PU_PD_SEL_3)

Base Address = 0xFFFE 1000, Offset Address = 0xC0				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PU_PD_W2	Configure pullup (=1) or pulldown (=0) on W2.	R/W	0X0
30	CONF_PU_PD_V4	Configure pullup (=1) or pulldown (=0) on V4.	R/W	0X0
29	CONF_PU_PD_Y1	Configure pullup (=1) or pulldown (=0) on Y1.	R/W	0X0
28	CONF_PU_PD_Y17	Configure pullup (=1) or pulldown (=0) on Y17.	R/W	0X0
27	CONF_PU_PD_D18	Configure pullup (=1) or pulldown (=0) on D18.	R/W	0X0
26	CONF_PU_PD_B21	Configure pullup (=1) or pulldown (=0) on B21.	R/W	0X0
25	CONF_PU_PD_C19	Configure pullup (=1) or pulldown (=0) on C19.	R/W	0X0
24	CONF_PU_PD_G14	Configure pullup (=1) or pulldown (=0) on G14.	R/W	0X0
23	CONF_PU_PD_H13	Configure pullup (=1) or pulldown (=0) on H13.	R/W	0X0

Table 46. Pullup/Pulldown Selection 3 Register (PU_PD_SEL_3) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xC0				
Bit	**Name**	**Function**	**R/W**	**Reset**
22	CONF_PU_PD_A20	Configure pullup (=1) or pulldown (=0) on A20.	R/W	0X0
21	CONF_PU_PD_B19	Configure pullup (=1) or pulldown (=0) on B19.	R/W	0X0
20	CONF_PU_PD_C18	Configure pullup (=1) or pulldown (=0) on C18.	R/W	0X0
19	Reserved	Reserved.	R/W	0X0
18	CONF_PU_PD_D17	Configure pullup (=1) or pulldown (=0) on D17.	R/W	0X0
17	CONF_PU_PD_D16	Configure pullup (=1) or pulldown (=0) on D16.	R/W	0X0
16	CONF_PU_PD_C17	Configure pullup (=1) or pulldown (=0) on C17.	R/W	0X0
15	CONF_PU_PD_B17	Configure pullup (=1) or pulldown (=0) on B17.	R/W	0X0
14	CONF_PU_PD_G13	Configure pullup (=1) or pulldown (=0) on G13.	R/W	0X0
13	CONF_PU_PD_A17	Configure pullup (=1) or pulldown (=0) on A17.	R/W	0X0
12	CONF_PU_PD_C16	Configure pullup (=1) or pulldown (=0) on C16.	R/W	0X0
11	CONF_PU_PD_D15	Configure pullup (=1) or pulldown (=0) on D15.	R/W	0X0
10	Reserved	Reserved.	R/W	0X0
9	Reserved	Reserved.	R/W	0X0
8	CONF_PU_PD_W11	Configure pullup (=1) or pulldown (=0) on W11.	R/W	0x0
7	Reserved	Reserved.	R/W	0x0
6	CONF_PU_PD_M4	Configure pullup (=1) or pulldown (=0) on M4.	R/W	0x0
5	CONF_PU_PD_W4	Configure pullup (=1) or pulldown (=0) on W4.	R/W	0x0
4	CONF_PU_PD_Y4	Configure pullup (=1) or pulldown (=0) on Y4.	R/W	0x0
3	CONF_PU_PD_V6	Configure pullup (=1) or pulldown (=0) on V6.	R/W	0x0
2	CONF_PU_PD_W5	Configure pullup (=1) or pulldown (=0) on W5.	R/W	0x0
1	CONF_PU_PD_Y5	Configure pullup (=1) or pulldown (=0) on Y5.	R/W	0x0
0	CONF_PU_PD_R9	Configure pullup (=1) or pulldown (=0) on R9.	R/W	0x0

This register controls the selection of the pullup or pulldown (0 = pulldown, 1 = pullup). The pinout documentation in SPRS231 should be consulted to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control the selection.

Table 47. Pullup/Pulldown Selection 4 Register (PU_PD_SEL_4)

Base Address = 0xFFFE 1000, Offset Address = 0xC4				
Bit	**Name**	**Function**	**R/W**	**Reset**
31	CONF_PU_PD_Y18	Configure pullup (=1) or pulldown (=0) on Y18.	R/W	0X0
30	CONF_PU_PD_W18	Configure pullup (=1) or pulldown (=0) on W18.	R/W	0X0
29	CONF_PU_PD_V17	Configure pullup (=1) or pulldown (=0) on V17.	R/W	0X0
28	CONF_PU_PD_Y19	Configure pullup (=1) or pulldown (=0) on Y19.	R/W	0X0
27	CONF_PU_PD_V18	Configure pullup (=1) or pulldown (=0) on V18.	R/W	0X0
26	CONF_PU_PD_L3	Configure pullup (=1) or pulldown (=0) on L3.	R/W	0x0
25	CONF_PU_PD_M8	Configure pullup (=1) or pulldown (=0) on M8.	R/W	0x0
24	CONF_PU_PD_M7	Configure pullup (=1) or pulldown (=0) on M7.	R/W	0x0
23	CONF_PU_PD_M3	Configure pullup (=1) or pulldown (=0) on M3.	R/W	0x0
22	CONF_PU_PD_N8	Configure pullup (=1) or pulldown (=0) on N8.	R/W	0x0
21	CONF_PU_PD_N3	Configure pullup (=1) or pulldown (=0) on N3.	R/W	0X0
20	CONF_PU_PD_J8	Configure pullup (=1) or pulldown (=0) on J8.	R/W	0x0
19	CONF_PU_PD_D3	Configure pullup (=1) or pulldown (=0) on D3.	R/W	0x0
18	CONF_PU_PD_C1	Configure pullup (=1) or pulldown (=0) on C1.	R/W	0x0
17	CONF_PU_PD_E4	Configure pullup (=1) or pulldown (=0) on E4.	R/W	0x0
16	CONF_PU_PD_D2	Configure pullup (=1) or pulldown (=0) on D2.	R/W	0x0
15	CONF_PU_PD_F4	Configure pullup (=1) or pulldown (=0) on F4.	R/W	0x0
14	CONF_PU_PD_E3	Configure pullup (=1) or pulldown (=0) on E3.	R/W	0x0
13	CONF_PU_PD_J7	Configure pullup (=1) or pulldown (=0) on J7.	R/W	0x0
12	CONF_PU_PD_F3	Configure pullup (=1) or pulldown (=0) on F3.	R/W	0x0
11	CONF_PU_PD_G4	Configure pullup (=1) or pulldown (=0) on G4.	R/W	0x0
10	CONF_PU_PD_G3	Configure pullup (=1) or pulldown (=0) on G3.	R/W	0X0

Table 47. Pullup/Pulldown Selection 4 Register (PU_PD_SEL_4) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0xC4				
Bit	**Name**	**Function**	**R/W**	**Reset**
9	CONF_PU_PD_G2	Configure pullup (=1) or pulldown (=0) on G2.	R/W	0X0
8	CONF_PU_PD_K8	Configure pullup (=1) or pulldown (=0) on K8.	R/W	0X0
7	CONF_PU_PD_H4	Configure pullup (=1) or pulldown (=0) on H4.	R/W	0X0
6	CONF_PU_PD_H3	Configure pullup (=1) or pulldown (=0) on H3.	R/W	0X0
5	CONF_PU_PD_K7	Configure pullup (=1) or pulldown (=0) on K7.	R/W	0X0
4	CONF_PU_PD_L4	Configure pullup (=1) or pulldown (=0) on L4.	R/W	0X0
3	CONF_PU_PD_V2	Configure pullup (=1) or pulldown (=0) on V2.	R/W	0X0
2	CONF_PU_PD_P3	Configure pullup (=1) or pulldown (=0) on P3.	R/W	0X0
1	CONF_PU_PD_U4	Configure pullup (=1) or pulldown (=0) on U4.	R/W	0X0
0	CONF_PU_PD_W1	Configure pullup (=1) or pulldown (=0) on W1.	R/W	0X0

This register controls the selection of the pullup or pulldown (0 = pulldown, 1 = pullup). Consult the pinout section of the Application Processor Data Manual (SPRS231) to determine whether a pullup or pulldown exists on the specified I/O. COMP_MODE_CTRL_0 must be programmed to 0xEAEF for this register to control the selection.

Table 48. Module Configuration Control 1 Register (MOD_CONF_CTRL_1)

Base Address = 0xFFFE 1000, Offset Address = 0x110					
Bit	**Name**	**Value**	**Function**	**R/W**	**Reset**
31	CONF_CAM_CLKMUX_R		Selection of camera_interface clock (MCLK) between ARMXOR and CAM_MCKO. Note: Reserved for TMS (production) devices. It is recommended that this bit be set to 0.	R/W	0x0
		0	Corresponds to ARMXOR clock from OMAP3.2.		
		1	Corresponds to CAM_MCKO from ULPD module.		

Table 48. Module Configuration Control 1 Register (MOD_CONF_CTRL_1) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x110					
Bit	**Name**	**Value**	**Function**	**R/W**	**Reset**
30:29	CONF_PMT_DCB_ SELECT_R		Generates the selection signal for the multiplexer in OMAP3.2 for observability of DLL output bus (DCB[7:0]).	R/W	0x0
		00 10	Observe DCB bus from URD_DLL.		
		01 11	Observe DCB bus from WRQ_DLL.		
28	CONF_OSC1_GZ_R		Disables oscillator. See Table 49.	R/W	0x0
			0: 12-MHz oscillator GZ pin is not activated. 1: 12-MHz oscillator GZ pin is activated (oscillator is disabled).		
27	CONF_OSC1_PWRDN_R		See Table 49.	R/W	0x0
			0: 12-MHz oscillator is not powered-down (uses crystal).		
			1: 12-MHZ PWRDN pin is activated.		
26	RESERVED		Reserved	R/W	0x1
25	OCP_INTERCON_ GATE_EN_R		This bit enables the OCP interconnect to use its autoidle feature on OCP interface.	R/W	0x1
24	CONF_MMC2_CLKFB_ SEL_R		This bit selects clock feedback into MMC/SDIO.	R/W	0x0
			0: Output clock from MMC/SDIO is feedback. 1: Feedback comes from pad.		
23	RESERVED		Reserved	R/W	0x1
22	CONF_MCBSP3_CLK_ DIS_R		This bit enables the McBSP3 interface clock.	R/W	0x0
			0: McBSP3 clock is enabled. 1: McBSP3 clock is disabled.		

Table 48. Module Configuration Control 1 Register (MOD_CONF_CTRL_1) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x110					
Bit	**Name**	**Value**	**Function**	**R/W**	**Reset**
21	CONF_MCBSP2_CLK_DIS_R		This bit enables the McBSP2 interface clock.	R/W	0x0
		0	McBSP2 clock is enabled.		
		1	McBSP2 clock is disabled.		
20	CONF_MCBSP1_CLK_DIS_R		This bit enables the McBSP1 interface clock.	R/W	0x0
		0	McBSP1 clock is enabled.		
		1	McBSP1 clock is disabled.		
19:17	RESERVED		Reserved	R/W	0x2
16	RESERVED		Reserved	R/W	0x0 or 0x1
15:14	CONF_MOD_GPTIMER8_CLK_SEL_R		This register selects the clock source for general-purpose timer 8.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		
13:12	CONF_MOD_GPTIMER7_CLK_SEL_R		This register selects the clock source for general-purpose timer 7.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		
11:10	CONF_MOD_GPTIMER6_CLK_SEL_R		This register selects the clock source for general-purpose timer 6.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		

Table 48. Module Configuration Control 1 Register (MOD_CONF_CTRL_1) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x110					
Bit	**Name**	**Value**	**Function**	**R/W**	**Reset**
9:8	CONF_MOD_GPTIMER5_CLK_SEL_R		This register selects the clock source for general-purpose timer 5.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		
7:6	CONF_MOD_GPTIMER4_CLK_SEL_R		This register selects the clock source for general-purpose timer 4.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use.		
5:4	CONF_MOD_GPTIMER3_CLK_SEL_R		This register selects the clock source for general-purpose timer 3.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		
3:2	CONF_MOD_GPTIMER2_CLK_SEL_R		This register selects the clock source for general-purpose timer 2.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		
1:0	CONF_MOD_GPTIMER1_CLK_SEL_R		This register selects the clock source for general-purpose timer 1.	R/W	0x0
		00	ARMXOR_CLK		
		01	32-kHz clock		
		10	EXT_CLK of the device external timer clock		
		11	Reserved; do not use		

This register controls the module configuration of the device.

Table 49. GZ and PWRDN Bits in MOD_CONF_CTRL_1

CONF_OSC1_GZ_R	CONF_OSC1_PWRDN_R†	Comments
0	0	Normal operating mode w/internal bias resistor.
0	1	Normal operating mode w/disconnected internal bias resistor. Enables the use of an external square clock.
1	X	Oscillator disabled.

† In reset mode 1, the PWRDN bit is forced to 1.

Table 50. Configuration Status Register (CONF_STATUS)

Base Address = 0xFFFE 1000, Offset Address = 0x130				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:6	UNUSED	These bits are not implemented.	R	N/A
5:4	CONF_DEVICE_TYPE_R	Contains the status of the eFuses that determine the type of device. 00: Production (normal) device 01: Bad device 10: Emulator device 11: Test device	R	N/A
3	CONF_STATUS[3]	Contains the status of GPIO1 input pin. Value is latched on the rising edge of PWRON_RESET. For internal boot, software configures the external chip-select after reading this bit. For external boot, the external chip-select configuration is forced after reading this bit. 0: Nonaddress/data multiplexed 1: Address/data multiplexed	R	N/A
2	CONF_EMIFS_MUX_STAT_R	This bit contains information about EMIFS protocol at boot. 0: Nonaddress/data multiplexed 1: Address/data multiplexed Reset value for this signal depends on GPIO1, MPU_BOOT, and EFUSE_DEVICE_TYPE signals.	R	N/A

Table 50. Configuration Status Register (CONF_STATUS) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x130				
Bit	**Name**	**Function**	**R/W**	**Reset**
1	CONF_ARM_BOOT_STAT_R	This register contains boot mode active chip-select (CONF_ARM BOOT MODE), latched at the rising edge of PWRON_RESET. Emulator type devices only, 0: MPU boots from internal ROM 1: MPU boots from external memory Reset value for this signal depends on MPU_BOOT and EFUSE_DEVICE_TYPE signals.	R	N/A
0	CONF_RESET_MODE_STAT_R	This register contains the status of the RESET_MODE pin latched at the rising edge of the reset pin PWRON_RESET. 0: Reset mode 0 1: Reset mode 1	R	N/A

The actual reset value for all bits in this register depends on the device configuration at power-up reset. The values from the Reset column are not applicable.

The boot ROM code uses CONF_STATUS register bits to determine the execution path during boot time.

Table 51. Reset Control Register (RESET_CONTROL)

Base Address = 0xFFFE 1000, Offset Address = 0x140				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:7	UNUSED	Not implemented.	R	0x0000000
6	CONF_RNG_IDLE_MODE	RNGidle control. 0: RNGidle disabled 1: RNGidle enabled	R/W	0x1
5	CONF_CAMERAIF_RESET_R	This register controls reset of the camera IF. 0: Module is in reset. 1: Module is in functional mode.	R/W	0x1
4	CONF_UWIRE_RESET_R	This register controls reset of the µWire. 0: µWire is in reset. 1: µWire is in functional mode.	R/W	0x1

Table 51. Reset Control Register (RESET_CONTROL) (Continued)

Base Address = 0xFFFE 1000, Offset Address = 0x140				
Bit	**Name**	**Function**	**R/W**	**Reset**
3	CONF_OSTIMER_ RESET_R	This register controls reset of the OS timer. 0: OS timer is in reset. 1: OS timer is in functional mode.	R/W	0x1
2	CONF_ARMIO_RESET_R	This register controls reset of the MPUIO. 0: MPUIO is in reset. 1: MPUIO is in functional mode.	R/W	0x1
1	RESERVED	This bit should be set to 0.	R/W	0x1
0	CONF_OCP_RESET_R	This register controls reset of the OCP interconnect. 0: OCP interconnect is in reset. 1: OCP interconnect is in functional mode.	R/W	0x1

This register can be used for power management for the various modules listed in the bit fields above. These peripherals can be held under reset by this register.

Table 52. XOMAP5912 Configuration Control Register (CONF_5912_CTRL)

Base Address = 0xFFFE 1000, Offset Address = 0x150				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:16	RESERVED	Reserved	R	0x0000
15:4	RESERVED	Reserved	R/W	0x000
3	RESERVED	Reserved	R/W	0
2	RESERVED	This bit should be set to 0.	R/W	0
1	RESERVED	Reserved	R/W	1
0	RESERVED	Reserved	R/W	0

Table 53. OMAP5912 Configuration Control Register (CONF_5912_CTRL) Bit Descriptions

Base Address = 0xFFFE 1000, Offset Address = 0x150					
Bit	**Name**	**Value**	**Function**	**R/W**	**Reset**
31:16	RESERVED	0	Reserved	R	0x0000
15:8	SPARE_REGS	0	Reserved. Do not modify these bits.	R/W	0x0000
7	5912_SPI_MODE		Set the SPI multiplexing mode.	R/W	0x0
		0	Multi master support		
		1	Single master support (5912)		
6	CAMERA_T1/T2		Define OCP target souces of TI CAMERA	R/W	0x0
		0	TI camera is on OCP T1		
		1	TI camera is on OCP T2		
5	RESERVED		Reserved	R/W	0x0
4	ENABLE_FB_CLK		Power saving feature. This bit gates the frame buffer (FB) core when unused.		0x0
		0	FB clock is gated to save power.		
		1	FB clock is active.		
3	RESERVED		Reserved	R/W	0
2	RESERVED		This bit should be set to 0.	R/W	0
1	RESERVED		Reserved	R/W	1
0	RESERVED		Reserved		0

3 External Interfaces

This section describes the various external interfaces supported by this device. It also gives an overview of duplicated interfaces.

3.1 External Interface Descriptions

This device supports different classes of interfaces:

- Reset, clocks, and power management
- General-purpose input/output
- Keyboard interface
- General-purpose counter
- Memory interfaces
  - SDRAM interface
  - Mobile DDR interface
  - NOR flash interface (nonmultiplexed address/data and multiplexed address/data)
  - MMC/SD (1,2)
- Serial interfaces
  - SPI (master/slave)
  - μWire
  - McBSP (1,2,3)
  - MCSI (1,2)
  - I^2C (master/slave)
  - HDQ/1-Wire
  - UART (1,2,3)
  - USB On The Go (OTG)
    - 1 port with on-chip transceiver
    - 3 ports that can interface with external transceivers
- Camera interface
  - Parallel camera interface
- Display interface

- LCD interface

❑ Emulation

- JTAG

The user selects the appropriate interfaces for an application during the boot sequence. In effect, only a subset of all possible interfaces is available at power-on reset. For flexibility, some interfaces are duplicated. See the pinout section of the Application Processor Data Manual (SPRS231) to select the desired configuration.

3.2 Duplicated Interfaces

Table 54 provides an example of duplicated interfaces with the MMC/SDIO2. The software programs (via the appropriate FUNC_MUX_CTRL register) the desired configuration and ensures that no input/output is enabled twice.

Table 54. Example of Duplicated Interfaces

Ball	I/O Description	Mode
M19	MMC2.CLK	011
Y10	MMC2.CLK	110
R18	MMC2.CLKIN	110
J19	MMC2.CMD/SPI.DO	011
Y8	MMC2.CMD/SPI.DO	110
V9	MMC2.CMDDIR	110
L15	MMC2.DAT0/SPI.DI	011
W8	MMC2.DAT0/SPI.DI	110
L18	MMC2.DAT1	011
V8	MMC2.DAT1	110
J18	MMC2.DAT2	011
W15	MMC2.DAT2	110
L19	MMC2.DAT3	011
R10	MMC2.DAT3	110
V5	MMC2.DATDIR0	110
W19	MMC2.DATDIR1	110

Table 55 indicates the interfaces after programming the configuration registers.

Table 55. Configuration After Programming

Ball	I/O Description	Mode
Y10	MMC2.CLK	110
Y8	MMC2.CMD/SPI.DO	110
V9	MMC2.CMDDIR	110
W8	MMC2.DAT0/SPI.DI	110
V8	MMC2.DAT1	110
R10	MMC2.DAT3	110
V5	MMC2.DATDIR0	110
W19	MMC2.DATDIR1	110
L15	ETM_PSTAT[1]	001
L18	ETM_PSTAT[2]	001
M19	ETM_PSTAT[0]	001
J19	ETM_D[6]	001
J18	ETM_D[7]	001
L19	ETM_D[0]	001

4 OMAP Device Identification Registers

The following registers are chip revision registers for the device. Reset values depend on the device are are listed in the tables as unknown.

Table 56. OMAP Die ID Register (OMAP_DIE_ID_0)

Address = 0xFFFE 1800				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:0	RESERVED	Reserved for special identification.	R	U

Table 57. OMAP Die ID Register (OMAP_DIE_ID_1)

Address = 0xFFFE 1804				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:21	RESERVED	Reserved for special identification.	R	U
20:17	DEV_REV	Device revision.	R	See Table 61
16:0	RESERVED	Reserved for special identification.	R	U

Table 58. OMAP Die ID Register (OMAP_PRODUCTION_ID_0)

Address = 0xFFFE 2000				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:30	SECURITY	Security device type. 00: General-purpose device type (GP)	R	U
29:25	RESERVED	Reserved.	R	U
24:9	ID_KEY	Reserved for special identification.	R	0x5555
8	SP	Secure protect.	R	U
7	WA	DFT write MPU. MPU DFT write value.	R	U
6	RA	DFT read MPU. MPU DFT read value.	R	U
5	WD	DFT write MGS3. MGS3 DFT write value.	R	U
4	RD	DFT read MGS3. MGS3 DFT read value.	R	U
3:2	NORMAL	00: Not a normal (production) device. 01,10,11: Normal device.	R	U
1:0	EMULATION	00: Not an emulation device. 01,10,11: Emulation device.	R	U

Table 59. OMAP Die ID Register (OMAP_PRODUCTION_ID_1)

Address = 0xFFFE 2004				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:17	RESERVED	Reserved.	R	U
16:1	PROD_ID	Prod ID.	R	See Table 61
0	RESERVED	Reserved.	R	U

Table 60. OMAP32_ID Register (OMAP32_ID)

Address = 0xFFFE D400				
Bit	**Name**	**Function**	**R/W**	**Reset**
31:0	OMAP32_ID	OMAP 3.2 device revision.	R	U

Some of the bit fields described above will change depending on the chip revision. Table 61 lists device revisions. Note that new revisions may exist. Please contact your TI representative for more information.

Table 61. Revision Table

Revision	Part #	PROD_ID	DEV_REV	OMAP32_ID
1.1	XOMAP5912B	0xB576	0x2	0x0332 0200
2.2	POMAP5912	0xB65F	0x2	0x0332 0500
2.2	OMAP5912B	0xB65F	0x2	0x0332 0500

Revision History

The table below lists the changes made since the previous version of this document.

Location	Additions, Modifications, Deletions
84	Modified Table 48 by adding a note to Bit 31 and changing the reset value on bit 23 from 0x0 to 0x1.
90	Modified Table 52 by changing the name to *XOMAP5912 Configuration Control Register* to differentiate the silicon version
91	Added Table 53, *OMAP5912 Configuration Control Register*
18	Modified Figure 1 by removing Compact Flash Controller, and moving and connecting Camera I/F to OCP interconnect.
20	Modified Table 5 by removing the Camera I/F and CompactFlash controller from Class 2 Modules
28	Modified Table 6 by removing the Camera clock output row, changing CK_REF to ARMPER_CK/TC2_CK for SYS_CLK_OUT, and adding footnote.
91	Modified Table 53 by changing 1621 to 5912.
92	Modified section 3.1 by removing the bullets for CompactFlash interface and Trace interface
95	Removed the *Reset/Boot Overview* chapter before Chapter 4, *OMAP Device Identification Registers*.

This page is intentionally left blank.