TMS320DM643x DMP
Pulse-Width Modulator (PWM) Peripheral

User's Guide

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Preface **5**
1 Introduction **6**
1.1 Purpose of the Peripheral 6
1.2 Features 6
1.3 Industry Standard(s) Compliance Statement 6
2 Peripheral Architecture **7**
2.1 Clock Control 7
2.2 Signal Descriptions 7
2.3 Functional Operation 8
2.4 Pin Multiplexing 11
2.5 Reset Considerations 11
2.6 Initialization 11
2.7 Interrupt Support 11
2.8 EDMA Event Support 11
2.9 Power Management 12
2.10 Emulation Considerations 12
3 Registers **12**
3.1 Pulse Width Modulator (PWM) Peripheral Identification Register (PID) 13
3.2 Pulse Width Modulator (PWM) Peripheral Control Register (PCR) 13
3.3 Pulse Width Modulator (PWM) Configuration Register (CFG) 14
3.4 Pulse Width Modulator (PWM) Start Register (START) 15
3.5 Pulse Width Modulator (PWM) Repeat Count Register (RPT) 15
3.6 Pulse Width Modulator (PWM) Period Register (PER) 16
3.7 Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D) 16
Appendix A Revision History **17**

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List of Figures

1 PWM Waveform Polarity Control (PWM_RPT = 2, for 3 periods) 7
2 PWM One-Shot Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 0, PWM_RPT = 2) 8
3 PWM Event-Triggered One-Shot Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 1, PWM_RPT = 1) 9
4 PWM Continuous Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 1, PWM_RPT = 0) 10
5 Pulse Width Modulator (PWM) Peripheral Identification Register (PID) 13
6 Pulse Width Modulator (PWM) Peripheral Control Register (PCR) 13
7 Pulse Width Modulator (PWM) Configuration Register (CFG) 14
8 Pulse Width Modulator (PWM) Start Register (START) 15
9 Pulse Width Modulator (PWM) Repeat Count Register (RPT) 15
10 Pulse Width Modulator (PWM) Period Register (PER) 16
11 Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D) 16

List of Tables

1 Pulse Width Modulator (PWM) Registers 12
2 Pulse Width Modulator (PWM) Peripheral Identification Register (PID) Field Descriptions 13
3 Pulse Width Modulator (PWM) Peripheral Control Register (PCR) Field Descriptions 13
4 Pulse Width Modulator (PWM) Configuration Register (CFG) Field Descriptions 14
5 Pulse Width Modulator (PWM) Start Register (START) Field Descriptions 15
6 Pulse Width Modulator (PWM) Repeat Count Register (RPT) Field Descriptions 15
7 Pulse Width Modulator (PWM) Period Register (PER) Field Descriptions 16
8 Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D) Field Descriptions 16
9 Document Revision History 17

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Read This First

About This Manual

This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM643x Digital Media Processor (DMP).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM643x Digital Media Processor (DMP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM643x DMP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRU978 — *TMS320DM643x DMP DSP Subsystem Reference Guide.* Describes the digital signal processor (DSP) subsystem in the TMS320DM643x Digital Media Processor (DMP).

SPRU983 — *TMS320DM643x DMP Peripherals Overview Reference Guide.* Provides an overview and briefly describes the peripherals available on the TMS320DM643x Digital Media Processor (DMP).

SPRAA84 — *TMS320C64x to TMS320C64x+ CPU Migration Guide.* Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — *TMS320C64x+ DSP Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

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Pulse-Width Modulator (PWM) Peripheral

1 Introduction

This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM643x Digital Media Processor (DMP).

1.1 Purpose of the Peripheral

The pulse-width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable.

1.2 Features

The PWM has the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- Configurable to operate in either one-shot mode, which generates a single interrupt at the end of operation, or continuous mode, which generates an interrupt per period.
- 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value.
- One-shot operation can be triggered by the CCD VSYNC output of the video processing subsystem to allow any of the PWM instantiations to be used as a CCD timer.
- Configurable PWM output pin inactive state.
- Interrupt and EDMA synchronization events.
- Emulation support for stop or free-run operation.

1.3 Industry Standard(s) Compliance Statement

The PWM does not conform to any recognized industry standards.

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2 Peripheral Architecture

2.1 Clock Control

The PWM peripheral is driven by the equivalent of the DM643x input clock. This clock is normally 27 MHz and is not affected by the configuration of the PLLs. The PWM timer counts are referenced to this clock.

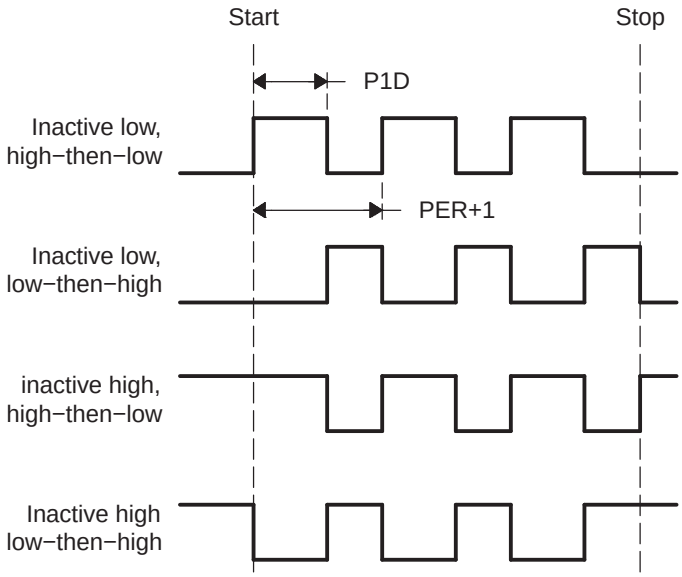
2.2 Signal Descriptions

Each instance of the PWM peripheral has a single output signal, PWM*n*. The output signal is driven based on the state of the PWM as described below:

- **Inactive state**: When the PWM is idle, the output pin is driven to its inactive output level. This inactive logic state is determined by configuring the INACTOUT bit in the PWM configuration register (CFG).
- **First-phase active state**: During the first phase of an active PWM period, the output signal is driven to the state defined in the P1OUT bit in the PWM configuration register (CFG). The duration of the first phase is controlled by the PWM first-phase duration register (PH1D). The duration of the entire period is controlled by the PWM period register (PER).
- **Second-phase active state**: After the first phase of the period is complete, the output signal is driven to the opposite state of the first phase for the remainder of the period (the second phase).

Figure 1 shows the behavior of PWM*n* with different combination of active and inactive polarities.

Figure 1. PWM Waveform Polarity Control (PWM_RPT = 2, for 3 periods)



If PH1D value is 0, the first phase has zero time and the opposite of the first-phase output value is driven on PWM*n* for the entire period. If PH1D is greater than or equal to (PER + 1), the first phase is 100% of the period and the P1OUT output level is sent for the duration of the period.

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2.3 Functional Operation

The PWM module can operate in either one-shot or continuous mode. In both modes, the PWM peripheral has a first-phase duration register (PH1D) and a period register (PER) to specify, respectively, the first-phase duration and period of the waveform. The first-phase output level can be configured to be either high or low in the P1OUT bit of the PWM configuration register (CFG) and the second phase output is automatically the opposite polarity of the first-phase level. The inactive state before and after the PWM operation can also be configured to be either a 0 or a 1 in the INACTOUT bit of CFG. For one-shot mode operation, see Section 2.3.1; for continuous mode operation, see Section 2.3.2.

2.3.1 One-Shot Mode Operation

In one-shot mode operation, the PWM produces a series of periods but does not run continuously. The number of periods in the series is controlled by the repeat count contained in the PWM repeat count register (RPT). To select one-shot mode, configure the MODE bit in the PWM configuration register (CFG) to 1h.

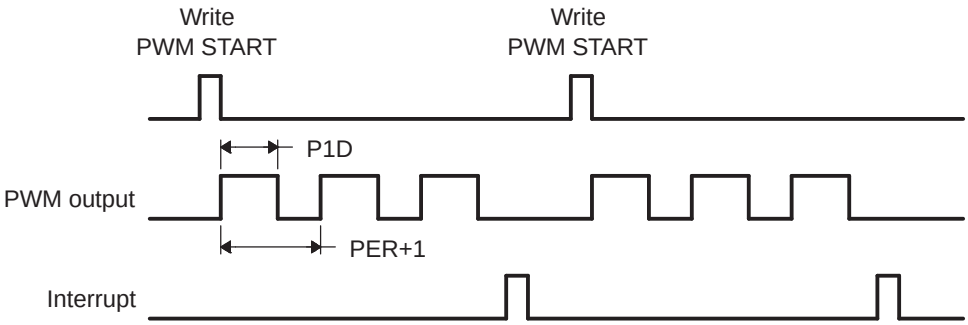
For one-shot mode operation, the PWM should first be configured for mode, period, and first-phase duration, along with other configuration options. The PWM uses the last programmed set of parameters once it is started by writing a 1 to the START bit in the PWM start register (START).

Once started, the PWM asserts/deasserts the output as configured, driving to the first-phase output level during the first phase and the opposite level during the second phase. When the prescribed number of RPT + 1 periods of pulses expire, the peripheral sends an interrupt to the system (if the interrupt is enabled in CFG). The PWM then becomes inactive until the START bit is written a 1 again.

The PWM is stopped during one-shot mode operation by changing the MODE bit to 0 (disable). When the PWM is disabled, the output is immediately driven to the configured inactive state.

Figure 2 shows the one-shot mode operation. The waveform generation is started by writing to the START bit (assuming event triggering is disabled). After RPT + 1 number of periods, the waveform stops and an interrupt is generated. The polarity is configured as inactive low, first phase high-then-low.

Figure 2. PWM One-Shot Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 0, PWM_RPT = 2)



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2.3.1.1 Event-Triggered One-Shot Mode Operation

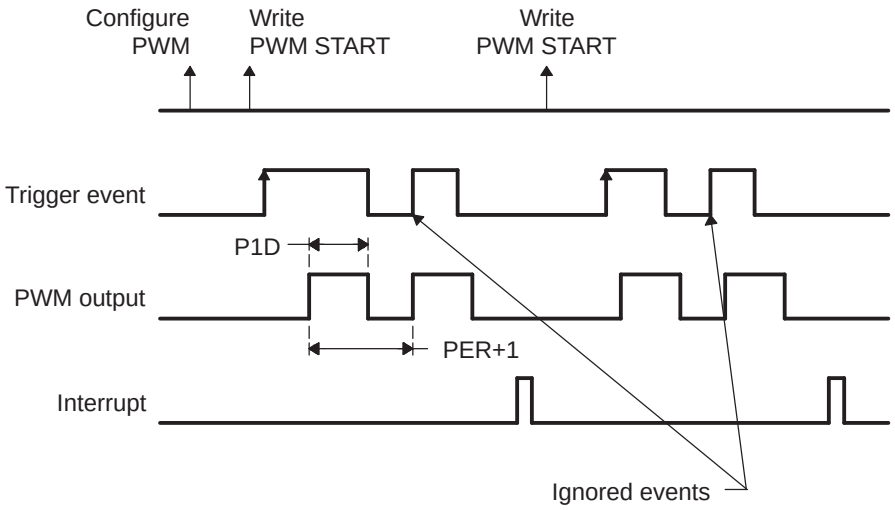
In one-shot mode, the PWM senses a rising or falling transition on an event-trigger input signal to start the operation. This event trigger input is synchronized to the PWM clock inside the module and is driven by the video processing subsystem CCDC_VD output signal. This capability is provided to allow the PWM to be used as a CCD timer.

The trigger event can be detected on the rising edge or the falling edge of CCDC_VD. After event triggering is enabled as part of the configuration process, a write to the PWM START register (START) starts the sensing circuitry in the PWM and after the first event, the PWM starts the period counting.

Figure 3 shows the event-triggered one-shot mode operation. Note that each subsequent event does not restart period counting. It takes another write to the START bit to sense the event signal again. Also note, that events received within the PWM period are ignored as well.

The PWM is stopped from the event-triggered one-shot mode operation by changing the MODE bit to 0 (disable). When the PWM is disabled, the output is immediately driven to the configured inactive state.

Figure 3. PWM Event-Triggered One-Shot Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 1, PWM_RPT = 1)



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2.3.2 Continuous Operation

In continuous mode operation, the PWM produces the repeating output waveforms continuously without stopping. For continuous mode operation, the PWM should first be configured for mode, period, and first-phase duration, along with other configuration options. The PWM uses the last programmed set of parameters once it is started by writing a 1 to the START bit in the PWM start register (START). Unlike the one-shot mode, the repeat count does not affect the continuous operation. To select continuous mode, configure the MODE bit in the PWM configuration register (CFG) to 2h.

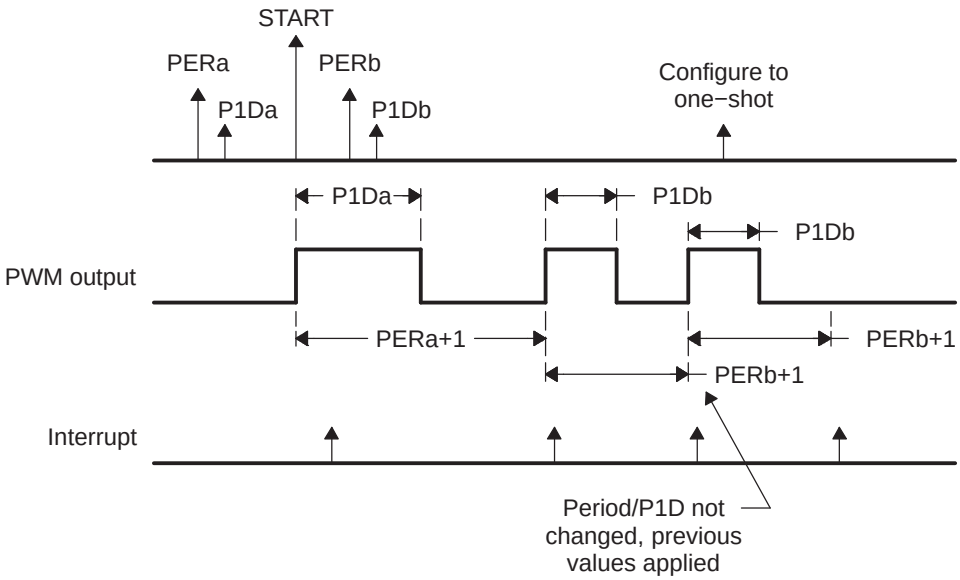
Once started, the PWM asserts/deasserts the output as configured, driving to first-phase output level during the first phase and the opposite level during the second phase. Once a period expires, the next period starts. When a period starts, the PWM copies the period and first-phase duration registers into a set of internal shadow registers and maintains the counts there. An interrupt is also generated (if enabled) after the registers are copied. This buffering scheme and interrupt timing allows the CPU or EDMA to program the durations for the next period while the current period is running.

The PWM is stopped during the continuous mode operation by either disabling it or by reconfiguring it to one-shot mode using the MODE bit. Whenever the PWM is disabled, the output is immediately driven to the configured inactive state. To allow the PWM to stop gracefully from continuous operation, upon an interrupt, configure the PWM to one-shot mode operation. The PWM then operates for RPT + 1 periods and stops by itself (sending an interrupt, if enabled). Note that unlike normal one-shot mode operation, another write to the START bit is not required for the one-shot mode operation to start.

While operating in continuous mode, the minimum period for the PWM is 8 cycles.

Figure 4 shows programming of period/first-phase-duration, and the resulting output waveform, and interrupt signal for continuous operation.

Figure 4. PWM Continuous Mode Operation (P1OUT = 1, INACTOUT = 0, EVTRIG = 1, PWM_RPT = 0)



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2.4 Pin Multiplexing

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the PWM.

2.5 Reset Considerations

2.5.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) causes the PWM peripheral registers to return to their default state after reset.

2.5.2 Hardware Reset Considerations

A hardware reset of the processor causes the PWM peripheral registers to return to their default values after reset.

2.6 Initialization

To initialize and start the PWM:

1. Perform the necessary device pin multiplexing setup (see the device-specific data manual).
2. Program the VDD3P3V_PWDN register in the System Module to power up the IO pins (see the device-specific data manual).
3. Write the desired period duration to the PWM period register (PER).
4. Write the desired first-phase duration to the PWM first-phase duration register (PH1D).
5. If one-shot mode will be used, write the desired repeat value to the PWM repeat count register (RPT).
6. Configure the operating mode, inactive output level, first-phase output level, and event trigger behavior in the PWM configuration register (CFG).
7. If interrupts will be used, enable interrupts in CFG.
8. Configure how the PWM responds to emulation suspend events in the PWM peripheral control register (PCR). See Section 2.10 for more information.
9. Start the PWM by writing a 1 to the START bit in the PWM start register (START).

2.7 Interrupt Support

There is a single interrupt from the CPU interrupt controller for each PWM instance.

When the PWM is configured in one-shot mode and the interrupt bit (INTEN) in the PWM configuration register (CFG) is enabled, the peripheral generates an interrupt when RPT + 1 number of periods have been completed.

When the PWM is configured in continuous mode and the interrupt bit (INTEN) in CFG is enabled, the PWM peripheral generates an interrupt every period after the first-phase duration register and period register values have been copied to the associated shadow registers. This event indicates it is safe to program the duration values for the next period.

2.7.1 Interrupt Multiplexing

The interrupts from the PWM peripheral instances are not multiplexed with any other interrupt sources on the DM643x DMP.

2.8 EDMA Event Support

The PWM provides EDMA synchronization events to allow the EDMA to update the values for the first-phase duration and period registers. The EDMA events occur at the same times as the interrupts previously described. For detailed information on EDMA synchronization events, see the device-specific data manual.

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2.9 Power Management

The PWM peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the PWM peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978).

When the PWM peripheral exits the power-down state, it will resume normal function (no register values are altered), but a write to the START bit in the PWM start register (START) is required to restart operation. If the PWM was configured to be event-triggered before power-down, a trigger event will also be required to restart the PWM after it exits the power-down state.

2.10 Emulation Considerations

The PWM implements a FREE bit in the PWM peripheral control register (PCR) to determine operation during an emulation stop. If FREE is set to 1, the PWM continues to run during an emulation stop; if FREE is cleared to 0 (default), then the following occurs:

- Suspend operation immediately.
- Freeze PWM output at its current state.
- Suspend internal counters.
- Suspend interrupt generation.
- Keep the event capture circuitry functional. If the PWM is configured for event-triggered operation and is waiting for an event, an event coming in during suspend is registered and the PWM period starts as soon as the emulation suspend is deasserted.

3 Registers

Table 1 lists the memory-mapped registers for the pulse-width modulator (PWM) controller. See the device-specific data manual for the memory addresses of these registers.

Table 1. Pulse Width Modulator (PWM) Registers

Offset	Acronym	Register Description	Section
0h	PID	PWM Peripheral Identification Register	Section 3.1
4h	PCR	PWM Peripheral Control Register	Section 3.2
8h	CFG	PWM Configuration Register	Section 3.3
Ch	START	PWM Start Register	Section 3.4
10h	RPT	PWM Repeat Count Register	Section 3.5
14h	PER	PWM Period Register	Section 3.6
18h	PH1D	PWM First-Phase Duration Register	Section 3.7

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3.1 Pulse Width Modulator (PWM) Peripheral Identification Register (PID)

The pulse-width modulator (PWM) peripheral identification register (PID) contains identification data (type, class, and revision) for the peripheral. PID is shown in Figure 5 and described in Table 2.

Figure 5. Pulse Width Modulator (PWM) Peripheral Identification Register (PID)

31	24	23	16
Reserved		TID	
R-42h		R-07h	

15	8	7	0
CID		REV	
R-11h		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 2. Pulse Width Modulator (PWM) Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Identifies type of peripheral.
15-8	CID	0-FFh	Identifies class of peripheral.
7-0	REV	0-FFh	Identifies revision of peripheral.

3.2 Pulse Width Modulator (PWM) Peripheral Control Register (PCR)

The pulse-width modulator (PWM) peripheral control register (PCR) is shown in Figure 6 and described in Table 3.

Figure 6. Pulse Width Modulator (PWM) Peripheral Control Register (PCR)

31	16
Reserved	
R-0	

15	1	0
Reserved		FREE
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. Pulse Width Modulator (PWM) Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	FREE		Free-running enable mode bit. This bit determines the behavior of the PWM when an emulation suspend event occurs (halt or breakpoint).
		0	The PWM stops immediately.
		1	Free-running mode is enabled; the PWM continues to run free.

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3.3 Pulse Width Modulator (PWM) Configuration Register (CFG)

The pulse-width modulator (PWM) configuration register (CFG) is shown in Figure 7 and described in Table 4.

Figure 7. Pulse Width Modulator (PWM) Configuration Register (CFG)

31	18	17	16
Reserved		OPST	CURLEV
R-0		R-0	R-0

15	7	6	5	4	3	2	1	0
Reserved		INTEN	INACTOUT	P1OUT	EVTRIG		MODE	
R-0		R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read; -*n* = value at reset

Table 4. Pulse Width Modulator (PWM) Configuration Register (CFG) Field Descriptions

Bit	Field	Value	Description
31-18	Reserved	0	Reserved
17	OPST		PWM operation status.
		0	Idle mode
		1	Running mode
16	CURLEV		PWM output status.
		0	Low
		1	High
15-7	Reserved	0	Reserved
6	INTEN		Interrupt enable.
		0	Disable interrupt
		1	Enable interrupt
5	INACTOUT		Inactive output level.
		0	Low
		1	High
4	P1OUT		First-phase output level.
		0	Low
		1	High
3-2	EVTRIG	0-3h	Event trigger.
		0	Disable
		1h	Positive edge triggered
		2h	Negative edge triggered
		3h	Reserved
1-0	MODE	0-3h	Operating mode.
		0	Disable
		1h	One shot mode
		2h	Continuous mode
		3h	Reserved

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3.4 Pulse Width Modulator (PWM) Start Register (START)

The pulse-width modulator (PWM) start register (START) is shown in Figure 8 and described in Table 5.

Figure 8. Pulse Width Modulator (PWM) Start Register (START)

31	16
Reserved	
R-0	

15	1	0
Reserved		START
R-0		W-0

LEGEND: R/W = Read/Write; W= Write only; -*n* = value after reset

Table 5. Pulse Width Modulator (PWM) Start Register (START) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	START		PWM start bit. Writing a 1 to this bit starts the PWM.
		0	No effect
		1	Start PWM.

3.5 Pulse Width Modulator (PWM) Repeat Count Register (RPT)

The pulse-width modulator (PWM) repeat count register (RPT) is shown in Figure 9 and described in Table 6.

Figure 9. Pulse Width Modulator (PWM) Repeat Count Register (RPT)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		RPT	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. Pulse Width Modulator (PWM) Repeat Count Register (RPT) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	RPT	0-FFh	One-shot mode repeat count is RPT + 1.

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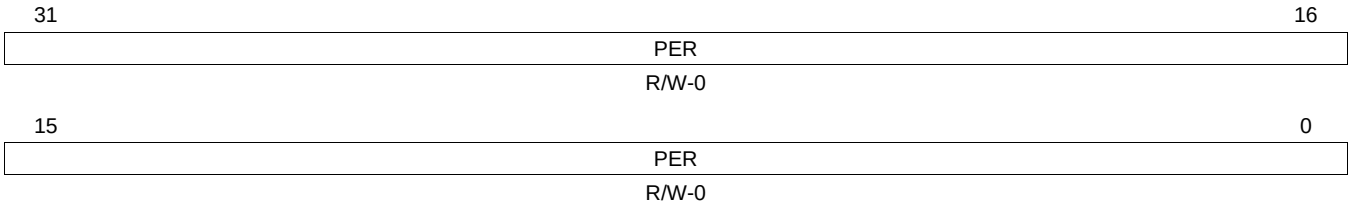
3.6 Pulse Width Modulator (PWM) Period Register (PER)

The pulse-width modulator (PWM) period register (PER) is shown in Figure 10 and described in Table 7.

Figure 10. Pulse Width Modulator (PWM) Period Register (PER)



LEGEND: R/W = Read/Write; *-n* = value after reset

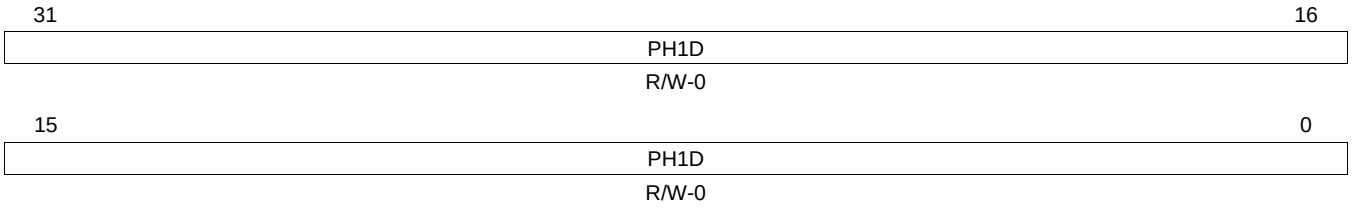
Table 7. Pulse Width Modulator (PWM) Period Register (PER) Field Descriptions

Bit	Field	Value	Description
31-0	PER	0-FFFF FFFFh	Output period is PER + 1 clock cycles.

3.7 Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D)

The pulse-width modulator (PWM) first-phase duration register (PH1D) is shown in Figure 11 and described in Table 8.

Figure 11. Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D)



LEGEND: R/W = Read/Write; *-n* = value after reset

Table 8. Pulse Width Modulator (PWM) First-Phase Duration Register (PH1D) Field Descriptions

Bit	Field	Value	Description
31-0	PH1D	0-FFFF FFFFh	First-phase duration is PH1D clock cycles.

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Appendix A Revision History

Table 9 lists the changes made since the previous version of this document.

Table 9. Document Revision History

Reference	Additions/Modifications/Deletions
Figure 5	Changed reset value for all bits.
Table 2	Changed table.

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