

TMS320DM36x

Digital Media System-on-Chip (DMSoC)

General-Purpose Input/Output (GPIO)

User's Guide



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Read This First

This document describes the General-Purpose Input/Output (GPIO) on the TMS320DM36x Digital Media System-on-Chip.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
 - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
 - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation from Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

[SPRUFG5](#) — *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

[SPRUFG8](#) — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide* This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

[SPRUFG9](#) — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide* This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

[SPRUFH0](#) — *TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide* This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

[SPRUFH1](#) — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide* This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

[SPRUFH2](#) — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide* This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

- [SPRUFH3](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.
- [SPRUFH5](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH6](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH7](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUFH8](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.
- [SPRUFH9](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.
- [SPRUF10](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.
- [SPRUF11](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.
- [SPRUF12](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.
- [SPRUF13](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.
- [SPRUF14](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF15](#) — TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide** This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

- [SPRUF17](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF18](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).
- [SPRUF19](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.
- [SPRUFJ0](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).
- [SPRUGG8](#)** — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*** This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

General-Purpose Input/Output (GPIO)

1 Introduction

The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

1.1 Purpose of the Peripheral

Most system-on-chip (SoC) devices require some general-purpose input/output (GPIO) functionality in order to interact with other components in the system using low-speed interface pins. The control and use of the GPIO capability on this device is grouped together in the GPIO peripheral and is described in the following sections.

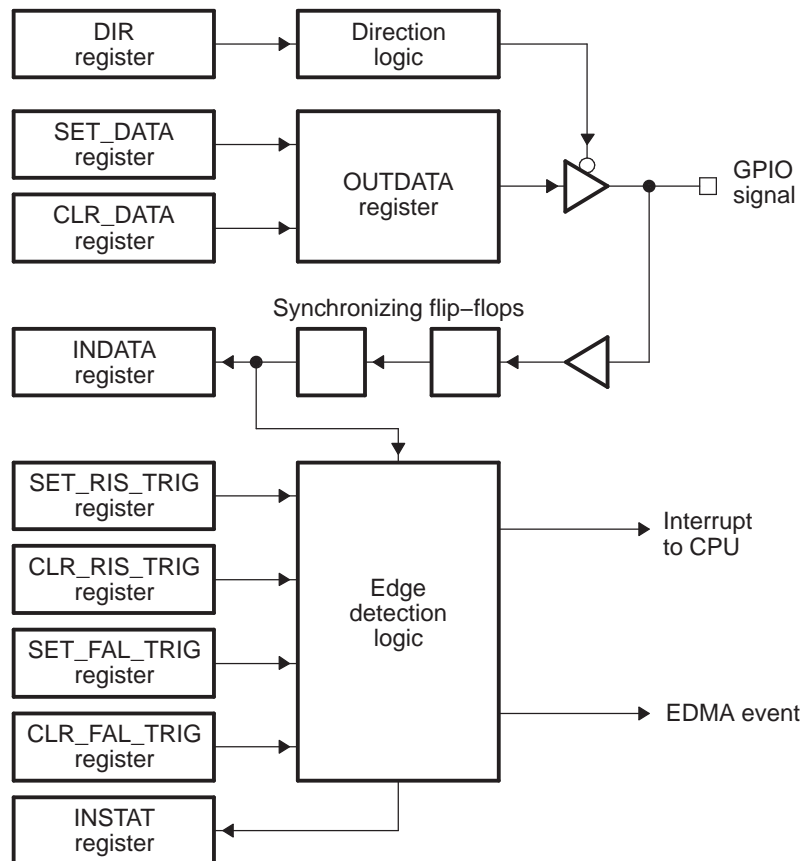
1.2 Features

The GPIO peripheral consists of the following features:

- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers
 - Output register can be read to reflect output drive status.
 - Input register can be read to reflect pin status.
- All GPIO signals can be used as interrupt sources with configurable edge detection.
- All GPIO signals can be used to generate events to the EDMA.
- Programmable debounce circuit provided on [7:0].

1.3 Functional Block Diagram

[Figure 1](#) shows a block diagram of the GPIO peripheral.

Figure 1. GPIO Peripheral Block Diagram


1.4 Industry Standard(s) Compliance Statement

The GPIO peripheral connects to external devices. While it is possible that the software implements some standard connectivity protocol over GPIO, the GPIO peripheral itself is not compliant with any such standards.

2 Peripheral Architecture

The following sections describe the architecture of the GPIO peripheral.

2.1 Clock Control

The input clock to the GPIO peripheral is driven by PLLC1. The maximum operation speed for the GPIO peripheral is 10 MHz.

2.2 Signal Descriptions

The device supports up to 104 signals, GIO[103:0]. These GPIOs are 3.3v I/O signals. The device also supports up to seven 1.8v GIO pins dedicated to the PRTC subsystem. These pins are labeled as PWRCTRIO[6:0]. For information on the package pinout of each GPIO signal, refer to the device-specific data manual.

2.3 GPIO Register Structure

The GPIO signals are grouped into banks of 16 signals per bank.

The GPIO configuration registers are organized as one 32-bit register per pair of banks. When there are

an odd number of banks, the upper 16-bit of registers for the last pair are reserved and have no effect. For the interrupt configuration, the registers associated with GPIO signals that do not support interrupt capability are also reserved and have no effect. [Table 1](#) shows the banks and register control bit information associated with each GIO pin on the device. The table can be used to locate the register bits that control each GPIO signal. For detailed information on the GPIO registers, see section [Section 3](#).

Table 1. GIO Register Bits and Banks Associated With GIO Pins

GIO Signal	Bank Number	Register Pair Number	Register Field Number	Bit Number
GIO0	0	<i>register_name01</i>	<i>field_name0</i>	Bit 0
GIO1	0	<i>register_name01</i>	<i>field_name1</i>	Bit 1
GIO2	0	<i>register_name01</i>	<i>field_name2</i>	Bit 2
GIO3	0	<i>register_name01</i>	<i>field_name3</i>	Bit 3
GIO4	0	<i>register_name01</i>	<i>field_name4</i>	Bit 4
GIO5	0	<i>register_name01</i>	<i>field_name5</i>	Bit 5
GIO6	0	<i>register_name01</i>	<i>field_name6</i>	Bit 6
GIO7	0	<i>register_name01</i>	<i>field_name7</i>	Bit 7
GIO8	0	<i>register_name01</i>	<i>field_name8</i>	Bit 8
GIO9	0	<i>register_name01</i>	<i>field_name9</i>	Bit 9
GIO10	0	<i>register_name01</i>	<i>field_name10</i>	Bit 10
GIO11	0	<i>register_name01</i>	<i>field_name11</i>	Bit 11
GIO12	0	<i>register_name01</i>	<i>field_name12</i>	Bit 12
GIO13	0	<i>register_name01</i>	<i>field_name13</i>	Bit 13
GIO14	0	<i>register_name01</i>	<i>field_name14</i>	Bit 14
GIO15	0	<i>register_name01</i>	<i>field_name15</i>	Bit 15
GIO16	1	<i>register_name01</i>	<i>field_name16</i>	Bit 16
GIO17	1	<i>register_name01</i>	<i>field_name17</i>	Bit 17
GIO18	1	<i>register_name01</i>	<i>field_name18</i>	Bit 18
GIO19	1	<i>register_name01</i>	<i>field_name19</i>	Bit 19
GIO20	1	<i>register_name01</i>	<i>field_name20</i>	Bit 20
GIO21	1	<i>register_name01</i>	<i>field_name21</i>	Bit 21
GIO22	1	<i>register_name01</i>	<i>field_name22</i>	Bit 22
GIO23	1	<i>register_name01</i>	<i>field_name23</i>	Bit 23
GIO24	1	<i>register_name01</i>	<i>field_name24</i>	Bit 24
GIO25	1	<i>register_name01</i>	<i>field_name25</i>	Bit 25
GIO26	1	<i>register_name01</i>	<i>field_name26</i>	Bit 26
GIO27	1	<i>register_name01</i>	<i>field_name27</i>	Bit 27
GIO28	1	<i>register_name01</i>	<i>field_name28</i>	Bit 28
GIO29	1	<i>register_name01</i>	<i>field_name29</i>	Bit 29
GIO30	1	<i>register_name01</i>	<i>field_name30</i>	Bit 30
GIO31	1	<i>register_name01</i>	<i>field_name31</i>	Bit 31
GIO32	2	<i>register_name23</i>	<i>field_name32</i>	Bit 0
GIO33	2	<i>register_name23</i>	<i>field_name33</i>	Bit 1
GIO34	2	<i>register_name23</i>	<i>field_name34</i>	Bit 2
GIO35	2	<i>register_name23</i>	<i>field_name35</i>	Bit 3
GIO36	2	<i>register_name23</i>	<i>field_name36</i>	Bit 4
GIO37	2	<i>register_name23</i>	<i>field_name37</i>	Bit 5
GIO38	2	<i>register_name23</i>	<i>field_name38</i>	Bit 6
GIO39	2	<i>register_name23</i>	<i>field_name39</i>	Bit 7
GIO40	2	<i>register_name23</i>	<i>field_name40</i>	Bit 8
GIO41	2	<i>register_name23</i>	<i>field_name41</i>	Bit 9

Table 1. GIO Register Bits and Banks Associated With GIO Pins (continued)

GIO Signal	Bank Number	Register Pair Number	Register Field Number	Bit Number
GIO42	2	register_name23	field_name42	Bit 10
GIO43	2	register_name23	field_name43	Bit 11
GIO44	2	register_name23	field_name44	Bit 12
GIO45	2	register_name23	field_name45	Bit 13
GIO46	2	register_name23	field_name46	Bit 14
GIO47	2	register_name23	field_name47	Bit 15
GIO48	3	register_name23	field_name48	Bit 16
GIO49	3	register_name23	field_name49	Bit 17
GIO50	3	register_name23	field_name50	Bit 18
GIO51	3	register_name23	field_name51	Bit 19
GIO52	3	register_name23	field_name52	Bit 20
GIO53	3	register_name23	field_name53	Bit 21
GIO54	3	register_name23	field_name54	Bit 22
GIO55	3	register_name23	field_name55	Bit 23
GIO56	3	register_name23	field_name56	Bit 24
GIO57	3	register_name23	field_name57	Bit 25
GIO58	3	register_name23	field_name58	Bit 26
GIO59	3	register_name23	field_name59	Bit 27
GIO60	3	register_name23	field_name60	Bit 28
GIO61	3	register_name23	field_name61	Bit 29
GIO62	3	register_name23	field_name62	Bit 30
GIO63	3	register_name23	field_name63	Bit 31
GIO64	4	register_name45	field_name64	Bit 0
GIO65	4	register_name45	field_name65	Bit 1
GIO66	4	register_name45	field_name66	Bit 2
GIO67	4	register_name45	field_name67	Bit 3
GIO68	4	register_name45	field_name68	Bit 4
GIO69	4	register_name45	field_name69	Bit 5
GIO70	4	register_name45	field_name70	Bit 6
GIO71	4	register_name45	field_name71	Bit 7
GIO72	4	register_name45	field_name72	Bit 8
GIO73	4	register_name45	field_name73	Bit 9
GIO74	4	register_name45	field_name74	Bit 10
GIO75	4	register_name45	field_name75	Bit 11
GIO76	4	register_name45	field_name76	Bit 12
GIO77	4	register_name45	field_name77	Bit 13
GIO78	4	register_name45	field_name78	Bit 14
GIO79	4	register_name45	field_name79	Bit 15
GIO80	5	register_name45	field_name80	Bit 16
GIO81	5	register_name45	field_name81	Bit 17
GIO82	5	register_name45	field_name82	Bit 18
GIO83	5	register_name45	field_name83	Bit 19
GIO84	5	register_name45	field_name84	Bit 20
GIO85	5	register_name45	field_name85	Bit 21
GIO86	5	register_name45	field_name86	Bit 22
GIO87	5	register_name45	field_name87	Bit 23
GIO88	5	register_name45	field_name88	Bit 24

Table 1. GIO Register Bits and Banks Associated With GIO Pins (continued)

GIO Signal	Bank Number	Register Pair Number	Register Field Number	Bit Number
GIO89	5	<i>register_name45</i>	<i>field_name89</i>	Bit 25
GIO90	5	<i>register_name45</i>	<i>field_name90</i>	Bit 26
GIO91	5	<i>register_name45</i>	<i>field_name91</i>	Bit 27
GIO92	5	<i>register_name45</i>	<i>field_name92</i>	Bit 28
GIO93	5	<i>register_name45</i>	<i>field_name93</i>	Bit 29
GIO94	5	<i>register_name45</i>	<i>field_name94</i>	Bit 30
GIO95	5	<i>register_name45</i>	<i>field_name95</i>	Bit 31
GIO96	6	<i>register_name6</i>	<i>field_name96</i>	Bit 0
GIO97	6	<i>register_name6</i>	<i>field_name97</i>	Bit 1
GIO98	6	<i>register_name6</i>	<i>field_name98</i>	Bit 2
GIO99	6	<i>register_name6</i>	<i>field_name99</i>	Bit 3
GIO100	6	<i>register_name6</i>	<i>field_name100</i>	Bit 4
GIO101	6	<i>register_name6</i>	<i>field_name101</i>	Bit 5
GIO102	6	<i>register_name6</i>	<i>field_name102</i>	Bit 6
GIO103	6	<i>register_name6</i>	<i>field_name103</i>	Bit 7

2.4 Using a GPIO Signal as an Output

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an output signal.

2.4.1 Configuring a GPIO Output Signal

To configure a given GPIO signal as an output, clear the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see [Section 3](#).

2.4.2 Controlling the GPIO Output Signal State

There are three registers that control the output state driven on a GPIO signal configured as an output:

- GPIO set data register (SET_DATA) controls driving GPIO signals high
- GPIO clear data register (CLR_DATA) controls driving GPIO signals low
- GPIO output data register (OUT_DATA) contains the current state of the output signals

Reading SET_DATA, CLR_DATA, and OUT_DATA returns the output state not necessarily the actual signal state (since some signals may be configured as inputs). The actual signal state is read using the GPIO input data register (IN_DATA) associated with the desired GPIO signal. IN_DATA contains the actual logic state on the external signal.

For detailed information on these registers, see [Section 3](#).

2.4.2.1 Driving a GPIO Output Signal High

To drive a GPIO signal high, use one of the following methods:

- Write a logic 1 to the bit in SET_DATA associated with the desired GPIO signal(s) to be driven high. Bit positions in SET_DATA containing logic 0 do not affect the state of the associated output signals.
- Modify the bit in OUT_DATA associated with the desired GPIO signal by using a read-modify-write operation. The logic states driven on the GPIO output signals match the logic values written to all bits in OUT_DATA.

For GPIO signals configured as inputs, the values written to the associated SET_DATA, CLR_DATA, and OUT_DATA bits have no effect.

2.4.2.2 Driving a GPIO Output Signal Low

To drive a GPIO signal low, use one of the following methods:

- Write a logic 1 to the bit in CLR_DATA associated with the desired GPIO signal(s) to be driven low. Bit positions in CLR_DATA containing logic 0 do not affect the state of the associated output signals.
- Modify the bit in OUT_DATA associated with the desired GPIO signal by using a read-modify-write operation. The logic states driven on the GPIO output signals match the logic values written to all bits in OUT_DATA.

For GPIO signals configured as inputs, the values written to the associated SET_DATA, CLR_DATA, and OUT_DATA bits have no effect.

2.5 Using a GPIO Signal as an Input

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an input signal.

2.5.1 Configuring a GPIO Input Signal

To configure a given GPIO signal as an input, set the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see [Section 3](#).

2.5.2 Reading a GPIO Input Signal

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA).

- For GPIO signals configured as inputs, reading IN_DATA returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA returns the output value being driven by the device.

Some signals may utilize open-drain output buffers for wired-logic operations. For open-drain GPIO signals, reading IN_DATA returns the wired-logic value on the signal (which will not be driven by the device alone). Information on any signals using open-drain outputs is available in the device data manual.

To use GPIO input signals as interrupt sources, see section [Section 2.8](#).

2.6 Debounce

The GIO[7:0] feature is a debounce circuit which provides the capability to filter out noise and spurious signals that occur on the input, by ignoring switching that occurs faster than a selected rate. This can be useful in systems for debouncing mechanical switches, or for sampling the state of a slowly varying input.

This debounce capability is controlled by the eight DEBOUNCEn (n = 0-7) registers, one each for GIO0-GIO7. The DEBOUNCEn registers each contain two bit fields which control the debounce circuit - the ENABLE bit, and the INTERVAL bits. The ENABLE bit controls whether the debounce circuit for the corresponding GIO pin is enabled or not, and the INTERVAL bits determine the duration of the debounce interval in clock cycles.

Once enabled, the debounce circuit stays idle until the input in question changes state. When this occurs, a counter starts counting out the debounce interval selected, and as long as the input stays at the new state until the end of the count, the circuit will pass the new state to the rest of the GPIO logic. If the input changes state again before the end of the count, the counter is reset to zero, and starts counting again. When the debounce circuit is enabled, no input state changes are propagated to the rest of the GPIO logic unless the selected count interval has been counted. Note that this also results in a delay of the length of the interval count until any state changes are propagated to the rest of the GPIO logic. The interval counter is clocked at PLLC1.SYSCLK4 .

For more information on DEBOUNCEn register bit field definitions, clocking and memory addresses, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide (SPRUFG5)*.

2.7 Reset Considerations

The GPIO peripheral has two reset sources: software reset and hardware reset.

2.7.1 Software Reset Considerations

A software reset (such as a reset initiated through the emulator) does not modify the configuration and state of the GPIO signals.

2.7.2 Hardware Reset Considerations

A hardware reset does reset the GPIO configuration and data registers to their default states, which therefore affects the configuration and state of the GPIO signals.

2.8 Interrupt Support

The GPIO peripheral can send an interrupt event to the ARM CPU.

2.8.1 Interrupt Events and Requests

A subset of the GPIO signals can also be configured to generate interrupts. The device supports interrupts from single GPIO signals. The interrupt mapping from the GPIO peripheral to the ARM CPU is shown in [Table 2](#). The device also supports up to three unique GIO[106:104] interrupts dedicated to the PRTC subsystem. For more details please refer to the device-specific data manual.

Table 2. GIO Interrupts to the ARM CPU

Interrupt Source	Acronym	ARM Interrupt Number
GIO0	GIO0	44
GIO1	GIO1	45
GIO2	GIO2	46
GIO3	GIO3	47
GIO4	GIO4	48
GIO5	GIO5	49
GIO6	GIO6	50
GIO7	GIO7	51
GIO8	GIO8	52
GIO9	GIO9	53
GIO10	GIO10	54
GIO11	GIO11	55
GIO12	GIO12	56
GIO13	GIO13	57
GIO14	GIO14	58
GIO15	GIO15	59

2.8.2 Enabling GPIO Interrupt Events

GPIO interrupt events are enabled in banks of 16 by setting the appropriate bit(s) in the GPIO interrupt per-bank enable register (BINTEN). For example, to enable bank 0 interrupts (events from GIO[15-0]), set bit 0 in BINTEN.

For detailed information on BINTEN, see [Section 3](#).

2.8.3 Configuring GPIO Interrupt Edge Triggering

Each GPIO interrupt source can be configured to generate an interrupt on the GPIO signal rising edge, falling edge, both edges, or neither edge (no event). The edge detection is synchronized to the GPIO peripheral module clock.

The following four registers control the configuration of the GPIO interrupt edge detection:

- The GPIO set rising edge interrupt register (SET_RIS_TRIG) enables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO clear rising edge interrupt register (CLR_RIS_TRIG) disables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO set falling edge interrupt register (SET_FAL_TRIG) enables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.
- The GPIO clear falling edge interrupt register (CLR_FAL_TRIG) disables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.

To configure a GPIO interrupt to occur only on rising edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG
- Write a logic 1 to the associated bit in CLR_FAL_TRIG

To configure a GPIO interrupt to occur only on falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_FAL_TRIG
- Write a logic 1 to the associated bit in CLR_RIS_TRIG

To configure a GPIO interrupt to occur on both the rising and falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG
- Write a logic 1 to the associated bit in SET_FAL_TRIG

To disable a specific GPIO interrupt:

- Write a logic 1 to the associated bit in CLR_RIS_TRIG
- Write a logic 1 to the associated bit in CLR_FAL_TRIG

For detailed information on these registers, see [Section 3](#).

Note that the direction of the GPIO signal does not have to be an input for the interrupt event generation to work. When a GPIO signal is configured as an output, the software can change the GPIO signal state and, in turn, generate an interrupt. This can be useful for debugging interrupt signal connectivity.

2.8.4 GPIO Interrupt Status

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTAT). Pending GPIO interrupts are indicated with a logic 1 in the associated bit position; interrupts that are not pending are indicated with a logic 0.

For individual GPIO interrupts that are directly routed to the ARM interrupt controller, the interrupt status can be read by reading the associated interrupt flag in the ARM interrupt controller. For the GPIO bank interrupts, INTSTAT can be used to determine which GPIO interrupt occurred. It is the responsibility of software to ensure that all pending GPIO interrupts are appropriately serviced.

Pending GPIO interrupt flags can be cleared by writing a logic 1 to the associated bit position in INTSTAT.

For detailed information on INTSTAT, see [Section 3](#).

2.8.5 Interrupt Multiplexing

GPIO interrupts are multiplex with other interrupts function. For more information, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Users Guide* ([SPRUFG5](#)).

2.9 EDMA Event Support

The GPIO peripheral can provide synchronization events to the EDMA. The EDMA events supported on this device are listed in [Table 3](#).

Table 3. GPIO Synchronization Events to the EDMA

Interrupt Source	EDMA Synchronization Event Number
GIO0	32
GIO1	33
GIO2	34
GIO3	35
GIO4	36
GIO5	37
GIO6	38
GIO7	39
GIO8	47
GIO9	25
GIO10	40
GIO11	41
GIO12	42
GIO13	43
GIO14	44
GIO15	45

2.10 Power Management

The GPIO peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the GPIO peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Users Guide* ([SPRUFG5](#)).

When the GPIO peripheral is placed in a low-power state by the PSC, the interrupt generation capability is suspended until the GPIO peripheral is removed from the low-power state. While in the low-power state, the GPIO signals configured as outputs are maintained at their state prior to the GPIO peripheral entering the low-power state.

2.11 Emulation Considerations

The GPIO peripheral is not affected by emulation suspend events (such as halts and breakpoints).

3 Registers

Table 4 lists the memory-mapped registers for the general-purpose input/output (GPIO). See the device-specific data manual for the memory address of these registers.

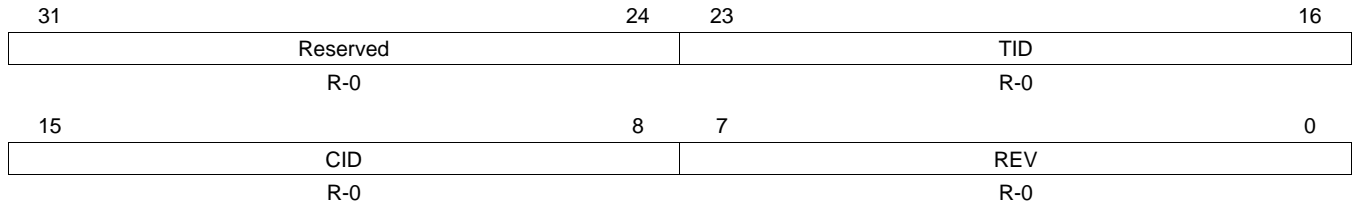
Table 4. General-Purpose Input/Output (GPIO) Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral Identification Register	Section 3.1
8h	BINTEN	GPIO Interrupt Per-Bank Enable Register	Section 3.2
GPIO Banks 0 and 1			
10h	DIR01	GPIO Banks 0 and 1 Direction Register	Section 3.3
14h	OUT_DATA01	GPIO Banks 0 and 1 Output Data Register	Section 3.4
18h	SET_DATA01	GPIO Banks 0 and 1 Set Data Register	Section 3.5
1Ch	CLR_DATA01	GPIO Banks 0 and 1 Clear Data Register	Section 3.6
20h	IN_DATA01	GPIO Banks 0 and 1 Input Data Register	Section 3.7
24h	SET_RIS_TRIG01	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register	Section 3.8
28h	CLR_RIS_TRIG01	GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register	Section 3.9
2Ch	SET_FAL_TRIG01	GPIO Banks 0 and 1 Set Falling Edge Interrupt Register	Section 3.10
30h	CLR_FAL_TRIG01	GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register	Section 3.11
34h	INTSTAT01	GPIO Banks 0 and 1 Interrupt Status Register	Section 3.12
GPIO Banks 2 and 3			
38h	DIR23	GPIO Banks 2 and 3 Direction Register	Section 3.3
3Ch	OUT_DATA23	GPIO Banks 2 and 3 Output Data Register	Section 3.4
40h	SET_DATA23	GPIO Banks 2 and 3 Set Data Register	Section 3.5
44h	CLR_DATA23	GPIO Banks 2 and 3 Clear Data Register	Section 3.6
48h	IN_DATA23	GPIO Banks 2 and 3 Input Data Register	Section 3.7
GPIO Bank 4 and 5			
60h	DIR45	GPIO Bank 4 and 5 Direction Register	Section 3.3
64h	OUT_DATA45	GPIO Bank 4 and 5 Output Data Register	Section 3.4
68h	SET_DATA45	GPIO Bank 4 and 5 Set Data Register	Section 3.5
6Ch	CLR_DATA45	GPIO Bank 4 and 5 Clear Data Register	Section 3.6
70h	IN_DATA45	GPIO Bank 4 and 5 Input Data Register	Section 3.7
GPIO Bank 6			
88h	DIR6	GPIO Bank 6 Direction Register	Section 3.3
8Ch	OUT_DATA6	GPIO Bank 6 Output Data Register	Section 3.4
90h	SET_DATA6	GPIO Bank 6 Set Data Register	Section 3.5
94h	CLR_DATA6	GPIO Bank 6 Clear Data Register	Section 3.6
98h	IN_DATA6	GPIO Bank 6 Input Data Register	Section 3.7
9Ch	SET_RIS_TRIG6	GPIO Bank 6 Set Rising Edge Interrupt Register	Section 3.8
A0h	CLR_RIS_TRIG6	GPIO Bank 6 Clear Rising Edge Interrupt Register	Section 3.9
A4h	SET_FAL_TRIG6	GPIO Bank 6 Set Falling Edge Interrupt Register	Section 3.10
A8h	CLR_FAL_TRIG6	GPIO Bank 6 Clear Falling Edge Interrupt Register	Section 3.11
ACH	INTSTAT6	GPIO Bank 6 Interrupt Status Register	Section 3.12

3.1 Peripheral Identification Register (PID)

The peripheral identification register (PID) contains identification data (type, class, and revision) for the peripheral. PID is shown in [Figure 2](#) and described in [Table 5](#).

Figure 2. Peripheral Identification Register (PID)



LEGEND: R = Read only; -n = value after reset

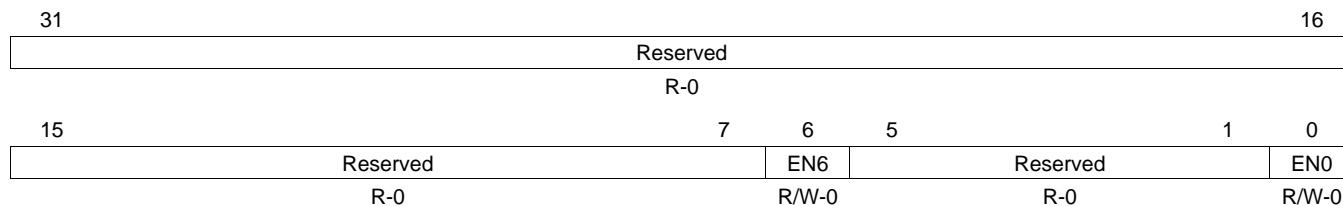
Table 5. Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-Fh	Identifies type of peripheral.
15-8	CID	0-Fh	Identifies class of peripheral.
7-0	REV	0-Fh	Identifies revision of peripheral.

3.2 GPIO Interrupt Per-Bank Enable Register (BINTEN)

The GPIO interrupt per-bank enable register (BINTEN) is shown in [Figure 3](#) and described in [Table 6](#). For information on which GPIO signals are associated with each bank, see [Table 1](#).

Figure 3. GPIO Interrupt Per-Bank Enable (BINTEN) Register



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. GPIO Interrupt Per-Bank Enable (BINTEN) Register Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6	EN6	0	Bank 6 interrupt enable is used to disable or enable the bank GIO[106:104] interrupts. Bank 6 interrupts are disabled.
		1	Bank 6 interrupts are enabled.
5-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN0	0	Bank 0 interrupt enable is used to disable or enable the bank GIO[15:0] interrupts. Bank 0 interrupts are disabled.
		1	Bank 0 interrupts are enabled.

3.3 GPIO Direction Registers (DIRn)

The GPIO direction register (DIR n) determines if GIO pin n in GPIO bank I is an input or an output. Each of the GPIO banks may have up to 16 GIO pins. By default, all the GIO pins are configured as inputs (bit value = 1). The GPIO direction register (DIR01) is shown in [Figure 4](#), DIR23 is shown in [Figure 5](#), DIR45 is shown in [Figure 6](#), DIR6 is shown in [Figure 7](#), and described in [Table 7](#). See [Table 1](#) to determine the DIR n bit associated with each GPIO bank and pin number.

Figure 4. GPIO Banks 0 and 1 Direction Register (DIR01)

31	30	29	28	27	26	25	24
DIR31	DIR30	DIR29	DIR28	DIR27	DIR26	DIR25	DIR24
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23	22	21	20	19	18	17	16
DIR23	DIR22	DIR21	DIR20	DIR19	DIR18	DIR17	DIR16
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
15	14	13	12	11	10	9	8
DIR15	DIR14	DIR13	DIR12	DIR11	DIR10	DIR9	DIR8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; - n = value after reset

Figure 5. GPIO Banks 2 and 3 Direction Register (DIR23)

31	30	29	28	27	26	25	24
DIR63	DIR62	DIR61	DIR60	DIR59	DIR58	DIR57	DIR56
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23	22	21	20	19	18	17	16
DIR55	DIR54	DIR53	DIR52	DIR51	DIR50	DIR49	DIR48
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
15	14	13	12	11	10	9	8
DIR47	DIR46	DIR45	DIR44	DIR43	DIR42	DIR41	DIR40
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
DIR39	DIR38	DIR37	DIR36	DIR35	DIR34	DIR33	DIR32
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; - n = value after reset

Figure 6. GPIO Banks 4 and 5 Direction Register (DIR45)

31	30	29	28	27	26	25	24
DIR95	DIR94	DIR93	DIR92	DIR91	DIR90	DIR89	DIR88
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
23	22	21	20	19	18	17	16
DIR87	DIR86	DIR85	DIR84	DIR83	DIR82	DIR81	DIR80
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
15	14	13	12	11	10	9	8
DIR79	DIR78	DIR77	DIR76	DIR75	DIR74	DIR73	DIR72
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
DIR71	DIR80	DIR69	DIR68	DIR67	DIR66	DIR65	DIR64
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; -n = value after reset

Figure 7. GPIO Bank 6 Direction Register (DIR6)

31	Reserved							16
R-0								
15	Reserved				11	10	9	8
R-0				R-1		R-1	R-1	
7	6	5	4	3	2	1	0	
DIR103	DIR102	DIR101	DIR100	DIR99	DIR98	DIR97	DIR96	
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. GPIO Direction Register (DIR6) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-8	DIR n	1	Direction of GIO pin n on GPIO bank 6. GIO pin n is an input.
7-0	DIR n	0	Direction of GIO pin n . The DIR n bit is used to control the direction (output = 0, input = 1) of pin n on GPIO bank 6. GIO pin n is an output.
		1	GIO pin n is an input.

3.4 GPIO Output Data Register (OUT_DATA n)

The GPIO output data register (OUT_DATA n) determines the value driven on the corresponding GIO pin n in GPIO bank l , if the pin is configured as an output (DIR n = 0). Writes do not affect pins not configured as GPIO outputs. The bits in OUT_DATA n are set or cleared by writing directly to this register. A read of OUT_DATA n returns the value of the register not the value at the pin (that might be configured as an input). The GPIO output data register (OUT_DATA01) is shown in [Figure 8](#), OUT_DATA23 is shown in [Figure 9](#), OUT_DATA45 is shown in [Figure 10](#), OUT_DATA6 is shown in [Figure 11](#), and described in [Table 8](#). See [Table 1](#) to determine the OUT_DATA n bit associated with each GPIO bank and pin number.

Figure 8. GPIO Banks 0 and 1 Output Data Register (OUT_DATA01)

31	30	29	28	27	26	25	24
OUT31	OUT30	OUT29	OUT28	OUT27	OUT26	OUT25	OUT24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
OUT23	OUT22	OUT21	OUT20	OUT19	OUT18	OUT17	OUT16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 9. GPIO Banks 2 and 3 Output Data Register (OUT_DATA23)

31	30	29	28	27	26	25	24
OUT63	OUT62	OUT61	OUT60	OUT59	OUT58	OUT57	OUT56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
OUT55	OUT54	OUT53	OUT52	OUT51	OUT50	OUT49	OUT48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
OUT47	OUT46	OUT45	OUT44	OUT43	OUT42	OUT41	OUT40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
OUT39	OUT38	OUT37	OUT36	OUT35	OUT34	OUT33	OUT32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 10. GPIO Banks 4 and 5 Output Data Register (OUT_DATA45)

31	30	29	28	27	26	25	24
OUT95	OUT94	OUT93	OUT92	OUT91	OUT90	OUT89	OUT88
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
OUT87	OUT86	OUT85	OUT85	OUT83	OUT82	OUT81	OUT80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
OUT79	OUT78	OUT77	OUT76	OUT75	OUT74	OUT73	OUT72
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
OUT71	OUT70	OUT69	OUT68	OUT67	OUT66	OUT65	OUT64
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 11. GPIO Bank 6 Output Data Register (OUT_DATA6)

31	Reserved							16
R-0								
15	14	13	12	11	10	9	8	
Reserved								
R-0								
7	6	5	4	3	2	1	0	
OUT103	OUT102	OUT101	OUT100	OUT99	OUT98	OUT97	OUT96	
R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. GPIO Output Data Register (OUT_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	OUT n		Output drive state of GIO pin n . The OUT n bit is used to drive the output (low = 0, high = 1) of pin n on GPIO bank $2l + 1$ only when pin n is configured as an output (DIR n = 0). The OUT n bit is ignored when GIO pin n is configured as an input. This bit field configures the GIO pins on GPIO banks 1 and 3.
		0	GIO pin n is driven low.
		1	GIO pin n is driven high.
15-0	OUT n		Output drive state of GIO pin n . The OUT n bit is used to drive the output (low = 0, high = 1) of pin n on GPIO bank $2l$ only when pin n is configured as an output (DIR n = 0). The OUT n bit is ignored when GIO pin n is configured as an input. This bit field configures the GIO pins on GPIO banks 0, 2, and 4.
		0	GIO pin n is driven low.
		1	GIO pin n is driven high.

3.5 GPIO Set Data Register (SET_DATA n)

The GPIO set data register (SET_DATA n) controls driving high the corresponding GPIO pin n in GPIO bank l , if the pin is configured as an output (DIR n = 0). Writes do not affect pins not configured as GPIO outputs. The bits in SET_DATA n are set or cleared by writing directly to this register. A read of the SET n bit returns the output drive state of the corresponding GPIO pin n . The GPIO set data register (SET_DATA01) is shown in Figure 12, SET_DATA23 is shown in Figure 13, SET_DATA45 is shown in Figure 14, SET_DATA6 is shown in Figure 15, and described in Table 9. See Table 1 to determine the SET_DATA n bit associated with each GPIO bank and pin number.

Figure 12. GPIO Banks 0 and 1 Set Data Register (SET_DATA01)

31	30	29	28	27	26	25	24
SET31	SET30	SET29	SET28	SET27	SET26	SET25	SET24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SET23	SET22	SET21	SET20	SET19	SET18	SET17	SET16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SET15	SET14	SET13	SET12	SET11	SET10	SET9	SET8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 13. GPIO Banks 2 and 3 Set Data Register (SET_DATA23)

31	30	29	28	27	26	25	24
SET63	SET62	SET61	SET60	SET59	SET58	SET57	SET56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SET55	SET54	SET53	SET52	SET51	SET50	SET49	SET48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SET47	SET46	SET45	SET44	SET43	SET42	SET41	SET40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SET39	SET38	SET37	SET36	SET35	SET34	SET33	SET32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 14. GPIO Banks 4 and 5 Set Data Register (SET_DATA45)

31	30	29	28	27	26	25	24
SET95	SET94	SET93	SET92	SET91	SET90	SET89	SET88
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SET87	SET86	SET85	SET84	SET83	SET82	SET81	SET80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SET79	SET78	SET77	SET76	SET75	SET74	SET73	SET72
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SET71	SET70	SET69	SET68	SET67	SET66	SET65	SET64
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 15. GPIO Bank 6 Set Data Register (SET_DATA6)

31	Reserved							16
R-0								
15	14	13	12	11	10	9	8	
Reserved								
R-0								
7	6	5	4	3	2	1	0	
SET103	SET102	SET101	SET100	SET99	SET98	SET97	SET96	
R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. GPIO Set Data Register (SET_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	SET n	0	Set output drive state of GIO pin n . The SET n bit is used to set the output of pin n on GPIO bank $2l + 1$ only when pin n is configured as an output (DIR n = 0). The SET n bit is ignored when GIO pin n is configured as an input. Writing a 1 to the SET n bit sets the output drive state of the corresponding GIO pin n ; reading the SET n bit returns the output drive state of the corresponding GIO pin n . This bit field configures the GIO pins on GPIO banks 1 and 3.
		1	No effect.
15-0	SET n	0	Set output drive state of GIO pin n . The SET n bit is used to set the output of pin n on GPIO bank $2l$ only when pin n is configured as an output (DIR n = 0). The SET n bit is ignored when GIO pin n is configured as an input. Writing a 1 to the SET n bit sets the output drive state of the corresponding GIO pin n ; reading the SET n bit returns the output drive state of the corresponding GIO pin n . This bit field configures the GIO pins on GPIO banks 0, 2, and 4.
		1	No effect.
			Set GIO pin n output to 1.

3.6 GPIO Clear Data Register (CLR_DATA n)

The GPIO clear data register (CLR_DATA n) controls driving low the corresponding GIO pin n in GPIO bank l , if the pin is configured as an output (DIR n = 0). Writes do not affect pins not configured as GPIO outputs. The bits in CLR_DATA n are set or cleared by writing directly to this register. A read of the CLR n bit returns the output drive state of the corresponding GIO pin n . The GPIO clear data register (CLR_DATA01) is shown in [Figure 16](#), CLR_DATA23 is shown in [Figure 17](#), CLR_DATA45 is shown in [Figure 18](#) CLR_DATA6 is shown in [Figure 19](#), and described in [Table 10](#). See [Table 1](#) to determine the CLR_DATA n bit associated with each GPIO bank and pin number.

Figure 16. GPIO Banks 0 and 1 Clear Data Register (CLR_DATA01)

31	30	29	28	27	26	25	24
CLR31	CLR30	CLR29	CLR28	CLR27	CLR26	CLR25	CLR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLR23	CLR22	CLR21	CLR20	CLR19	CLR18	CLR17	CLR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLR15	CLR14	CLR13	CLR12	CLR11	CLR10	CLR9	CLR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 17. GPIO Banks 2 and 3 Clear Data Register (CLR_DATA23)

31	30	29	28	27	26	25	24
CLR63	CLR62	CLR61	CLR60	CLR59	CLR58	CLR57	CLR56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLR55	CLR54	CLR53	CLR52	CLR51	CLR50	CLR49	CLR48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLR47	CLR46	CLR45	CLR44	CLR43	CLR42	CLR41	CLR40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLR39	CLR38	CLR37	CLR36	CLR35	CLR34	CLR33	CLR32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 18. GPIO Banks 4 and 5 Clear Data Register (CLR_DATA45)

31	30	29	28	27	26	25	24
CLR95	CLR94	CLR93	CLR92	CLR91	CLR90	CLR89	CLR88
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLR87	CLR86	CLR85	CLR84	CLR83	CLR82	CLR81	CLR80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLR79	CLR78	CLR77	CLR76	CLR75	CLR74	CLR73	CLR72
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLR71	CLR70	CLR69	CLR68	CLR67	CLR66	CLR65	CLR64
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 19. GPIO Bank 6 Clear Data Register (CLR_DATA6)

31	Reserved							16
R-0								
15	14	13	12	11	10	9	8	
Reserved								
R-0								
7	6	5	4	3	2	1	0	
CLR103	CLR102	CLR101	CLR100	CLR99	CLR698	CLR97	CLR96	
R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. GPIO Clear Data Register (CLR_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	CLR n		Clear output drive state of GIO pin n . The CLR n bit is used to clear the output of pin n on GPIO bank $2/ + 1$ only when pin n is configured as an output (DIR n = 0). The CLR n bit is ignored when GIO pin n is configured as an input. Writing a 1 to the CLR n bit clears the output drive state of the corresponding GIO pin n ; reading the CLR n bit returns the output drive state of the corresponding GIO pin n . This bit field configures the GIO pins on GPIO banks 1 and 3.
		0	No effect.
		1	Clear GIO pin n output to 0.
15-0	CLR n		Clear output drive state of GIO pin n . The CLR n bit is used to clear the output of pin n on GPIO bank $2/$ only when pin n is configured as an output (DIR n = 0). The CLR n bit is ignored when GIO pin n is configured as an input. Writing a 1 to the CLR n bit clears the output drive state of the corresponding GIO pin n ; reading the CLR n bit returns the output drive state of the corresponding GIO pin n . This bit field configures the GIO pins on GPIO banks 0, 2, and 4.
		0	No effect.
		1	Clear GIO pin n output to 0.

3.7 GPIO Input Data Register (IN_DATA n)

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA n).

- For GPIO signals configured as inputs, reading IN_DATA n returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA n returns the output value being driven by the device.

The GPIO input data register (IN_DATA01) is shown in [Figure 20](#), IN_DATA23 is shown in [Figure 21](#), IN_DATA45 is shown in [Figure 22](#), IN_DATA6 is shown in [Figure 23](#), and described in [Table 11](#) and [Table 12](#). See [Table 1](#) to determine the IN_DATA n bit associated with each GPIO bank and pin number.

Figure 20. GPIO Banks 0 and 1 Input Data Register (IN_DATA01)

31	30	29	28	27	26	25	24
IN31	IN30	IN29	IN28	IN27	IN26	IN25	IN24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
IN23	IN22	IN21	IN20	IN19	IN18	IN17	IN16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 21. GPIO Banks 2 and 3 Input Data Register (IN_DATA23)

31	30	29	28	27	26	25	24
IN63	IN62	IN61	IN60	IN59	IN58	IN57	IN56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
IN55	IN54	IN53	IN52	IN51	IN50	IN49	IN48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
IN47	IN46	IN45	IN44	IN43	IN42	IN41	IN40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
IN39	IN38	IN37	IN36	IN35	IN34	IN33	IN32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Figure 22. GPIO Banks 4 and 5 Input Data Register (IN_DATA45)

31	30	29	28	27	26	25	24
IN95	IN94	IN93	IN92	IN91	IN90	IN89	IN88
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
IN87	IN86	IN85	IN84	IN83	IN82	IN81	IN80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
IN79	IN78	IN77	IN76	IN75	IN74	IN73	IN72
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
IN71	IN70	IN69	IN68	IN67	IN66	IN65	IN64
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 11. GPIO Input Data Register (IN_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	IN n	0 1	Status of GIO pin n . Reading the IN n bit returns the state of pin n on GPIO bank 2/ l + 1. This bit field returns the status of the GIO pins on GPIO banks 1, 3, and 5. GIO pin n is logic low. GIO pin n is logic high.
15-0	IN n	0 1	Status of GIO pin n . Reading the IN n bit returns the state of pin n on GPIO bank 2/ l . This bit field returns the status of the GIO pins on GPIO banks 0, 2, and 4. GIO pin n is logic low. GIO pin n is logic high.

Figure 23. GPIO Bank 6 Input Data Register (IN_DATA6)

31	Reserved							16
R-0								
15	Reserved				11	10	9	8
R-0				R/W-0		R/W-0	R/W-0	
7	6	5	4	3	2	1	0	
IN103	IN102	IN101	IN100	IN99	IN98	IN97	IN96	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. GPIO Input Data Register (IN_DATA6) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	IN n	0 1	Status of GIO pin n . Reading the IN n bit returns the state of pin n on GPIO bank 2/ l . This bit field returns the status of the GIO pins on GPIO banks 0, 2 and 4. GIO pin n is logic low. GIO pin n is logic high.

3.8 GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG n)

The GPIO set rising edge interrupt register (SET_RIS_TRIG n) enables a rising edge on the GIO pin to generate a GPIO interrupt. The GPIO set rising edge interrupt register (SET_RIS_TRIG n) is shown in Figure 24 and described in Table 13. See Table 1 to determine the (SET_RIS_TRIG n) bit associated with each GIO pin number.

Figure 24. GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG n)

Reserved							
R-0							
Reserved							SETRIS16
R-0							R/W-0
15	14	13	12	11	10	9	8
SETRIS15	SETRIS14	SETRIS13	SETRIS12	SETRIS11	SETRIS10	SETRIS9	SETRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETRIS7	SETRIS6	SETRIS5	SETRIS4	SETRIS3	SETRIS2	SETRIS1	SETRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 13. GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG n) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved		Any writes to these bit(s) must always have a value of 0.
16-0	SETRIS n		Enable rising edge interrupt detection on GIO pin n . Reading the SETRIS n bit returns the state of GIO pin n .
		0	No effect.
		1	Interrupt is caused by a low-to-high transition on GIO pin n .

3.9 GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGN)

The GPIO clear rising edge interrupt register (CLR_RIS_TRIGN) disables a rising edge on the GIO pin from generating a GPIO interrupt. The GPIO clear rising edge interrupt register (CLR_RIS_TRIGN) is shown in Figure 25 and described in Table 14. See Table 1 to determine the (CLR_RIS_TRIGN) bit associated with each GIO pin number.

Figure 25. GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGN)

Reserved							
R-0							
Reserved							CLRRIS16
R-0							R/W-0
15	14	13	12	11	10	9	8
CLRRIS15	CLRRIS14	CLRRIS13	CLRRIS12	CLRRIS11	CLRRIS10	CLRRIS9	CLRRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRRIS7	CLRRIS6	CLRRIS5	CLRRIS4	CLRRIS3	CLRRIS2	CLRRIS1	CLRRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 14. GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGN) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved		Any writes to these bit(s) must always have a value of 0.
16-0	CLRRIS n	0	Disable rising edge interrupt detection on GIO pin n . Reading the CLRRIS n bit returns the complement state of GIO pin n .
		1	No effect.
			No interrupt is caused by a low-to-high transition on GIO pin n .

3.10 GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGN)

The GPIO set falling edge interrupt register (SET_FAL_TRIGN) enables a falling edge on the GIO pin to generate a GPIO interrupt. It is shown in Figure 26 and described in Table 15. See Table 1 to determine the SET_FAL_TRIGN bit associated with each GIO pin number.

Figure 26. GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGN)

Reserved							
R-0							
Reserved							SETFAL16
R-0							R/W-0
15	14	13	12	11	10	9	8
SETFAL15	SETFAL14	SETFAL13	SETFAL12	SETFAL11	SETFAL10	SETFAL9	SETFAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETFAL7	SETFAL6	SETFAL5	SETFAL4	SETFAL3	SETFAL2	SETFAL1	SETFAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIGN) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved		Any writes to these bit(s) must always have a value of 0.
16-0	SETFAL n	0	Enable falling edge interrupt detection on GIO pin n . Reading the SETFAL n bit returns the state of GIO pin n . No effect.
		1	Interrupt is caused by a high-to-low transition on GIO pin n .

3.11 GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG n)

The GPIO clear falling edge interrupt register (CLR_FAL_TRIG n) disables a falling edge on the GIO pin from generating a GPIO interrupt. The GPIO clear falling edge interrupt register (CLR_FAL_TRIG n) is shown in Figure 27 and described in Table 16. See Table 1 to determine the CLR_FAL_TRIG n bit associated with each GIO pin number.

Figure 27. GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG n)

Reserved							
R-0							
Reserved							CLR_FAL16
R-0							R/W-0
CLR_FAL15	CLR_FAL14	CLR_FAL13	CLR_FAL12	CLR_FAL11	CLR_FAL10	CLR_FAL9	CLR_FAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLR_FAL7	CLR_FAL6	CLR_FAL5	CLR_FAL4	CLR_FAL3	CLR_FAL2	CLR_FAL1	CLR_FAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; - n = value after reset

Table 16. GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG n) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved		Any writes to these bit(s) must always have a value of 0.
65-0	CLR_FAL n		Disable falling edge interrupt detection on GIO pin n . Reading the CLR_FAL n bit returns the complement state of GIO pin n .
		0	No effect.
		1	No interrupt is caused by a high-to-low transition on GIO pin n .

3.12 GPIO Interrupt Status Register (INTSTAT n)

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTAT n). In the associated bit position, pending GPIO interrupts are indicated with a logic 1 and GPIO interrupts that are not pending are indicated with a logic 0. The GPIO interrupt status register (INTSTAT n) is shown in Figure 28 and described in Table 17. See Table 1 to determine the INTSTAT n bit associated with each GIO pin number.

Figure 28. GPIO Interrupt Status Register (INTSTAT n)

Reserved							
R-0							
Reserved							STAT16
R-0							R/W1C-0
STAT15	STAT14	STAT13	STAT12	STAT11	STAT10	STAT9	STAT8
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit (writing 0 has no effect); - n = value after reset

Table 17. GPIO Interrupt Status Register (INTSTAT n) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved		Any writes to these bit(s) must always have a value of 0.
16-0	STAT n	0	No pending interrupt on GIO pin n .
		1	Pending interrupt on GIO pin n .

Appendix A Revisions

This document has been revised because of the following technical changes.

Table 18. Revisions

Location	Changes/Edits/Additions
Table 4	Added last 5 registers to Bank 6 (Offsets 9Ch - ACh).
Section 3.2	Added EN6 bit to register.
Figure 7	Updated figure.
Table 7	Corrected descriptions.
Figure 23	Updated figure.
Table 12	Corrected descriptions.

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