TMS320DM335
Digital Media System-on-Chip (DMSoC)
Video Processing Front End (VPFE)

Reference Guide

Literature Number: SPRUFX8
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About This Manual

This document describes the operation of the Video Processing Front End in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM335 Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFX7 — TMS320DM335 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide This document describes the ARM Subsystem in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFX8 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Reference Guide This document describes the Video Processing Front End (VPFE) in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

SPRUFX9 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Reference Guide This document describes the Video Processing Back End (VPBE) in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

SPRUFY0 —TMS320DM335 Digital Media System-on-Chip (DMSoC) 64-bit Timer Reference Guide This document describes the operation of the software-programmable 64-bit timers in the TMS320DM335 Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUFY1 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Reference Guide This document describes the serial peripheral interface (SPI) in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFY2 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Reference Guide This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFY3 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFY5 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUFY6 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Reference Guide This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

SPRUFY7 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Reference Guide This document describes the Real Time Out (RTO) controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC).

SPRUFY8 —TMS320DM335 Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUFY9 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Reference Guide This document describes the universal serial bus (USB) controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFZ0 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFZ1 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Reference Guide This document describes the asynchronous external memory interface (EMIF) in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFZ2 — TMS320DM335 Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide This document describes the DDR2/mDDR memory controller in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFZ3 —TMS320DM335 Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP) Reference Guide This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM335 Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

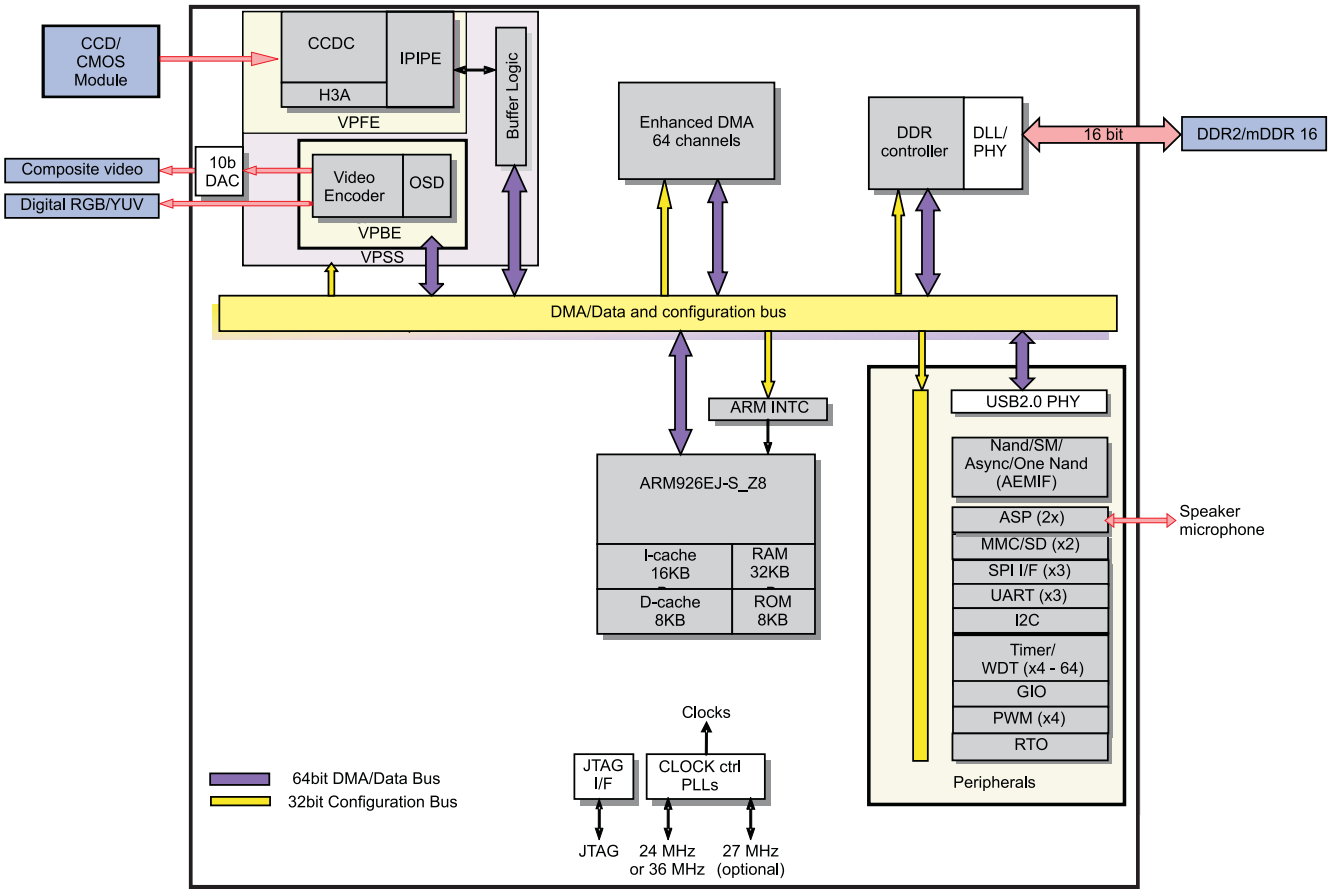
Trademarks

Video Processing Front End (VPFE)

1 Video Processing Front End Overview

The TMS320DM335 processor is a low cost, low power processor providing advanced graphical user interface for display applications that do not require video compression and decompression. Coupled with a video processing subsystem (VPSS) that provides 720p display, the DM335 processor is powered by an ARM926EJ-S CPU core so developers can create feature rich graphical user interfaces allowing customers to interact with their portable electronic devices. The new DM335 device delivers a sophisticated suite of capabilities allowing for flexible image capture and display. Through its user interface technology, such as a four-level on-screen display, developers are able to create picture-within-picture and video-within-video as well as innovative graphic user interfaces. Additional advanced capture and imaging technologies include support for CCD/CMOS image sensors, resize capability and video stabilization. The 1280-by-960-pixel digital LCD connection runs on a 75-MHz pixel clock and supports TV composite output for increased expandability. The device also enables seamless interface to most additional external devices via the Video Processing Front End Subsystem (VPFE). The interface is flexible enough to support various types of CCD and CMOS sensors, signal conditioning circuits, power management, SDRAM, SRAM, shutter, Iris and auto-focus motor controls.

Figure 1. Functional Block Diagram

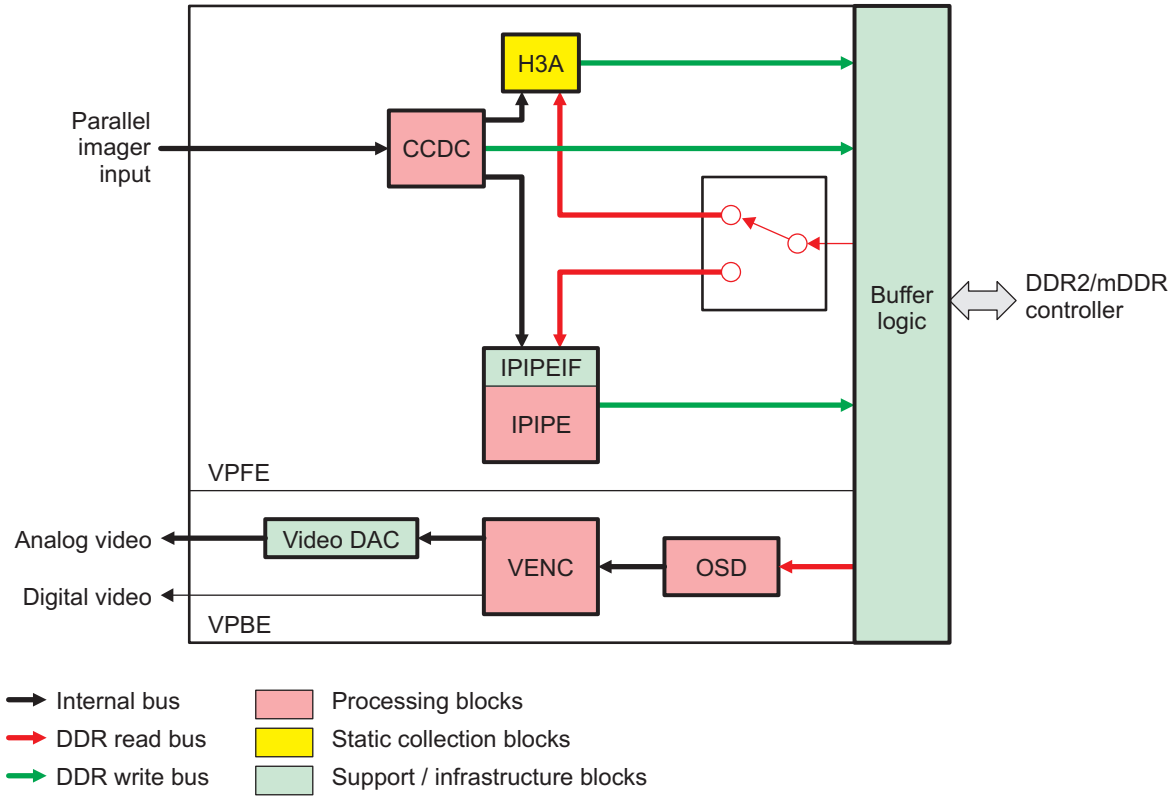


1.1 Purpose of the Video Processing Front End

The device contains a Video Processing Subsystem (VPSS), Figure 2, that provides an input interface (Video Processing Front End or VPFE) for external imaging peripherals such as image sensors, video decoders, etc.; and an output interface (Video Processing Back End or VPBE) for display devices, such as analog SDTV displays, digital LCD panels, HDTV video encoders, etc.

In addition to these peripherals, there is a set of common buffer memory and DMA control to ensure efficient use of the DDR2/mDDR controller burst bandwidth. The buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2/mDDR controller. In order to efficiently utilize the external DDR2/mDDR controller bandwidth, the buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The buffer logic/memory (divided into the read and write buffers and arbitration logic) is capable of performing the following functions. It is imperative that the VPSS utilize DDR2/mDDR controller bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules.

Figure 2. Video Processing Subsystem (VPSS) Block Diagram



1.2 Features

The VPFE block is comprised of the CCD Controller (CCDC), Image Pipe (IPIPE), Image Pipe Interface (IPIPEIF), and Hardware 3A Statistic Generator (H3A) blocks. Together, these modules provide the device with a powerful and flexible front-end interface. These modules can be broken down into two distinct types. The first type consists of major processing modules that are in the direct data flow path and affect the input image data stream. These are described below:

- The CCD Controller (CCDC) provides an interface to image sensors and digital video sources.
- The image pipe (IPIPE) is a parameterized hardwired image processing block whose image processing functions can be customized for each sensor type to realize good still image quality as well supporting video frame rates for digital still camera preview displays and video recording modes. An image resizer is also fully integrated within this module. Additionally, the IPIPE contains the following statistic collection function: histogram and the boundary signal calculator (for motion vector compensation).

In addition to the modules that directly affect that input image data, there is one independent module that provides statistics on the incoming images to aid designers of camera systems.

- The hardware 3A (H3A) module is designed to support the control loops for auto focus (AF), auto white balance (AWB) and auto exposure (AE) by collecting metrics on the RAW image data from the CCD controller.

1.2.1 CCD Controller (CCDC)

The CCDC is responsible for accepting RAW (unprocessed) image/video data from a sensor (CMOS or CCD). In addition, the CCDC can accept YCbCr video data in numerous formats, typically from so-called video decoder devices. In the case of RAW inputs, the CCDC output requires additional image processing to transform the RAW input image to the final processed image. This processing can be done in the Image Pipe. The CCDC is programmed via control and parameter registers. The following features are supported by the CCDC module.

- Support for conventional Bayer pattern sensor format.
- Support for complimentary color pattern input via a color space converter.
- Generates HD/VD timing signals to an external timing generator or can synchronize to the external timing generator.
- Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors).
- Support for up to 75-MHZ sensor pixel clock, if H3A is not used; otherwise, the pixel clock must be less than 67.5 MHZ.
- Support for ITU-R BT.656 standard format, either 8-bit or 10-bit.
- Support for YCbCr422 format, either 8-bit or 16-bit with discrete H and VSYNC signals.
- Support for up to 14-bit raw data from a CCD/CMOS sensor.
- Generates optical black clamping signals.
- Support for shutter signal control.
- Support for digital clamping and black level compensation.
- Defect correction based on a lookup table that contains row and column position of the pixel to be corrected.
- Programmable Lens Shading Correction.
- Support for 10-bit to 8-bit A-law compression.
- Support for a low-pass filter prior to writing to SDRAM. If this filter is enabled, 2 pixels each in the left and right edges of each line are cropped from the output.
- Support for generating output to range from 14-bits to 8-bits wide (8-bits wide allows for 50% saving in storage area).
- Support for down-sampling via programmable culling patterns.
- Ability to control output to the DDR2/mDDR controller via an external write enable signal.
- Supported maximum CCD imager size is 32,768 × 32,768.

1.2.2 Image Pipe – Hardware Image Signal Processor (IPIPE)

The Image Pipe (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 format from raw CCD/CMOS data. The IPIPE can also be configured to operate in a resize only mode, which allows YCbCr-4:2:2 to be resized without applying the processing of every module in the IPIPE. The following features are supported by the IPIPE.

- Support for 14 bit RAW data image processing or 16 bit YCbCr resizing
- Support RGB Bayer pattern for input color filter array. (Support for complementary CMYG pattern is also provided via the Color Space Converter.)
- Require at least 8 pixels for horizontal blanking and 4 lines for vertical blanking. In one shot mode, 10 blanking lines after processing area are required.
- Maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 8191.
- Support for a maximum input and output widths up to 1344 pixels wide (640 for RSZ[1]).
- Support dark frame subtract in IPIPEIF by providing a raw pass-though mode supporting images wider than 1344 pixels.
- Support for automatic mirroring of pixels/lines when edge processing is performed so that the width and height is consistent throughout.
- Defect correction based on a lookup table that contains row and column position of the pixel to be corrected.
- Horizontal /Vertical noise reduction filter
- Gain control for white balancing at each component
- CFA interpolation for good quality CFA interpolation with reduced false color artifacts
- Programmable RGB-to-RGB blending matrix (9 coefficients for the 3×3 matrix).
- Programmable coefficients for RGB to YCbCr conversion
- Programmable lookup table for Luminance edge enhance
- Faulty-color suppression filter
- Programmable down or up-sampling filter for both horizontal and vertical directions with range from 1/16x to 8x, in which the filter outputs two images with different magnification simultaneously.
- Flipping image vertically and/or horizontally
- RGB (32bit/16bit) output to SDRAM
- Programmable Histogram engine (4 windows, 256 bins)
- Boxcar calculation

1.2.3 Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto focus engine
- Auto exposure and auto white balance engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a *paxel* for the case of AF.

The AE/AWB engine accumulates the values and checks for saturated values in a sub sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a “window”. Thus, other than referring them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

1.2.3.1 Auto Focus Engine Features

The following features are supported by the AF engine.

- Support for a peak mode in a paxel (a paxel is defined as a two dimensional block of pixels).
  - Accumulate the maximum focus value of each line in a paxel
- Support for an accumulation/sum mode (instead of peak mode).
- Support for an accumulation/sum mode (instead of peak mode).
- Support for up to 36 paxels in the horizontal direction and up to 128 paxels in the vertical direction.
- Programmable width and height for the paxel. All paxels in the frame will be the same size.
- Programmable red, green, and blue position within a 2×2 matrix.
- Separate horizontal start for paxel and filtering.
- Programmable horizontal and vertical line increments within a paxel.
- Parallel IIR filters configured in a dual-biquad configuration with individual coefficients (two filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.

1.2.3.2 Auto Exposure and Auto White Balance Features

The following features are supported by the AE/AWB engine.

- Accumulate clipped pixels along with all non-saturated pixels.
- Support for up to 36 horizontal windows and up to 128 vertical windows..
- Programmable width and height for the windows. All windows in the frame will be the same size.
- Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels.
- Programmable horizontal sampling points in a window
- Programmable vertical sampling points in a window

1.2.4 Image Pipe Interface (IPIPEIF)

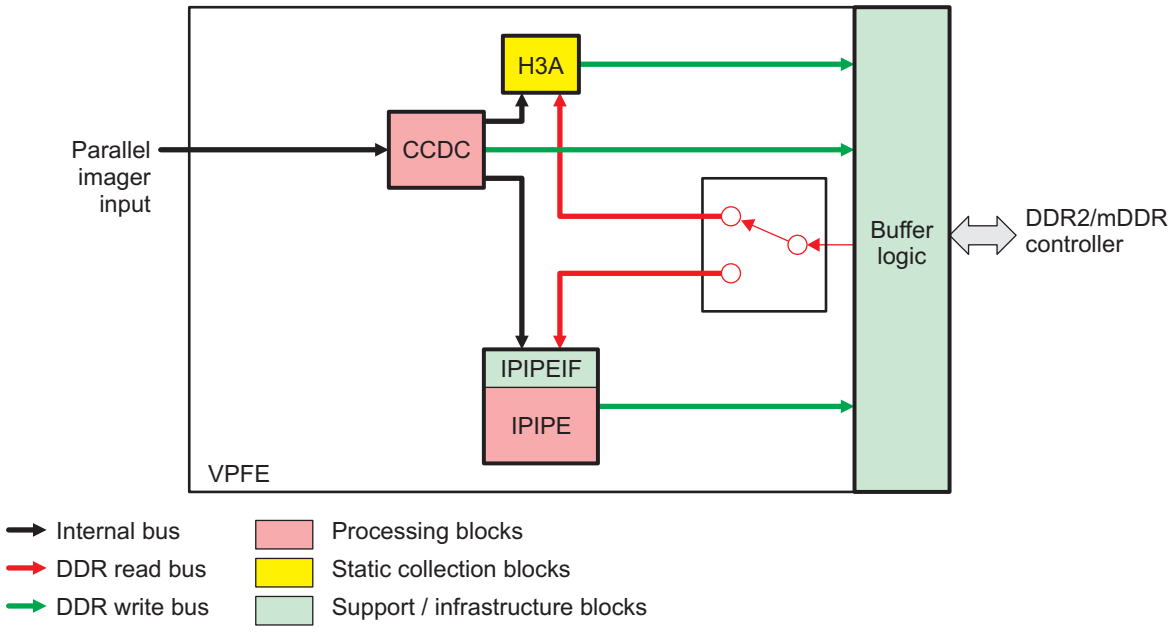
The image pipe input interface module is an input extension to the image pipe. It can receive data from the CCDC, SDRAM, or both (darkframe subtract) and pass the data to the IPIPE. Depending on the functions performed, it may also readjust the HD, VD, and PCLK timing to the IPIPE input.

- Supports dark-frame subtract of raw image stored in DDRAM from image from CCDC
- Supports inverse ALAW decompression of RAW data from DDRAM.
- Supports (1,2,1) average filtering before horizontal decimation
- Supports horizontal decimation (downsizing) of input lines to <= 1344 maximum required by the image pipe
- Supports gain multiply for raw data

1.3 Functional Block Diagram

Figure 3 shows a high-level functional block diagram of the VPFE functional blocks, along with the different data flow paths. These data flow paths show how the various modules of the VPFE interact. The parallel input to the CCDC is either 14-bit RAW digital sensor image data from an AFE or 8- to-16 bit YCbCr video data. The input to the H3A is only RAW sensor image data. The input to the IPIPE can be RAW or YCbCr video data (for resizing). Since the DDR2/mDDR controller read buffer is shared by the H3A and IPIPE, these modules can not concurrently read from the DDR2/mDDR controller.

Figure 3. Video Processing Front End (VPFE) Block Diagram and Data Flows



1.4 Supported Use Case Statement

The VPFE supports image data acquisition from sensor and digital video sources in various modes/formats. YCbCr sources have minimal image processing applied and can either be passed directly to the DDR2/mDDR controller or passed through the IPIPE's Resizer for scaling prior to writing to the DDR2/mDDR controller. RAW imager data modes (non-YCbCr sources) are supported by the statistics collection modules (H3A and IPIPE's histogram) as well as full image pipe processing functions, including resize.

The same processing options are supported when processing data sourced from the DDR2/mDDR controller. The only exception is that the IPIPEIF module cannot perform dark frame subtract on data from the DDR2/mDDR controller.

Zooming at ratios greater than the 8× ratio in a single pass are not supported by the IPIPE's resizer. However, this can be done by passing the resized data from the DDR2/mDDR controller through the resizer again as long as the real-time deadlines can be met.

1.5 Industry Standard(s) Compliance Statement

ITU-R BT.656, REC601

2 VPFE/ISP I/O Interfacing

This section addresses the configuration of any external connections that the VPFE/ISP may have at the interface of the device, including I/O signals lists, I/O pin multiplexing, and protocol/data formats for typical application(s).

The VPFE signals are shown in Table 1. Note that these signals can take on different meanings depending on the specific interface chosen. All of the digital input signals below are multiplexed as GIO signals at reset (not shown in Table 1), and some are also multiplexed as SPI2 signals. Pin multiplexing is controlled from the System Module. The following sections describe each of the input interface scenarios supported.

Table 1. Interface Signals for Video Processing Front End

Pin Name	I/O	Description
PCLK	Bidi	Pixel Clock
CAM_VD	Bidi	V sync
CAM_HD	Bidi	H sync
CIN7/SPI2_SCLK	Bidi	C IN signal
CIN6/SPI2_SDO	Bidi	C IN signal
CIN5/CCD13/SPI2_SDENA	Bidi	C IN signal/CCD in signal
CIN4/CCD12/SPI2_SDENB/SPI2_SDI3	Bidi	C IN signal/CCD in signal
CIN3/CCD11	Bidi	C IN signal/CCD in signal
CIN2/CCD10	Bidi	C IN signal/CCD in signal
CIN1/CCD9	Bidi	C IN signal/CCD in signal
CIN0/CCD8	Bidi	C IN signal/CCD in signal
YIN7/CCD7	Bidi	C IN signal/CCD in signal
YIN6/CCD6	Bidi	C IN signal/CCD in signal
YIN5/CCD5	Bidi	C IN signal/CCD in signal
YIN4/CCD4	Bidi	C IN signal/CCD in signal
YIN3/CCD3	Bidi	C IN signal/CCD in signal
YIN2/CCD2	Bidi	C IN signal/CCD in signal
YIN1/CCD1	Bidi	C IN signal/CCD in signal
YIN0/CCD0	Bidi	C IN signal/CCD in signal
CAM_WEN_FIELD	Bidi	CCD Write Enable/Field ID signal

2.1 Parallel Generic Interface Configuration (RAW)

The generic RAW interface configuration is typically used for interfacing to image sensors. The device can support up to 14 bits of resolution for each sample.

2.1.1 Parallel Generic Configuration (RAW) Signal Interface

Table 2 shows the interface connections for the RAW Mode interface.

Table 2. Interface Signals for Parallel Raw Mode

Pin Name	I/O	Description
PCLK	Bidi	Pixel Clock
CAM_VD	Bidi	V sync
CAM_HD	Bidi	H sync
SPI2_SCLK/GIO101	Bidi	Optional SPI signal or GIO
SPI2_SDO/GIO100	Bidi	Optional SPI signal or GIO
CCD13/SPI2_SDENA/GIO099	Bidi	CCD in signal/Optional SPI signal or GIO
CCD12/SPI2_SDENB/SPI2_SDI3/GIO098	Bidi	CCD in signal/Optional SPI signal or GIO
CCD11	Bidi	CCD in signal
CCD10	Bidi	CCD in signal
CCD9	Bidi	CCD in signal
CCD8	Bidi	CCD in signal
CCD7	Bidi	CCD in signal
CCD6	Bidi	CCD in signal
CCD5	Bidi	CCD in signal
CCD4	Bidi	CCD in signal
CCD3	Bidi	CCD in signal
CCD2	Bidi	CCD in signal
CCD1	Bidi	CCD in signal
CCD0	Bidi	CCD in signal
CAM_WEN_FIELD/GIO083	Bidi	CCD Write Enable/Field ID signal

The device can support up to 14 bits of resolution for each sample but sensors typically only output 8, 10, 12, or 14 bits of useful resolution depending on the imager and associated AFE. When the number of data lines is less than 14, it is recommended to connect RAW data to the upper data lines of CCD[13:0]. The exception to this rule is as follows:

- If there are less than 14 data lines, and
- The application requires the use of the SPI2 peripheral OR extra GPIOs.

If the above conditions above are met, then it is required to connect RAW data to the upper data lines of CCD[12:0] (for RAW13) or CCD[11:0] (for less than 13 data lines) instead of CCD[13:0] to make the SPI2 peripheral pins or GIOs available. Table 3 outlines examples of CCD RAW data connection options based on the number of data lines available. Lines not connected (indicated by '-' in the table) should be floating (since there are internal pull-downs) or tied low.

Table 3. Imager Data Connection Examples

	Imager Data Line Numbers				
Data Pin	RAW14	RAW13 + SPI2	RAW12 + SPI2	RAW11 + SPI2	RAW10 + SPI2
CCD13	13	SPI2	SPI2	SPI2	SPI2
CCD12	12	12	SPI2	SPI2	SPI2
CCD11	11	11	11	10	9
CCD10	10	10	10	9	8
CCD9	9	9	9	8	7
CCD8	8	8	8	7	6
CCD7	7	7	7	6	5
CCD6	6	6	6	5	4
CCD5	5	5	5	4	3
CCD4	4	4	4	3	2
CCD3	3	3	3	2	1
CCD2	2	2	2	1	0
CCD1	1	1	1	0	
CCD0	0	0	0		

If the input interface is configured on the upper lines of CCD[12:0] or CCD[11:0], then the CCDC, IPIPEIF, or IPIPE gain functions will need to be used to increase multiply the data by 2× or 4×, respectively to effectively shift the data up. Table 4 indicates the available gain function options where this multiply can be applied.

Table 4. Available Gain Functions for Bit Shifting the Data

Name	Block	Module	Max Gain	Comments
Color Space conversion	CSC	CCDC	3.969	
Lens Shading	LCS	CCDC	1.9	
IPIPEIF Gain	GAIN	IPIPEIF	1.998	After subtraction of dark frame
White Balance Total gain	WB2_DGN	IPIPE	3.969	Affects all colors
White Balance For Each color	WB2_WG_x	IPIPE	7.992	Separate gain for each color
RGB2RGB	RGB_MUL_xx	IPIPE	7.996	

2.1.2 Parallel Generic Configuration (RAW) Signal Interface Description

The signal interface is described in Table 5.

Table 5. CCD/CMOS Interface Signals

Name	I/O	Description
CCD[13:0]	I	Image data. Mode set by INPMOD (not R656ON). • Bit width can be can be configured between 8 and 16 bits (DATSIZ) • The polarity of the input image data can be reversed (DATAPOL)
CAM_VD	I/O	VSYNC. This vertical sync signal can be configured as an input or an output (VDHDOUT). • When configured as an input, the CCD or CMOS sensor must supply the VD signal • When configured as an output, supplies the VD signal and the Vd width and lines per frame must be configured (VDW, HLPFR) • The polarity of VD can be reversed. (VDPOL)
CAM_HD	I/O	HSYNC. This horizontal sync signal can be configured as an input or an output (VDHDOUT). • When configured as an input, the CCD or CMOS sensor must supply the HD signal • When configured as an output, supplies the HD signal and the Hd width and pixels per line must be configured (HDW, PPLN) • The polarity of HD can be reversed (HDPOL)
CAM_WEN_FIELD	I	Field identification signal (optional – FLDMODE) • Supplied by the external CCD or CMOS sensor • Can be configured to be latched by the VD signal (FIDMD) • The polarity of the field identification signal can be reversed (FLDPOL) CCD write enable signal (optional – EXWEN). This write enable signal determines when data is captured/processed/saved to memory or sent for further processing. • If enabled (EXWEN), image data will only be captured/processed/saved to memory or sent for further processing depending on the state of WENLOG. • Data can be saved when either $\overline{\text{C\_WE}}$ is active AND the pixels are within the internal frame (SPH, NPH, SLV, NLV) when either the $\overline{\text{C\_WE}}$ signal is active; or data can be save only when $\overline{\text{C\_WE}}$ is active OR the pixels are within the internal frame (WENLOG)
PCLK	I	Pixel clock. This signal is used to load image data into the CCDC. • The CCDC can be configured to capture on either the rising or falling edge of the PCLK signal (PCLK_INV in SYSTEM module)

2.1.3 Parallel Generic Configuration (RAW) Protocol and Data Formats

As described in Table 5, the device can be separately configured to either source or sink the VD/HD signals. If these signals are sourced, then the CCD/CMOS Controller must be configured via register settings for the proper timing generation. The definition of the captured frame must be set regardless of the control signal settings but these settings are described in the data processing section below.

2.1.3.1 Mode Information – Always Required

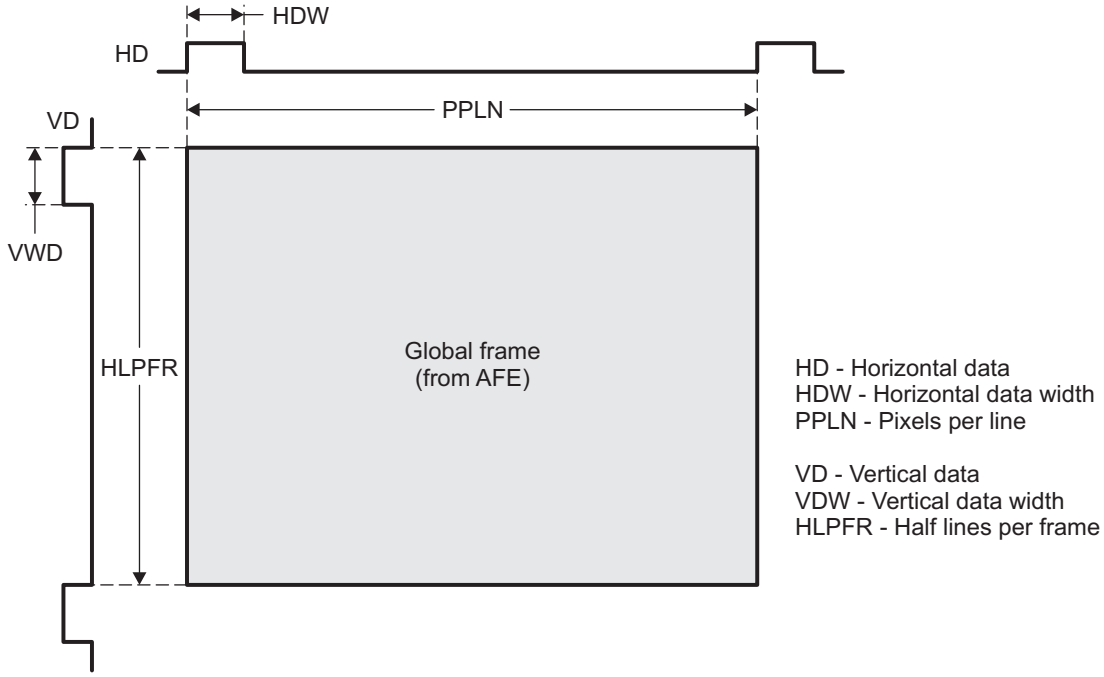
- INPMOD – input mode
- DATAPOL – polarity of input data
- VDPOL – Vd polarity
- HDPOL – Hd polarity
- VDHDOUT – Vd/Hd signal direction
- FLDMOD – Field mode

2.1.3.2 Timing Information – Optional, Depending on Control Signals and Sensor Mode

- If FLDMODE is enabled
  - FLDPOL – polarity of CAM_WEN_FIELD signal for FIELD function
  - FIDMD – CAM_WEN_FIELD latch information
- If VDHDOUT is output
  - VDW – Vd width
  - HLPFR – Half lines per frame
  - HDW – Hd width
  - PPLN – Pixels per line
- EXWEN – external CAM_WEN_FIELD signal enabled for WEN function
  - WENLOG – determines when data is valid along with frame settings

The timing generator in the CCDC either enables the use of external sync signals (HD/VD) or internal generated timing signals. If timing signals are generated internally, the ARM can set the width, polarity, position and direction of internal generated signals. Figure 4 shows various CCDC register settings related to the timing. The shaded area is the physical imager size.

Figure 4. Raw Mode Timing Diagram



The bits of data from each pixel are stored in the lower bits of a 16-bit SDRAM word, and the unused bit positions are filled with zeros. The DDR data format is shown in Figure 5. There is an optional 10-to-8-bit A-Law compression so that 10-bit data can be reduced to 8-bit dynamic range and packed to save DDR memory usage.

Figure 5. DDR2/mDDR controller Output Format

	Upper word		Lower word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
14 bit	0	Pixel 1	0	Pixel 0
13 bit	0	Pixel 1	0	Pixel 0
12 bit	0	Pixel 1	0	Pixel 0
11 bit	0	Pixel 1	0	Pixel 0
10 bit	0	Pixel 1	0	Pixel 0
9 bit	0	Pixel 1	0	Pixel 0
8 bit	0	Pixel 1	0	Pixel 0
8 bit pack	Pixel 3	Pixel 2	Pixel 1	Pixel 0

2.2 ITU-R BT.656 Interface Configuration

ITU-R BT.656 (sometimes referred to as REC656) is a specification that provides a method to transfer YCbCr-4:2:2 formatted digital video data over an 8/10-bit wide interface. Note that the BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with BT.601.

2.2.1 ITU-R BT.656 Configuration Signal Interface

Table 6 shows the interface connections for the ITU-R BT.656 interface.

Data and timing codes are transferred over the same 8/10-bit interface. When in BT.656 mode, only the data lines and clock signal are connected between the external device and the CCDC module of VPFE. An NTSC/PAL decoder is an example of an external device that may be connected to the REC656 interface.

Data lines CCD[7:0] are used for 8-bit YCbCr data and data lines CCD[9:0] are used for 10-bit YCbCr data. The video timing signals, HD, VD, and FIELD, are generated internally by the CCDC module of VPFE.

Note that an additional SPI can be supported in this mode without interference.

Table 6. Interface Signals for ITU-R BT.656 Mode

Pin Name	I/O	Description
PCLK	Bidi	Pixel Clock
GIO084	Bidi	GIO
GIO085	Bidi	GIO
SPI2_SCLK/GIO101	Bidi	Optional SPI signal or GIO
SPI2_SDO/GIO100	Bidi	Optional SPI signal or GIO
SPI2_SDEN A/GIO099	Bidi	Optional SPI signal or GIO
SPI2_SDENB/SPI2_SDI3/GIO098	Bidi	Optional SPI signal or GIO
GIO097	Bidi	GIO
GIO096	Bidi	GIO
CCD9/GIO095	Bidi	BT.656 Data (optional for 10-bit I/F)
CCD8/GIO094	Bidi	BT.656 Data (optional for 10-bit I/F)
CCD7	Bidi	BT.656 Data
CCD6	Bidi	BT.656 Data
CCD5	Bidi	BT.656 Data
CCD4	Bidi	BT.656 Data
CCD3	Bidi	BT.656 Data
CCD2	Bidi	BT.656 Data
CCD1	Bidi	BT.656 Data
CCD0	Bidi	BT.656 Data
GIO083	Bidi	GIO

2.2.2 ITU-R BT.656 Configuration Signal Interface Description

The REC656 interface supports either 8-bit or 10-bit processing if input Video YCbCr data. See the programming guide section for configuring this mode.

Since the sync information is carried along with the data lines, there are no sync signal interfaces or CCD controller configuration settings to make other that the start/end pixels and the line length and vertical frame size. The signal interface is described in Table 7.

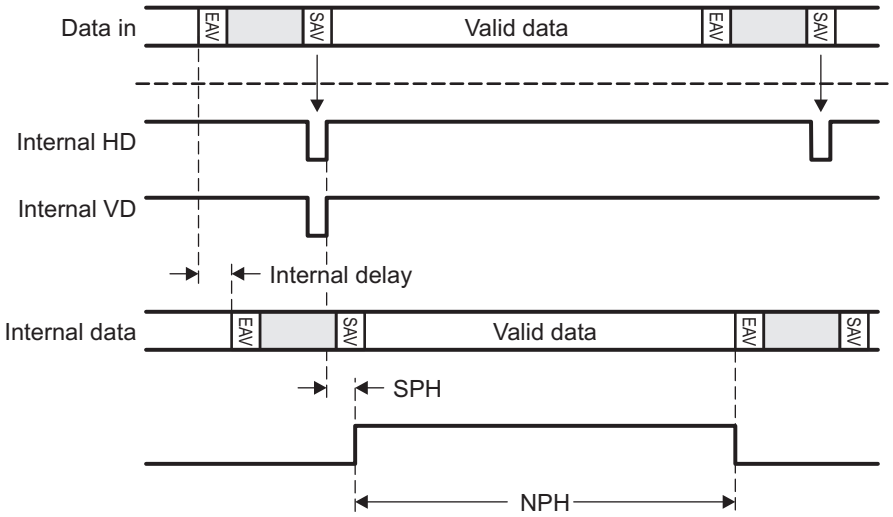
Table 7. ITU-R BT.656 Interface Signals

Name	I/O	Description
CCD[9:0]	I	Image Data, Mode set by R656ON • Bit width can be can be configured to either 8 or 10 bits (BW656) • The polarity of the input image data can be reversed (DATAPOL)
PCLK	I	Pixel clock. This signal is used to load image data into the CCDC. • The CCDC can be configured to capture on either the rising or falling edge of the PCLK signal (PCLK_INV in SYSTEM module).

2.2.3 ITU-R BT.656 Configuration Protocol and Data Formats

Two timing reference codes synchronize HD, VD, and FIELD to the video data. At the start and end of each video data block the device sends a unique timing reference code. The start code is called the Start of Active Video signal (SAV), and the end code is called the End of Active Video signal (EAV). The SAV and EAV codes proceed and follow valid data as shown in Figure 6. HD, VD, and FIELD are generated internally by the CCDC based on the SAV and EAV codes. Other CCDC register settings allow the user to control when valid data will be read/saved to DDR2/mDDR controller.

Figure 6. BT.656 Signal Interface



Both timing reference signals, SAV and EAV, consist of a four word sequence in the following format: FF 00 00 XY, where FF 00 00 are a set preamble and the fourth word defines the field identification, the state of vertical field blanking, the state of horizontal line blanking, and protection (error correction) codes. The bit format of the fourth word is shown in Table 8 and the definitions for bits, F, V, and H are given in Table 9. F, V, and H are used in place of the usual horizontal sync, vertical sync, and blank timing control signals. Bits P3, P2, P1, and P0 are protection (error correction) bits for F, V, and H. The relationship between F, V, and H and the protection (error correction) bits is given in Table 10. To enable error correction, set bit ECCFVH in the REC656IF register. The CCDC will automatically detect and apply error correction when ECCFVH is enabled.

Table 8. Video Timing Reference Codes for SAV and EAV

Data Bit Number	Data Bit Number	Second Word (00)	Third Word (00)	Fourth Word (XY)
9	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P3
4	1	0	0	P2
3	1	0	0	01
2	1	0	0	P0
1	1	0	0	0
0	1	0	0	0

Table 9. F, V, H Signal Descriptions

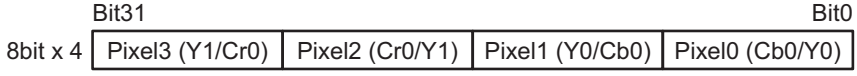
Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

Table 10. F, V, H Protection (Error Correction) Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

When operating in REC656 mode, data is stored in SDRAM according to the format shown in Figure 7.

Figure 7. BT.656 Mode Data Format in SDRAM



2.3 Generic YCbCr Interface Configuration

The CCD Controller can accept generic YCbCr-4:2:2 formatted digital video data over an 8/16 bit wide interface. Note that the BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with BT.601.

2.3.1 Generic YCbCr Configuration Signal Interface

Table 11 shows the interface connections for the generic YCbCr interface.

Unlike the BT.656 mode, discrete HD, and VD signals are required. An NTSC/PAL decoder is an example of an external device that may be connected to the YCbCr interface.

In 8-bit mode, data lines YIN[7:0] and CIN[7:0] can be used for input. When using an 8-bit interface, the YIN[7:0] inputs are typically used. However, either set of data inputs can be used or, alternately, two separate imagers can be physically connected (but only one can be active at any given time, though). A register setting (CCDCFG.YCINSWP) determines which set of 8-bit inputs are active. Note that if only the lower 8 bits are used, an additional SPI can be supported in this mode without interference.

In 16-bit mode, data lines YIN[7:0] and CIN[7:0] are used for input with the Cr/Cb data multiplexed on the CIN[7:0] signals. A register setting (CCDCFG.YCINSWP) can be used to swap the Y and Cr/Cb data lines.

Table 11. Interface Signals for Generic YCbCr Mode

Pin Name	I/O	Description
PCLK	Bidi	Pixel Clock
CAM_VD	Bidi	V sync
CAM_HD	Bidi	H sync
CIN7/SPI2_SCLK/GIO101	Bidi	C IN signal
CIN6/SPI2_SDO/GIO100	Bidi	C IN signal
CIN5/GIO099 SPI2_SDENA	Bidi	C IN signal
CIN4/GIO098 SPI2_SDENB/SPI2_SDI3	Bidi	C IN signal
CIN3 / GIO097	Bidi	C IN signal
CIN2 / GIO096	Bidi	C IN signal
CIN1 / GIO095	Bidi	C IN signal
CIN0 / GIO094	Bidi	C IN signal
YIN7 / GIO093	Bidi	Y IN signal
YIN6 / GIO092	Bidi	Y IN signal
YIN5 / GIO091	Bidi	Y IN signal
YIN4 / GIO090	Bidi	Y IN signal
YIN3 / GIO089	Bidi	Y IN signal
YIN2 / GIO088	Bidi	Y IN signal
YIN1 / GIO087	Bidi	Y IN signal
YIN0 / GIO086	Bidi	Y IN signal
GIO083	Bidi	GIO

2.3.2 Generic YCbCr Configuration Signal Interface Description

The digital YCbCr interface supports either 8-bit or 16-bit devices. The signal interface is described in Table 12.

Table 12. Table 16. YCbCr Interface Signals

Name	I/O	Description
CCD[15:0] = YI[7:0] / CI[7:0]	I	Image data. Mode set by INPMOD (not R656ON). • Bit width can be can be configured between 8 and 16 bits (DATSIZ) • The polarity of the input image data can be reversed (DATAPOL) • When 16-bit interface is used, the Y and C inputs can be swapped (YCINSWP) • When 8-bit interface is used, either half of the bus can be connected (YCINSWP) • When 8-bit interface is used, the position of the Y data can be set to either the even or odd pixel (Y8POS)
CAM_VD	I/O	VSYNC. This vertical sync signal can be configured as an input or an output (VDHDOUT). • When configured as an input, the CCD or CMOS sensor must supply the VD signal • When configured as an output, supplies the VD signal and the Vd width and lines per frame must be configured (VDW, HLPFR) • The polarity of VD can be reversed. (VDPOL)
CAM_HD	I/O	HSYNC. This horizontal sync signal can be configured as an input or an output (VDHDOUT). • When configured as an input, the CCD or CMOS sensor must supply the HD signal • When configured as an output, supplies the HD signal and the Hd width and pixels per line must be configured (HDW, PPLN) • The polarity of HD can be reversed (HDPOL)
CAM_WEN_FIELD	I	Field identification signal (optional – FLDMODE) • Supplied by the external CCD or CMOS sensor • Can be configured to be latched by the VD signal (FIDMD) • The polarity of the field identification signal can be reversed (FLDPOL)
PCLK	I	Pixel clock. This signal is used to load image data into the CCDC. • The CCDC can be configured to capture on either the rising or falling edge of the PCLK signal (PCLK_INV in SYSTEM module)

2.3.3 Generic YCbCr Configuration Protocol and Data Formats

In 8-bit mode, the position on the Y data in relation to Cr/Cb data can be configured by the register setting:`CCDCFG.Y8POS`.

The byte ordering of data can be swapped by the register setting: `CCDCFG.BSWD`.

Table 13. DDR2/mDDR Controller Storage Format for YCbCr Processing

	Upper Word		Lower Word	
SDRAM Address	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr2	Y2	Cb2
N + 2	Y5	Cr4	Y4	Cb4

2.4 VPFE I/O Multiplexing

The various VPFE Imager interfaces modes have unique pin multiplexing options as shown in Table 14. Some of these settings are controlled in the System Module, described in detail in the *TMS320DM335 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFX7). The remaining settings are controlled via the mode in which the controller is placed.

Table 14. Signals for VPFE Digital Capture Modes

Pin Name	Serial In	Parallel RAW	Parallel YCC16	Parallel YCC8	REC656
PCLK	GIO082	PCLK	PCLK	PCLK	PCLK
CAM_VD	GIO084	VD	VD	VD	GIO084
CAM_HD	GIO085	HD	HD	HD	GIO085
CIN7	SPI2_SCLK/ GIO101	SPI2_SCLK/ GIO101	C7/Y7	Y7,Cb7,Cr7/ SPI2_SCLK/ GIO101	SPI2_SCLK/ GIO101
CIN6	SPI2_SDO/ GIO100	SPI2_SDO/ GIO100	C6/Y6	Y6,Cb6,Cr6/ SPI2_SDO/ GIO100	SPI2_SDO/ GIO100
CIN5	GIO099/ SPI2_SDENA	D[13]/GIO099/ SPI2_SDENA	C5/Y5	Y5,Cb5,Cr5/ SPI2_SDENA/ GIO099	SPI2_SDENA/ GIO099
CIN4	GIO098/ SPI2_SDENB/ SPI2_SDI3	D[12]/GIO098/ SPI2_SDEN/ PI2_SDI3	C4/Y4	Y4,Cb4,Cr4/ SPI2_SDENB/ SPI2_SDI3/ GIO098	SPI2_SDENB/ SPI2_SDI3/ GIO098
CIN3	GIO097	D[11]	C3/Y3	Y3,Cb3,Cr3	GIO097
CIN2	GIO096	D[10[	C2/Y2	Y2,Cb2,Cr2	GIO096
CIN1	GIO095	D[9]	C1/Y1	Y1,Cb1,Cr1	Y9,Cb9,Cr9
CIN0	GIO094	D[8]	C0/Y0	Y0,Cb0,Cr0	Y8,Cb8,Cr8
YIN7	GIO093	D[7]	Y7/C7	Y7,Cb7,Cr7	Y7,Cb7,Cr7
YIN6	GIO092	D[6]	Y6/C6	Y6,Cb6,Cr6	Y6,Cb6,Cr6
YIN5	GIO091	D[5]	Y5/C5	Y5,Cb5,Cr5	Y5,Cb5,Cr5
YIN4	GIO090	D[4]	Y4/C4	Y4,Cb4,Cr4	Y4,Cb4,Cr4
YIN3	GIO089	D[3]	Y3/C3	Y3,Cb3,Cr3	Y3,Cb3,Cr3
YIN2	GIO088	D[2]	Y2/C2	Y2,Cb2,Cr2	Y2,Cb2,Cr2
YIN1	GIO087	D[1]	Y1/C1	Y1,Cb1,Cr1	Y1,Cb1,Cr1
YIN0	GIO086	D[0]	Y0/C0	Y0,Cb0,Cr0	Y0,Cb0,Cr0
CAM_WEN_FIELD	GIO083	WEN/FIELD/ GIO083	WEN/FIELD/ GIO083	WEN/FIELD/ GIO083	GIO083

2.4.1 SPI and GIO Signal Multiplexing

The SPI2 peripheral and several GIOs may be made available to the system depending on the pin usage of the particular capture mode used by the VPFE. Table 14 shows which pins are required by the VPFE for particular image capture modes and which pins can be made available for use by the SPI2 peripheral and/or extra GIOs. The PINMUX0 register shown in Table 14 must be programmed according to the appropriate capture mode.

2.4.2 Y/C Data BUS Swap

There is an option to swap the upper and lower portion of the 16-bit YCbCr data bus (`CCDC.CCDCFG.YCINSWP`). This will swap the luma and chroma samples in 16-bit YCbCr mode. This will determine which half of the bus is used as the input source in 8-bit mode and can be used in 8-bit YCbCr mode to support two separate YCbCr input ports.

2.4.3 WEN/FIELD Signal Selection

Since the field ID and the write enable signal share the same pin, only one of these external signals can be connected. To enable the FIELD ID input, bit-5 of the CCDC.MODESET register should be set to INTERLACE MODE. To enable the write enable (WEN) signal, bit-7 of CCDC.MODESET register should be set. These two bits should not be set concurrently or indeterminate results may occur.

2.4.4 Pin Mux 0 Register (PINMUX0)

The PINMUX0 register controls pin multiplexing for the VPFE pins. The pin mux 0 register (PINMUX0) is shown in Figure 8 and described in Table 15. The address for this register is 0x01C4:0000.

Figure 8. Pin Mux 0 Register (PINMUX0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved	PCLK	CAM_WEN_FIELD	CAM_VD	CAM_HD	YIN_70	CIN_10	CIN_32
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CIN_4		CIN_5		CIN_6		CIN_7	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Pin Mux 0 Register (PINMUX0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	PCLK		PCLK pin function
		0	GIO082
		1	PCLK
13	CAM_WEN_FIELD		CAM_WEN_FIELD pin function
		0	GIO083
		1	CAM_WEN_FIELD
12	CAM_VD		CAM_VD pin function
		0	GIO084
		1	CAM_VD
11	CAM_HD		CAM_HD pin function
		0	GIO085
		1	CAM_HD
10	YIN_70		YIN0 – YIN7 pin functions
		0	GIO086, GIO087, GIO088, GIO089, GIO090, GIO091, GIO092, GIO093
		1	YIN0, YIN1, YIN2, YIN3, YIN4, YIN5, YIN6, YIN7
9	CIN_10		CIN0 & CIN1 pin functions
		0	GIO094, GIO095
		1	CIN2, CIN3
8	CIN_32		CIN2 & CIN3 pin functions
		0	GIO096, GIO097
		1	CIN2, CIN3

Table 15. Pin Mux 0 Register (PINMUX0) Field Descriptions (continued)

Bit	Field	Value	Description
7-6	CIN_4	0-3h	CIN4 pin function
		0	GIO098
		1h	CIN4
		2h	SPI2_SDI3
		3h	SPI2_SDENB
5-4	CIN_5	0-3h	CIN5 pin function
		0	GIO099
		1h	CIN5
		2h	SPI2_SDENA
		3h	Reserved
3-2	CIN_6	0-3h	CIN6 pin function
		0	GIO100
		1h	CIN6
		2h	SPI2_SDO
		3h	Reserved
1-0	CIN_7	0-3h	CIN7 pin function
		0	GIO101
		1h	CIN7
		2h	SPI2_SCLK
		3h	Reserved

3 VPFE/ISP Integration

This section describes how the VPFE/ISP subsystem is integrated, including any interactions it may have with other subsystems on the device.

3.1 Clocking, Reset and Power Management Scheme

3.1.1 Clocks

There are five clock domains in the VPFE:

Table 16. Clock Domains

Name	Frequency	Description
MMR	PLL1/4	Used for clocking the memory-mapped register (MMR) port for the control registers
DMA	PLL1/4	Used for clocking the DMA port for data transfers to and from the DDR2/mDDR controller.
VPSSCLK	PLL1/(2 or 4)	Used for clocking the VPFE module internal logic. This is programmable in the PLL1 controller. The VPSSCLK divider should be programmed such that the VPSSCLK < 144MHz. Please reference the PLLC documentation for information on configuring this clock.
Parallel	< VPSSCLK/2	If the CCDC receives data via the parallel imager interface: this is the external pixel clock (PCLK) driven by the imager. This must be < VPSSCLK/2

Note that there is an option to drive the VPBE module with the VPFE pixel clock (PCLK).

3.1.2 Resets

The VPFE module resets are tied to the device reset signals.

In addition, the VPSS modules can be reset by transitioning to the SyncReset state of the PSC. Note that the VPSS has two module domains, the VPSSmstr processing domain and the VPSSslv register interface.

3.1.3 Power Management

When powered, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. When the VPSS is not required for the application, its MMR clocks (VPSSslv) and operating clocks (VPSSmstr) can be gated by the Power Sleep Controller (PSC) to conserve dynamic power.

Additionally, when certain sub-modules within the VPFE are not required for the application mode, they can be disabled by software by configuring the VPSSCLK.CLKCTRL register appropriately.

3.2 Hardware Requests

The VPSS can generate the 13 interrupts/events shown in Table 17. However, only nine of them can be sent to the ARM as interrupts and four of them can be sent to the EDMA as events. A mapping of which events are sent to the ARM and EDMA can be configured in the VPSSBL.INTSEL and VPSSBL.EVTSEL registers. The VPSSBL.INTSTAT register can also be used to poll for events. More details on each module's events can be found in Section 5.

Table 17. VPSS Events

Event Number	Acronym	Module	Description
0	CCDC VDINT0	CCDC	Triggered after a programmable number of input lines for each frame.
1	CCDC VDINT1	CCDC	Triggered after a programmable number of input lines for each frame.
2	CCDC VDINT2	CCDC	Triggered at the rising edge of WEN signal
3	H3AINT	H3A	Triggered at the end of AF or AEW writes to DDR for each frame
4	VENCINT	VENC	Triggered at the rising edge of VSYNC
5	OSDINT	OSD	Triggered at the end of each frame read from DDR
6	IPIPEIFINT	IPIPEIF	Triggered at the rising edge of VD if enabled
7	IPIPE_INT0_HST	IPIPE	Triggered when Histogram processing is finished for each frame
8	IPIPE_INT1_SDR	IPIPE	Triggered when writes to DDR are finished for each frame
9	IPIPE_INT2_RZA	IPIPE	Triggered when the number of lines programmed has been output of RZA
10	IPIPE_INT3_RZB	IPIPE	Triggered when the number of lines programmed has been output of RZB
12	IPIPE_INT5_MMR	IPIPE	Triggered when MMR modifications for the next frame can be made

3.2.1 Interrupt Requests

The 9 interrupts selected in the VPSSBL.INTSEL and VPSSBL.EVTSEL registers are assigned to the ARM interrupt controller as shown in Table 18.

Table 18. ARM Interrupts - VPSS

INT Number	Acronym
0	VPSSINT0
1	VPSSINT1
2	VPSSINT2
3	VPSSINT3
4	VPSSINT4
5	VPSSINT5
6	VPSSINT6
7	VPSSINT7
8	VPSSINT8

3.2.2 EDMA Requests

The four events selected in the VPSSBL.EVTSEL register are assigned to the EDMA as shown in Table 19.

Table 19. EDMA Events - VPSS

Event Number	Binary	Event Name
4	0000100	VPSSEVT1
5	0000101	VPSSEVT2
6	0000110	VPSSEVT3
7	0000111	VPSSEVT4

The primary reason for using an EDMA event from the VPSS is to allow for an update of the module registers by using the DMA scheme vs. direct CPU write. Normally, the ARM performs this function, but in some cases the ARM can be tied up with other activities and the interrupt latency is critical when dealing with the VPFE modules. Consider the following example: a still image is processed by the Image Pipe. Since the still image is too wide for a single pass through the Image Pipe, several passes are required. The Image Pipe registers need to be altered as soon as each pass is complete. Tying an IPIPE event to the EDMA allows instantaneous DMA of the new register settings for the subsequent passes.

3.3 VPSS Top-Level Register Mapping Summary

Table 20. VPFE Module Register Map

VPSS Registers	Address Range		Size
VPSSCLK	0x01C70000	0x01C7007F	128B
H3A	0x01C70080	0x01C700FF	128B
IPIPEIF	0x01C70100	0x01C701FF	256B
OSD	0x01C70200	0x01C702FF	256B
VENC	0x01C70400	0x01C705FF	512B
CCDC	0x01C70600	0x01C707FF	512B
VPSSBL	0x01C70800	0x01C708FF	256B
IPIPE	0x01C71000	0x01C73FFF	12K

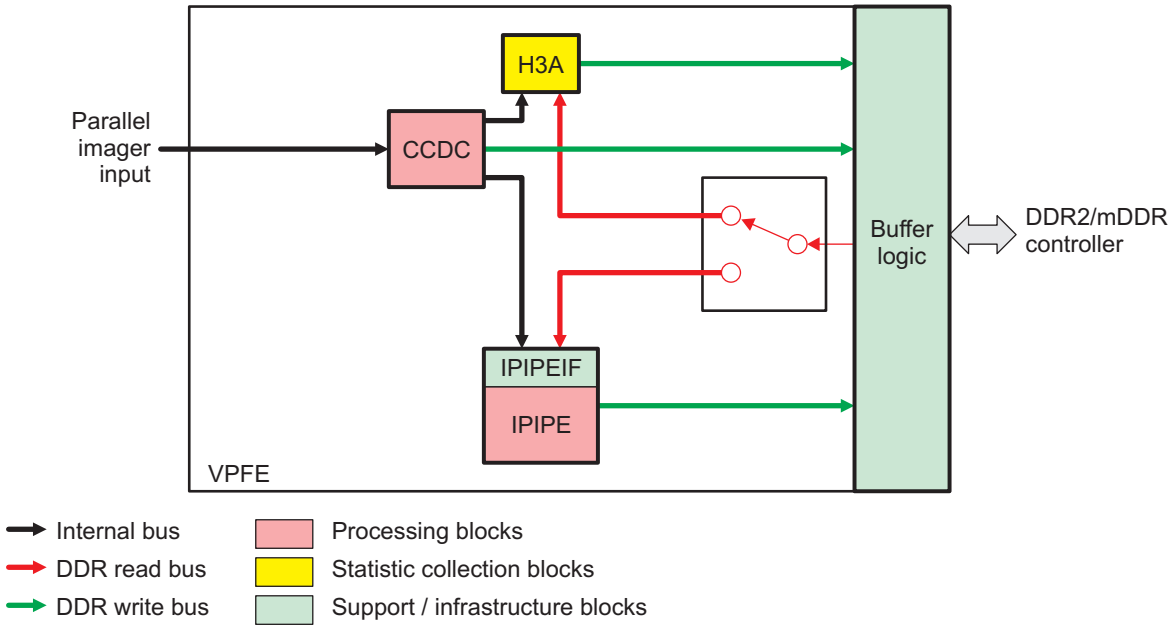
3.4 VPFE/ISP Top-Level Signal Interaction

In the system, the CCDC_VD signal drives the event-trigger input signal of all four PWM modules. The PWM can configure the trigger to detect the rising or falling edge of the CCDC_VD signal. This capability is provided to allow the PWM module to be used as a CCDC timer.

4 VPFE/ISP Functional Description

The VPFE block diagram is shown in Figure 9. Additional detailed block diagrams are shown in the interface and image processing sub-sections.

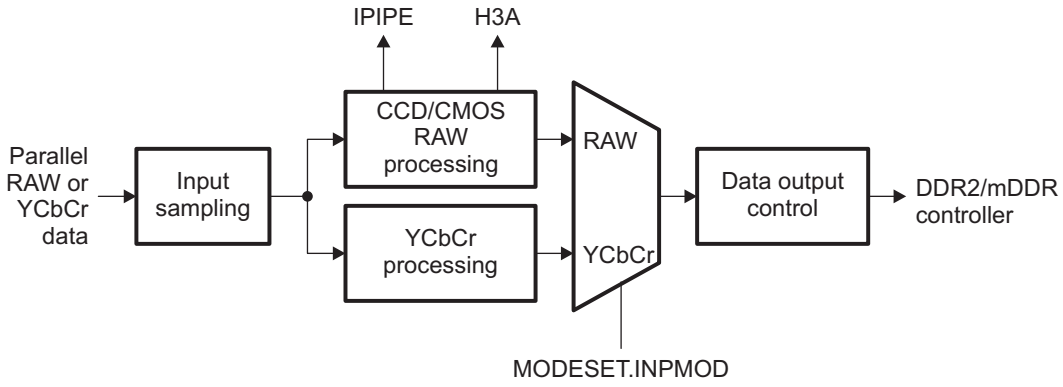
Figure 9. Video Processing Front End (VPFE) Block Diagram



4.1 CCD/CMOS Controller (CCDC)

The CCD Controller interfaces with external image sources, not just CCD sensors. It supports both RAW Bayer data from CCD/CMOS sensors and processed YCbCr data from either a CMOS sensor with integrated image processing or a Video Decoder interface. A high-level block diagram of the CCD Controller is shown in Figure 10.

Figure 10. CCD Controller – Top Level Block Diagram

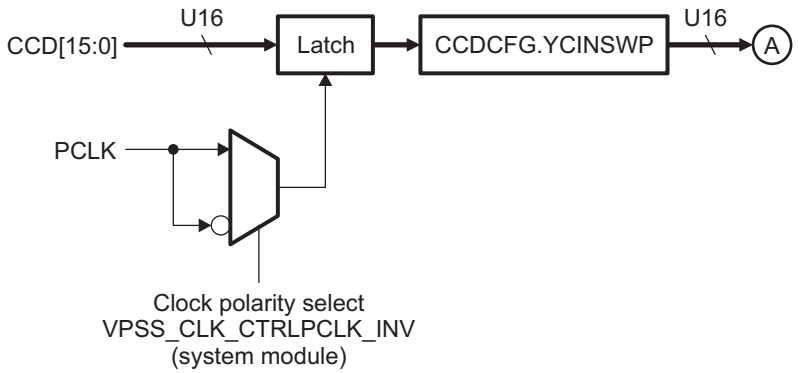


4.1.1 CCDC Input Sampling

The CCD/CMOS Controller input sampling and formatting is shown in Figure 11.

- Data is latched by the pixel clock
- Pixel clock polarity can be either rising or falling edge. This is set in the system module via the register.field: VPSS_CLK_CTRL.PCLK_INV
- There is an option to swap the upper and lower portion of the 16-bit YCbCr data bus (`CCDCFG.YCINSWP`). This will swap the luma and chroma samples in 16-bit YCbCr mode. This will determine which half of the bus is used as the input source in 8-bit mode and can be used in 8-bit YCbCr mode to support two separate YCbCr input ports. Since this bit affects both RAW and YCbCr input modes, `CCDCFG.YCINSWP` should always be set to 0 in RAW input mode (`MODESET.INPMOD= 0`) .

Figure 11. CCD Controller – Input Formatting



4.1.2 CCD/CMOS RAW Data Processing

The following sections describes the CCD controller processing for the CCD/CMOS RAW data input mode (`MODESET.INPMOD = 0 && REC656IF.REC656ON = 0`) in more detail. In this mode, RAW sensor data, typically one color per pixel in a color filter array (or CFA) at 8 to 6-bits in dynamic range is input (usually between 10-14 bits). The color filter array applied is typically a Bayer pattern as show below for RGB color space. Complementary (Yellow, Cyan, Green, and Magenta) color filters are also supported via the color space converter.

Figure 12. CCD Controller Color Patterns

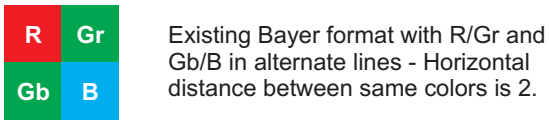
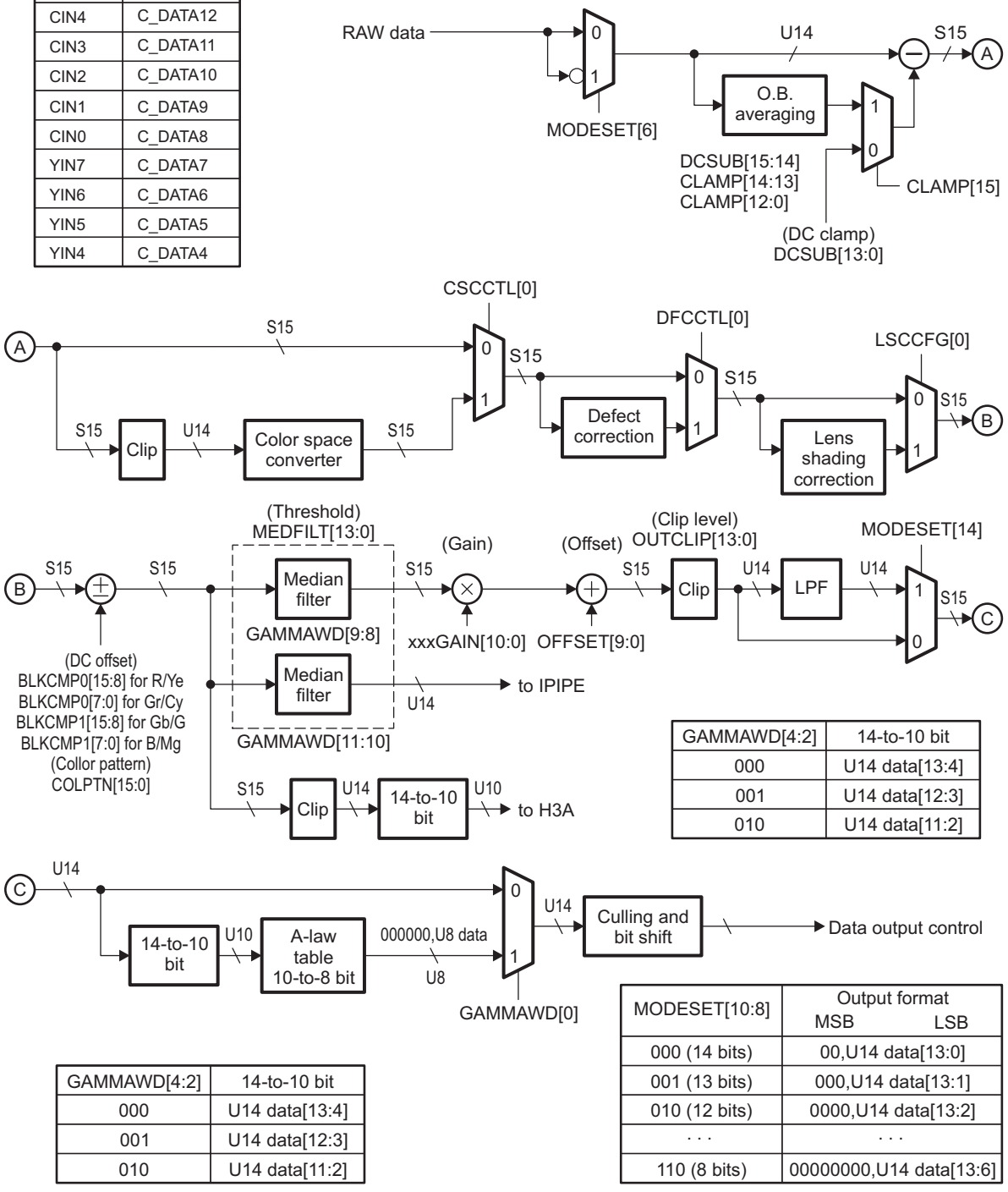


Figure 13 shows the data flow of the CCD/CMOS RAW data processing. The first optional operation of the RAW data flow is data inversion. Data can be interpreted as either normal or inverted by setting the MODESET.DATAPOL register field.

Figure 13. CCD/CMOS Controller RAW Data Processing Flow

Pin name	Signal name
CIN5	C_DATA13
CIN4	C_DATA12
CIN3	C_DATA11
CIN2	C_DATA10
CIN1	C_DATA9
CIN0	C_DATA8
YIN7	C_DATA7
YIN6	C_DATA6
YIN5	C_DATA5
YIN4	C_DATA4



GAMMAWD[4:2]	14-to-10 bit
000	U14 data[13:4]
001	U14 data[12:3]
010	U14 data[11:2]

GAMMAWD[4:2]	14-to-10 bit
000	U14 data[13:4]
001	U14 data[12:3]
010	U14 data[11:2]

MODESET[10:8]	Output format MSB LSB
000 (14 bits)	00,U14 data[13:0]
001 (13 bits)	000,U14 data[13:1]
010 (12 bits)	0000,U14 data[13:2]
. . .	. . .
110 (8 bits)	00000000,U14 data[13:6]

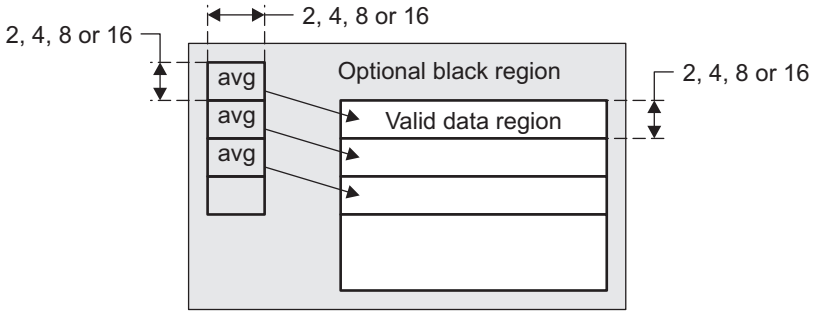
4.1.2.1 Digital Clamp

Sensor manufacturers typically provide some optically masked pixels at the beginning/end of each line to allow the user to determine the noise floor on any given frame of data. The optical black clamping function provides a means to average the optically black pixels and subtract that value from each input pixel as a first step in reducing the noise on the input pixels.

The averaging circuit takes an average of masked (black) pixel values from the image sensor and this value is subtracted from the image data in the next DCSUB.OBSLN number of lines. The user can control the starting position of the black pixels (CLAMP.OBST), the number of pixels (2, 4, 8, or 16) in each line averaged (CLAMP.OBSLEN), and the number of lines (2, 4, 8, or 16) averaged (DCSUB.OBSLN).

Alternately, the user can disable black clamp averaging (CLAMP.CLAMPEN), and select a constant black value for subtraction (DCSUB.DCSUB), instead of using the calculated average value.

Figure 14. CCD Controller Optical Black Averaging and Application



4.1.2.2 Color Space Conversion

Color space converter (CSC) includes four 8-bit × 10-bit multipliers and one adder for the color space conversion. These multiplier/adder units are used for the operation described in Figure 15. Data are taken from two input lines during the operation.

Figure 15. Color Space Converter Functional Block Diagram

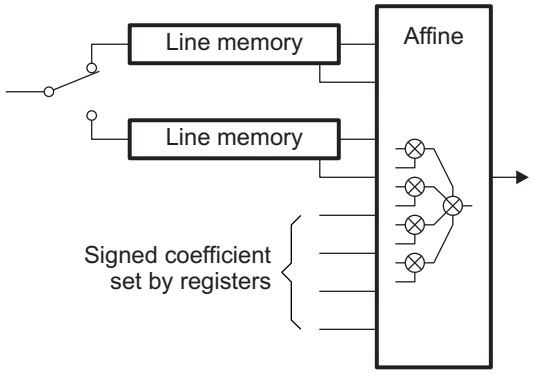
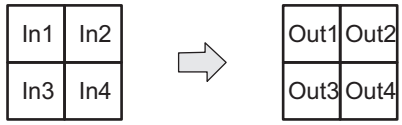


Figure 16. Color Space Converter Operation

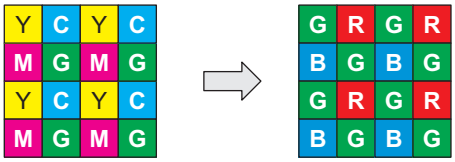


$$\begin{bmatrix} Out1 \\ Out2 \\ Out3 \\ Out4 \end{bmatrix} = \begin{bmatrix} M00 & M01 & M02 & M03 \\ M10 & M11 & M12 & M13 \\ M20 & M21 & M22 & M23 \\ M30 & M31 & M32 & M33 \end{bmatrix} \begin{bmatrix} In1 \\ In2 \\ In3 \\ In4 \end{bmatrix}$$

M00-M33: Signed 8-bits data with 5-bit decimal
the value range -4 =< Mxx < 4

Coefficients are signed 8-bit (decimal is 5-bits). The CSC can convert CMYG filtered CCD data to Bayer matrix (RGBG) data as shown in Figure 17.

Figure 17. Color Space Converter Operation



$$\begin{bmatrix} G \\ R \\ B \\ G \end{bmatrix} = \begin{bmatrix} 0.5 & 0.5 & -0.5 & 0 \\ 0.5 & -0.5 & 0.5 & 0 \\ -0.5 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} Y \\ C \\ M \\ G \end{bmatrix}$$

The following figures explain which input pixels are used for the operation. There is a one-line latency between the input and the output. In addition to the registers specific to the color space converter, the following registers are needed to configure the valid area: FMTSPH, FMTLNH, FMTSLV, and FMTLNV. There should be at least one invalid pixel at the end of the line, and also one invalid line at the end of the frame.

Figure 18. Color Space Conversion

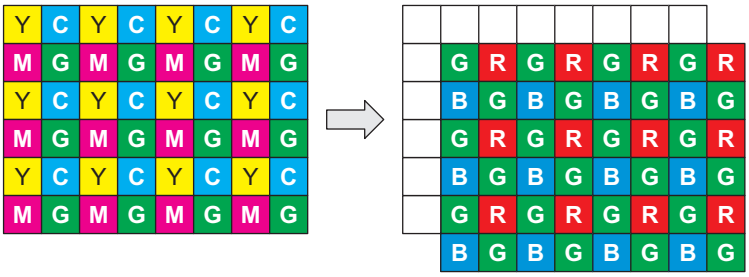


Figure 19. First Pixel/First Line Generation

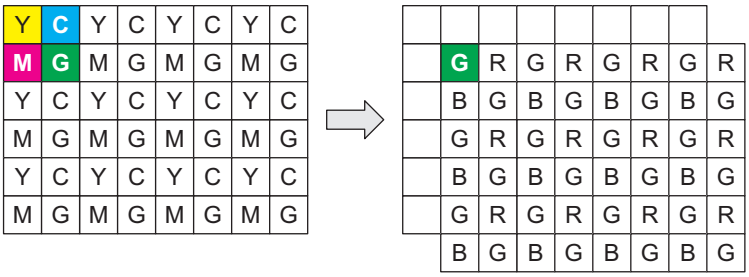


Figure 20. Second Pixel/First Line Generation

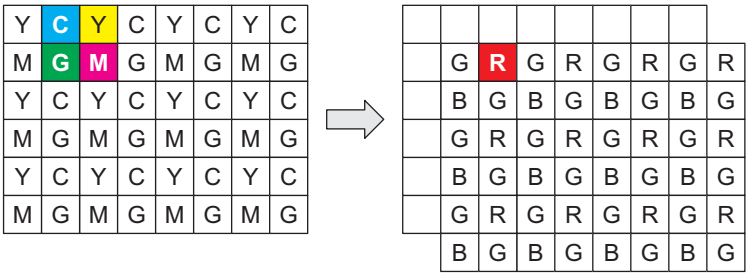


Figure 21. Second Last Pixel/First Line Generation

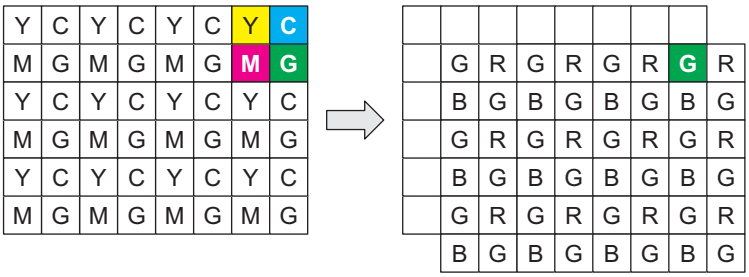
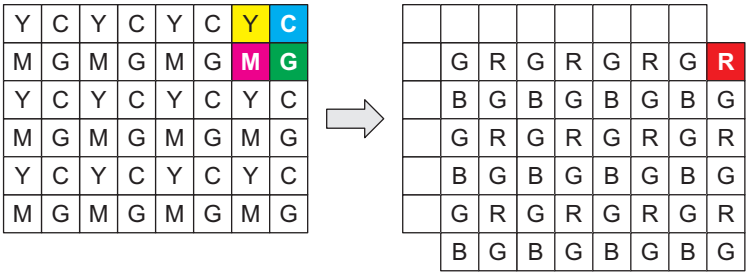


Figure 22. Last Pixel/First Line Generation



As shown in Figure 21 and Figure 22, the operation for the last pixel and the second to last pixel uses the same input data. Also the operation for the last line and the second to last line uses the same input data.

Figure 23. First Pixel/Last Line Generation

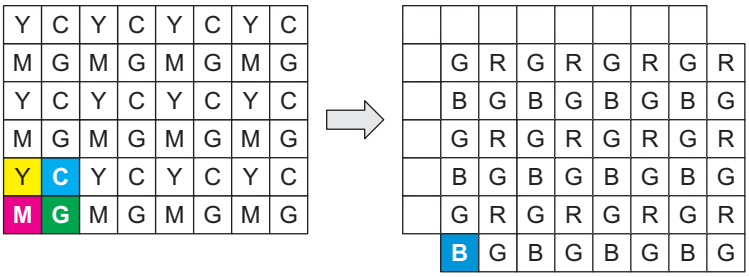


Figure 24. Second Pixel/Last Line Generation

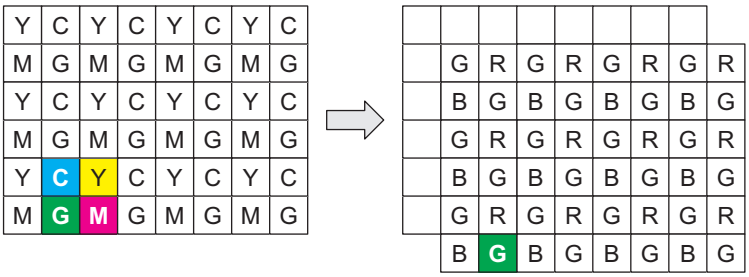


Figure 25. Second Last Pixel/Last Line Generation

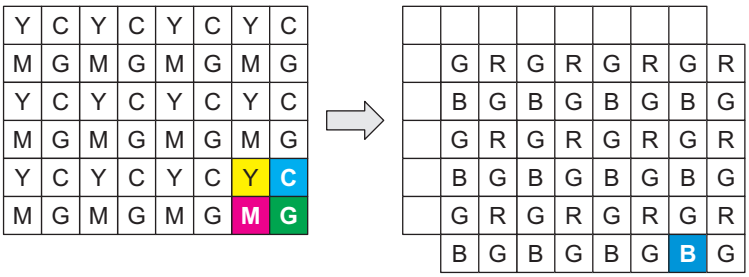
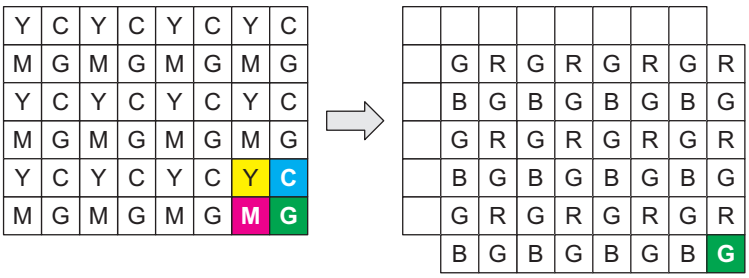


Figure 26. Last Pixel/Last Line Generation



4.1.2.3 Defect Correction

The defect correction block can correct up to 1,024 defects. The coordinates of the defects need to be set to the memory prior to the processing using the IPIPE registers: RAM_ADR & RAM_WDT. If the current pixel (I) is identified as a defect, it will be replaced by the average of pixel (I - 2) and pixel (I + 2), or just copied from (I - 2) or (I + 2). This block can also correct up to 16 vertical line defects.

4.1.2.4 Lens Shading Correction

Some optics show significant Lens Shading, the phenomenon that the image is bright in the center and decrease in brightness towards the edge of the field. To compensate this effect, each pixel's illumination is controlled according to the distance from the optical center. The shading correction is performed on a color-by-color basis.

4.1.2.5 Black Level Compensation

In this operation, a fixed offset can be applied to the data depending on the color; i.e., R/Ye, Gr/Cy, Gb/G, and B/Mg. The offset (`BLKCMP0.R_YE`, `BLKCMP0.GR_CY`, `BLKCMP1.GB_G`, `BLKCMP1.B_MG`), applied to each data sample is selected according to the even/odd phase and the color (0/1/2/3) specified for each pixel position (`COLPTN`).

4.1.2.6 Median Filter

The median filter block has two separate filters: one for the output to SDRAM, and another for the output to IPIPE. Each of these filters can be individually disabled, enabled as an average filter, or enabled as a median filter (`GAMMAWD.MFILT1` and `GAMMAWD.MFILT2`).

4.1.2.6.1 Average Filter Configuration

The average filter calculates the absolute difference between the current pixel (I) and the pixel (I - 2), and between the current pixel (I) and the pixel (I + 2). If the absolute differences exceeds the threshold (`MEDFILT.MFTHR`), the average of pixel (I - 2) and pixel (I + 2) replaces pixel (I). Filter's threshold is configurable and the filter can be either enabled or disabled.

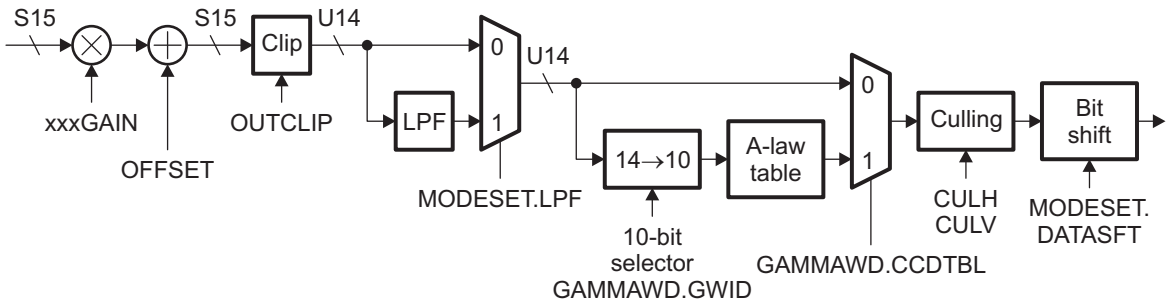
4.1.2.6.2 Median Filter Configuration

The median filter corrects the current pixel if it differs from both same-color neighbors by more than a programmable threshold. If the pixel is faulty, it is replaced by the median of the 3 pixels.

4.1.2.7 SDRAM RAW Output Formatting

The final stage of the CCD/CMOS RAW data processing is the SDRAM RAW output formatter, as shown in Figure 27. This module includes separate color gains, offset, clip, optional low-pass filtering, a-law compression, culling, and a final bit shift of the data being stored to SDRAM.

Figure 27. Output Formatter Functional Model



4.1.2.7.1 Gain, Offset, and Clip

A gain factor from 0 to 7.9921875 can be applied separately to each color of the output of the median filter for SDRAM output (RYEGAIN, GRCYGAIN, GBGGAIN, and BMGGAIN). After multiplying the data by the gain factor, a single offset value can be added to the result (OFFSET). The offset can range from 0 to 1023. The result of gain control is clipped to signed 15-bit data after offset control. The output can additionally be clipped to a user programmed value (OUTCLIP), which is defaulted to unsigned 14-bit data.

4.1.2.7.2 Low Pass Filter

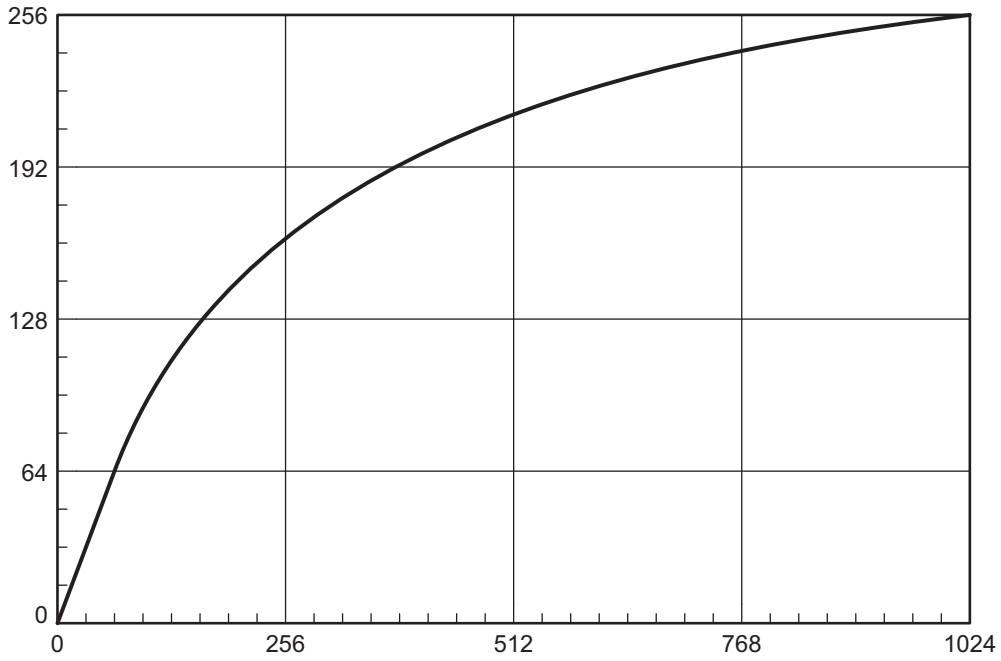
The output formatter block provides an option for applying an anti-aliasing filter (MODESET.LPF) for bandwidth reduction if horizontal culling is enabled. The low-pass filter consists of a simple three-tap (1/4, 1/2, 1/4) filter. Two pixels on the left and two pixels on the right of each line are cropped if the filter is enabled.

4.1.2.7.3 A-Law Transformation

An optional 10-to-8-bit A-Law transformation using a fixed A-Law table can be applied (GAMMAWD.CCDTBL) to the LPF output. Using this causes the data width to be reduced to 8-bits and allows packing to 8-bits/pixel when saving to DDR2/mDDR controller for buffer memory reduction. Since the data resolution is greater than 10-bits at this stage, the 10-bits for input to the A Law operation must be selected (GAMMAWD.GWID). The A-law table has a same characteristic as the Voice codec and is shown in Figure 28.

Note that IPIPEIF has an inverse A-Law table option so it can reverse this non-linear operation if this saved data is to be read back in for further processing.

Figure 28. A-Law Table



4.1.2.7.4 Culling

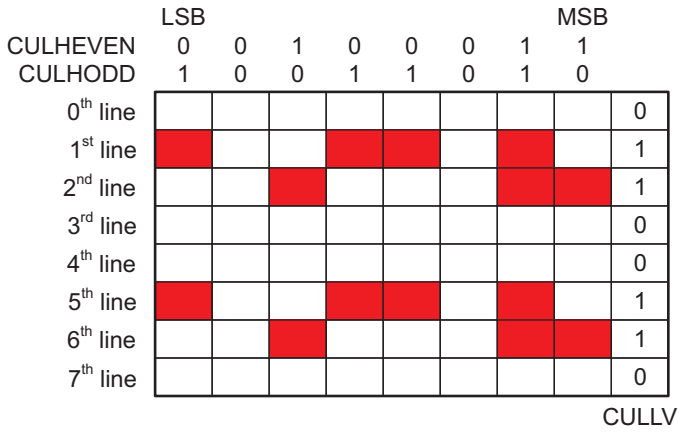
The culling module performs a programmable decimation function for both horizontal and vertical directions.

The horizontal and vertical decimation of CCD data can be controlled by two registers. The 16-bit CULH register specifies the horizontal culling pattern for even and odd lines. The 8-bit CULV register specifies the pattern for the vertical direction. The LSB of CULV represent the top line of the CCD, the MSB is the seventh line.

Figure 29 is an example showing how CULH and CULV apply a decimation pattern to the data. The shaded pixels are transferred to SDRAM. In this case:

- CULH.CULHEVN = 0x59
- CULH.CULHODD = 0xC4, and
- CULV.CULV = 0x66

Figure 29. Example for Decimation Pattern



4.1.2.7.5 Bit Shift

The final stage in the CCD/CMOS RAW data output formatter is a bit shift function. The MODESET.DATASFT field can be programmed to right-shift the RAW data to be stored to SDRAM up to 6 bits.

4.1.2.8 SDRAM Data Storage

The data bits comprising each pixel are stored in the lower bits of a 16-bit SDRAM word and the unused bits are zero-filled. The SDRAM data format is shown in Figure 30, with the format used determined by the MODESET.DATASFT setting for all but the packed format. If 8-bit data is input, or if the A-Law compression is applied in RAW input mode, the data can be packed via the MODESET.PACK8 setting so that a pixel will only occupy 8-bits.

Figure 30. SDRAM Output Format

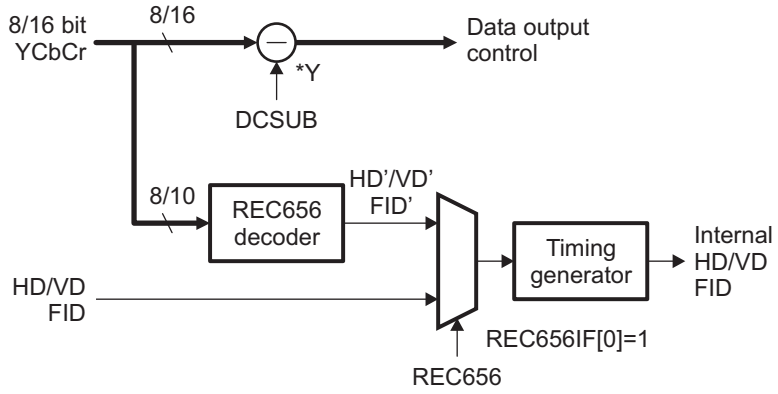
	Upper word		Lower word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
14 bit	0	Pixel 1	0	Pixel 0
13 bit	0	Pixel 1	0	Pixel 0
12 bit	0	Pixel 1	0	Pixel 0
11 bit	0	Pixel 1	0	Pixel 0
10 bit	0	Pixel 1	0	Pixel 0
9 bit	0	Pixel 1	0	Pixel 0
8 bit	0	Pixel 1	0	Pixel 0
8 bit pack	Pixel 3	Pixel 2	Pixel 1	Pixel 0

4.1.3 YCbCr Data Processing

The following sections describe the CCD controller processing for the YCbCr data input mode (MODESET.INPMOD = 1 or 2 || REC656IF.REC656ON = 1) in more detail. In this mode, YCbCr 4:2:2 data typically at 8-bits per luma/chroma sample is input.

Figure 31 shows the data flow of the YCbCr data processing.

Figure 31. CCD/CMOS Controller YCbCr Data Processing Flow



4.1.3.1 DC Subtract

An offset can optionally be subtracted from the luma (Y) component of the data by programming the DCSUB.DCSUB register field. Please note that in YCbCr processing, the CLAMP.CLAMPEN field must be disabled 0 or indeterminate results may occur.

4.1.3.2 REC656 Mode

Processing of the data in REC656 mode is identical to that of the other YCbCr modes; however, there is an additional decoder block that extracts the sync information from the data signal and generates the HD/VD/Field signals for downstream processing. Data at 10-bit resolution is reduced to 8 bits before being saved to SDRAM.

4.1.3.3 SDRAM Data Storage

In packed YCbCr 4:2:2 mode, data is stored in SDRAM with two pixels per 32 bits, as shown in Table 21. If the input mode is not 16 bits, then this packing of data must be achieved by setting the MODESET.PACK8 bit.

Table 21. YCbCr Mode SDRAM Output Format

	Upper Word		Lower Word	
SDRAM Address	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr1	Y2	Cb1
N + 2	Y5	Cr2	Y4	Cb2

4.1.4 Data Output Control

Data output to SDRAM is enabled via the MODESET.WEN setting.

The MSB of the chroma signal can also be inverted (CCDCFG.MSBINVI).

The CCD/CMOS Controller's final stage is the Line Output Control, which controls how the input lines are written to DDR2/mDDR controller. The values SRADRH and SRADRL define the starting address where the frame should be written in SDRAM. The value HSIZE.LNOFST defines the distance between the beginning of output lines, in bytes. Both the starting address and line offset values are programmed in 32-byte units; i.e., either 16 or 32 pixels, depending on the MODESET.PACK8 setting. The HSIZE.ADR_UPDT register bit can be set to decrement the addresses across each line to invert an image horizontally. The register SDOFST can be used to define additional offsets depending on the Field ID and even/odd line numbers. This provides a means to de-interlace an interlaced, 2-field input and also to invert an input image vertically. See Figure 32 and Figure 33 for some example usage.

- SDOFST.FIINV – invert interpretation of the Field ID signal
- SDOFST.FIINV – invert interpretation of the Field ID signal
- SDOFST.LOFTS0 – offset, in lines, between even lines on even fields (field 0)
- SDOFST.LOFTS1 – offset, in lines, between odd lines on even fields (field 0)
- SDOFST.LOFTS2 – offset, in lines, between even lines on odd fields (field 1)
- SDOFST.LOFTS3 – offset, in lines, between odd lines on odd fields (field 1)

Figure 32. Frame Image Format Conversion

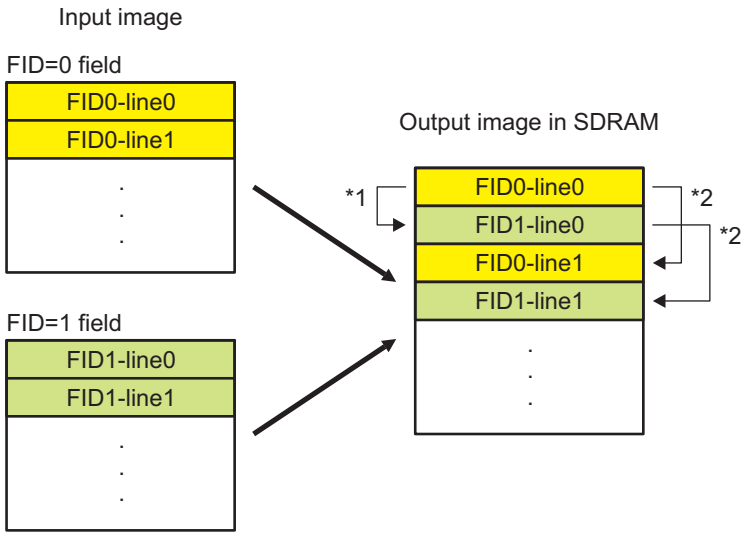
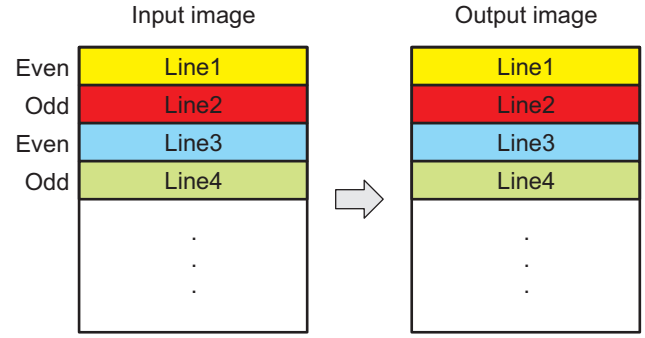
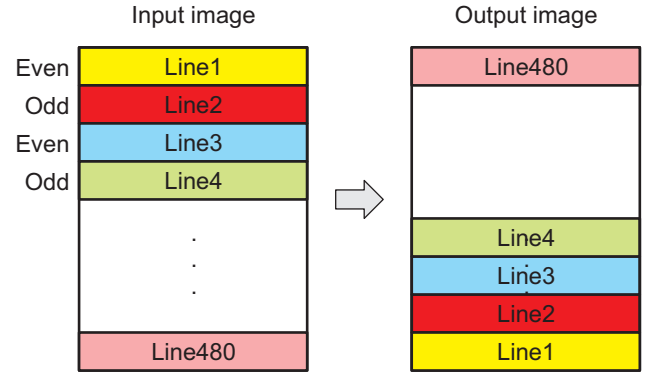


Figure 33. Example Formats of Input and Output Image




```
SDOFST[14] = 0          ;Non inverse
SDOFST[13:12] = 00B     ;+1 line when field ID is 1
SDOFST[11:9] = 001B     ;+2 line, even line and field ID = 0
SDOFST[8:6] = 001B      ;+2 line, odd line and field ID = 0
SDOFST[5:3] = 001B      ;+2 line, even line and field ID = 1
SDOFST[2:0] = 001B      ;+2 line, odd line and field ID = 1
```

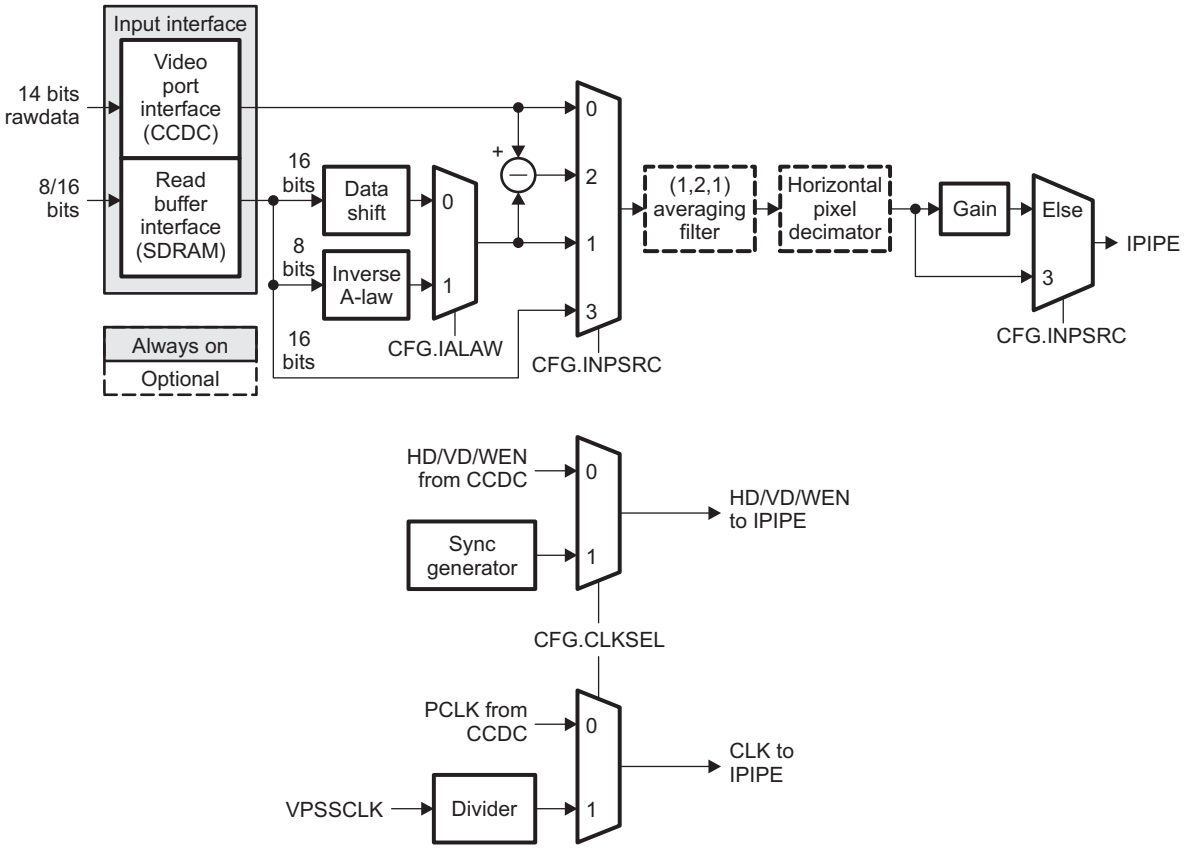



```
SDOFST[14] = 1          ;Non inverse
SDOFST[13:12] = 000B    ;-1 line when field ID is 1
SDOFST[11:9] = 101B     ;-2 line, even line and field ID = 0
SDOFST[8:6] = 101B      ;-2 line, odd line and field ID = 0
SDOFST[5:3] = 101B      ;-2 line, even line and field ID = 1
SDOFST[2:0] = 101B      ;-2 line, odd line and field ID = 1
```

4.2 Image Pipe Interface (IPIPEIF)

The IPIPE Interface (IPIPEIF) is the data and sync signals input interface module for the IPIPE. The rest of this section describes, in detail, the functionality of each sub-block in the IPIPEIF as shown in Figure 34.

Figure 34. Image Pipe Interface Processing Flow

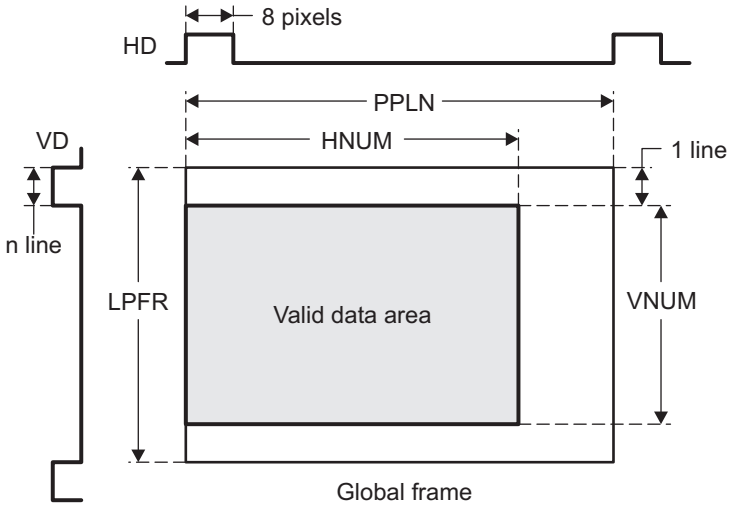


4.2.1 Input Interface and Preprocessing

The Image Pipe I/F can receive data from both the video port interface via the CCD/CMOS Controller module and from the read buffer interface via SDRAM/DDRAM. The input sources and data type (RAW or YCbCr) are configured in the CFG.INPSRC register field. The four available options for input source/type combinations and any preprocessing operations are discussed further in the following sub-sections.

When input from SDRAM/DDRAM is required, the SDRAM/DDRAM address (ADDRU, ADDRL) and line offset (ADOFS) registers must be programmed in units of 32 bytes. Additionally, the HNUM and VNUM registers define the number of pixels per line and lines per frame to read from the SDRAM as shown in Figure 35. For all SDRAM input modes except Darkfame subtract, the LPFR and PPLN registers define the interval of VD and HD, respectively.

Figure 35. Global Frame Definition in SDRAM Input Modes (except Darkframe)



n = 4 for continuous mode
n = 10 for one-shot mode

4.2.1.1 CCDC RAW Input Mode (CFG.INPSRC = 0)

The input data from the video port interface of the CCDC is 14 bits RAW data.

4.2.1.2 SDRAM RAW Input Mode (CFG.INPSRC = 1h)

When the input source is RAW data from the SDRAM read buffer interface, the data can either be read as 1 pixel for every 8 bits, or 16 bits in memory (CFG.PACK8IN). The 8-bit RAW data can either be linear or non-linear.

In order to save DDR2/mDDR controller capacity and bandwidth, the CCD Controller includes an option to apply 10-bit to 8-bit A-Law compression and to pack the sensor data to 1 byte per pixel. In order to process this data properly, the Inverse A-law block is provided to decompress the 8-bit non-linear data back to 10-bit linear data if enabled (CFG.IALAW). This 10-bit data is padded with four low zeros to form a 14-bit bus.

If the Inverse A-law is not enabled, then the data read from SDRAM can be shifted by the CFG.DATASFT register field to select which 14 bits to use.

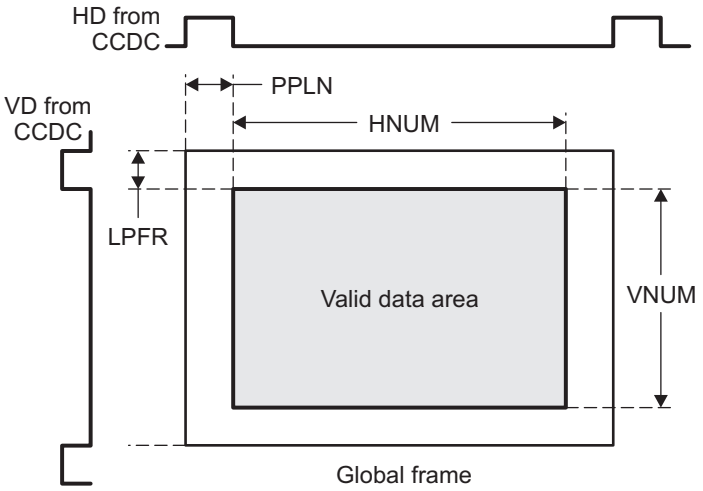
4.2.1.3 CCDC RAW Input With Dark Frame Subtract From SDRAM Mode (CFG.INPSRC = 2h)

The dark frame subtract function is used to remove pattern baseline noise in the sensor. Typically, the CCDC will previously write a dark frame (frame captured when the shutter is closed) to SDRAM using 8 bits of linear data packed into 2 pixels per 16 bits. Eight bits should be enough even if the resolution of the RAW data is 14 bits, since a dark frame should not have values greater than 255 unless it is a fault pixel.

In this mode, everything from the previous two sections also applies since RAW data is used from both the CCDC and SDRAM. Data should be read from SDRAM with `CFG.ALAW` set to 0 and `CFG.PACK8IN` set to 1. Each pixel read from SDRAM will be subtracted from each pixel sent from the CCDC.

The output of the dark frame Subtract operation is 14-bits wide (U14Q0). Note that there must be adequate SDRAM/DDRAM bandwidth if this feature is enabled. If the data fetched from memory arrives late, then there is no way of knowing. Also note that in dark frame subtract mode, the PPLN and LPFR registers should be used to indicate the horizontal and vertical start position of the subtraction from the CCDC data as shown in Figure 36. The value of the LPFR must be greater than 0 since the first line from the CCDC can not be subtracted from.

Figure 36. Global Frame Definition in Darkframe Subtract Mode



4.2.1.4 SDRAM YCbCr 4:2:2 Input Mode (CFG.INPSRC = 3h)

When the input source is YCbCr 4:2:2 data from the SDRAM read buffer interface, the data is expected to be stored as 16 bits in memory so there is no shifting or other pre-processing done.

4.2.2 Timing Generation

When the input source is from the video port interface of the CCDC (CFG.INPSRC = 0 or 2), HD/VD/WEN signals are taken from the CCDC. The CFG.CLKSEL should be set to 0 so that data is latched into the IPIPE using the PCLK from the CCDC.

When the input source is not from the CCDC (CFG.INPSRC = 1 or 3), the HD/VD signals are generated in the IPIPEIF based on the LPFR and PPLN registers (WEN is not generated). The CFG.CLKSEL can be set to either 0 (to continue to use the CCDC PCLK for reading SDRAM data) or 1 (so that the IPIPEIF generates the proper timing of PCLK). If CFG.CLKSEL is set to 1, then the CFG.CLKDIV register is then used to select a divide ratio of the VPSS functional clock (VPSSCLK) for the pixel clock frequency which is used to clock the data into the PCLK. The value of this register should be set based on the maximum PCLK that the resize ratios of the IPIPE resizers require (see equation in Section 4.3.15). Once this is satisfied, then further consideration may be given to the available DDR2/mDDR controller system bandwidth and the real time requirement of the IPIPE processing of the frame.

When CFG.INPSRC is not set to 0, then the IPIPE I/F SDRAM data reading and timing generation can be enabled (ENABLE.ENABLE) in either one-shot mode, or continuous mode (CFG.ONESHOT).

4.2.3 (1,2,1) Averaging Filter

The averaging filter can be optionally enabled by setting the CFG.AVGFILT register bit. It acts as an anti-aliasing low-pass filter for the horizontal pixel decimator. It typically is only needed when the pixel decimator is used (CFG.DECM = 1). It operates on every other pixel (same color) in a RAW bayer input or every Y component in YCbCr data in the following equation:

$$output = (input[I - 1] + 2 * input[I] + input[I + 1]) >> 2$$

4.2.4 Horizontal Pixel Decimator (Downsizer)

The image pipe input is limited to 1344 pixels per horizontal line due to line memory width restrictions in the various filtering blocks. In order to support sensors that output greater than 1344 pixels per line, a line width decimator can be enabled (CFG.DECM) to downsample the input lines to a width equal to or less than the 1344 pixel maximum. The resize ratio can be configured by programming the RSZ register to be within the range from 16 to 112 to give a resampling range from 1× to 1/7× (16/RSZ).

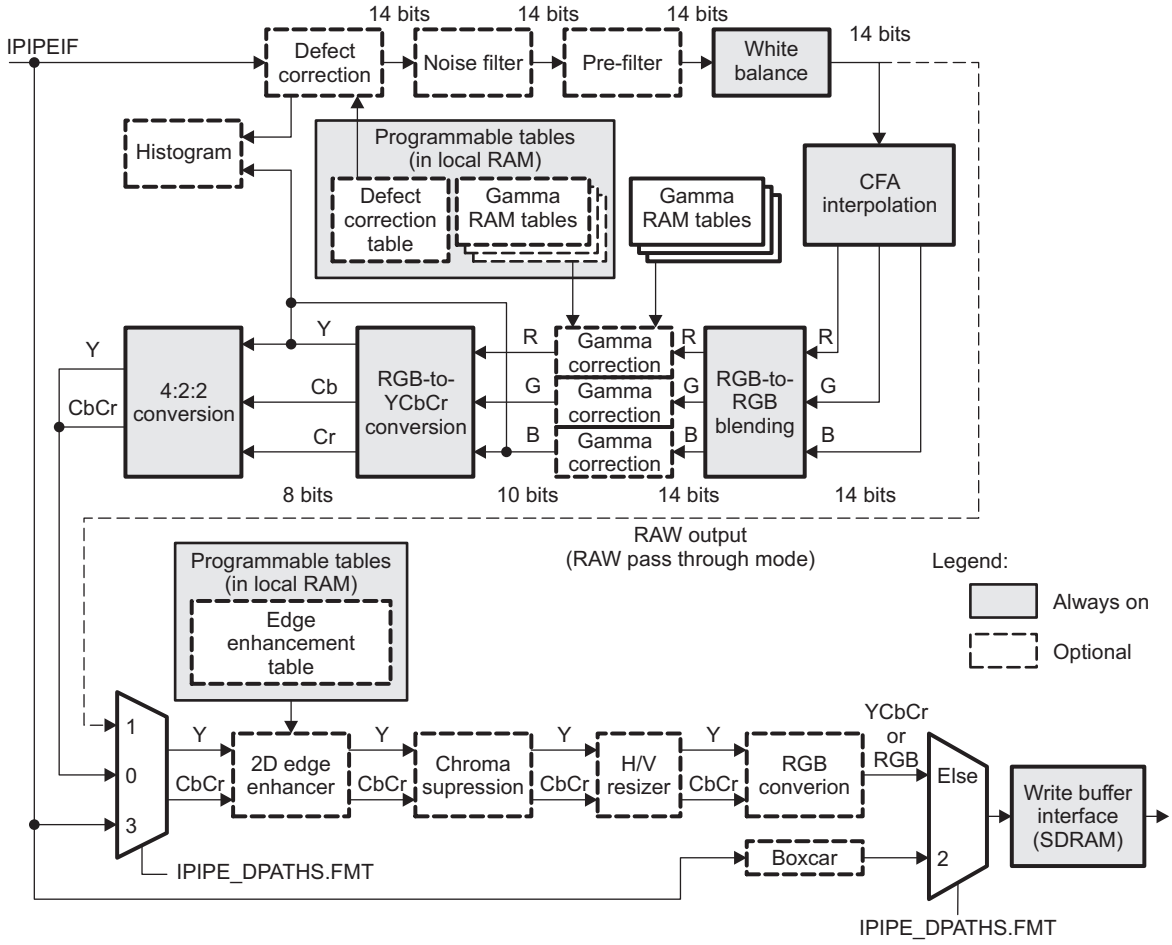
4.2.5 RAW Data Gain

A gain factor ranging from 0.00195(1/512) to 1.99805(1023/512) is multiplied to the RAW output of the IPIPEIF. The gain constant is set in the GAIN register using U10Q9 format.

4.3 Image Pipe (IPIPE)

The Image Pipe (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 format from RAW CCD/CMOS data. The IPIPE can also be configured to operate in a resize only mode, which allows YCbCr-4:2:2 to be resized without applying the processing of every other module in the IPIPE. The input and output data type (data path) can be configured by setting the IPIPE_DPATHS.FMT register field. The output of the IPIPE is typically used for both video/image compression and display. The rest of this section describes, in detail, the functionality of each sub-block in the IPIPE as shown in Figure 37.

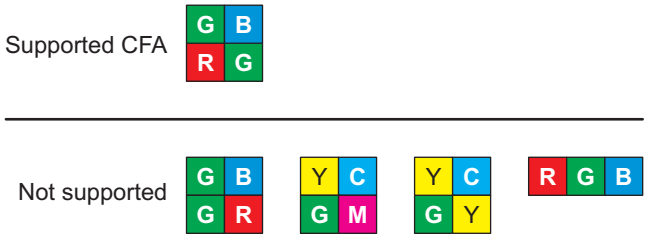
Figure 37. Image Pipe Processing Flow



4.3.1 CFA Arrangements

Figure 38 shows the CFA arrangements that the IPIPE supports. Notice that although complementary CFA patterns are not supported directly by the IPIPE, the CCDC can perform a color space conversion from complimentary to bayer, which the IPIPE supports.

Figure 38. CFA Arrangements



4.3.2 Input Interface

The IPIPE receives 14bit RAW image data or 16 bit YCbCr data via IPIPEIF. The IPIPE can work with up to 1344 pixels in each horizontal line, except in RAW pass through mode where no image processing is applied. If the image width is larger than 1344, the image must be scaled down at PIPEIF. Otherwise, the input image must be split into several blocks. If the input data is YCbCr, all RGB processing modules are skipped, and only edge enhancer, chroma suppression, and resizer are applied to the input data. In RAW pass through mode, images up to 4096 pixels per line may be processed. In RAW pass through mode, the input data is directly written out to SDRAM. The processing steps available for the different input modes are shown in Table 22. The bolded rows are the functions which are required and can not be disabled.

Table 22. Available Processing for Input Modes

	Input Modes (IPIPE_DPATHS.FMT)			
Functions	**0: RAW to YCbCr**	**1: RAW to RAW**	**2: RAW to Boxcar**	**3: YCbCr to YCbCr**
Defect Correction	X	X		
Noise Filter	X	X		
Pre Filter	X	X		
White Balance	X	X		
CFA Interpolation	X			
RGB to RGB Blending	X			
Gamma Correction	X			
RGB to YCbCr Conversion	X			
4:2:2 Down-Sampling	X			
Edge Enhancement	X			X
Color Suppression	X			X
H/V Resize	X			X
RGB Conversion	X			X
Histogram	X	X		
Boxcar			X	

The input interface sub-module clips the processing area in the global frame by setting the start position (IPIPE_HST, IPIPE_VST) and size (IPIPE_HSZ, IPIPE_VSZ) horizontally and vertically as shown in Figure 39. Table 23 further describes the labels in the figure.

Figure 39. Processing Area Within Global Frame

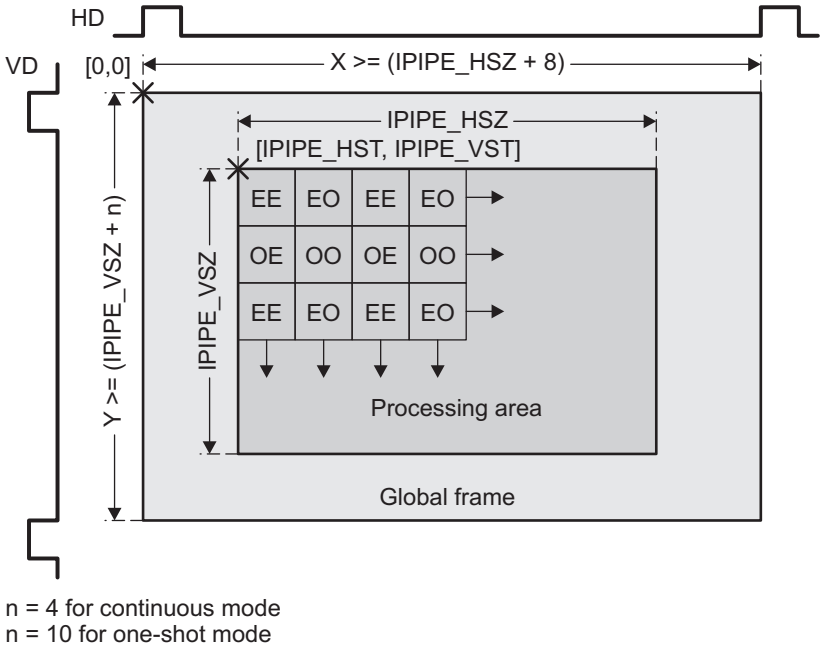


Table 23. Label Descriptions From Figure 39

Label	Description
VD	The vertical synchronous signal from the IPIPEIF module. The IPIPE module judges this signal by the rising edge only.
HD	The horizontal synchronous signal from the IPIPEIF module. The IPIPE module judges this signal by rising edge only.
EE, EO, OE, OO	Color pattern as defined in the IPIPE_COLPAT register.
X	Number of the clock counts between HD and HD. The IPIPE module requires that X is larger than IPIPE_HSZ by at least 8 clocks.
Y	The number of the line counts between VD and VD. The IPIPE module requires that Y is larger than IPIPE_VSZ by at least 4 lines. When the frame is operated in one shot mode (IPIPE_MODE.ONESHOT = 1), there need be at least 10 lines after processing area, i.e. Y>= IPIPE_VSZ + IPIPE_VST + 10.

4.3.3 Defect Correction

The defect correction (or fault pixel correction) module fixes fault pixels in input data due to sensor defects known at camera manufacture time. This function can be optionally enabled by setting the DFC_EN.EN register bit. The defect correction module supports up to 1024 defect points. The module uses a 1024 × 27-bit local memory to store the defect information table. The programmable table contains the information of horizontal position (12 bits), vertical position (12 bits), and correction method (3 bits) for each defect as shown in Figure 40. The information must be listed in raster scan order: "from left to right" and "from the top to the bottom". The first position in the defect information table (DFC_ADR) and the number of defects which are actually used (DFC_SIZ) may be specified through register values.

Figure 40. Defect Information Packet

Correction method	Vertical position	Horizontal position
26..24	23..12	11..0

The correction methods are as follows. Each method is explained in the following section. The pixels in defect correction algorithm are numbered as in Figure 41.

Bits 26-24	Correction method
0	Horizontal interpolation
1h	Copy from left
2h	Copy from right
3h	4-directional interpolation ((d2 + d4 + d5 + d7)/4)
4h	Vertical interpolation after horizontal interpolation
5h	Vertical interpolation after copy from left
6h	Vertical interpolation after copy from right
7h	Copy from top (DFC_SEL = 0) or bottom (DFC_SEL = 1) after horizontal interpolation

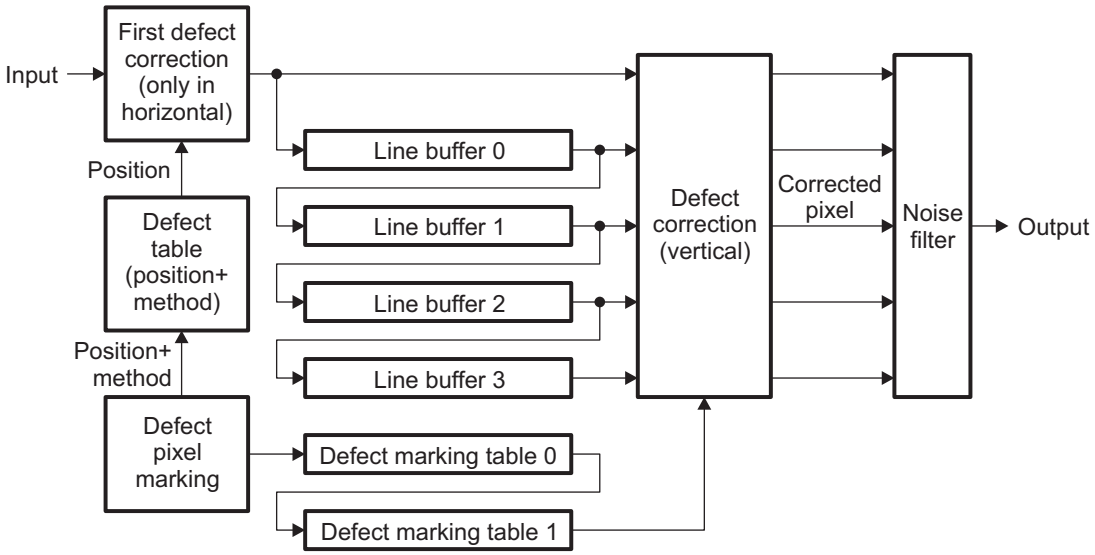
Method	Horizontal Processing	Vertical Processing
0	(d4 + d5)/2	None
1	d4	None
2	d5	None
3	(d4 + d5)/2	((d4 + d5)/2 + (d2 + d7)/2)/2
4	((d4 + d5)/2)	(d2 + d7)/2
5	d4	(d2 + d7)/2
6	d5	(d2 + d7)/2
7	(d4 + d5)/2	d2 or d7

Figure 41. Numbering in Defect Correction Algorithm

d1		d2		d3
d4		d0		d5
d5		d7		d8

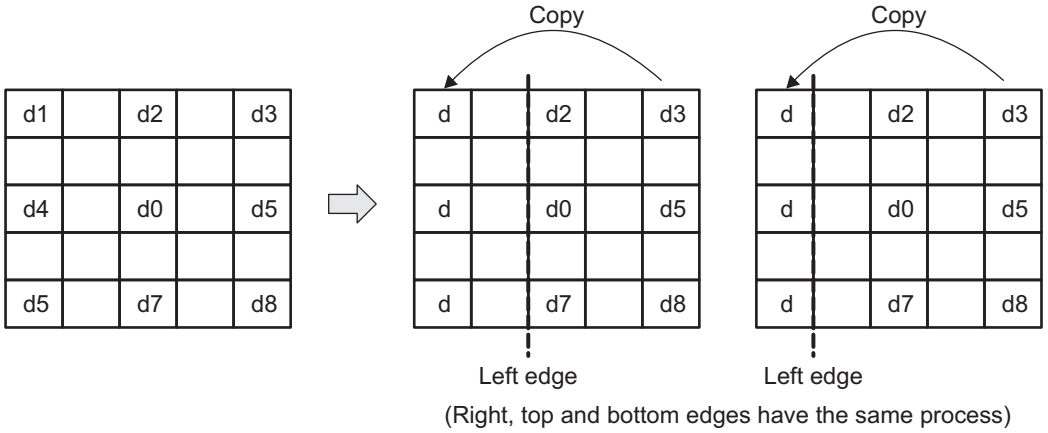
The defect correction process is divided into horizontal correction and vertical correction. For method 0, 1, and 2, only the horizontal correction is applied. For methods 3-7, horizontal correction is applied first, then vertical correction replaces the pixels in the center line at the noise filter. This process is described in Figure 42.

Figure 42. Defect Correction Functional Model



The pixels at the edges are mirrored as shown in Figure 43 to avoid copying the defect center pixel.

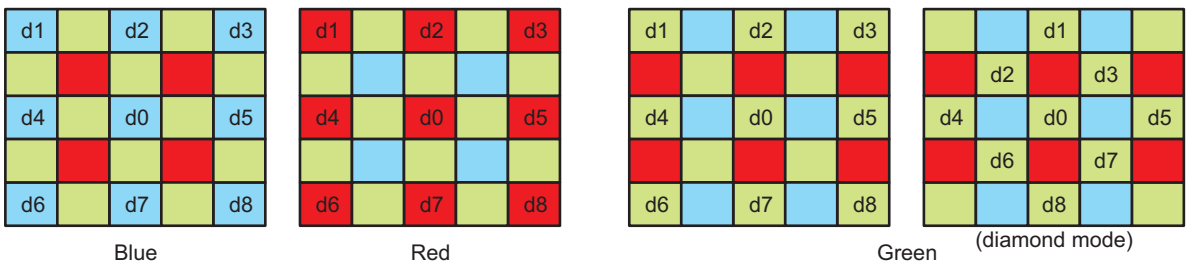
Figure 43. Mirroring in Defect Correction and Noise Filter



4.3.4 Noise Filter

The two-dimensional noise filter reduces noise in raw input data and can be enabled by setting the D2F_EN.EN bit. The 3×3 grid of same color pixels used for this filtering is shown in Figure 44. The pixel being filtered is "d0". "d0" ~ "d8" are same color pixels. For green, one of two numbering methods can be selected (D2F_CFG.TYP), box or diamond.

Figure 44. Noise Filter Array



4.3.5 Pre Filter

The 2-D pre-filter can be enabled (PRE_EN.EN) to reduce the effect of line-crawling and is applied only to green pixels. One of the following two algorithms can be selected (PRE_TYP):

- Averaging filter with constant gain
- Adaptive gain control algorithm

4.3.6 White Balance

The white balance module executes a digital gain adjustment and a white balance adjustment to CCD raw data. Digital gain is for adjusting a total brightness of image, and white balance gains are for adjusting a ratio of each color in a CFA pattern.

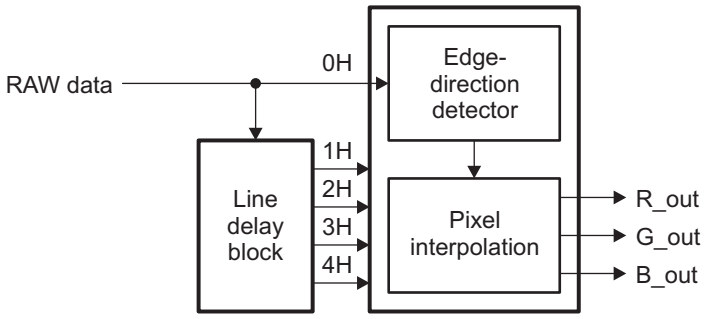
There are two multipliers for the two gain adjustments: a digital gain adjuster and a white balance adjuster. In the digital gain adjuster, the raw data is multiplied by a fixed value gain (WB2_DGN) regardless of the color. In the white balance gain adjuster, the raw data is multiplied by a selected gain corresponding to the color. The white balance gain can be selected from four 10-bit values (WB2_WG_R, WB2_WG_GR, WB2_WG_GB, & WB2_WG_B). Firmware can assign any combination of 4 pixels in the horizontal and vertical direction. The precision of each gain is as follows:

- TOTAL GAIN : x 0 – x 3.996 (step = 1/256)
- WB GAIN: x 0 – x 7.992 (step = 1/128)

4.3.7 CFA Interpolation

The IPIPE's CFA (color filter array) interpolation module generates RGB 4:4:4 data from a Bayer RGB pattern. The block diagram of the CFA (color filter array) interpolation module is shown in Figure 45. The color filter array consists of the line delay block, the edge-direction detector and the pixel interpolator. The edge-direction detector detects most probable edge direction of an object to which the target pixel belongs, and the pixel interpolator calculates the missing color according to its edge direction within 5×5 pixel window.

Figure 45. CFA Interpolation Functional Model



4.3.8 RGB2RGB Blending

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3×3 square matrix transformation in combination with an added offset. This is programmable (RGB_MUL_[R,G,B][R,G,B], & RGB_OFT_[R,G,B]) so that the color spectrum of the sensor can be adjusted to the human color spectrum. The RGB to RGB blending is calculated using the following formula. Each gain range is from -8 to +7.996 with step 1/256 = 0.004 (signed 12 bits). The offset takes -8192 ~ 8191 (signed 14 bits) value range.

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

4.3.9 Gamma Correction Module

The gamma correction module performs a gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. The gamma correction function for each color can be separately bypassed (GMM_CFG.BYPR, GMM_CFG.BYPG, and GMM_CFG.BYPB). Either a fixed ROM table or programmable local RAM table can be used (GMM_CFG.TBL). Each RAM table has up to 512-entries, but can also be programmed to use only 256 or 128 (GMM_CFG.SIZ). Each entry accommodates a 10-bit gain and 10-bit slope. The ROM table has 1024 entries and outputs 8-bit values. As shown in Figure 46, this module exists independently for each color so that independent settings are possible.

Figure 46 shows a block diagram of the gamma correction module. It is composed of two tables and one selector. When the BYPASS bit is asserted, the input data is divided by 16. Figure 47 shows an example of a RAM gamma curve. The ROM gamma table is shown in Figure 48.

Figure 46. Gamma Correction Functional Model

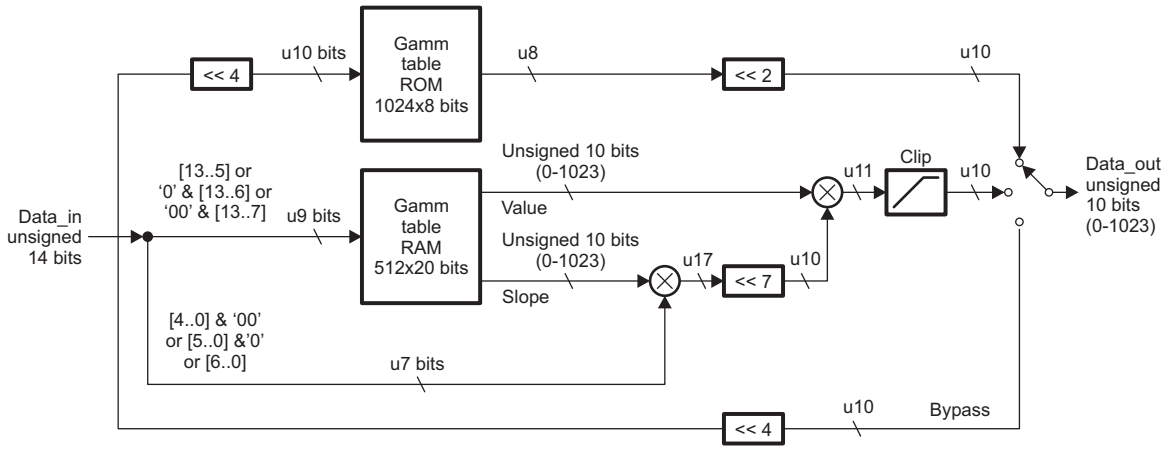


Figure 47. Example of Gamma Curve

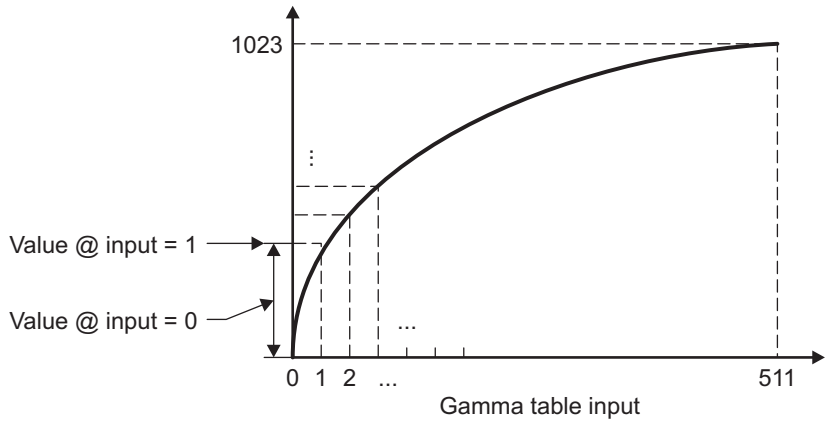
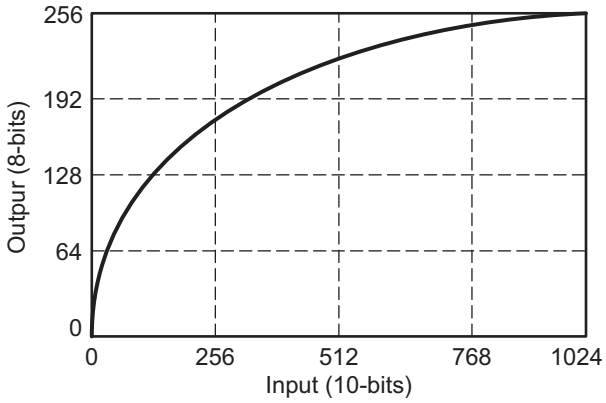


Figure 48. ROM Gamma Table



4.3.10 RGB2YCbCr Conversion Module

This module transforms the RGB data into YCbCr data format using a 3×3 square matrix transformation in combination with an added offset (YCC_MUL_[R,G,B][Y,CB,CR], and YCC_OFT_[Y,CB,CR]). Each gain range is from –2 to +1.984 with step 1/256 = 0.004. The offset range is -256 to 255. A block diagram of the RGB to YCbCr blending module is shown in Figure 49. The output is calculated with the following equation:

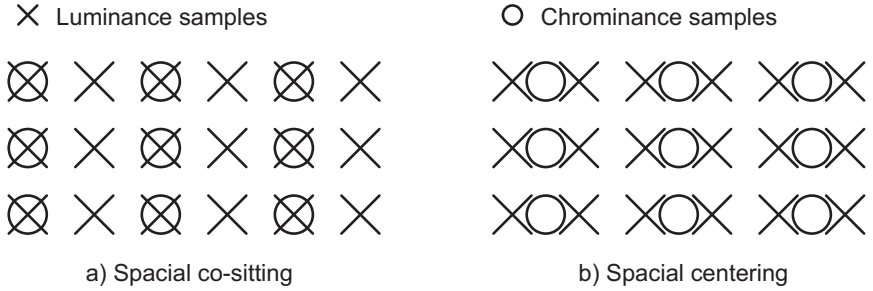
Figure 49. RGB2YCbCr Conversion Functional Model

$$\begin{bmatrix} Y\_out \\ Cb\_out \\ Cr\_out \end{bmatrix} = \begin{bmatrix} gain\_RY & gain\_GY & gain\_BY \\ gain\_RCb & gain\_GCb & gain\_BCb \\ gain\_RCr & gain\_GCr & gain\_BCr \end{bmatrix} \begin{bmatrix} R\_in \\ G\_in \\ B\_in \end{bmatrix} + \begin{bmatrix} offset\_Y \\ offset\_Cb \\ offset\_Cr \end{bmatrix}$$

4.3.11 4:2:2 Conversion Module

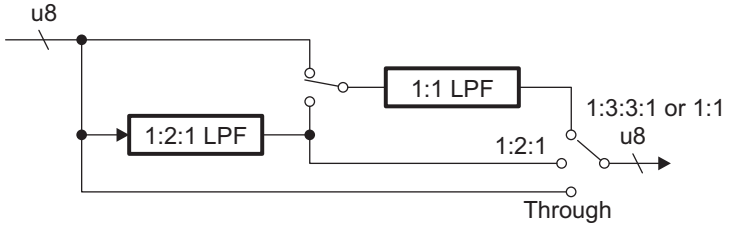
The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by taking the average of every two Cb and Cr components. The Y and Cb/Cr sampling point of either spatial co-siting or spatial centering are selectable (YCC_PHS.POS). Horizontal 3 taps and 4 or 2 taps filters are used for spatial co-siting and spatial centering, respectively. An anti-aliasing filter can also optionally be enabled in the YCC_PHS.LPF register field.

Figure 50. Chroma Sub-Sampling Position



A block diagram of 4:2:2 conversion module is shown in Figure 51.

Figure 51. 4:2:2 Conversion Functional Model



4.3.12 2-D Edge Enhancer

The edge-enhancer module optionally operates on the luminance (Y data) component of images to improve the image quality (YEE_EN.EN). Edges in input images are detected by a 5×5 2D high-pass filter with programmable coefficients (YEE_MUL_[0,1,2][0,1,2]). The output of the filter can be optionally down shifted by the length of the high pass filter (YEE_SHF.SHF). The sharpness is increased by the value from a non-linear programmable table in local RAM.

4.3.13 Median NR

The Median-NR is optionally used to reduce the pseudo peak in edge intensities (YEE_EMF.EN). Median-NR takes median values from four directions in the 3×3 edge intensities arrays. Then it outputs the intensity that is closest to the center value.

4.3.14 Chrominance Suppression

Occasionally, in very bright portions of an image, only one or two of the color channels may be saturated but the remaining channel(s) may not be. This may lead to a false color effect. One common example would be the appearance of a pink color where white should be. Chrominance suppression can be used to reduce this pseudo-coloring of images. The chrominance suppression operation can optionally be enabled or disabled using the `FCS_EN.EN` parameter.

False color pixels can also be introduced on edges by the CFA interpolation function. The luminance value used in the chroma suppression calculation can optionally be configured to be the actual luminance value, or the high pass filtered version of the luminance value for identifying this edge information.

4.3.15 Horizontal and Vertical Resize Module

The Resize module is capable of re-scaling images into various sizes ranging from x1/16 scale-down to x8 scale-up in both the horizontal and vertical directions. After resizing process, the processed data are transferred to the SDRAM. Table 24 shows the format of YCbCr image data in SDRAM.

The scaling process in horizontal direction is carried out using interpolation with 4-tap filter. The interpolation method is either 4-tap cubic convolution, or 2-tap linear filter depending on the setting of the RSZ[n].RSZ_H_TYP register. For scale down, the horizontal resize process is also equipped with an adjustable 7-tap anti-alias filter. Vertical resizing is processed with 2-tap linear filter. The range of resizing ratio is determined by two parameters HRSZ (RSZ[n].RSZ_H_DIF) and VRSZ (RSZ[n].RSZ_V_DIF), which may be set independently. The resizing ratio of output image equals to 256/HRSZ for horizontal process and 256/VRSZ for vertical process. The upper and lower limits of HRSZ and VRSZ are 32 and 4096, which correspond to x8 scale-up and x1/16 scale-down respectively. The sizes of output images are limited to below 1344 pixels/line for RSZ[0] and 640 pixels/line for RSZ[1].

Scale-up performance of the module depends on the frequency ratio between the pixel clock and SDRAM clock. When the pixel and SDRAM clock are 20MHz and 90MHz respectively, the total scale-up capability is approximately (90 MHZ/20 MHZ) × 2 pallaral-output = ×9-scale-up, i.e. ×6-scale-up for image-a and ×3-scale-up for image-b. More precise measure of the performance limit is as following. The vertical resize ratio for image-a and image-b must satisfy:

$$(\text{number of clocks per horizontal line of IPIPE input}) \times \left(\frac{\text{VPSSCLK frequency}}{\text{pixel clock frequency}} \right) > \text{ha} \times \text{ra} + \text{hb} \times \text{rb} + \text{overhead}$$

where

$$\text{ha} = \frac{\text{horizontal size of image-a output} + \text{output start position of image-a}}{\min(1, \text{horizontal resize ratio of image-a})}$$

$$\text{hb} = \frac{\text{horizontal size of image-b output} + \text{output start position of image-b}}{\min(1, \text{horizontal resize ratio of image-b})}$$

$$\text{ra} = \text{ceil}\left((\text{vertical resize ratio of image-a}) / 2 \right)$$

$$\text{rb} = \text{ceil}\left((\text{vertical resize ratio of image-b}) / 2 \right)$$

$$\text{overhead} = 100 \times (\text{ra} + \text{rb})$$

Here, min(a, b) is the smaller of a and b, and ceil(x) is the smallest integer number that is equal to or greater than x. The right side value should be well below the left side value.

Actual performance limit of resize output is also limited by the band-width of the attached SDRAM. Average output pixel per clock of each line must not exceed the band-width available to IPIPE module. For example, if the allowed band-width is 1 byte/clock, output pixel per clock in each line must be lower than 1 pixel per every two clocks with some margin for overhead. Therefore, allowed resize ratio in this case will be:

image-a ratio <= x1, and image-b ratio <= x1

or

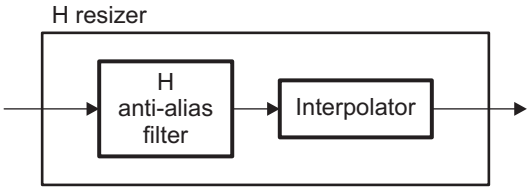
image-a ratio <= x2, and no image-b

Table 24. YcbCr-422 Memory Format

Byte Address	YCbCr Data
4n	Cb0
4n + 1	Y0
4n + 2	Cr0
4n + 3	Y1

Figure 52 shows a block diagram of the horizontal resize block which has anti-alias filter.

Figure 52. Horizontal Resize Functional Model

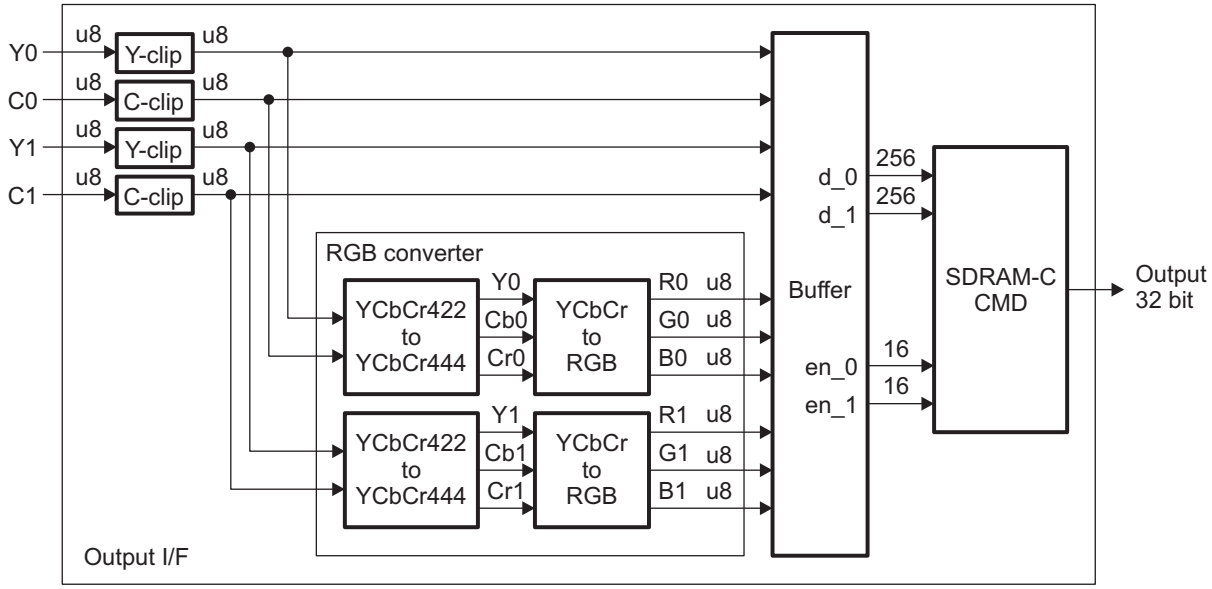


Vertical resize module supports two operation modes, input line number confined mode and continuous mode, for vertically split blocks (frame division mode). When input line number confined mode is selected (RSZ_SEQ.TMM = 1), the vertical resize module continues processing until the defined input lines are all processed. In this mode, the last state of the vertical interpolation operation is outputted to the RSZ[n].RSZ_V_PHS_O register. This value may be used in the following resizing operation of the next vertical block as an initial phase input. (There needs be an overlap of one line; the last line of the previous block must be duplicated to make the first line of the next block.) Continuous mode is a mode which preserves the last state of the previous operation, and continues resizing as if the first processed line of the current frame directly follows the last line of the previous operation. With vertically split blocks, this mode may be used for processing of the second and latter blocks. Continuous mode works only in combination with input line number confined mode.

4.3.16 Output Interface

The block diagram of the output interface module is shown in Figure 53. Y-Clip and C-Clip modules limit the range of image data to [ymin to ymax] or [cmin to cmax]. The min and max values are specified in the YCC_Y_MAX, YCC_Y_MIN, YCC_C_MAX, and YCC_C_MIN registers.

Figure 53. Output Interface Functional Model



4.3.17 RGB Converter

The IPIPE optionally supports output of RGB data to SDRAM (RSZ[n].RGB_EN.EN). The YCbCr 4:2:2 data from the resizer module is first converted to YCbCr 4:4:4 data by linear interpolation. Since the pixels at the left and right edges are mirrored for the interpolation, two pixels at each edge are affected. To remove this effect, two pixels at the start of each line (RSZ[n].RGB_TYP.MSK0) and end of each line (RSZ[n].RGB_TYP.MSK1) may be removed from the output. In this case, the horizontal size of the output image is 2 or 4 pixels smaller than what is specified in resizer output width register.

The YCbCr 4:4:4 data is converted to RGB using the following equation.

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.34414 & -0.71414 \\ 1 & 1.772 & 0 \end{pmatrix} \cdot \begin{pmatrix} Y \\ Cb-128 \\ Cr-128 \end{pmatrix}$$

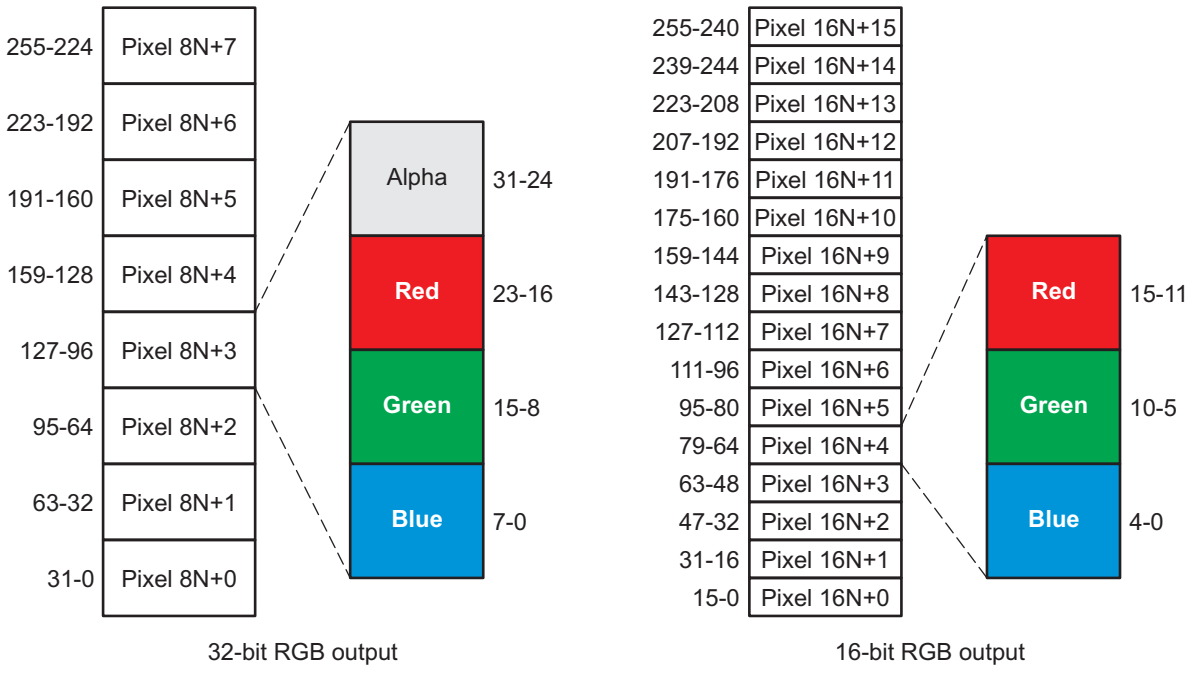
This equation is realized in actual circuit using the following equations.

$$R = (512 \cdot Y/128 + 718 \cdot Cb'/128)/4$$
$$G = (512 \cdot Y/128 - 176 \cdot Cr'/128 - 366 \cdot Cb'/128)/4$$
$$B = (512 \cdot Y/128 + 907 \cdot Cr'/128)/4$$
$$Cb' = Cb - 128$$
$$Cr' = Cr - 128$$

The output image data is packed in each SDRAM access burst (256 bit) as shown in Figure 54. There are two packing modes: 32-bit mode and 16-bit mode (RSZ[n].RGB_TYP.TYP). In 32-bit mode, RGB data (8-bit each) and the alpha value (8-bit blending factor) are written to SDRAM. The alpha value is set in the RSZ[n].RGB_BLD register. In 16-bit mode, R (5-bit), G (6-bit), and B (5-bit) are written.

Enabling RGB conversion and 32-bit/16-bit selection can be independently configured for both resizers.

Figure 54. RGB Data Format



4.3.18 SDRAM Writing Modes

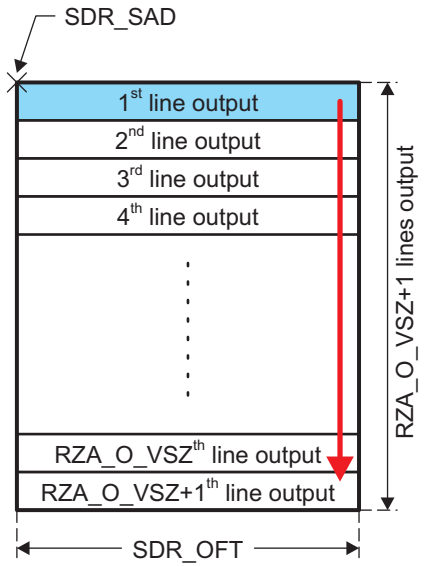
Table 25 describes the registers used for writing the output of the resizers to SDRAM.

Table 25. SDRAM Write Registers

Label	Description
RSZ[n].RSZ_SDR_BAD_H RSZ[n].RSZ_SDR_BAD_L	SDRAM base address of the output buffer in SDRAM
RSZ[n].RSZ_SDR_SAD_H RSZ[n].RSZ_SDR_SAD_L	SDRAM starting address of the output buffer in SDRAM for the first frame
RSZ[n].RSZ_SDR_OFT	SDRAM starting address of the output buffer in SDRAM for the first frame
RSZ[n].RSZ_SDR_PTR_S	Start line of SDRAM pointer
RSZ[n].RSZ_SDR_PTR_E	The maximum number of lines to be stored in SDRAM
RSZ[n].RSZ_SDR_PTR_O	Position of last line within the output buffer in previous resize process

For the simple case where there is one linear output buffer, only the RSZ[n].RSZ_SDR_SAD_H/L and RSZ[n].RSZ_SDR_OFT registers are used along with the RSZ[n].RSZ_O_VSZ register as shown in Figure 55.

Figure 55. Linear Buffer



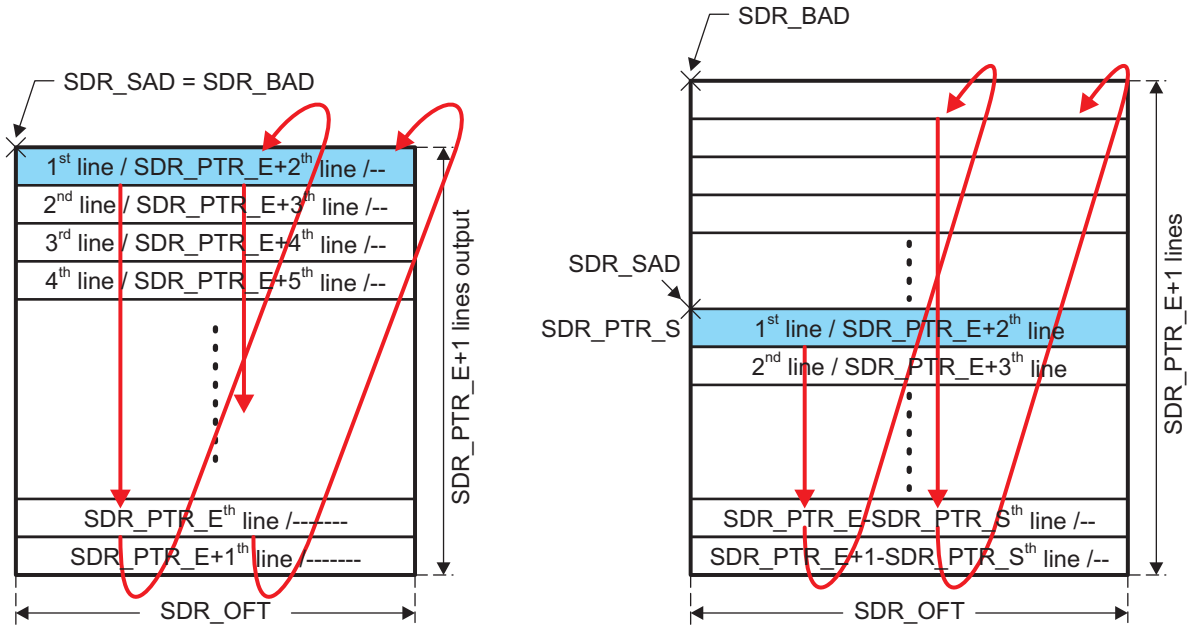
The other registers mentioned in Table 25 are used for implementing a ring buffer (or circular buffer) in SDRAM.

4.3.18.1 Ring Buffer

The resizer can output data to a small size buffer by using a ring buffer as shown in Figure 56.

The first address of output buffer is set in RSZ[n].RSZ_SDR_SAD_H/L register. The first address in the allowed memory space is set in RSZ[n].RSZ_SDR_BAD_H/L register. The ring buffer size is set in the RSZ[n].RSZ_SDR_PTR_E register. The first output line is set in RSZ[n].RSZ_SDR_PTR_S register.

Figure 56. Ring Buffer



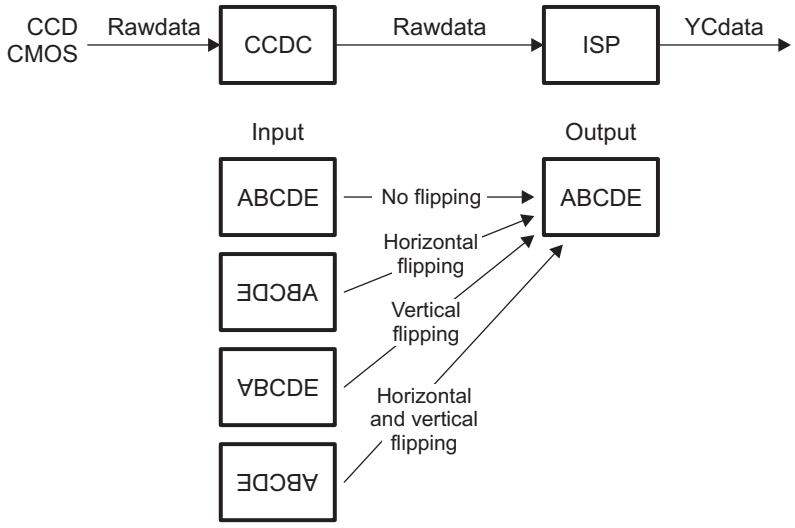
(a) Ring buffer
(SDR_SAD = CDR_BAD)

(b) Ring buffer
(SDR_SAD ! = CDR_BAD)

4.3.18.2 Horizontal and Vertical Image Flipping

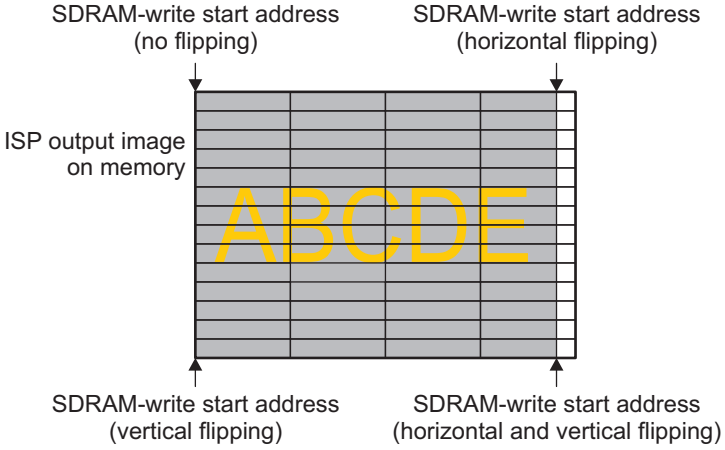
Flipping image function is implemented to support flipped input raw data. *Horizontal*, *vertical* and *horizontal & vertical* flipping modes are implemented as shown below (RSZ_SEQ.HRV enables horizontal flip, and RSZ_SEQ.VRV enables vertical flip).

Figure 57. Data Flipping Mode



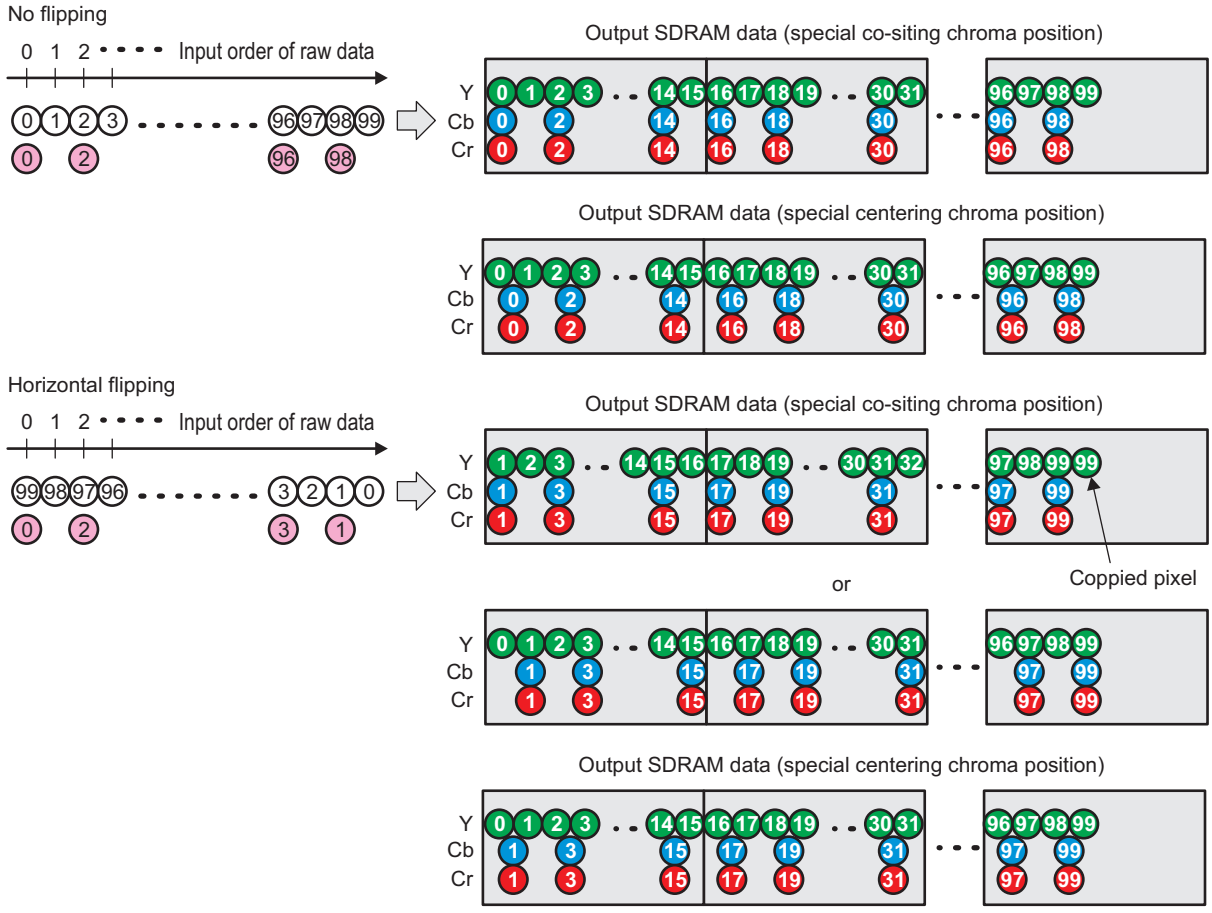
SDRAM write-start-address is needed to be set at the register by ARM. The address at each flipping mode is illustrated in Figure 58.

Figure 58. Write Start Address at Each Flipping Mode



In the non on-the-fly operation mode, CCDC flips the data and write raw data in the SDRAM. IPIPE does not flip data in this mode. Therefore horizontal flipping mode does not support the frame division mode - H/V. Figure 59 illustrates output data format to SDRAM at no flipping and horizontal flipping modes.

Figure 59. Output Data Format to SDRAM

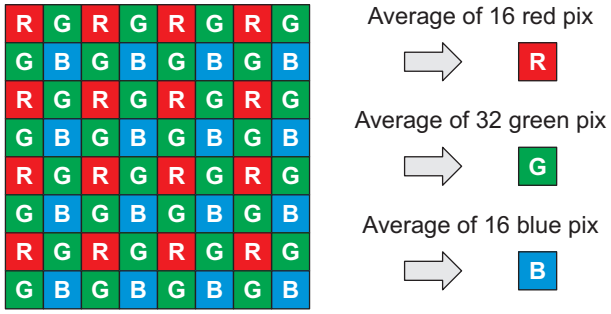


4.3.19 Boxcar

Boxcar module generates a boxcar by taking mosaic CCD data and averaging the red green and blue pixels in an 8×8 or 16×16 (BOX_TYP) block to produce one red, green and blue output as shown in Figure 60 and in Section 4.3.20.

The result from this operation is a full color image with (1/64) or (1/256) area of the original image. The maximum input horizontal width is 4096 pixels wide when (16x16) block is used. If (8×8) is used, it is 2048. Also, the image size (width and height) must be multiple of 16 for (16×16) block, and multiple of 8 for (8×8) block. Boxcar operation works on up to 14 bit Bayer data and output 16-bit data. The output data are 48-bit RGB data for each 8×8 or 16×16 block. The 48 bit data is aligned in 64 bit format in SDRAM as shown in Boxcar Data Packing in SDRAM. The first address of SDRAM access is specified by RSZ[0].RSZ_SDR_SAD_H and RSZ[0].RSZ_SDR_SAD_L. The output data are written to SDRAM continuously line by line; there is no address offsets between lines.

Figure 60. Boxcar Operation (8 × 8 block)



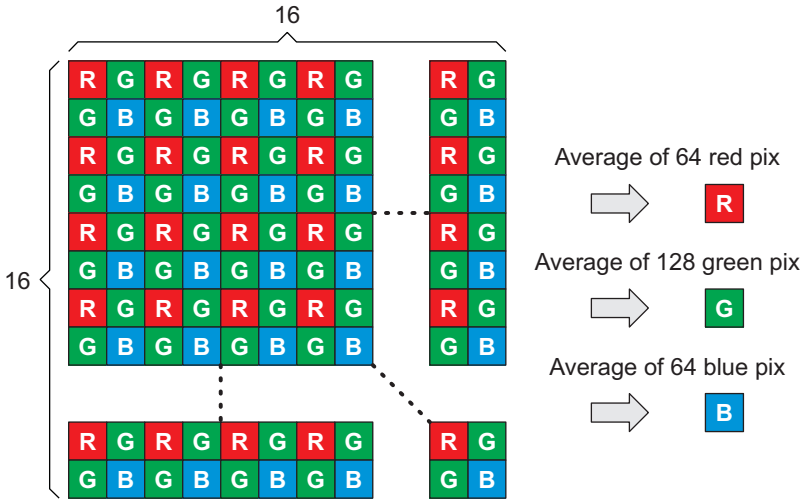
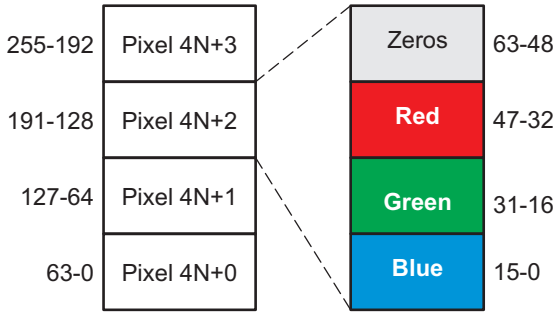


Figure 61. Boxcar Data Packing in SDRAM



4.3.20.1 Averaging

First, the boxcar separately sums each color for a given block of pixels. For example, in the 8×8 case, all 16 red pixels per block are added together; same with blue. In the case of green, all of the green pixels are added together, and then divided by 2 since there are twice as many green pixels per block as there are red or blue. Then, the sum for each color in each block is right shifted by the value provided in the BOX_SHF register to calculate the average to 16-bit dynamic range. The following equation can be used to calculate the required shift value:

BOX_SHF = (input bit resolution) + log2(summed pixels per color) - (output bit resolution)

8×8 mode: $\log_2(16) = \mathbf{4}$ 16×16 mode: $\log_2(64) = \mathbf{6}$

For example, in the 16x16 mode, where in the input is 14 bits and the output is 16 bits:

BOX_SHF = 14 + 6 - 16 = 4

The recommended shift values to get 16-bit output pixel resolution are shown in Table 25. The shaded row indicates the input bit width when the input is already aligned to the upper bits of the 14-bit data bus. The other two rows indicate the recommended shift values when the RAW input to the IPIPE is not aligned to the upper bits of the 14-bit bus.

Table 26. Recommended SHIFT Values to Get 16-Bit Output Resolution

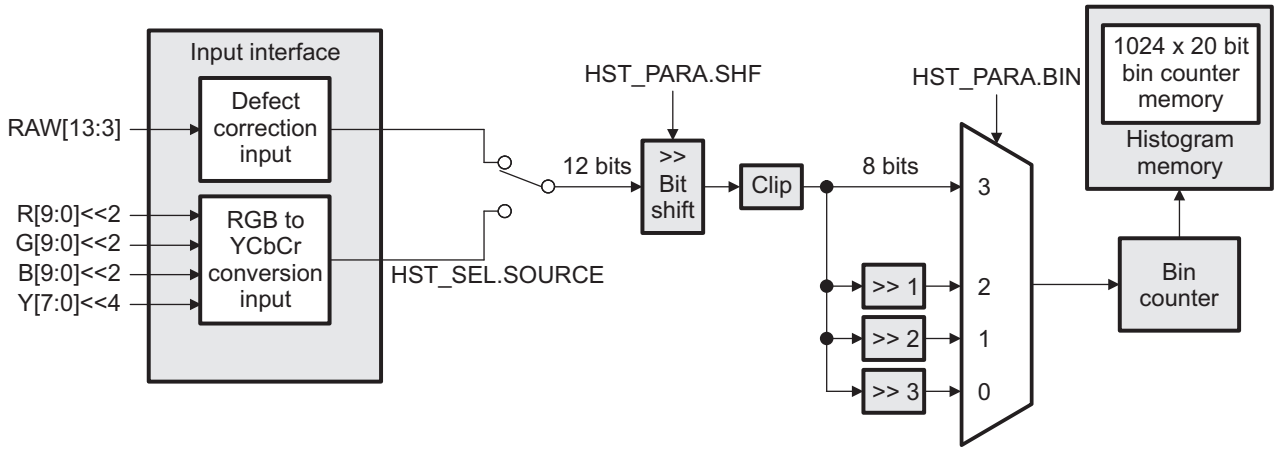
RAW IPIPE Input Resolution	8×8 Mode	16×16 Mode
12-bit RAW	0	2
13-bit RAW	1	3
14-bit RAW	2	4

Boxcar module runs only in stand-alone mode, i.e. no parallel IPIPE operation is allowed. Boxcar module shares memories with histogram module.

4.3.21 Histogram

The histogram accepts RAW image/video data from the defect correction function of the IPIPE, or color interpolated RGBY from the RGB to YCbCr conversion function of the IPIPE. It performs a color-separate gain on each pixel (white/channel balance), and bins them according to the amplitude, color, and region which are all specified via its register settings. It can support one, two, three, or four colors, and up to four regions simultaneously. Figure 62 shows the processing flow of the histogram module.

Figure 62. Histogram Processing Flow



4.3.21.1 Features List

The histogram module counts number of pixels having a value in a region. Features of the histogram function are as follows:

- The histogram function normalizes input pixels to 12 bit resolution
- The data to be summed will be taken either from horizontal defect correction or from Gamma correction + RGB2YCbCr module.
- When sampled from defect correction, the R, G, B, Y data are taken from the output of line buffer, which is after horizontal defect correction and before vertical correction. The upper 12 bits of the 14 bit data (raw_input[13:2]) are input to Histogram module.
- When sampled from Gamma correction + RGB2YCbCr module, R, G, B are sampled at the output of gamma correction, and Y is sampled at the output of RGB2YCbCr module. The 10-bit RGB and 8 bit Y are up-shifted to occupy the MSB of the 12 bit Histogram input.
- The colors to be summed are R/G/B/Y. If the data are taken from horizontal defect correction, Y is derived in the following method.
  $Y = (R + Gr + Gb + B)/4$
- For G histogram, either Gb or Gr is used
- If the data are taken from Gamma correction + RGB2YCbCr module, R is sampled at even pixels on even lines, G is sampled at odd pixels on even lines, B is sampled at even pixels on odd lines, and Y is sampled at odd pixels on odd lines.
- 1024 × 20-bit memory is used
- *the number of regions* × *the number of bins* <= 256
- The number of regions (areas): 1, 2, 3, or 4
- Each region can be turned on/off counting
- The regions have priority orders
- Each region has its own start coordinate X/Y (12-bit) and horizontal/vertical sizes (12-bit)
- When regions are overlapped, value in the overlapped region is only accumulated in the region with the highest priority.
- The number of colors to be counted: 1, 2, 3, or 4

- Each color in all regions can be turned off counting
- Value of each pixel is down-shifted before counting
- Down-shift bit number: 0 ~ 11 bits
- When value of a bin reaches to (2^{20} - 1), the value is saturated until the memory is cleared.
- Number of bins: 32, 64, 128, or 256

4.3.21.2 Input Interface

The histogram function can be configured to receive RAW image/video data from the defect correction module or YCbCr 4:4:4 image/video data from the RGB2YCBCR module (HST_SEL.SOURCE).

4.3.21.3 Histogram Binning

The histogram bins the input data by amplitude, color, and region. Each bin is a counter, counting the number of pixels of a color in the range associated with the bin. The number of bins can be programmed to 32, 64, 128, or 256 bins in the HST_PARA.BIN field. However, due to the limited histogram memory size (1024 words), the number of bins (times four colors) limits the number of regions that can be active. The following equation must hold true:

$$\textit{the number of regions} \times \textit{the number of bins} <= 256$$

Table 27 lists the possibilities based on this equation.

Table 27. Regions and Bins for Histogram

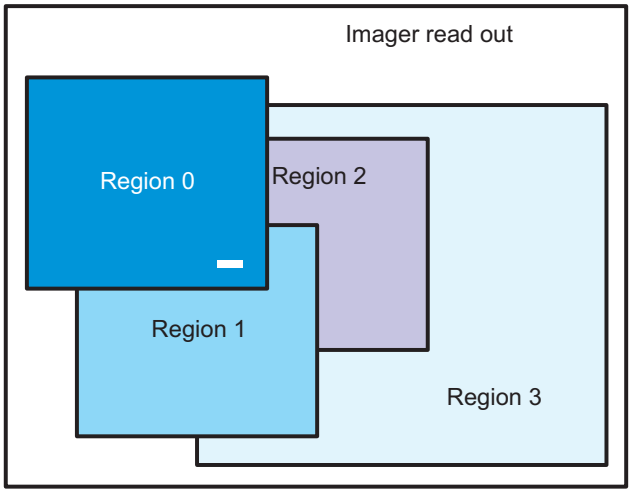
Number of Bins	Number of Regions Allowed
256	1
128	2
64	4
32	4

As indicated by Table 27, up to four overlapping regions can be designated within the frame and each of them can be separately enabled/disabled by configuring the HST_PARA.RGNn fields. Each region is defined by the horizontal starting pixel (HST_RGN[n].HST_HST) and width (HST_RGN[n].HST_HSZ), and vertical starting line (HST_RGN[n].HST_VST) and height (HST_RGN[n].HST_VSZ) (where n is the region number 0..3).

4.3.21.3.1 Region Priority

Up to four regions can be active at any time but a pixel is only binned into one region. The priority is Region 0 > Region 1 > Region 2 > Region 3. For example, the white pixel in Figure 63 will be binned only for *Region 0*, although it is present in all the four regions.

Figure 63. Region Priority



4.3.21.3.2 Bin Clipping and Right Shifting

As shown in Figure 62, the input pixels to the Histogram are normalized to 12-bit values. In between the input and the binning function is a right-shift function. In order to properly distribute the dynamic range of the pixel values across all the bins, the bit-width of each pixel after right-shifting by HST_PARA.SHF should always be 8-bits. Within these 8 bits, the histogram binning function automatically shifts as necessary based on the selected bin size. Since the input to the shift function is normalized to 12 bits, then the HST_PARA.SHF value should always be set to 4 to avoid bin clipping and under-utilization of the chosen number of bins. If the shift value is too low, then the most significant bits will be clipped, and the highest bin will be incremented for a disproportionate number of pixel values. If the shift value is too high, then the full dynamic range of the pixel is not properly utilized, and the histogram will bin all the values to only the lower bin numbers, while the high bin numbers will never be incremented.

EXCEPTION: If the input is selected from the defect correction function, and if the dynamic range of the RAW data input to the IPIPE is less than 14 bits, then the shift value should not be set to 4. In this case, you will need to shift less to align the most significant bit with bit 7 on the output of the shift function. This is not considered for the RGB to YCbCr input since the data should have been fully shifted up to 14 bits before the CFA interpolation function.

The recommended shift values are shown in Table 28. The shaded row indicates the input bit width when the input is from the RGB2YCbCr module and typical input from the defect correction module. The other 2 rows indicate the recommended shift values when the RAW input to the IPIPE is not aligned to the upper bits of the 14 bit bus.

Table 28. Recommended SHIFT Values

RAW IPIPE Input Resolution	Shift Value
12-bit RAW	2
13-bit RAW	3
14-bit RAW RGB to YCbCr Input	4

4.3.21.3.3 Bin Saturation

The histogram bin counter memory is 20 bits wide. If incrementing a histogram bin would cause the value to become greater than what this memory word could hold, the value is saturated to the maximum value, which is 2^{20} - 1.

4.4 Statistics Collection - Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto Focus Engine (AF) and
- Auto Exposure and Auto White Balance Engine (AE/AWB)

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a *Paxel* for the case of AF.

The AE/AWB Engine accumulates the values and checks for saturated values in a sub sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a *window*. Thus, other than referring to them by different names, a Paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF Paxels and the AE/AWB windows are separately programmable.

4.5 VPFE Arbitration and Data Transfer Control (VPSSBL)

The buffer logic (VPSSBL) manages the flow of data between the VPSS modules and the DDR2/mDDR controller. In order to efficiently utilize the external DDR2/mDDR controller bandwidth, the buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide) at the DMA clock frequency (PLL1/4). The buffer logic/memory also interfaces with all the VPFE and VPBE modules via a 32-bit wide bus at the VPSS functional clock frequency (VPSSCLK).

Due to the real time demands of image processing at high speeds and image resolutions, the VPSS demands the highest bandwidth requirements in the system. The VPSS buffer logic optimizes data transactions with the DDR2/mDDR controller by buffering data internally to absorb instantaneous peak traffic. The VPSS DMA master is required to be the highest priority (default) in the system to guarantee functionality. This priority can be lowered (not advised) by modifying the PCR.CPRIORITY register field of the VPSSBL module.

4.5.1 Memory Multiplexing

In order to save internal memory space, the buffer logic shares internal memories between modules which wouldn't normally use them at the same time. Memory access multiplexers can be programmed in the VPSSBL so that only one master can access the shared memories at a time. Figure 64 shows all of the shared memories and programmable multiplexer switches in the VPFE.

Figure 64. VPFE Shared Memories and Multiplexers

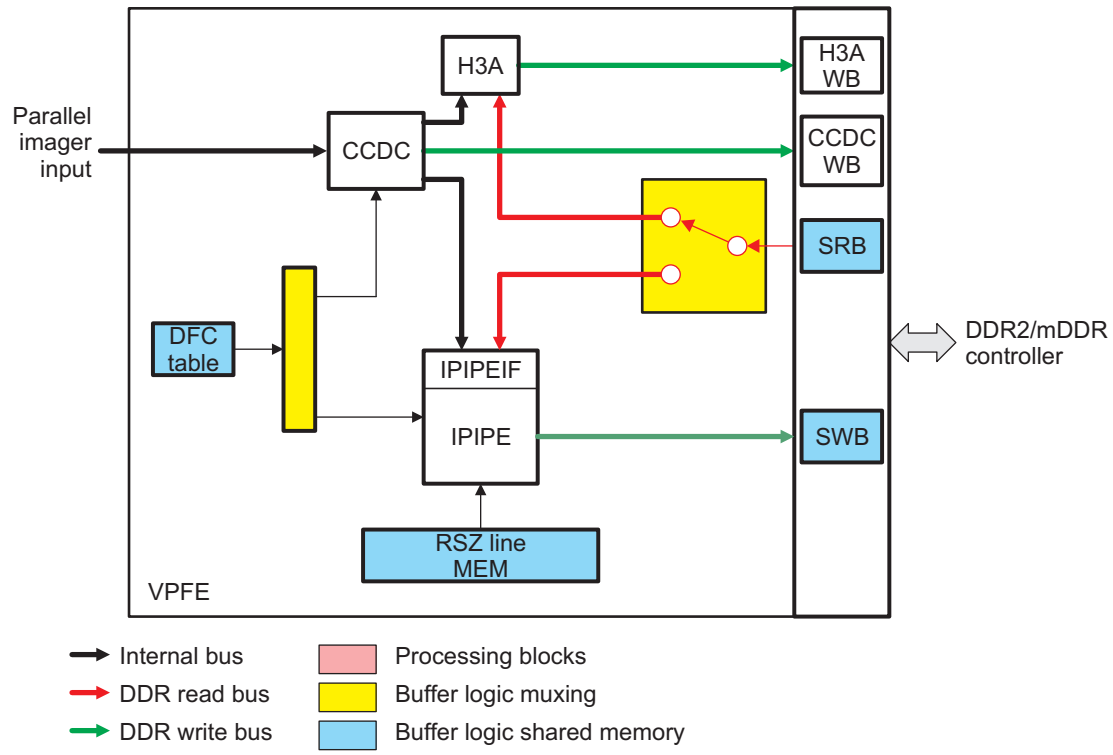


Table 29 outlines the register settings required to assign master modules to the shared memories.

Table 29. VPFE Memory Master Selection

Shared Memory	Register Field	Settings
Shared Read Buffer (SRB)	PCR.RBLCTRL	0: IPIPEIF 1: Reserved 2: H3A
Shared Write Buffer (SWB)	PCR.WBLCTRL	0: IPIPEIF 1: Reserved
DFC Table	MEMCTRL.DFCCTRL	0: IPIPE 1: CCDC
RSZ Line Memory	MEMCTRL.RSZ_CTRL	0: IPIPEIF 1: Reserved

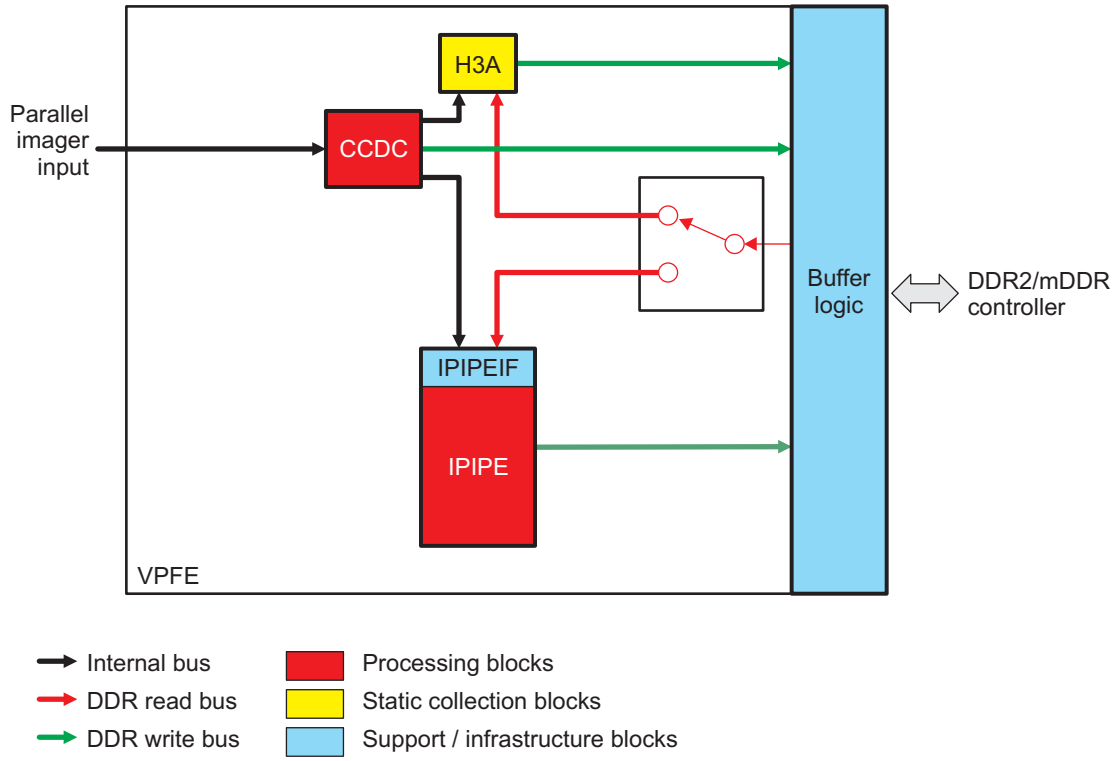
Please note that the CCDC does not have write access to the DFC table. So when the CCDC will use defect correction, the table must be programmed through the IPIPE memory table registers.

5 Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPFE for a digital camera application would include interfacing to a CCD+TG+AFE imager subsystem. In addition to programming these external devices, the VPFE would be programmed in Preview mode to capture data at a 30 Hz frame rate (draft mode). The VPFE sub-module would be configured to capture/read this data and format for display via the Image Pipe. Simultaneously, the H3A would collect data to be used by user defined focusing algorithms, etc. Figure 65 depicts the VPFE data flow diagram. The interfaces between the modules are configured using the register field values indicated in the diagram. The input to the CCDC is either RAW image data from an AFE or YCC data. The input to the Image Pipe and H3A is only RAW image data.

Figure 65. VPFE Data Flow Diagram



5.2 Resetting the Camera Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the power sleep controller.

5.3 Configuring the Clocks and the Control Signals

The input pixel data clock must be provided by the external imager device.

If the VPFE is to be configured in master mode in which the Hd/Vd sync signals are output, then the proper frame definition must be configured in the CCD Controller. Otherwise, in slave mode, the VPFE will sync to the externally provided signals.

5.4 Programming the CCD/CMOS Controller (CCDC)

This section discusses issues related to the software control of the CCD/CMOS Controller. It lists which registers are required to be programmed in different modes, how to enable and disable the CCD/CMOS Controller, how to check the status of the CCD/CMOS Controller, discusses the different register access types, and enumerates several programming constraints.

5.4.1 Hardware Setup/Initialization

This section discusses the configuration of the CCD/CMOS Controller required before image processing can begin.

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the CCD/CMOS Controller are reset to their reset values except the defect table registers. Since the defect table registers are stored in internal RAM, they do not have reset values. If the reset is a chip-level power-on reset (reset after power is applied), then the defect table register values are unknown. If the reset is a VPSS module reset (when power remains active) then the contents of this memory remains the same as before the reset.

5.4.1.2 Register Setup

Prior to enabling the CCD/CMOS controller, the hardware must be properly configured via register writes. Table 30 identifies the register parameters that must be programmed before enabling the CCD/CMOS Controller.

Table 30. CCDC Required Configuration Parameters

Function	Description
External Pin Signal Configuration	MODESET.VDHDOUT
	MODESET.VDPOL
	MODESET.HDPOL
	MODESET.FLDMODE
	MODESET.FLDPOL
	MODESET.EXWEN
	CCDCFG.VDLC
	CCDCFG.EXTRG
Input Mode	REC656.R656ON
	MODESET.INPMOD
YC Input Swap	CCDCFG.YCINSWP
SDRAM Output Enable	SYNCEN.WEN

Table 31 identifies additional configuration requirements depending on if the corresponding condition is met. It can be read as:

if(Condition is TRUE) then configuration-required parameters must be programmed.

Table 31. CCDC Conditional Configuration Parameters

Function	Condition	Configuration Required
VD/HD set as outputs	MODESET.VDHDOUT	HDWIDTH
		VDWIDTH
		PPLN
		LPFR
Interlaced Fields	MODESET.FLDMODE	CCDFCG.FIDMD
External WEN	MODESET.EXWEN	CCDCFG.WENLOG
External Trigger	CCDCFG.EXTRG	CCDCFG.TRGSEL
REC656 Input	REC656.R656ON	REC656.ECCFVH
		CCDCFG.BW656
YCC Input	MODESET.INPMOD != 0 && !REC656.R656ON	DCSUB.DCSUB
8 bit YCC Input	MODESET.INPMOD == 2 && !REC656.R656ON	CCDCFG.Y8POS

Table 31. CCDC Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
RAW input	MODESET.INPMOD == 0 && !REC656.R656ON	MODESET.DATAPOL CLAMP.CLAMPEN CSCCTL DFCCTL.GDFCEN DFCCTL.VDFCEN LSCCFG1.LSCEN BLKCMP0 BLKCMP1 COLPTN GAMMAWD.CFAP
Optical Black Clamp Enabled	CLAMP.CLAMPEN && MODESET.INPMOD == 0	CLAMP.OBST CLAMP.OBSLEN DCSUB.OBSLN
Optical Black Clamp Disabled	!CLAMP.CLAMPEN && MODESET.INPMOD == 0	DCSUB.DCSUB
CSC Enabled	CSC Enabled	CSCM0, CSCM1, CSCM2, CSCM3, CSCM4, CSCM5, CSCM6, CSCM7
CSC Disabled	!CSCCTL	
CSC Input	CSCCTL	FMTSPH, FMTLNH, FMTSLV, FMTLNV
General Defect Correction	DFCCTL.GDFCEN	VPSSBL.MEMCTRL.DFCCTRL Setup General Defect Table from IPIPE registers.
Vertical Defect Correction	DFCCTL.VDFCEN	DFCCTL.VDFCSL DFCCTL.VDFCUDA DFCCTL.VDFLSFT VDFSLV Setup Vertical Line Defect Table
Lens Shading Correction	LSCCFG1.LSCEN	LSCCFG1.GFMODE LSCCFG2 Setup LSC Table and Coordinates
Write to SDRAM	MODESET.WEN	MODESET.PACK8 CCDCFG.BSWD CCDCFG.MSBINVI SPH, NPH, SLV0, SLV1, NLV, STADRH, STADRL
Write to SDRAM in RAW Mode	MODESET.WEN && MODESET.INPMOD == 0	MODESET.LPF MODESET.DATASFT CULH, CULV, HSIZE, SDOFST, RYEGAIN, GRCYGAIN, GBGGAIN, BMGGAIN, OFFSET, OUTCLIP, GAMMAWD.CCDTBL GAMMAWD.MFIL2
A-law and H3A input bits selection	GAMMAWD.CCDTBL || H3A is receiving data from the CCDC	GAMMAWD.GWID
IPIPE input	MODESET.INPMOD == 0 && IPIPE is receiving data from the CCDC	GAMMAWD.MFILT1
Interrupt Usage	VDINT[1:0] Interrupts are enabled	VDINT0, VDINT1

5.4.2 Enable/Disable Hardware

Setting the SYNCEN.VDHDEN bit enables the CCD/CMOS controller. This should be done after all of the required registers mentioned in the previous section are programmed. With respect to the write enable bit and output address, the following procedure must be followed:

1. Set Data output address (STADRH & STADRL).
2. Enable HD/VD and WEN at the same time (MODESET.WEN & SYNCEN.VDHDEN)

If the SYNCEN.VDHDEN bit is written before the output address and SDRAM write enable bit (not recommended but may be required for a particular mode), then data will begin to be written to the old address value and not the on one recently programmed. The desired response can be achieved if the following procedure is followed:

1. Enable HD/VD (SYNCEN.VDHDEN)
2. Set output address (STADRH & STADRL)
3. Wait for next VD
4. Enable WEN (SYNCEN.WEN)

The CCD/CMOS controller always operates in continuous mode. In other words, after enabling the CCD/CMOS controller, it will continue to process sequential frames until the SYNCEN.VDHDEN bit is cleared by software. When this happens, the frame being processed will be disabled immediately, and will not continue to process the current frame.

When the CCD/CMOS controller is in master mode (HD/VD signals set to outputs), then fetching and processing of the frame begins immediately upon setting the SYNCEN.VDHDEN bit.

When the CCD/CMOS controller is in slave mode (HD/VD signals set to inputs), then processing of the frame is dependent upon the input timing of the external sensor/decoder. In order to guarantee that data from the external device is not missed, the CCD/CMOS controller should be enabled prior to data transmission from the external device. In this way, the CCD/CMOS controller will wait for data from the external device.

5.4.2.1 Enabling/Disabling the SDRAM Output

When enabling or disabling the SDRAM output port (SYNCEN.WEN), the timing of setting the following framing registers can be critical to achieve expected writing behavior: SPH, NPH, SLV0, SLV1, and NLV. In order to avoid potential unexpected data writes to the SDRAM, the following safeguards should be implemented:

- When clearing the SYNCEN.WEN bit to 0, the SDRAM framing registers (SPH, NPH, SLV0, SLV1, and NLV) should be cleared to 0 within the same VD period that the SYNCEN.WEN bit is cleared.
- Likewise, when setting the SYNCEN.WEN bit to 1, these SDRAM framing registers (SPH, NPH, SLV0, SLV1, and NLV) should be set from 0 to the appropriate values within the same VD period that the SYNCEN.WEN bit is set.

5.4.3 Events and Status Checking

The CCD/CMOS controller can generate three different interrupts: VDINT0, VDINT1, and VDINT2. Note that the SYNCEN.VDHDEN bit should be enabled to receive any of the CCD/CMOS controller interrupts.

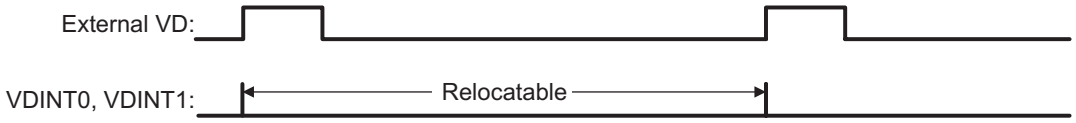
5.4.3.1 VDINT0 and VDINT1 Interrupts

As shown in Figure 66, the VDINT0 and VDINT1 interrupts occur relative to the VD pulse. The trigger timing is selected by using MODESET.VDPOL setting. VDINT0 and VDINT1 will occur after receiving the number of horizontal lines (HD pulse signals) set in the VDINT.VDINT0 and VDINT.VDINT1 register fields, respectively.

Note: In the case of BT.656 input mode, there is a VD at the beginning of each field. Therefore, there will be two interrupts for each frame (i.e., one for each field).

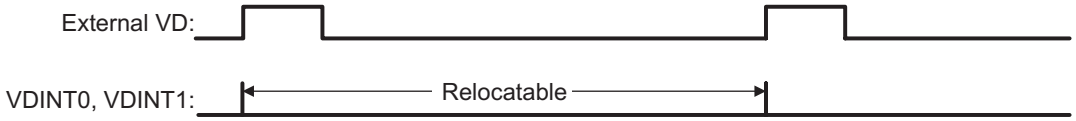
In case of the MODESET.VDPOL being 0, the VDINT0 and VDINT1 HD counters begin counting HD pulses from the rising edge of the external VD.

Figure 66. VDINT0/VDINT1 Interrupt Behavior When VDPOL = 0



In case of the MODESET.VDPOL being 1, the VDINT0 and VDINT1 HD counters begin counting HD pulses from the falling edge of the external VD.

Figure 67. VDINT0/VDINT1 Interrupt Behavior When VDPOL = 1



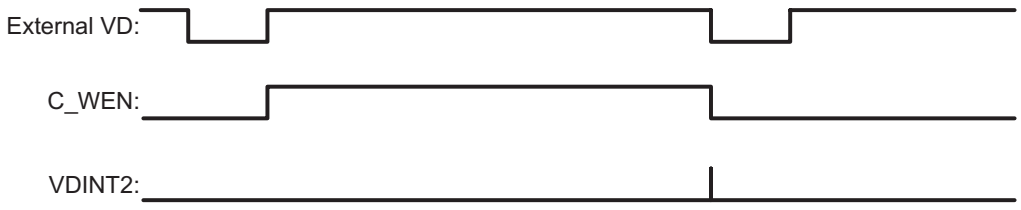
5.4.3.2 VDINT2 Interrupt

In addition to the VDINT0 and VDINT1 interrupts, the CCD/CMOS controller also has an interrupt called the VDINT2 interrupt. The VDINT2 interrupt always occurs at the falling edge of the CAM_WEN_FIELD signal (via external pin) if the following conditions are true:

- SYNCEN.VDHDEN = 1
- MODESET.EXWEN = 1
- MODESET.FLDMODE = 0

There are no registers in the CCD/CMOS controller module to configure this interrupt.

Figure 68. VDINT2 Interrupt Behavior



5.4.3.3 Status Checking

The MODESET.FLDSTAT bit is set when the field status is on an even field, and it is cleared when the field status is on an odd field.

5.4.4 Register Accessibility During Frame Processing

There are two types of register access in the CCD/CMOS Controller.

Shadowed Registers (event latched registers)— *Shadowed* registers are those which can be read and written at any time, but the written values only take effect (are latched) at certain times based on some event. Note that reads will still return the most recent write even though the settings are not used until the specific event occurs.

Busy-Writeable Registers— These registers/fields can be read or written even if the module is busy. Changes to the underlying settings takes place instantaneously.

The register/field list below can be all set as shadow registers, or optionally set as busy-writable registers. When CCDCFG.VDLC is 0, then these registers are shadowed; when CCDCFG.VDLC is 1, then these registers are busy-writable. All other CCD/CMOS controller registers not included in this list are always busy-writable.

SYNCEN.WEN	SLV1	BLKCMP1	LSCCFG1	CSCM0
MODESET.LPF	CULH	RYEGAIN	LSCCFG2	CSCM1
HDWIDTH	CULV	GRCYGAIN	LSCH0	CSCM2
VDWIDTH	HSIZE	GBGGAIN	LSCV0	CSCM3
PPLN	SDOFST	BMGGAIN	LSCKH	CSCM4
LPFR	STADRH	OFFSET	LSCKV	CSCM5
SPH	SDADRL	GAMMAWD	DFCCTL	CSCM6
NPH	CLAMP.CLAMPEN	FMTSPH	DFCVSAT	CSCM7
SLV0	BLKCMP0	FMTLNH	CSCCTL	

5.4.5 Inter-frame Operations

In between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since the SYNCEN.WEN register and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame, and the data will get latched in for the next frame. The host controller can perform these changes upon receiving an interrupt.

For more details on enabling/disabling the SDRAM output port during processing mode changes (e.g. from preview to still capture mode), see Section 5.4.2.1.

5.4.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the CCD/CMOS controller. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- PCLK must be less than VPSSCLK/2
- If SDRAM output port is enabled:
  - The memory output line offset and address should be on 32-byte boundaries.
  - NPH-1 must be a multiple of 32 bytes.
  - SPH, NPH, SLV0, SLV1, and NLV) should be cleared to 0 within the same VD period that the SYNCEN.WEN bit is cleared to 0.
  - SPH, NPH, SLV0, SLV1, and NLV) should be set from 0 to the appropriate values within the same VD period that the SYNCEN.WEN bit is set to 1.
- External WEN can not be used when at the same time as external FID.
- In RAW input mode,
  - CCDCFG.YCINSWP should be set to 0.

5.5 Programming the Image Pipe Interface (IPIPEIF)

This section discusses issues related to the software control of the IPIPE Interface. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE Interface, how to check the status of the IPIPE Interface, discusses the different register access types, and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the IPIPE Interface required before image processing can begin.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the IPIPE Interface are reset to their reset values.

5.5.1.2 Register Setup

Prior to enabling the IPIPE Interface, the hardware must be properly configured via register writes. Table 32 identifies the register parameters that must be programmed before enabling the IPIPE Interface.

Table 32. IPIPE Interface Required Configuration Parameters

Function	Configuration Required
Input Source	CFG.INPSRC
Input Clock	CFG.CLKSEL
Decimation and Anti-aliasing filter	CFG.DECM CFG.AVGFILT

Table 33 identifies additional configuration requirements depending on if the corresponding condition is met. It can be read as:

if(Condition is TRUE) then

Configuration Required parameters must be programmed

Table 33. Table 52. IPIPE Interface Conditional Configuration Parameters

Function	Condition	Configuration Required
Decimation Value	CFG.DECM	RSZ
Clock Divider	CFG.CLKSEL	CFG.CLKDIV
Input from SDRAM	CFG.INPSRC != 0	PPLN
		LPFR
		HNUM
		VNUM
		ADDRU
		ADDRL
		ADOFS
		VPSSBL.PCR.RBLCTRL
RAW input	CFG.INPSRC = 0,1,2	GAIN
RAW input from SDRAM	CFG.INPSRC = 1,2	CFG.IALAW
		CFG.PACK8IN
RAW input from SDRAM when Inverse A-law is disabled	CFG.INPSRC = 1,2 && !CFG.IALAW	CFG.DATASFT
Input from SDRAM only	CFG.INPSRC = 1,3	CFG.ONESHOT

5.5.2 Enable/Disable Hardware

When CFG.INPSRC = 0, the IPIPEIF does not need to be enabled. It processes whatever the CCDC sends. If CFG.INPSRC != 0, then the IPIPE Interface begins to fetch data from SDRAM by setting ENABLE.ENABLE bit. This should be done after all of the required registers in the IPIPE and IPIPEIF are programmed.

When the input source is the SDRAM/DDRAM, the IPIPE Interface can optionally operate in one shot mode or continuous mode by setting the CFG.ONESHOT parameter. If one shot mode is enabled, then after enabling the IPIPE Interface, the ENABLE.ENABLE bit is automatically turned off (set to 0) and only a single frame is processed from memory. In this mode, fetching and processing of the frame begins immediately upon setting the ENABLE.ENABLE bit.

When the input source is the CCD/CMOS Controller processing of the frame is dependent upon the timing of the CCDC. In order to guarantee that data from the CCDC is not missed, the IPIPE Interface should be enabled prior to the CCDC. In this way, the IPIPE Interface will wait for data from the CCDC.

When the IPIPE Interface is in continuous mode, it can be disabled by clearing the ENABLE.ENABLE bit after processing of the last frame. The disable will take place immediately since it is a busy-writable register.

5.5.3 Events and Status Checking

The IPIPE Interface will generate an IPIPEIF event to the VPSSBL at the end of each frame.

5.5.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPE Interface.

- Shadow registers

  These registers/fields can be read and written (if the field is writeable) at any time. However, the written values take effect only at the start of a frame (VD rising edge). Note that reads will still return the most recent write even though the settings are not used until the next start of frame. The following are the shadowed registers in the IPIPE Interface.

CFG.DECM	HNUM	ADOFS
CFG.AVGFILT	VNUM	RSZ
PPLN	ADDRU	GAIN
LPFR	ADDRL	

- Busy-writeable registers

  These registers/fields can be read or written even if the module is busy. Changes to the underlying settings takes place instantaneously. The following register fields are busy-writable:

ENABLE	CFG.CLKDIV	CFG.CLKSEL
CFG.ONESHOT	CFG.PACK8IN	CFG.DATASFT
CFG.INPSRC	CFG.IALAW	

The ideal procedure for changing the IPIPE Interface registers is IF (PCR.BUSY == 0) OR IF (EOF interrupt occurs):

- Disable IPIPE interface
- Change registers
- Enable IPIPE interface

5.5.5 Inter-Frame Operations

In between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several of the registers are shadowed, these modifications can take place any time before the end of the frame, and the data will get latched in for the next frame. The host controller can perform these changes upon receiving an interrupt, or an EDMA transfer can be programmed to make these changes upon receiving an event.

5.5.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPE Interface. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- If SDRAM output port is enabled:
  - The memory output line offset and address should be on 32 byte boundaries.
  - Data will be fetched starting on the second HD
  - In Darkframe subtract, LPFR must be > 0 since the first line can not be fetched.

5.6 Programming the Image Pipe (IPIPE)

This section discusses issues related to the software control of the IPIPE. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE, how to check the status of the IPIPE, discusses the different register access types, and enumerates several programming constraints.

5.6.1 Hardware Setup/Initialization

This section discusses the configuration of the IPIPE required before image processing can begin.

5.6.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the IPIPE are reset to their reset values. However, since the IPIPE programmable tables (gamma, luminance enhancer, defect correction, and histogram) are stored in internal RAM, their contents do not have reset values. If the reset is a chip-level power-on reset (reset after power is applied), then the contents of these tables are unknown. If the reset is a VPSS module reset (when power remains active) then the contents of these tables remains the same as before the reset.

5.6.1.2 Register Setup

Prior to enabling the IPIPE, the hardware must be properly configured via register writes. In order to write to the IPIPE registers, the GCL_ARM register must first be set to 1. Table 34 identifies the register parameters that must be programmed before enabling the IPIPE.

Table 34. IPIPE Required Configuration Parameters

Function	Description
Function Enable/Disable	IPIPE_MODE
	IPIPE_DPATHS
Input Size	IPIPE_VST
	IPIPE_VSZ
	IPIPE_HST
	IPIPE_HST
Clocks	GCL_CCD
	GCL_SDR
SDRAM Output	RSZ[0].RSZ_SDR_SAD_H
	RSZ[0].RSZ_SDR_SAD_L
VPSSBL Configuration	VPSSBL.PCR.WBLCTRL
	VPSSBL.MEMCTRL.IPIPE_WD_EN
	VPSSBL.MEMCTRL.RESZ_CTRL

Table 35 identifies additional configuration requirements depending on if the corresponding condition is met. It can be read as:

if(Condition is TRUE), then configuration-required parameters must be programmed.

Table 35. IPIPE Conditional Configuration Parameters

Function	Condition	Configuration Required	
IPIPE RAW Processing Path Functions	IPIPE_DPATHS < 2	IPIPE_COLPAT	WB2_WG_GB
		DFC_EN	WB2_WG_B
		D2F_EN	
		PRE_EN	YCC_ADJ
		HST_EN	YCC_Y_MIN
		WB2_DGAIN	YCC_Y_MIN
		WB2_WG_R	YCC_C_MIN
		WB2_WG_GR	YCC_C_MAX
IPIPE RAW to YCbCr Processing Path Functions	IPIPE_DPATHS = 0	RGB_MUL_RR	
		RGB_MUL_GR	
		RGB_MUL_BR	YCC_MUL_RY
		RGB_MUL_RG	YCC_MUL_GY
		RGB_MUL_GG	YCC_MUL_BY
		RGB_MUL_BG	YCC_MUL_RCB
		RGB_MUL_RB	YCC_MUL_GCB
		RGB_MUL_GB	YCC_MUL_BCB
		RGB_MUL_BG	YCC_MUL_RCR
		RGB_OFT_OR	YCC_MUL_GCR
		RGB_OFT_OG	YCC_MUL_BCR
		RGB_OFT_OB	YCC_OFT_Y
		GMM_CFG.BYPR	YCC_MUL_CB
		GMM_CFG.BYPG	YCC_MUL_CR
		GMM_CFG.BYPB	YCC_PHS
YCbCr Processing Path Functions	IPIPE_DPATHS != 3	YEE_EN, FCS_EN,	
		RSZ_SEQ, RZA_AAL,	
		RSZ[0].EN, RSZ[1].EN	
Boxcar	IPIPE_DPATHS = 3 && BOX_EN	BOX_MODE	
		BOX_TYP	
		BOX_SHF	
Defect Correction	DFC_EN	DFC_SEL, DFC_ADR,	
		DFC_SIZ,	
		VPSSBL.MEMCTRL.DFCCTRL	
		Setup Defect Table	

Table 35. IPIPE Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
Noise Filter	D2F_EN	D2F_CFG
		D2F_THR[32]
		D2F_STR[32]
Pre Filter	PRE_EN	PRE_TYP, PRE_SHF,
		PRE_GAIN, PRE_THR_G,
		PRE_THR_B, PRE_THR_1
Histogram	HST_EN	HST_MODE, HST_SEL,
		HST_PARA, HST[x].HST_VST,
		HST[x].HST_VSZ
		HST[x].HST_HST
		HST[x].HST_HSZ
Gamma Correction	GMM_CFG.BYPR ||	GMM_CFG.TBL
	GMM_CFG.BYPG ||	GMM_CFG.SIZ
	GMM_CFG.BYPB	Setup Gamma Table(s) if in RAM
Edge Enhancement	YEE_EN	YEE_EMF, YEE_SHF,
		YEE_MUL_00, YEE_MUL_01,
		YEE_MUL_02, YEE_MUL_10,
		YEE_MUL_11, YEE_MUL_12,
		YEE_MUL_20, YEE_MUL_21,
		YEE_MUL_22
		Setup Luminance Enhancement Table
False Color Suppression	FCS_EN	FSC_TYP, FSC_SHF_Y,
		FSC_SHF_C, FSC_THR,
		FSC_SGN, FSC_LTH
RSZ Enabled (where z = 0 or 1)	RSZ[x].EN	RSZ[x].RSZ_MODE
		RSZ[x].RSZ_I_VST
		RSZ[x].RSZ_I_HST
		RSZ[x].RSZ_O_VSZ
		RSZ[x].RSZ_O_HST
		RSZ[x].RSZ_O_HSZ
		RSZ[x].RSZ_V_PHS
		RSZ[x].RSZ_V_DIF
		RSZ[x].RSZ_H_PHS
		RSZ[x].RSZ_H_DIF
		RSZ[x].RSZ_H_TYP
		RSZ[x].RSZ_H_LSE
		RSZ[x].RSZ_RGB_EN
		RSZ[x].RSZ_SDR_BAD_H
		RSZ[x].RSZ_SDR_BAD_L
		RSZ[x].RSZ_SDR_SAD_H
		RSZ[x].RSZ_SDR_SAD_L
		RSZ[x].RSZ_SDR_OFT
		RSZ[x].RSZ_SDR_PTR_S
		RSZ[x].RSZ_SDR_PTR_E

Table 35. IPIPE Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
RSZ Enabled (where z = 0 or 1)	RSZ[x].EN && !RSZ[x].RSZ_RGB_EN	RSZ[x].RSZ_SDR_BAD_H RSZ[x].RSZ_SDR_BAD_L RSZ[x].RSZ_SDR_SAD_H RSZ[x].RSZ_SDR_SAD_L RSZ[x].RSZ_SDR_OFT RSZ[x].RSZ_SDR_PTR_S RSZ[x].RSZ_SDR_PTR_E
RSZ Input Line Confined Mode	RSZ_SEQ.TMM = 1	RSZ[x].RSZ_I_VSZ
RSZ Horizontal LPF Programmed Value	RSZ[x].RSZ_H_LSE = 1	RSZ[x].RSZ_H_LPF
RSZ RGB Output Configuration	RSZ[x].RSZ_RGB_EN	RSZ[x].RSZ_RGB_TYP
RSZ RGB Alpha Value in 32 Bit Output Mode	RSZ[x].RSZ_RGB_TYP. TYP = 0	RSZ[x].RSZ_RGB_BLD
Interrupt Usage	If IPIPE interrupts are required	IRQ_EN
IRQ RZA Config	IRQ_EN.INT2	IRQ_RZA
IRQ RZB Config	IRQ_EN.INT3	IRQ_RZB

In certain bypass modes, the data still passes through modules which need to be reset to their default values in order to not modify the data being passed through. The following sections identify which registers need to be set to which values in the various bypass modes.

5.6.1.2.1 Resizer Bypass Mode

Since the YCbCr data still passes through the RZA block in resizer bypass mode, the following registers must be set accordingly:

GCK_SDR = 0
RSZ_SEQ.SEQ = 0
RSZ_SEQ.TMM = 0
RSZ_AAL = 0
RSZ[0].RSZ_O_HPS = 0
RSZ[0].RSZ_V_PHS = 0
RSZ[0].RSZ_V_DIF = 256
RSZ[0].RSZ_H_PHS = 0
RSZ[0].RSZ_H_DIF = 256
RSZ[0].RSZ_H_LSE = 0
RSZ[1].RSZ_EN = 0

5.6.1.2.2 RAW input, RAW output Mode (IPIPE_DPATHS.FMT = 1)

In this mode, the RAW data bypasses the RAW to YCbCr processes (see Figure 37), but since it still passes through the YCbCr processing blocks, the following registers must be set accordingly:

IPIPE_DPATHS.FMT = 1
BOX_EN = 0
YCC_ADJ.CTR = 16
YCC_ADJ.BRT = 0
YCC_Y_MIN = 0
YCC_Y_MAX = 255
YCC_C_MIN = 0
YCC_C_MAX = 255
YEE_EN = 0
FCS_EN = 0
RSZ_SEQ.TMM = 0
RSZ[0].RSZ_EN = 1
RSZ[0].RSZ_I_VPS = 0
RSZ[0].RSZ_I_HPS = 0
RSZ[0].RSZ_O_HPS = 0
RSZ[0].RSZ_V_PHS = 0
RSZ[0].RSZ_V_DIF = 256
RSZ[0].RSZ_H_PHS = 0
RSZ[0].RSZ_H_DIF = 256
RSZ[0].RSZ_H_TYP = 0
RSZ[0].RSZ_H_LSE = 0
RSZ[0].RSZ_H_LPF = 0
RSZ[0].RSZ_RGB_EN = 0
RSZ[1].RSZ_EN = 0

5.6.1.2.3 RAW Bypass Mode (IPIPE_DPATHS.FMT = 1 and IPIPE_DPATHS.BYPASS = 1)

In this mode, the RAW data bypasses the RAW to YCbCr processes (see Figure 377), but since it still passes through the YCbCr processing blocks, the registers listed in Section 5.6.1.2.2 must be set accordingly. Additionally, since no processing should be done in this mode, the following registers must also be set accordingly:

DFC_EN = 0	WB2_WG_R = 128
D2F_EN = 0	WB2_WG_GR = 128
PRE_EN = 0	WB2_WG_GB = 128
WB2_DGAIN = 256	WB2_WG_B = 128

5.6.1.3 Internal Memory Access

The RAM_xxx registers are used to access the internal RAM of the IPIPE. This RAM is used to store defect correction, gamma correction, and edge enhancement tables, as well as Histogram outputs. If these functions are to be used in the application, then the internal RAM corresponding to these functions must be initialized prior to enabling the IPIPE. Note that the histogram memory is not self-clearing, so it must be initialized to 0s before enabling, and cleared to zeros during reads (write-after-read procedure below).

Note: In order to access the RAM_xxx registers, the GCL_ARM register must first be set to 1 AND the PCLK input to the IPIPE must be enabled. If PCLK is not being driven by an external imager at the time these registers need to be accessed, then the IPIPEIF can be configured to drive the PCLK input to IPIPE by setting the IPIPEIF->CFG.CLKSEL register bit to 1.

5.6.1.3.1 Read/Write Procedures

The IPIPE internal memory values can be written, read, and written after read. If multiple values need to be set in incremental addresses, then the RAM_MODE.ADR bit can be set so that only the first address needs to be set and subsequent reads/writes will auto-increment the internal address. The following procedures should be followed to access the internal memories:

For memory write:

1. Write to RAM_MODE: set memory selection and set EXT = 0 and WDT = 1.
2. Write to RAM_ADR: set starting offset into memory.
3. Write to RAM_WDT: Write data.

For memory read:

1. Write to RAM_MODE: set memory selection and set EXT = 0 and WDT = 0.
2. Write to RAM_ADR: set starting offset into memory.
3. Write to RAM_WDT: Write dummy data.
4. Read the data of the internal memory from RAM_RDT.

For memory write after read:

1. Write to RAM_MODE: set memory selection and set EXT = 0 and WDT = 1.
2. Write to RAM_ADR: set starting offset into memory.
3. Write to RAM_WDT: Write data.
4. Read the data of the internal memory from RAM_RDT.

5.6.1.3.2 Memory Map

This section indicates how the data is stored in each memory space.

- Histogram 0 and 1
  The memory map for histogram changes according to HST_PARA[BIN].

(1) HST_PARA[BIN] = 0 (HST_PARA[BIN]=0 indicates that the size of a bin of the histogram is 32)

Histogram 0:

Table address [8]	No use
Table address [7..6]	Region number 0~3
Table address [5]	Color number MSB. 0=R, 1=B
Table address [4..0]	Bin number 0~31

Histogram 1:

Table address [8]	No use
Table address [7..6]	Table address [7..6]
Table address [5]	Color number MSB. 0=G, 1=Y
Table address [4..0]	Bin number 0~31

(2) HST_PARA[BIN] = 1 (HST_PARA[BIN]=1 indicates that the size of a bin of the histogram is 64)

Histogram 0:

Table address [8..7]	Region number 0~3
Table address [6]	Color number MSB. 0=R, 1=B
Table address [5..0]	Bin number 0~63

Histogram 1:

Table address [8..7]	Region number 0~3
Table address [6]	Color number MSB. 0=G, 1=Y
Table address [5..0]	Bin number 0~63

(3) HST_PARA[BIN] = 3 (HST_PARA[BIN]=3 indicates that the size of a bin of the histogram is 128)

Histogram 0:

Table address [8]	Region number LSB
Table address [7]	Color number MSB. 0=R, 1=B
Table address [6..0]	Bin number 0~127

Histogram 1:

Table address [8]	Region number LSB
Table address [7]	Color number MSB. 0=G, 1=Y
Table address [6..0]	Bin number 0~127

(4) HST_PARA[BIN] = 4 (HST_PARA[BIN]=4 indicates that the size of a bin of the histogram is 256)

Histogram 0:

Table address [8]	Color number MSB. 0=R, 1=B
Table address [7..0]	Bin number 0~255

Histogram 1:

Table address [8]	Color number MSB. 0=G, 1=Y
Table address [7..0]	Bin number 0~255

Address	Description	WDT/RDT Depth
RAM_ADR[9..0] = 0x0000h	Table address = 0x0000h [15..0]	15..0
RAM_ADR[9..0] = 0x0001h	Table address = 0x0000h [19..16]	3..0
RAM_ADR[9..0] = 0x0002h	Table address = 0x0001h [15..0]	15..0
RAM_ADR[9..0] = 0x0003h	Table address = 0x0001h [19..16]	3..0
RAM_ADR[9..0] = 0x0004h	Table address = 0x0002h [15..0]	15..0
RAM_ADR[9..0] = 0x0005h	Table address = 0x0002h [19..16]	3..0
RAM_ADR[9..0] = 0x03FCh	Table address = 0x01FEh [15..0]	15..0
RAM_ADR[9..0] = 0x03FDh	Table address = 0x01FEh [19..16]	3..0
RAM_ADR[9..0] = 0x03FEh	Table address = 0x01FFh [15..0]	15..0
RAM_ADR[9..0] = 0x03FFh	Table address = 0x01FFh [19..16]	3..0

- Defect Correction

Address	Description	WDT/RDT Depth
RAM_ADR[9..0] = 0x0000h	Defect 0 [11..0]	11..0
RAM_ADR[9..0] = 0x0001h	Defect 0 [26..12]	14..0
RAM_ADR[9..0] = 0x0002h	Defect 1 [11..0]	11..0
RAM_ADR[9..0] = 0x0003h	Defect 1 [26..12]	14..0
RAM_ADR[9..0] = 0x0004h	Defect 2 [11..0]	11..0
RAM_ADR[9..0] = 0x0005h	Defect 2 [26..12]	14..0
RAM_ADR[9..0] = 0x07FCh	Defect 1022 [11..0]	11..0
RAM_ADR[9..0] = 0x07FDh	Defect 1022 [26..12]	14..0
RAM_ADR[9..0] = 0x07FEh	Defect 1023 [11..0]	11..0
RAM_ADR[9..0] = 0x07FFh	Defect 1023 [26..12]	14..0

- Gamma R & G & B & RGB-ALL

Address	Description	WDT/RDT Depth
RAM_ADR[9..0] = 0x0000h	Slope 0	9..0
RAM_ADR[9..0] = 0x0001h	Offset 0	9..0
RAM_ADR[9..0] = 0x0002h	Slope 1	9..0
RAM_ADR[9..0] = 0x0003h	Offset 1	9..0
RAM_ADR[9..0] = 0x0004h	Slope 2	9..0
RAM_ADR[9..0] = 0x0005h	Offset 2	9..0
RAM_ADR[9..0] = 0x03FCh	Slope 510	9..0
RAM_ADR[9..0] = 0x03FDh	Offset 510	9..0
RAM_ADR[9..0] = 0x03FEh	Slope 511	9..0
RAM_ADR[9..0] = 0x03FFh	Offset 511	9..0

- Edge Enhancer

Address	Description	WDT/RDT Depth
RAM_ADR[9..0] = 0x0200h	Parameter HPF = -512	8..0
RAM_ADR[9..0] = 0x0201h	Parameter HPF = -511	8..0
RAM_ADR[9..0] = 0x03FFh	Parameter HPF = -1	8..0
RAM_ADR[9..0] = 0x0000h	Parameter HPF = 0	8..0
RAM_ADR[9..0] = 0x0001h	Parameter HPF = 1	8..0
RAM_ADR[9..0] = 0x01FEh	Parameter HPF = 510	8..0
RAM_ADR[9..0] = 0x01FFh	Parameter HPF = 511	8..0

5.6.2 Enable/Disable Hardware

Setting the IPIPE_EN.EN bit enables the IPIPE. This should be done after all of the required registers and tables mentioned in the previous section are programmed.

When the IPIPE is set to one shot mode, only a single frame is processed. When the IPIPE is in continuous mode, it can be disabled by clearing the IPIPE_EN.EN bit during the processing of the last frame. The disable will be latched in at the end of the frame it was written in.

5.6.3 Events and Status Checking

The IPIPE can generate 6 different events to the VPSSBL interrupt and EDMA inputs as outlined in Table 36.

Table 36. IPIPE Events

Event	Description
IRQ0	Final pixel from each frame is flushed from the image pipe (not resizer) and histogram completion event
IRQ1	SDRAM Write Completion Event
IRQ2	RZA Interval Completion Event
IRQ3	RZB Interval Completion Event
IRQ5	Register Update Ready Notification Event

Each of these interrupt events can be separately enabled in the IRQ_EN register. The intervals for RZA and RZB interval completion events (IRQ2 and IRQ3) can be set in the IRQ_RZA and IRQ_RZB registers, respectively. The following timing diagrams indicate the relative timing of IRQ0, IRQ1, and IRQ5.

Figure 69. Interrupt Timing When Resized Area = Resize Frame

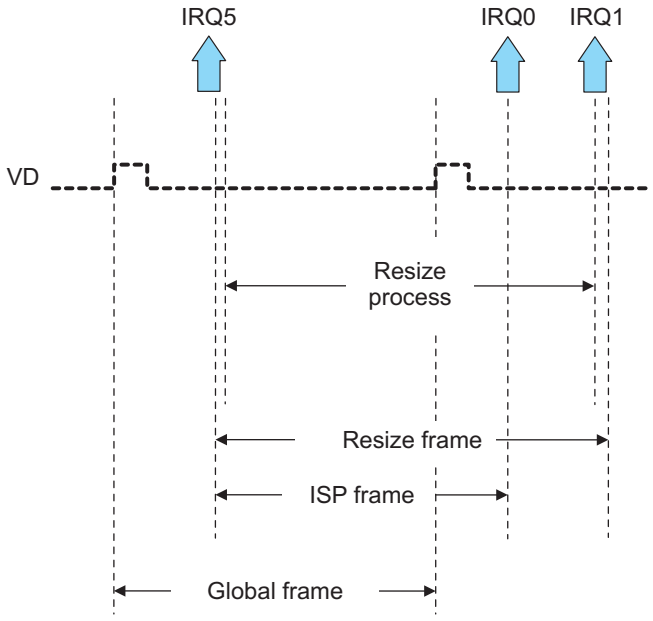
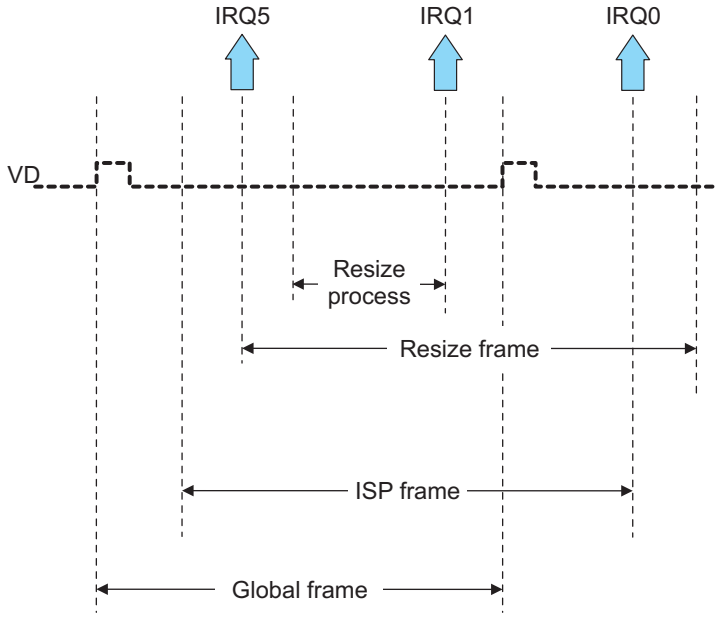


Figure 70. Interrupt Timing When Resized Area < Resize Frame



The resizers have the following status registers that are typically used in frame division mode - H and ring buffer output implementation:

Table 37. IPIPE Resizer Status Registers

Register	Description
RSZ[x].RSZ_V_PHS_O	Phase of last line in previous resize process
RSZ[x].RSZ_V_SIZ_O	Actual number of output lines in previous resize process.
RSZ[x].RSZ_SDR_PTR_O	Current output line in output buffer

5.6.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPE: busy-writeable registers, and shadow registers.

- Busy-writeable registers

  These registers/fields can be read or written when the module is busy. Changes to the underlying settings takes place instantaneously, therefore it is recommended that they only be written when the module is not busy in order to avoid unintended behavior. The following registers are busy-writable:

IPIPE_MODE	RAM_MODE	RSZ[x].RSZ_MODE
IPIPE_DPATHS	RAM_ADR	HST_MODE
GCL_ARM	RAM_WDT	HST_SEL.SOURCE
GCL_CCD	RAM_RDT	
GCL_SDR	IRQ_EN	

- Shadow registers

  These registers/fields can be read and written (if the field is writeable) at any time after receiving the IRQ5 event. However, the written values take effect only at the start of the next frame. Note that reads will still return the most recent write even though the settings are not used until the next start of frame. If these registers are written before receiving the IRQ5 event, the written values may apply to the current frame or the next frame. All the IPIPE registers not listed as "Busy-writable" above are included as "shadow" registers.

5.6.5 Inter-Frame Operations

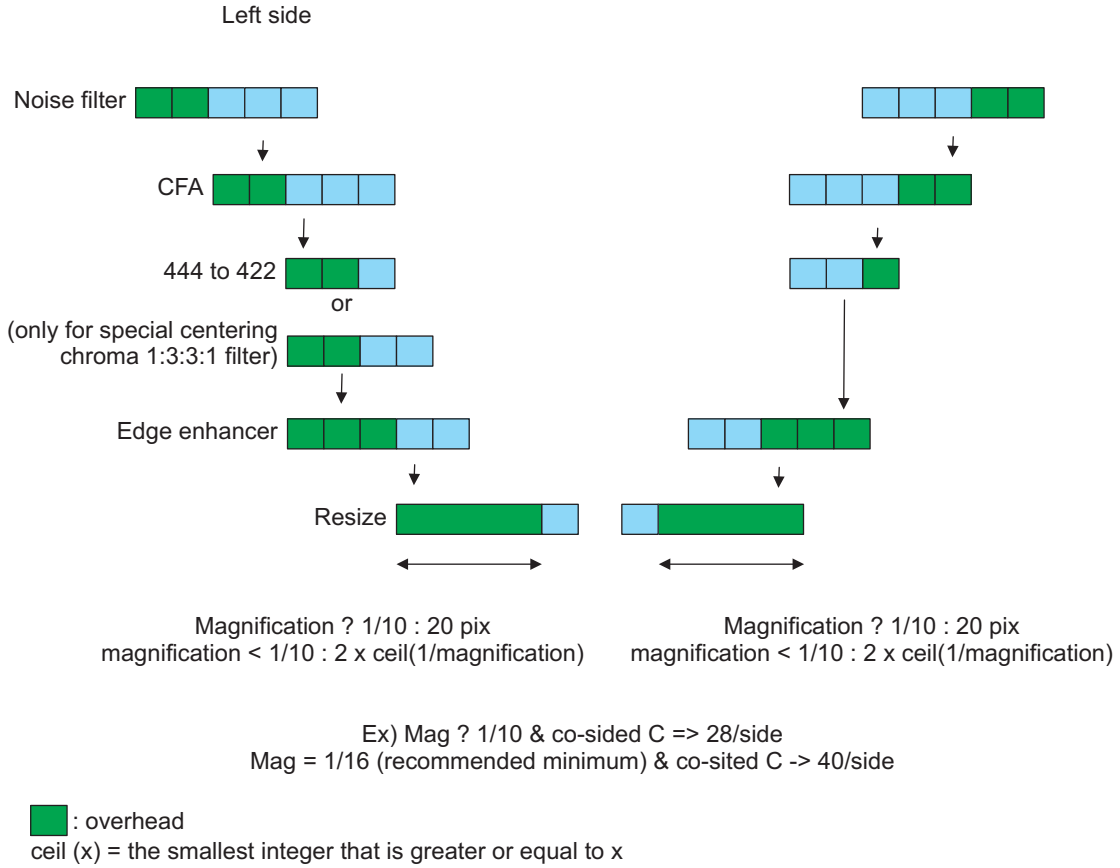
In between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several registers and the memory pointer registers are shadowed, these modifications can take place any time after the INT5 (update register) interrupt and before the end of the frame, and the data will get latched in for the next frame. The host controller can perform these changes upon receiving an interrupt, or an EDMA transfer can be programmed to make these changes upon receiving an event.

In between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several registers and the memory pointer registers are shadowed, these modifications can take place any time after the INT5 (update register) interrupt and before the end of the frame, and the data will get latched in for the next frame. The host controller can perform these changes upon receiving an interrupt, or an EDMA transfer can be programmed to make these changes upon receiving an event.

5.6.5.1 Overhead Lines and Pixels

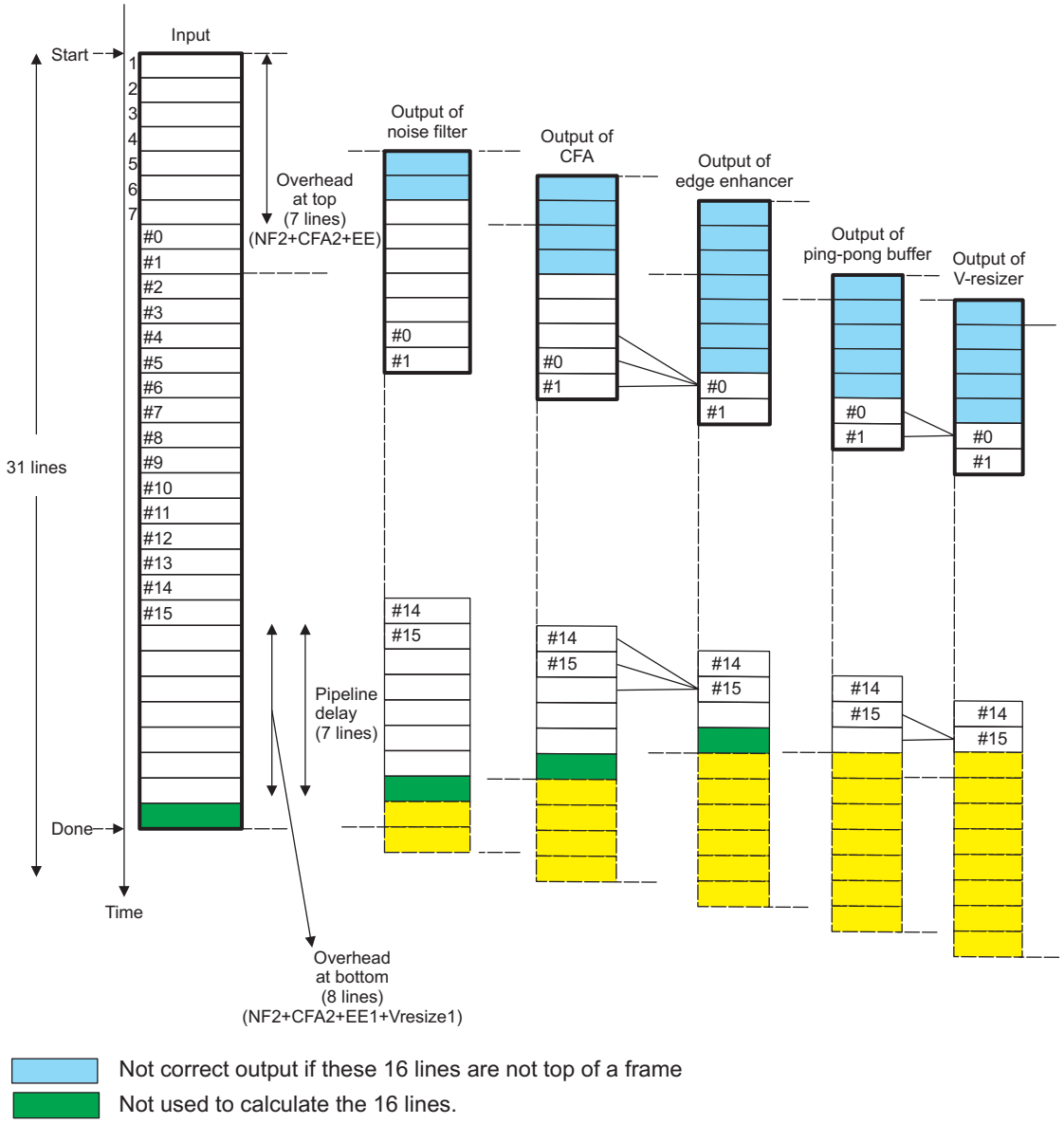
Filtering processes in IPIPE creates overhead pixels at each side (left/right/top/bottom). Figure 71 shows the lateral (left/right) overhead of each process. Noise Filter and CFA have two pixels of overhead at each side. The 444 to 422 module has one overhead pixel except when interpolation is in 1:3:3:1 mode. When in 1:3:3:1 mode, the 444 to 422 module has two overhead pixels. Edge Enhancer has three overhead pixels. Each resizer has variable overhead pixels depending on magnification rate. As a rule of thumb, the overhead for the Resizer can be described by the following equation.

Figure 71. Lateral Overhead Pixels



In the vertical direction, the noise filter module and the CFA module have two lines of overhead at top and bottom. The edge enhancer has three overhead lines at the both sides. The resizer has an overhead line only at the bottom. In addition to these overheads, the ping-pong buffer before resizer module consumes 1-line of pipeline delay. This delay does not affect output data. These overhead lines are described in Figure 72.

Figure 72. Vertical Overhead Pixels



5.6.5.2 Frame Division Mode

IPIPE supports input images split into sub-blocks (frame division mode). The overheads at the boundaries of each block are masked by the resizer module. In the following section, examples of these operations are described.

5.6.5.2.1 Frame Division Mode-V

In *Frame Division Mode-V*, the input image is horizontally split into multiple images as shown in Figure 73. Each image at right or left is processed separately, and the output is merged in SDRAM to make a single output image. Following are the example of the settings of RZA for this mode (same settings can apply to RZB).

The input image is split into the left side block with width of h1 and the right side block with width of h2. Each image is resized to the ratio of 256/d to make images with width of H0 and H2 = H - H0 respectably. These two images form the target image with width of H (Figure 73d).

An example of parameters for resizing of left side blocks and right side blocks are shown in Figure 74. For the matching of the output from left side block and right side block, a certain amount of overlap pixels are required. The minimum overlap size is 20 for d <= 2560, and 2 × ceil(d/256) for d > 2560. When other processes, such as CFA, are working, larger overlap is required (See Section 5.6.5.1).

Figure 73. Frame Division Mode - V

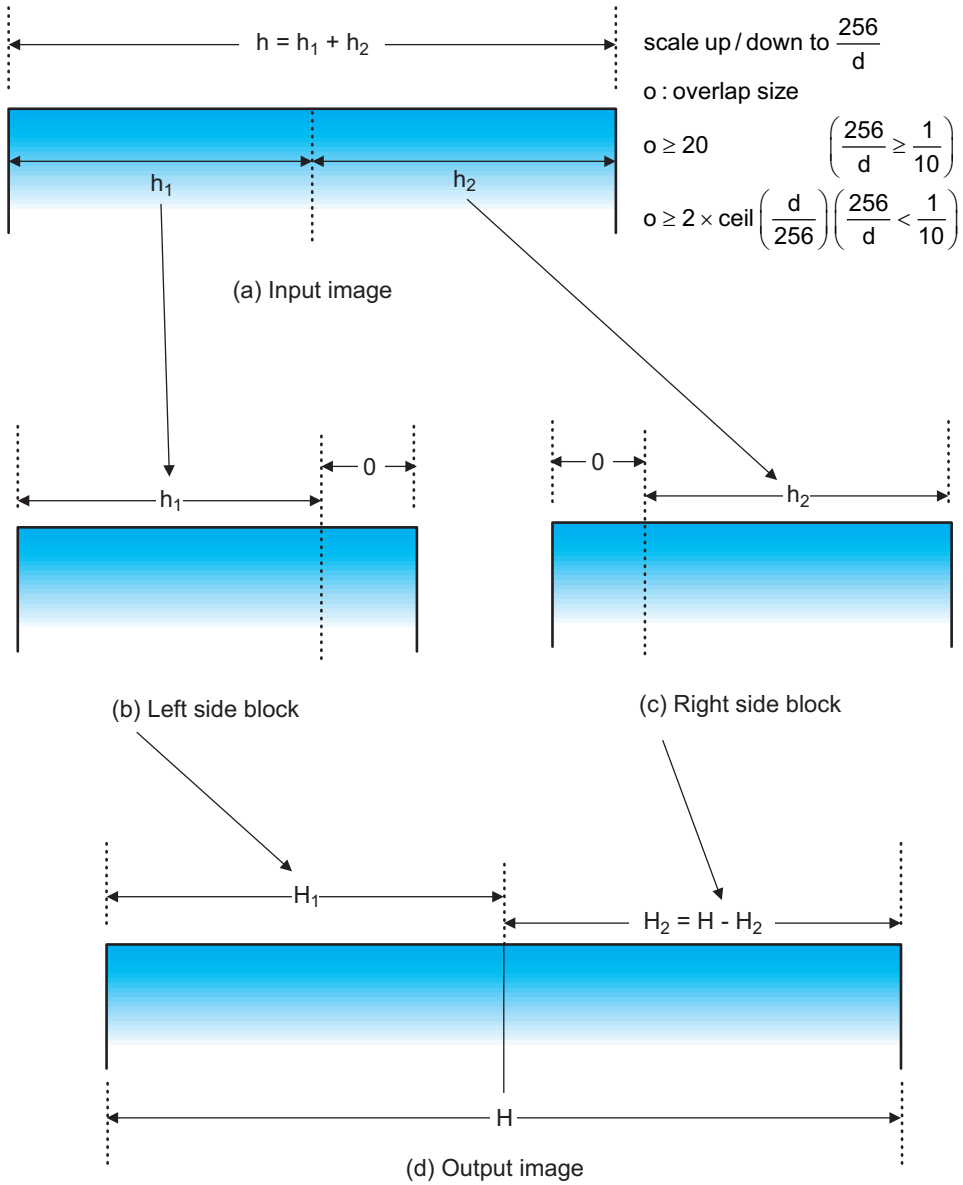


Figure 74. Register Settings for Frame Division Mode - V

input_h_position = 0
output_h_position = 0

$$tmp\_size = floor\left(\left(h_1 - 1\right) \times \frac{256}{d}\right)$$

$$output\_h\_size = \begin{cases} tmp\_size + 1 & \text{if } tmp\_size \text{ is odd} \\ tmp\_size & \text{if } tmp\_size \text{ is even} \end{cases}$$

h_initial_phase = 0

RSZ[0].RSZ_I_HST = input_h_position
RSZ[0].RSZ_0_HST = output_h_position
RSZ[0].RSZ_0_HSZ = output_h_size-1
RSZ[0]/RSZ_H_PHS = h_initial_phase

(a) register setting for left side blocks

$$X_0 = 2 \times ceil\left(\frac{\left(x_0 \times 256\right)}{\frac{d}{2}}\right)$$

$$x_1 = 2 \times floor\left(\frac{\left(\frac{X_0 \times d}{256}\right)}{2}\right)$$

$$input\_h\_size = h_2 + o$$

input_h_position = x_1 - x_0
output_h_position = H_1 - X_0
output_h_size = H_2 = H - H_1
h_initial_phase = X_0 x d - x_1 x 256

RSZ[0].RSZ_I_HST = input_h_position
RSZ[0].RSZ_0_HST = output_h_position
RSZ[0].RSZ_0_HSZ = output_h_size-1
RSZ[0].RSZ_H_PHS = h_initial_phase

(b) register setting for right side blocks

input_h_size : The width of input image for that block.
input_h_position : The pixel at which resize modules start proceeding.
output_h_position : The number of pixels to skip in the produced image.
output_h_size : The number of pixels to output.
h_initial_phase : The first interpolation ratio in horizontal direction.

Note: ceil9x0: the smallest interger number not smaller than x
floor(x): the largest interger number not larger than x

5.6.5.2.1.1 Frame Division Mode-H

This section describes the example of parameter setting values in frame division mode-H, where the input image is split into several boxes (Figure 75).

In this section, it is assumed that the width of the input image is h and the height v. Also, those of the output image are H and V. The input image is split into left side and right side. Left side blocks have the dimension of h1 by b, right side blocks h2 by b, as shown in Figure 75b. Each block is scaled up or down to the size of 256/d to form a part of the target image.

The input image is split into blocks as shown in Figure 75. In this section, the blocks are numbered from left to right, top to bottom. Therefore, block - 2n is the left side block at the n-th row. Also, block - (2m + 1) is the right side block at the m-th row. Each block need one overlap line between vertical adjacent blocks. Each block also needs some more overlap lines (overlap1 lines at the top and overlap2 lines at the bottom where overlap1 = overlap2) for other processes such as CFA. Therefore, the height of each input block after the first row of blocks should be (b + 1 + overlap1 + overlap2) as shown in Figure 75b.

Figure 75. Frame Division Mode - H

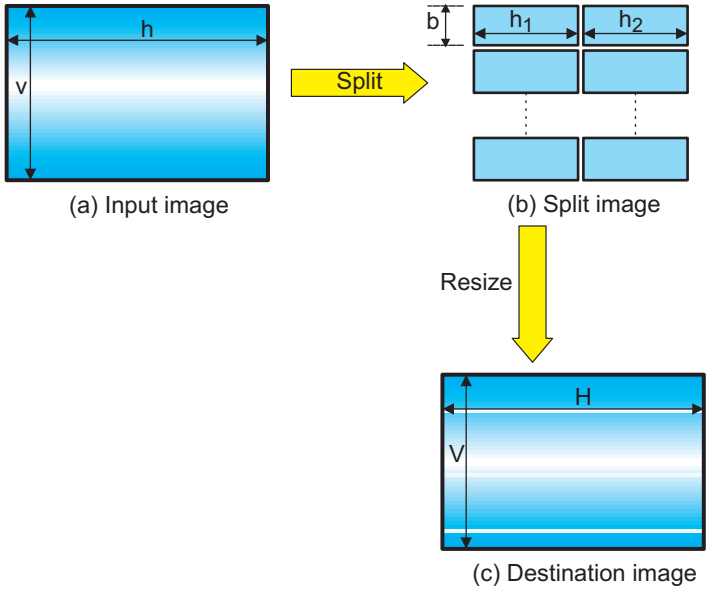
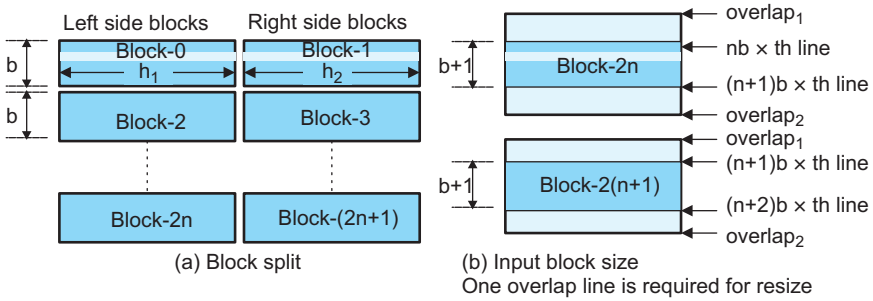


Figure 76. Blocks in Frame Division Mode - H



An example of parameter setting for frame division mode-H is shown in Figure 77.

The first vertical mixing ratio (initial phase) of each block may be acquired from register value. The last phase (the mixing ratio of the last line) of block - 2(n - 1) is written to register RSZ[0].RSZ_V_PHS_O by IPIPE module after the completion of that block. Let this value be p_{last}, the next initial phase (the first mixing ratio) of block-2n will be either p_{last} + d - 256 (when p_{last} is smaller than 256) or p_{last} - 256 (otherwise). This value should be set to register RSZ[0].RSZ_V_PHS for block - 2n and block - (2n + 1).

Also, *input line number confined mode* should be used for this operation (RSZ_SEQ.TMM = 1) The number of lines produced by each block is written to the register RSZ[0].RSZ_V_SIZ_O.

For the parameters in horizontal direction, see Section 5.6.5.2.1.

Figure 77. Register Settings for Frame Division Mode - H

$$v\_input\_size = \begin{cases} b + 1 + overlap & \text{first row of blocks} \\ b + 1 + (2 \times overlap) & \text{middlerows of blocks} \end{cases}$$

$$v\_input\_position = overlap$$

$$v\_initial\_phase = \begin{cases} \rho last + d - 256 \text{ if } \rho last \langle 256 \\ \rho last + d - 256 \text{ if } \rho last \langle 256 \end{cases}$$

d : vertical resize parameter, Re size ratio is 256 / d

terminal_mode = `1'

```
RSZ[0].RSZ_I_VST = v_input_position
RSZ[0].RSZ_I_VSZ = v_input_size
RSZ[0].RSZ_V_PHS = v_initial_phase
RSZ_SEQ.TMM = terminal_mode
```

v_input_size	:The height of each input block.
ρ_{last}	:The last phase of (2n-1)-th block. (RSZ[0].RSZ_V_PHS_0) Use 256 for block-0 and block-1.
v_initial_phase	:The mixing ratio of the first putput line.
terminal_mode	:The condition to finish the process. 1 is "input ;one confinded mode."

The output image will be placed in memory area as shown in Figure 78. In this figure, the first address of the destination area is *initial_address* (in byte address) and width of the area is *memory_area_width* (bytes). Also the area has the height of *memory_area_height* lines. Also, the output image of the blocks at the left has the width of H_1 pixels.

For the blocks at the left (block 0, 2, 4, ...), the register setting should be the values shown in Figure 79a. Here, rps_{last} is the register value of RSZ[0].RSZ_SDR_PTR_O written by IPIPE module for the blocks of previous row. This value shows the next destination line in the memory area. For block - 2n, RSZ[0].RSZ_SDR _PTR_O for block - 2(n - 1) should be used as rps_{last}. For the block at the right, the register setting are shown in Figure 79b.

Figure 78. Register Settings for Frame Division Mode - H

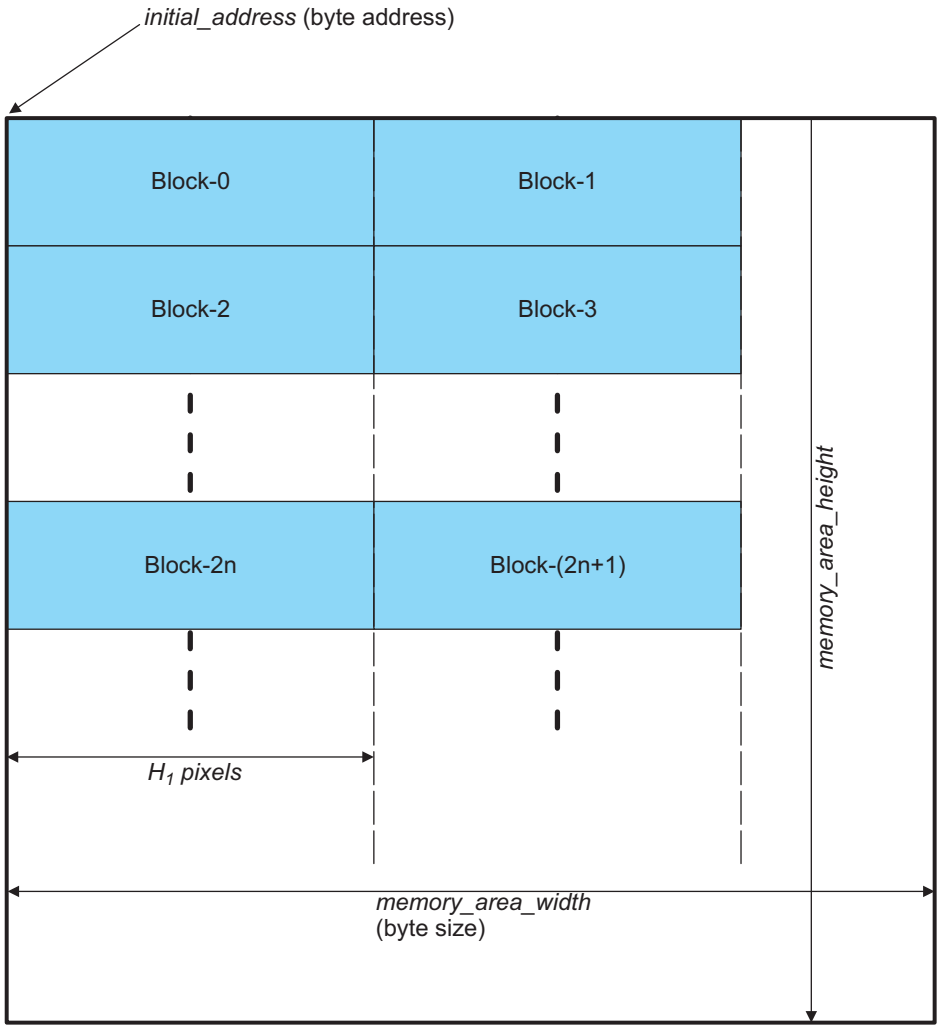


Figure 79. Memory Settings for Frame Division Mode - H

Left side blocks (block 0, 2, ..., 2n,

RSZ[0].RSZ_SDR_BAD = *initial_address*
RSZ[0].RSZ_SDR_SAD = *initial_address* + *memory_width* × rps_{new}
RSZ[0].RSZ_SDR_OFT = *memory_width*
RSZ[0].RSZ_SDR_PTR_S = rps_{new}

(a). Register setting for left side

Right side blocks (block 1, 3, ..., 2n+1,

RSZ[0].RSZ_SDR_BAD = *initial_address* + $2H_1$
RSZ[0].RSZ_SDR_SAD = *initial_address* + $2H_1$ + *memory_width* × rps_{new}
RSZ[0].RSZ_SDR_OFT = *memory_width*
RSZ[0].RSZ_SDR_PTR_S = rps_{new}

(b). Register setting for right side

$$rsp_{new} = \begin{cases} (\text{RSZ}[0].\text{RSZ\_SDR\_PTR\_O} + 1) \bmod memory\_height & \text{RSZ}[0].\text{RSZ\_V\_SIZ\_O} > 0 \\ \text{RSZ}[0].\text{RSZ\_SDR\_PTR\_O} & \text{RSZ}[0].\text{RSZ\_V\_SIZ\_O} = 0 \end{cases}$$

rsp_{new} : The line in memory space where the next line will be placed.
RZA_SDR_PTR_O : The line pointer at which the last output is written. this register value is written by ISP module.

5.6.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPE. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The first input pixel should be the RED pixel in order for the register names to be aligned with the appropriate colors.
- Both the input and output widths should be less than or equal to 1344 pixels.
- RSZ[1] output width should be less than or equal to 640 pixels.
- Input height and width should be equal to or smaller than CCD/CMOS Controller output height and width.
- Output width should be even
- Each input line should have at least IPIPE_HSZ + 1 + 8 PCLK cycles.
- Each input frame should have at least IPIPE_VSZ + 1 + 10 HD pulses (+4 in continuous mode).
- Resize ratios are limited to the range from 1/16x scale down to 8x scale up.

5.7 Programming the Hardware 3A (H3A)

This section discusses issues related to the software control of the H3A module. It lists which registers are required to be programmed in different modes, how to enable and disable the H3A, how to check the status of the H3A, discusses the different register access types, and enumerates several programming constraints.

5.7.1 Hardware Setup/Initialization

This section discusses the configuration of the H3A required before image processing can begin.

5.7.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the H3A are reset to their reset values.

5.7.1.2 Register Setup

For register configuration purposes, the AF Engine and the AEW Engine of the H3A can independently be configured. There are separate enable bits for each engine, so this section will be divided into the AF engine and the AEW engine.

5.7.1.2.1 AF Engine

Prior to enabling the AF engine, the hardware must be properly configured via register writes. Table 38 identifies the register parameters that must be programmed before enabling the AF engine of the H3A.

Table 38. AF Engine Required Configuration Parameters

Function	Configuration Required
Input Source	PCR.INP_SRC
AF Optional Preprocessing	PCR.AF_MED_EN, PCR.AF_ALAW_EN
AF Mode Configuration	PCR.RGBPOS, PCR.FVMODE
Paxel Start and Size Information	AFPAX1, AFPAX2, AFPAXSTART, AFIIRSH
Memory Address	AFBUFST
Filter Coefficients	AFCOEF0[10:0] , AFCOEF1[10:0]

Table 39 identifies additional configuration requirements depending on if the corresponding condition is met. It can be read as:

if(Condition is TRUE), then configuration-required parameters must be programmed.

Table 39. AF Engine Conditional Configuration Parameters

Function	Condition	Configuration Required
Horz. Median Filter	PCR.AF_MED_EN	PCR.MED_TH
DDR2/mDDR controller input	PCR.INP_SRC	PCR.INP_WIDTH, RSDR_ADDR, RADR_OFFSET SDR_FRSIZE.HSIZE, SDR_FRSIZE.VSIZE
Bit Selection	!PCD.INP_WIDTH	SDR_FRSIZE.BITSEL

The following references offer guidelines on how to program the filter coefficients and make use of the H3A output.

- M. Gamadia, V. Peddigari, N. Kehtarnavaz, S-Y. Lee, G. Cook, *Real-time Implementation of Auto Focus on the TI DSC Processor*, Proceedings of SPIE Real-Time Imaging Conference, Jan 2004
- N. Kehtarnavaz, H-J. Oh, *Development and Real-Time Implementation of a Rule-Based Auto-Focus Algorithm*, Journal of Real-Time Imaging, 9, 197-203, 2003

5.7.1.2.2 AEW Engine

Prior to enabling the AEW Engine, the hardware must be properly configured via register writes. Table 40 identifies the register parameters that must be programmed before enabling the AEW Engine of the H3A.

Table 40. AEW Engine Required Configuration Parameters

Function	Configuration Required
Input Source	PCR.INP_SRC
AEW Optional Preprocessing	PCR.AEW_ALAW_EN
Saturation Limit	PCR.AVE2LMT
Window Start and Size Information	AEWWIN1, AEWINSTART, AEWINBLK, AEWSUBWIN
Memory Address	AEWBUFST

Table 41 identifies additional configuration requirements depending on if the corresponding condition is met. It can be read as:

if(Condition is TRUE) then

Configuration Required parameters must be programmed

Table 41. AEW Engine Conditional Configuration Parameters

Function	Condition	Configuration Required
DDR2/mDDR controller Input	PCR.INP_SRC	PCR.INP_WIDTH
		RSDR_ADDR, RADR_OFFSET
		SDR_FRSIZE.HSIZE, SDR_FRSIZE.VSIZE
Bit Selection	!PCD.INP_WIDTH	SDR_FRSIZE.BITSEL

5.7.2 Enable/Disable Hardware

Setting the PCR.AF_EN bit enables the AF engine, and the PCR.AEW_EN bit enables the AEW engine. This should be done after all of the required registers mentioned in the previous section are programmed.

When the input source is SDRAM, the H3A operates in one-shot mode. Om addition to the enable bits mentioned above, the PCR.SDR_FETCH_EN bit must be set for each frame processed from SDRAM.

When the input source is the video port interface of the CCD/CMOS controller, the H3A operates in continuous mode. In this mode, processing of the frame is dependent upon the timing of the CCD controller. In order to guarantee that data from the CCD controller is not missed, the H3A should be enabled prior to the CCD controller. In this way, the H3A will wait for data from the CCD controller. The AF engine or the AEW engine can be disabled by clearing the PCR.AF_EN or PCR.AEW_EN bit, respectively, during the processing of the last frame. The disable will be latched in at the end of the frame in which it was written.

5.7.3 Events and Status Checking

Both the AF engine and the AEW engine generates an interrupt and an EDMA event at the end of processing each frame. However, these two interrupts are internally tied together so that only one H3A interrupt signal (and H3A EDMA event) is seen by the interrupt controller (and EDMA). If the AF engine and AEW engine are not processing the same frame concurrently, then this shouldn't be an issue. However, if both the AF and AEW engines are running concurrently, then one of two outcomes may occur:

- The H3A interrupt may seem to only trigger once for each frame. This can happen when the processing for both the AF Engine and the AEW engine is finished at/near the same time. The interrupt service routine does not have enough time to clear the interrupt flag for the first interrupt before the second interrupt occurs.

- The H3A interrupt may trigger twice for each frame. This can happen when either the AF engine or the AEW engine finishes processing the frame much earlier than the other one. In this case, the interrupt service routine does have enough time to clear the interrupt flag for the first interrupt by the time the second interrupt occurs.

The outcome is dependent on the difference in location of the last paxel/window in the frame (determines when processing is finished), the frequency of the relative clocks in the system, the occurrence and triggering of other interrupts in the system, and the latencies of the context switching and interrupt service routine execution.

The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits are set when the start of frame occurs (if the PCR.AF_EN and/or PCR.AEW_EN bits are 1 at that time). They are automatically reset to 0 at the end of processing a frame. The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits may be polled to determine the end of frame status.

5.7.4 Register Accessibility During Frame Processing

There are two types of register access in the H3A module.

- Shadow registers
  - These registers/fields can be read and written (if the field is writeable) at any time. However, the written values take effect only at the start of a frame. Note that reads will still return the most recent write even though the settings are not used until the next start of frame.
  - The PCR, AFBUFST, and AEWBUFST registers are the only shadowed registers in the H3A module.
- Busy-lock registers
  - All registers EXCEPT the PCR, AFBUFST, and AEWBUFST registers belong to this category.
  - Busy-lock registers cannot be written when the module is busy. Writes will be allowed to occur, but no change will occur in the registers (blocked writes from hardware perspective, but allowed write from the software perspective). Once the busy bit in the PCR register is reset to 0, the busy-lock registers can be written.

The ideal procedure for changing the H3A registers is

IF (busy == 0) OR IF (EOF interrupt occurs):

DISABLE AF or AE/AWB

CHANGE REGISTERS

ENABLE AF or AE/AWB

5.7.5 Inter-Frame Operations

In between frames, it may be necessary to modify the memory pointers before processing the next frame. Since the PCR and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame, and the data will get latched in for the next frame. The host controller can perform these changes upon receiving an interrupt, or an EDMA transfer can be programmed to make these changes upon receiving an event.

5.7.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the H3A. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The output addresses must be on 64-byte boundaries

AF Engine:

- The paxel horizontal start value must be greater than or equal to the IIR horizontal start position.
- The width and height of the paxels must be an even number.
- The minimum width of the auto focus paxel must be 8 pixels.

- Paxels cannot overlap the last pixel in a line.
- Paxels must be adjacent to one another.

AEW Engine:

- The width and height of the windows must be an even number.
- Sub-sampling windows can only start on even numbers.
- The minimum width of the AE/AWB windows must be 8 pixels.

5.8 Programming the Buffer Logic (VPSSBL and VPSSCLK Registers)

This section discusses issues related to the software control of the VPSS Buffer Logic. The VPSS Buffer Logic comprises the infrastructure data path switches, interrupt control multiplexing, and clock gating control within the VPSS. This section briefly lists which registers are required to be programmed in different configurations of the VPSS.

5.8.1 Hardware Setup/Initialization

This section discusses the configuration of the VPSSBL and VPSSCLK required before image processing can begin.

5.8.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the VPSSBL and VPSSCLK register modules are reset to their reset values.

5.8.1.2 Register Setup

Prior to enabling the modules within the VPSS, the buffer logic hardware must be properly configured via register writes. Table 42 identifies the register parameters that must be programmed properly before enabling the various modules. The items not bolded are optional, depending on if the operational mode of the module requires the setting or not.

Table 42. VPSSBL and VPSSCLK Required Configuration Parameters

Function	Configuration Required
CCDC	VPSSBL.MEMCTRL.DFCCTRL
	VPSSCLK.CLKCTRL.CCDCCLK
IPIPEIF	**VPSSBL.PCR.RBLCTRL**
	VPSSCLK.CLKCTRL.IPIPECLK
IPIPE	**VPSSBL.PCR.WBLCTRL**
	VPSSBL.MEMCTRL.IPIPE_WD_EN
	VPSSBL.MEMCTRL.RESZ_CTRL
	VPSSBL.MEMCTRL.DFCCTRL
	VPSSCLK.CLKCTRL.IPIPECLK
H3A	**VPSSBL.PCR.RBLCTRL**
	VPSSCLK.CLKCTRL.H3ACLK

5.8.2 Events and Status Checking

The VPSSBL controls the selection of which module interrupts are routed to the ARM interrupt controller and EDMA event controllers using the VPSSBL.INTSEL and VPSSBL.EVTSEL registers. The VPSSBL.INTSTAT register can also be used to poll for events. For more details, see Section 3.2.

5.8.3 Register Accessibility During Frame Processing

There is only one type of register access in the VPSSBL and VPSSCLK modules.

Busy-Writeable Registers— These registers/fields can be read or written even if the module is busy. Changes to the underlying settings takes place instantaneously.

5.8.4 Inter-Frame Operations

Since the VPSSBL and VPSSCLK registers are busy-writable, care must be taken when modifying any of these registers. It is recommended that affected modules be disabled while switching modes and modifying any of these registers.

5.8.5 Summary of Constraints

None noted.

6 Registers

There are eight sub-modules associated with the Video Processing Front End subsystem, as show in Table 43.

Table 43. Video Processing Front End Sub-Module Register Map

Address	Acronym	Register Description	Section
0x01C7:0600	CCDC	CCD Controller	Section 6.1
0x01C7:0100	IPIPEIF	Image Pipe IF	Section 6.2
0x01C7:1000	IPIPE	Image Pipe	Section 6.3
0x01C7:0080	H3A	Hardware 3A	Section 6.4
0x01C7:0800	VPSSBL	VPSS Buffer Logic	Section 6.5
0x01C7:0000	VPSSCLK	VPSS Clock Control	Section 6.6

6.1 CCD Controller (CCDC) Registers

The CCD controller (CCDC) registers are shown in Table 44.

Table 44. CCD Controller (CCDC) Registers

Address	Acronym	Register Description	Section
0x01C7:0600	SYNCEN	Synchronization Enable Register	Section 6.1.1
0x01C7:0604	MODESET	Mode Setup Register	Section 6.1.2
0x01C7:0608	HDWIDTH	HD Pulse Width Register	Section 6.1.3
0x01C7:060C	VDWIDTH	VD Pulse Width Register	Section 6.1.4
0x01C7:0610	PPLN	Pixels Per Line Register	Section 6.1.5
0x01C7:0614	LPFR	Lines Per Frame Register	Section 6.1.6
0x01C7:0618	SPH	Start Pixel Horizontal Register	Section 6.1.7
0x01C7:061C	NPH	Number Of Pixels Horizontal Register	Section 6.1.8
0x01C7:0620	SLV0	Start Line Vertical - Field 0 Register	Section 6.1.9
0x01C7:0624	SLV1	Start Line Vertical - Field 1 Register	Section 6.1.10
0x01C7:0628	NLV	Number Of Lines Vertical Register	Section 6.1.11
0x01C7:062C	CULH	Culling - Horizontal Register	Section 6.1.12
0x01C7:0630	CULV	Culling - Vertical Register	Section 6.1.13
0x01C7:0634	HSIZE	Horizontal Size Register	Section 6.1.14
0x01C7:0638	SDOFST	SDRAM Line Offset Register	Section 6.1.15
0x01C7:063C	STADRH	SDRAM Address - High Register	Section 6.1.16
0x01C7:0640	STADRL	SDRAM Address - Low Register	Section 6.1.17
0x01C7:0644	CLAMP	CCD Data Clamping Register	Section 6.1.18
0x01C7:0648	DCSUB	DC Clamp Register	Section 6.1.19
0x01C7:064C	COLPTN	CCD Color Pattern Register	Section 6.1.20
0x01C7:0650	BLKCMP0	Black Compensation #1 Register	Section 6.1.21
0x01C7:0654	BLKCMP1	Black Compensation #2 Register	Section 6.1.22
0x01C7:0658	MEDFILT	CCD Median Filter Register	Section 6.1.23
0x01C7:065C	RYEGAIN	CCD Gain Adjustment - R/Ye Register	Section 6.1.24
0x01C7:0660	GRCYGAIN	CCD Gain Adjustment - Gr/Cy Register	Section 6.1.25
0x01C7:0664	GBGGAIN	CCD Gain Adjustment - Gb/G Register	Section 6.1.26
0x01C7:0668	BMGGAIN	CCD Gain Adjustment - B/Mg Register	Section 6.1.27
0x01C7:066C	OFFSET	CCD Offset Adjustment Register	Section 6.1.28
0x01C7:0670	OUTCLIP	Output Clipping Value Register	Section 6.1.29
0x01C7:0674	VDINT0	VD Interrupt #0 Register	Section 6.1.30

Table 44. CCD Controller (CCDC) Registers (continued)

Address	Acronym	Register Description	Section
0x01C7:0678	VDINT1	VD Interrupt #1 Register	Section 6.1.31
0x01C7:0680	GAMMAWD	Gamma Correction Settings Register	Section 6.1.32
0x01C7:0684	REC656IF	REC656 Control Register	Section 6.1.33
0x01C7:0688	CCDCFG	CCD Configuration Register	Section 6.1.34
0x01C7:0694	FMTSPH	Start Pixel Horizontal Register	Section 6.1.35
0x01C7:0698	FMTLNH	Number Of Pixels Register	Section 6.1.36
0x01C7:069C	FMTSLV	Start Line Vertical Register	Section 6.1.37
0x01C7:06A0	FMTLNV	Number Of Lines Register	Section 6.1.38
0x01C7:06F4	LSCCFG1	Lens Shading Correction Configuration 1 Register	Section 6.1.39
0x01C7:06F8	LSCCFG2	Lens Shading Correction Configuration 2 Register	Section 6.1.40
0x01C7:06FC	LSCH0	Lens Shading Correction - Center Position (H0) Register	Section 6.1.41
0x01C7:0700	LSCV0	Lens Shading Correction - Center Position (V0) Register	Section 6.1.42
0x01C7:0704	LSCKH	Lens Shading Correction - Horizontal Coefficients Register	Section 6.1.43
0x01C7:0708	LSCKV	Lens Shading Correction - Vertical Coefficients Register	Section 6.1.44
0x01C7:070C	LSCMEMCTL	Lens Shading Correction - Memory Control Register	Section 6.1.45
0x01C7:0710	LSCMEMD	Lens Shading Correction - Memory Write Data Register	Section 6.1.46
0x01C7:0714	LSCMEMQ	Lens Shading Correction - Memory Read Data Register	Section 6.1.47
0x01C7:0718	DFCCTL	Defect Correction - Control Register	Section 6.1.48
0x01C7:071C	DFCVSAT	Defect Correction - Vertical Saturation Level Register	Section 6.1.49
0x01C7:0720	DFCMEMCTL	Defect Correction - Memory Control Register	Section 6.1.50
0x01C7:0724	DFCMEM0	Defect Correction - Set V Position Register	Section 6.1.51
0x01C7:0728	DFCMEM1	Defect Correction - Set H Position Register	Section 6.1.52
0x01C7:072C	DFCMEM2	Defect Correction - Set SUB1 Register	Section 6.1.53
0x01C7:0730	DFCMEM3	Defect Correction - Set SUB2 Register	Section 6.1.54
0x01C7:0734	DFCMEM4	Defect Correction - Set SUB3 Register	Section 6.1.55
0x01C7:0738	CSCCTL	Color Space Converter Enable Register	Section 6.1.56
0x01C7:073C	CSCM0	Color Space Converter - Coefficients #0 Register	Section 6.1.57
0x01C7:0740	CSCM1	Color Space Converter - Coefficients #1 Register	Section 6.1.58
0x01C7:0744	CSCM2	Color Space Converter - Coefficients #2 Register	Section 6.1.59
0x01C7:0748	CSCM3	Color Space Converter - Coefficients #3 Register	Section 6.1.60
0x01C7:074C	CSCM4	Color Space Converter - Coefficients #4 Register	Section 6.1.61
0x01C7:0750	CSCM5	Color Space Converter - Coefficients #5 Register	Section 6.1.62
0x01C7:0754	CSCM6	Color Space Converter - Coefficients #6 Register	Section 6.1.63
0x01C7:0758	CSCM7	Color Space Converter - Coefficients #7 Register	Section 6.1.64
0x01C7:075C	DATAOFST	Data Offset Register	Section 6.1.65

6.1.1 Synchronization Enable Register (SYNCEN)

The synchronization enable register (SYNCEN) is shown in Figure 80 and described in Table 45.

Figure 80. Synchronization Enable Register (SYNCEN)

15	2	1	0
Reserved		WEN	VDHDEN
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 45. Synchronization Enable Register (SYNCEN) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved
1	WEN		Data Write Enable. Controls whether or not CCD raw data is written to SDRAM. This bit is latched by VD.
		0	Disable.
		1	Enable.
0	VDHDEN		VD/HD Enable. If VD/HD are defined as output, activates internal timing generator. If VD/HD are defined as inputs, activates internal timing generator to synchronize with VD/HD.
		0	Disable.
		1	Enable

6.1.2 Mode Setup Register (MODESET)

The mode setup register (MODESET) is shown in Figure 81 and described in Table 46.

Figure 81. Mode Setup Register (MODESET)

15	14	13	12	11	10	8
FLDSTAT	LPF	INPMOD		PACK8	DATASFT	
R-0	R/W-0	R/W-2		R/W-0	R/W-0	

7	6	5	4	3	2	1	0
FLDMODE	DATAPOL	EXWEN	FLDPOL	HDPOL	VDPOL	Reserved	VDHDOUT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 46. Mode Setup Register (MODESET) Field Descriptions

Bit	Field	Value	Description
15	FLDSTAT		Field Status.
		0	Odd field
		1	Even field
14	LPF		3-tap Low-Pass (anti-aliasing) filter. 1/4, 1/2, 1/4 filtering applied to CCD data.
			This bit is latched by VD.
		0	Off
		1	On
13-12	INPMOD		Data input mode.
		0	CCD RAW data.
		1	YCbCr 16-bit.
		2	YCbCr 8-bit.
		3	Reserved.
11	PACK8		Pack to 8-bits/pixel (into SDRAM).
		0	Normal (16 bits/pixel).
		1	Pack to 8-bits/pixel.
10-8	DATASFT		CCD Data Right Shift for Data Written to SDRAM valid only when INPMOD is set to 0.
		0	No shift.
		1	1-bit
		2	2-bits
		3	3-bits
		4	4-bits
		5	5-bits
		6	6-bits
		7	Reserved
7	FLDMODE		Sensor field mode.
			This bit should not be set if the EXWEN bit is set.
		0	Non-interlaced (progressive).
		1	Interlaced.
6	DATAPOL		CCD data polarity.
		0	Normal (no change).
		1	One's complement.

Table 46. Mode Setup Register (MODESET) Field Descriptions (continued)

Bit	Field	Value	Description
5	EXWEN		External WEN selection. When set to 1 and when ENABLE is set to 1, the external WEN signal is used as the external memory write enable (to SDRAM/DDRAM). The data is stored to memory only when the external sync (HD and VD) signals are active.
			This bit should not be set if the FLDMODE bit is set.
		0	Do not use external WEN (Write Enable).
		1	Use external WEN (Write Enable).
4	FLDPOL		Field indicator polarity.
		0	Positive
		1	Negative
3	HDPOL		HD sync polarity.
		0	Positive
		1	Negative
2	VDPOL		VD sync polarity.
		0	Positive
		1	Negative
1	Reserved.	0	Reserved.
0	VDHDOUT		VD/HD sync direction.
		0	Input
		1	Output

6.1.3 HD Pulse Width Register (HDWIDTH)

The HD pulse width register (HDWIDTH) is shown in Figure 82 and described in Table 47.

Figure 82. HD Pulse Width Register (HDWIDTH)

15	12	11	0
Reserved		HDW	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 47. HD Pulse Width Register (HDWIDTH) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	HDW	0-FFFh	Width of HD sync pulse if output: HDW + 1 pixel clocks. HDWIDTH is not used when HD is input, i.e. when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.4 VD Pulse Width Register (VDWIDTH)

The VD pulse width register (VDWIDTH) is shown in Figure 83 and described in Table 48.

Figure 83. VD Pulse Width Register (VDWIDTH)

15	12	11	0
Reserved		VDW	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

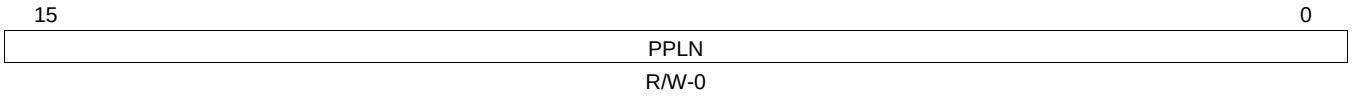
Table 48. VD Pulse Width Register (VDWIDTH) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VDW	0-FFFh	Width of VD sync pulse if output: VDW + 1 lines. VDWIDTH is not used when VD is input, i.e. when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.5 Pixels Per Line Register (PPLN)

The pixels per line register (PPLN) is shown in Figure 84 and described in Table 49.

Figure 84. Pixels Per Line Register (PPLN)



LEGEND: R/W = Read/Write; *-n* = value after reset

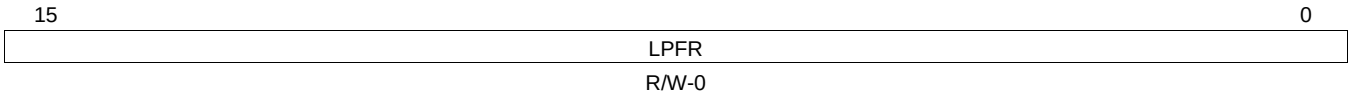
Table 49. Pixels Per Line Register (PPLN) Field Descriptions

Bit	Field	Value	Description
15-0	PPLN	0-FFFFh	Pixels per line. Number of pixel clock periods in one line. HD period = PPLN + 1 pixel clocks PPLN is not used when HD and VD are inputs, i.e. when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.6 Lines Per Frame Register (LPFR)

The lines per frame register (LPFR) is shown in Figure 85 and described in Table 50.

Figure 85. Lines Per Frame Register (LPFR)



LEGEND: R/W = Read/Write; *-n* = value after reset

Table 50. Lines Per Frame Register (LPFR) Field Descriptions

Bit	Field	Value	Description
15-0	LPFR	0-FFFFh	Half lines per filed or frame. Sets number of half lines per frame or field. VD period = (HLPFR + 1)/2 lines LPFR is not used when HD and are inputs, i.e. when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.7 Start Pixel Horizontal Register (SPH)

The start pixel horizontal register (SPH) is shown in Figure 86 and described in Table 51.

Figure 86. Start Pixel Horizontal Register (SPH)

15	14	0
Reserved	SPH	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 51. Start Pixel Horizontal Register (SPH) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	SPH	0-7FFFh	Start pixel, horizontal. Sets pixel clock position at which data output to SDRAM begins, measured from the start of HD. This bit field is latched by VD.

6.1.8 Number of Pixels Horizontal Register (NPH)

The number of pixels horizontal register (NPH) is shown in Figure 87 and described in Table 52.

Figure 87. Number of Pixels Horizontal Register (NPH)

15	14	0
Reserved	NPH	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 52. Number of Pixels Horizontal Register (NPH) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	NPH	0-7FFFh	Number of pixels, horizontal. Sets number of horizontal pixels that will be output to SDRAM = (NPH + 1) and 0xFFF0, i.e. the number of horizontal output pixels is truncated to multiples of 16. This bit field is latched by VD.

6.1.9 Start Line Vertical - Field 0 Register (SLV0)

The start line vertical - field 0 register (SLV0) is shown in Figure 88 and described in Table 53.

Figure 88. Start Line Vertical - Field 0 Register (SLV0)

15	14	0
Reserved	SLV0	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 53. Start Line Vertical - Field 0 Register (SLV0) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	SLV0	0-7FFFh	Start Line, Vertical (Field 0). Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.10 Start Line Vertical - Field 1 Register (SLV1)

The start line vertical - field 1 register (SLV1) is shown in Figure 89 and described in Table 54.

Figure 89. Start Line Vertical - Field 1 Register (SLV1)

15	14	0
Reserved	SLV1	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 54. Start Line Vertical - Field 1 Register (SLV1) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	SLV1	0-7FFFh	Start Line, Vertical (Field 1). Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.11 Number of Lines Vertical Register (NLV)

The number of lines vertical register (NLV) is shown in Figure 90 and described in Table 55.

Figure 90. Number of Lines Vertical Register (NLV)

15	14	0
Reserved	NLV	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 55. Number of Lines Vertical Register (NLV) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	NLV	0-7FFFh	Number of lines, vertical. Sets number of vertical lines that will be output to SDRAM. The number of lines output to SDRAM = (NLV + 1). This bit field is latched by VD.

6.1.12 Culling Horizontal Register (CULH)

The culling horizontal register (CULH) is shown in Figure 91 and described in Table 56.

Figure 91. Culling Horizontal Register (CULH)

15	8	7	0
CULHEVN		CULHODD	
R/W-255		R/W-255	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 56. Culling Horizontal Register (CULH) Field Descriptions

Bit	Field	Value	Description
15-8	CULHEVN		Horizontal culling pattern for even line. When writing to SDRAM, 8_bit mask:
		0	Cull.
		1	Retain.
			LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD.
7-0	CULHODD		Horizontal culling pattern for odd line. When writing to SDRAM, 8_bit mask:
		0	Cull.
		1	Retain.
			LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD.

6.1.13 Culling Vertical Register (CULV)

The culling vertical register (CULV) is shown in Figure 92 and described in Table 57.

Figure 92. Culling Vertical Register (CULV)

15	8	7	0
Reserved		CULV	
R-0		R/W-255	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 57. Culling Vertical Register (CULV) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	CULV		Vertical culling pattern.
			8_bit mask:
		0	Cull.
		1	Retain.
			LSB is first line, MSB is 8th line, then pattern repeats.
			This bit field is latched by VD.

6.1.14 Horizontal Size Register (HSIZE)

The horizontal size register (HSIZE) is shown in Figure 93 and described in Table 58.

Figure 93. Horizontal Size Register (HSIZE)

15	13	12	11	0
Reserved		ADR_UPDT	LNOFST	
R-0		R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 58. Horizontal Size Register (HSIZE) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved. Read as zero.
12	ADR_UPDT		SDRAM address update.
			By setting this bit, SDRAM address in a line is automatically decreased so that a line can be horizontally flipped in the SDRAM.
			This bit field is latched by VD.
		0	Address increment.
		1	Address decrement.
11-0	LNOFST	0-FFFh	Address offset for each line. Sets size of line in SDRAM, units: 32 bytes. Either 16 or 32 pixels depending on setting of PACK8.
			This bit field is latched by VD.

6.1.15 SDRAM Line Offset Register (SDOFST)

The SDRAM line offset register (SDOFST) is shown in Figure 94 and described in Table 59.

Figure 94. SDRAM Line Offset Register (SDOFST)

15	14	13 12	11 9	8 6	5 3	2 0
Reserved	FIINV	FOFST	LOFTS0	LOFTS1	LOFTS2	LOFTS3
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 59. SDRAM Line Offset Register (SDOFST) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14	FIINV		Field identification signal inverse.
			This field is latched by VD.
		0	Non inverse.
		1	Inverse.
13-12	FOFST		Line offset value of odd field (FID = 1).
			This field is latched by VD.
		0	+1 line.
		1	+2 line.
		2	+3 line.
		3	+4 line.
11-9	LOFTS0		Line offset values of even line and even field (FID = 0).
			This field is latched by VD.
		0	+1 line.
		1	+2 lines.
		2	+3 lines.
		3	+4 lines.
		4	-1 line.
		5	-2 lines.
		6	-3 lines.
		7	-4 lines.
8-6	LOFTS1		Line offset values of odd line and even field (FID = 0).
			This bit is latched by VD.
		0	+1 line.
		1	+2 lines.
		2	+3 lines.
		3	+4 lines.
		4	-1 line.
		5	-2 lines.
		6	-3 lines.
		7	-4 lines.

Table 59. SDRAM Line Offset Register (SDOFST) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	LOFTS2		Line offset values of even line and odd field (FID = 1).
			This bit is latched by VD.
		0	+1 line.
		1	+2 lines.
		2	+3 lines.
		3	+4 lines.
		4	-1 line.
		5	-2 lines.
		6	-3 lines.
		7	-4 lines.
2-0	LOFTS3		Line offset values of odd line and odd field (FID = 1).
			This bit is latched by VD.
		0	+1 line.
		1	+2 lines.
		2	+3 lines.
		3	+4 lines.
		4	-1 line.
		5	-2 lines.
		6	-3 lines.
		7	-4 lines.

6.1.16 SDRAM Address - High Register (STADRH)

The SDRAM address - high register (STADRH) is shown in Figure 95 and described in Table 60.

Figure 95. SDRAM Address - High Register (STADRH)

15	7	6	0
Reserved		ADRH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 60. SDRAM Address - High Register (STADRH) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved.
6-0	ADRH	0-7Fh	Upper 7 bits of the SDRAM starting address for CCDC output. The address is specified offset from the SDRAM base address in units of 32 bytes.
			This bit field is latched by VD.

6.1.17 SDRAM Address - Low Register (STADRL)

The SDRAM address - low register (STADRL) is shown in Figure 96 and described in Table 61.

Figure 96. SDRAM Address - Low Register (STADRL)

15	0
STADRL	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 61. SDRAM Address - Low Register (STADRL) Field Descriptions

Bit	Field	Value	Description
15-0	STADRL	0-FFFFh	Lower 16 bits of the SDRAM starting address for CCDC output. The address is specified offset from the SDRAM base address in units of 32 bytes. This bit field is latched by VD.

6.1.18 CCD Data Clamping Register (CLAMP)

The CCD data clamping register (CLAMP) is shown in Figure 97 and described in Table 62.

Figure 97. CCD Data Clamping Register (CLAMP)

15	14 13	12 0
CLAMPEN	OBSLEN	OBST
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 62. CCD Data Clamping Register (CLAMP) Field Descriptions

Bit	Field	Value	Description
15	CLAMPEN		Clamp enable. Enables clamping of CCD data based on the calculated average of Optical Black Samples. This should be disabled in YCbCr input modes. This bit is latched by VD.
		0	Disable.
		1	Enable.
14-13	OBSLEN		Optical black sample length. Number of Optical Black Sample pixels per line to include in the average calculation.
		0	2 pixels.
		1	4 pixels.
		2	8 pixels.
		3	16 pixels.
12-0	OBST	0-1FFFh	Start pixel of optical black samples. Start pixel position of Optical Black Samples, specified from the start of HD in pixel clocks.

6.1.19 DC Clamp Register (DCSUB)

The DC clamp register (DCSUB) is shown in Figure 98 and described in Table 63.

Figure 98. DC Clamp Register (DCSUB)

15	14	13	0
OBSLN		DCSUB	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 63. DC Clamp Register (DCSUB) Field Descriptions

Bit	Field	Value	Description
15-14	OBSLN		Optical black sample lines. Number of Optical Black Sample lines to include in the average calculation.
		0	2 lines.
		1	4 lines.
		2	8 lines.
		3	16 lines.
13-0	DCSUB	0-3FFFh	DC level to subtract from CCD data. The DC value set here is subtracted from the CCD data when OBS clamping is disabled, CLAMPEN is 0.

6.1.20 CCD Color Pattern Register (COLPTN)

The CCD color pattern register (COLPTN) is shown in Figure 99 and described in Table 64.

Figure 99. CCD Color Pattern Register (COLPTN)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPF1P0		CPF1P1		CPF1P2		CPF1P3		CPF0P0		CPF0P1		CPF0P2		CPF0P3	
R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 64. CCD Color Pattern Register (COLPTN) Field Descriptions

Bit	Field	Value	Description
15-14	CPF1P0		Color pattern for pixel position 0 (Field 1). Mosaic: Pixel count = 0 at EVEN line. Stripe: Pixel count = 0.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
13-12	CPF1P1		Color pattern for pixel position 1 (Field 1). Mosaic: Pixel count = 1 at EVEN line. Stripe: Pixel count = 1.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.

Table 64. CCD Color Pattern Register (COLPTN) Field Descriptions (continued)

Bit	Field	Value	Description
11-10	CPF1P2		Color pattern for pixel position 2 (Field 1).
			Mosaic: Pixel count = 0 at ODD line.
			Stripe: Pixel count = 2.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
9-8	CPF1P3		Color pattern for pixel position 3 (Field 1).
			Mosaic: Pixel count = 1 at ODD line.
			Stripe: Not applicable.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
7-6	CPF0P0		Color pattern for pixel position 0 (Field 0).
			Mosaic: Pixel count = 0 at EVEN line.
			Stripe: Pixel count = 0.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
5-4	CPF0P1		Color pattern for pixel position 1 (Field 0).
			Mosaic: Pixel count = 1 at EVEN line.
			Stripe: Pixel count = 1.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
3-2	CPF0P2		Color pattern for pixel position 2 (Field 0).
			Mosaic: Pixel count = 0 at ODD line.
			Stripe: Pixel count = 2.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.
1-0	CPF0P3		Color pattern for pixel position 3 (Field 0).
			Mosaic: Pixel count = 1 at ODD line.
			Stripe: Not applicable.
		0	R/Ye.
		1	Gr/Cy.
		2	Gb/G.
		3	B/Mg.

6.1.21 Black Compensation #1 Register (BLKCMP0)

The black compensation #1 register (BLKCMP0) is shown in Figure 100 and described in Table 65.

Figure 100. Black Compensation #1 Register (BLKCMP0)

15	8	7	0
R_YE		GR_CY	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 65. Black Compensation #1 Register (BLKCMP0) Field Descriptions

Bit	Field	Value	Description
15-8	R_YE	0-FFh	Black level compensation for R/Ye pixels (-128:+127) 2's complement, MSB is sign bit. This bit is latched by VD.
7-0	GR_CY	0-FFh	Black level compensation for Gr/Cy pixels (-128:+127) 2's complement, MSB is sign bit. This bit field is latched by VD.

6.1.22 Black Compensation #2 Register (BLKCMP1)

The black compensation #2 register (BLKCMP1) is shown in Figure 101 and described in Table 66.

Figure 101. Black Compensation #2 Register (BLKCMP1)

15	8	7	0
R_YE		GR_CY	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 66. Black Compensation #2 Register (BLKCMP1) Field Descriptions

Bit	Field	Value	Description
15-8	GB_G	0-FFh	Black level compensation for Gb/G pixels (-128:+127) 2's complement, MSB is sign bit. This bit is latched by VD.
7-0	B_MG	0-FFh	Black level compensation for B/Mg pixels (-128:+127) 2's complement, MSB is sign bit. This bit field is latched by VD.

6.1.23 CCD Median Filter Register (MEDFILT)

The CCD median filter register (MEDFILT) is shown in Figure 102 and described in Table 67.

Figure 102. CCD Median Filter Register (MEDFILT)

15	14	13	0
Reserved		MFTHR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 67. CCD Median Filter Register (MEDFILT) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	MFTHR	0-3FFFh	Threshold value for median filter.

6.1.24 CCD Gain Adjustment - R/Ye Register (RYEGAIN)

The CCD gain adjustment - R/Ye register (RYEGAIN) is shown in Figure 103 and described in Table 68.

Figure 103. CCD Gain Adjustment - R/Ye Register (RYEGAIN)

15	11	10	0
Reserved		GAIN	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 68. CCD Gain Adjustment - R/Ye Register (RYEGAIN) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved.
10-0	GAIN	0-7FFh	Gain adjustment factor for CCD data. Value is U11Q8, i.e., decimal point between bits 8 and 7. Range: 0-7.9921875. This bit is latched by VD.

6.1.25 CCD Gain Adjustment - Gr/Cy Register (GRCYGAIN)

The CCD gain adjustment - Gr/Cy register (GRCYGAIN) is shown in Figure 104 and described in Table 69.

Figure 104. CCD Gain Adjustment - Gr/Cy Register (GRCYGAIN)

15	11	10	0
Reserved		GAIN	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 69. CCD Gain Adjustment - Gr/Cy Register (GRCYGAIN) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved.
10-0	GAIN	0-7FFh	Gain adjustment factor for CCD data. Value is U11Q8, i.e., decimal point between bits 8 and 7. Range: 0-7.9921875. This bit is latched by VD.

6.1.26 CCD Gain Adjustment - Gb/G Register (GBGGAIN)

The CCD gain adjustment - Gb/G register (GBGGAIN) is shown in Figure 105 and described in Table 70.

Figure 105. CCD gain adjustment - Gb/G register (GBGGAIN)

15	11	10	0
Reserved		GAIN	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 70. CCD gain adjustment - Gb/G register (GBGGAIN) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved.
10-0	GAIN	0-7FFh	Gain adjustment factor for CCD data. Value is U11Q8, i.e., decimal point between bits 8 and 7. Range: 0-7.9921875. This bit is latched by VD.

6.1.27 CCD Gain Adjustment - B/Mg Register (BMGGAIN)

The CCD gain adjustment - B/Mg register (BMGGAIN) is shown in Figure 106 and described in Table 71.

Figure 106. CCD Gain Adjustment - B/Mg Register (BMGGAIN)

15	11	10	0
Reserved		GAIN	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 71. CCD Gain Adjustment - B/Mg Register (BMGGAIN) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved.
10-0	GAIN	0-7FFh	Gain adjustment factor for CCD data. Value is U11Q8, i.e., decimal point between bits 8 and 7. Range: 0-7.9921875. This bit is latched by VD.

6.1.28 CCD Offset Adjustment Register (OFFSET)

The CCD offset adjustment register (OFFSET) is shown in Figure 107 and described in Table 72.

Figure 107. CCD Offset Adjustment Register (OFFSET)

15	10	9	0
Reserved		OFFSET	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

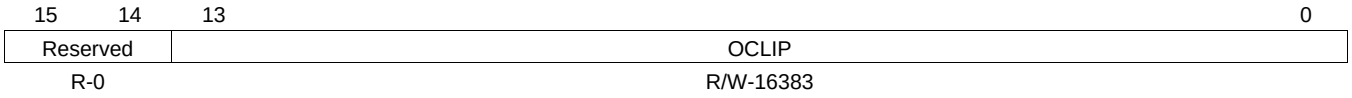
Table 72. CCD Offset Adjustment Register (OFFSET) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	OFFSET	0-3FFh	Offset adjustment after gain adjustment. Value is added to data after gain (0-1023). This bit is latched by VD.

6.1.29 Output Clipping Value Register (OUTCLIP)

The output clipping value register (OUTCLIP) is shown in Figure 108 and described in Table 73.

Figure 108. Output Clipping Value Register (OUTCLIP)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

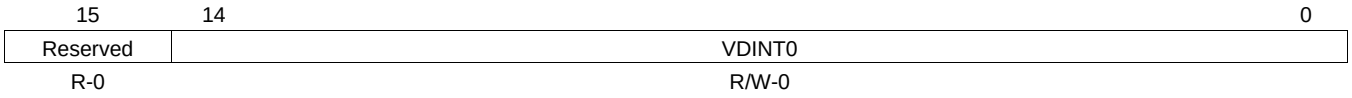
Table 73. Output Clipping Value Register (OUTCLIP) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	OCLIP	0-3FFFh	Output clipping value after gain and offset.

6.1.30 VD Interrupt #0 Register (VDINT0)

The VD interrupt #0 register (VDINT0) is shown in Figure 109 and described in Table 74.

Figure 109. VD Interrupt #0 Register (VDINT0)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

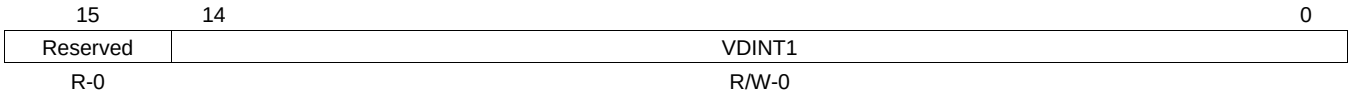
Table 74. VD Interrupt #0 Register (VDINT0) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	VDINT0	0-7FFFh	VD0 Interrupt Timing. Specify VDINT0 in units of horizontal lines from the start of VD pulse.

6.1.31 VD Interrupt #1 Register (VDINT1)

The VD interrupt #1 register (VDINT1) is shown in Figure 110 and described in Table 75.

Figure 110. VD Interrupt #1 Register (VDINT1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 75. VD Interrupt #1 Register (VDINT1) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	VDINT1	0-7FFFh	VD1 Interrupt Timing. Specify VDINT1 in units of horizontal lines from the start of VD pulse.

6.1.32 Gamma Correction Settings Register (GAMMAWD)

The gamma correction settings register (GAMMAWD) is shown in Figure 111 and described in Table 76.

Figure 111. Gamma Correction Settings Register (GAMMAWD)

15 12	11 10	9 8	7 6	5	4 2	1	0
Reserved	MFIL1	MFIL2	Reserved	CFAP	GWDI	Reserved	CCDTBL
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 76. Gamma Correction Settings Register (GAMMAWD) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved
11-10	MFIL1		Median filter mode for IPIPE.
			This bit is latched by VD.
		0	No Median filter.
		1	Average filter.
		2	Median filter.
		3	Reserved.
9-8	MFIL2		Median Filter for SDRAM capture.
			This bit is latched by VD.
		0	No Median filter.
		1	Average filter.
		2	Median filter.
		3	Reserved.
7-6	Reserved	0	Reserved.
5	CFAP		CFA Pattern.
			This bit is latched by VD.
		0	Mosaic.
		1	Stripe.
4-2	GWDI		Gamma Width Input (For A-LAW table & H3A port).
			This bit is latched by VD.
		0	Bits 13-4.
		1	Bits 12-3.
		2	Bits 11-2.
		3	Bits 10-1.
		4	Bits 9-0.
		5-7	Reserved.
1	Reserved	0	Reserved.
0	CCDTBL		Apply Gamma (A-LAW) to CCDC data saved to SDRAM.
			This bit is latched by VD.
		0	Disable.
		1	Enable.

6.1.33 REC656 Control Register (REC656IF)

The REC656 control register (REC656IF) is shown in Figure 112 and described in Table 77.

Figure 112. REC656 Control Register (REC656IF)

15	2	1	0
Reserved		ECCFVH	R656ON
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 77. REC656 Control Register (REC656IF) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved.
1	ECCFVH		FVH error correction enable.
		0	Disable.
		1	Enable.
0	R656ON		REC656 interface enable.
		0	Disable.
		1	Enable.

6.1.34 CCD Configuration Register (CCDCFG)

The CCD configuration register (CCDCFG) is shown in Figure 113 and described in Table 78.

Figure 113. CCD Configuration Register (CCDCFG)

15	14	13	12	11	10	9	8
VDLC	Reserved	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	0
Reserved	FIDMD	BW656	YCINSWP	Reserved	
R-0	R/W-0	R/W-0	R/W-0	R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 78. CCD Configuration Register (CCDCFG) Field Descriptions

Bit	Field	Value	Description
15	VDLC		Enable synchronizing function registers on VSYNC.
		0	Latched on VSYNC.
		1	Not latched on VSYNC.
14	Reserved		Reserved.
13	MSBINVI		MSB of Chroma input signal stored to SDRAM inverted.
		0	Normal.
		1	MSB inverted.
12	BSWD		Byte swap data stored to SDRAM.
		0	Normal.
		1	Swap Bytes.
11	Y8POS		Location of Y signal when YCbCr 8bit data is input.
		0	Even pixel.
		1	Odd pixel.
10	EXTRG		External trigger.
		0	Disable.
		1	Enable.
9	TRGSEL		Signal that initializes SDRAM address when EXTRG = 1.
		0	WEN bit (SYNCEN register).
		1	FID input port.
8	WENLOG		Specifies CCD valid area.
		0	Internal valid and WEN signals are ANDed logically.
		1	Internal valid and WEN signals are ORed logically.
7	Reserved	0	Reserved.
6	FIDMD		Setting of FID detection function.
		0	FID signal is latched at the VSYNC timing.
		1	FID signal is not latched.
5	BW656		The data width in REC656 input mode.
		0	8-bits.
		1	10-bits.
4	YCINSWP		Y input (YIN[7:0]) and C input (CIN[7:0]) are swapped.
		0	(NO_YCIN_SWAP) YIN[7:0] = Y signal / CIN[7:0] = C signal.
		1	(YCIN_SWAP) YIN[7:0] = C signal / CIN[7:0] = Y signal.
3-0	Reserved	0	Reserved.

6.1.35 Start Pixel Horizontal Register (FMTSPH)

The start pixel horizontal register (FMTSPH) is shown in Figure 114 and described in Table 79.

Figure 114. Start Pixel Horizontal Register (FMTSPH)

15 13	12 0
Reserved	FMTSPH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 79. Start Pixel Horizontal Register (FMTSPH) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	FMTSPH	0-1FFFh	Start pixel horizontal.

6.1.36 Number Of Pixels Register (FMTLNH)

The number of pixels register (FMTLNH) is shown in Figure 115 and described in Table 80.

Figure 115. Number Of Pixels Register (FMTLNH)

15 13	12 0
Reserved	FMTLNH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 80. Number Of Pixels Register (FMTLNH) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	FMTLNH	0-1FFFh	Number of pixels in horizontal. Number of pixels = FMTLNH + 1.

6.1.37 Start Line Vertical Register (FMTSLV)

The start line vertical register (FMTSLV) is shown in Figure 116 and described in Table 81.

Figure 116. Start Line Vertical Register (FMTSLV)

15 13	12 0
Reserved	FMTSLV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 81. Start Line Vertical Register (FMTSLV) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	FMTSLV	0-1FFFh	Start line vertical.

6.1.38 Number of Lines Register (FMTLNV)

The number of lines register (FMTLNV) is shown in Figure 117 and described in Table 82.

Figure 117. Number of Lines Register (FMTLNV)

15	14 0
Reserved	FMTLNV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 82. Number of Lines Register (FMTLNV) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	FMTLNV	0-7FFFh	Number of lines in vertical. Number of lines = FMTLNV + 1.

6.1.39 Lens Shading Correction Configuration 1 Register (LSCCFG1)

The lens shading correction configuration 1 register (LSCCFG1) is shown in Figure 118 and described in Table 83.

Figure 118. Lens Shading Correction Configuration 1 Register (LSCCFG1)

15	6	5	4	3	1	0
Reserved		GFMODE		Reserved		LSCEN
R-0		R/W-0		R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 83. Lens Shading Correction Configuration 1 Register (LSCCFG1) Field Descriptions

Bit	Field	Value	Description
15-6	Reserved	0	Reserved.
11	GFMODE		Gain Factor Mode.
		0	U8Q8 + 1 with Interpolation.
		1	U16Q14 with Interpolation.
		2	Reserved.
		3	U16Q14 without Interpolation.
			Gain factor range is:
			U8Q8 + 1: 1 <= Gain Factor <= 1 + 255/256
			U16Q14: 0 <= Gain Factor <= 3 + 16383/16384
		0	(U8Q8_interpolation) U8Q8 with interpolation.
		1	(U16Q14_interpolation) U16Q14 with interpolation.
		2	Reserved.
		3	(U16Q14) U16Q14 without interpolation.
3-1	Reserved	0	Reserved.
0	LSCEN		Lens shading correction enable.
			This bit field is latched by VD.
		0	Disable.
		1	Enable.

6.1.40 Lens Shading Correction Configuration 2 Register (LSCCFG2)

The lens shading correction configuration 2 register (LSCCFG2) is shown in Figure 119 and described in Table 84.

Figure 119. Lens Shading Correction Configuration 2 Register (LSCCFG2)

15 14	13 12	11 10	9 8
GFTSEL_OPOL	GFTSEL_EPOL	GFTSEL_OPEL	GFTSEL_EPEL
R/W-0	R/W-0	R/W-0	R/W-0

7 4	3 1	0
GFTINV	GFTSF	Reserved
R/W-0	R/W-7	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 84. Lens Shading Correction Configuration 2 Register (LSCCFG2) Field Descriptions

Bit	Field	Value	Description
15-14	GFTSEL_OPOL		Gain factor table selection for odd pixel, odd line.
		0	Table 1.
		1	Table 2.
		2	Table 3.
13-12	GFTSEL_EPOL	0-3	Gain factor table selection for even pixel, odd line.
11-10	GFTSEL_OPEL	0-3	Gain factor table selection for odd pixel, even line.
9-8	GFTSEL_EPEL	0-3	Gain factor table selection for even pixel, even line.
7-4	GFTINV	0-Fh	Gain factor table interval (n).
3-1	GFTSF	0-7	Gain factor table scaling factor (m). LUT address = (m + 9)/16 × 2^-n × SQRDST (SQRDST = kh × (H - H0)^2 + kv × (V- V0)^2)
0	Reserved	0	Reserved.

6.1.41 Lens Shading Correction - Center Position (H0) Register (LSCH0)

The lens shading correction - center position (H0) register (LSCH0) is shown in Figure 120 and described in Table 85.

Figure 120. Lens Shading Correction - Center Position (H0) Register (LSCH0)

15	14	13	0
LSCCSW		LSCH0	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 85. Lens Shading Correction - Center Position (H0) Register (LSCH0) Field Descriptions

Bit	Field	Value	Description
15-14	LSCCSW		Color channel switch for shading factors (H 0 , V 0 , k h , k v) configuration. By switching LSCCSW, you can configure H0, V0, kh, kv for each color channel. Values set to LSCH0, LSCV0, LSCKHL, LSCKHR, LSCKVU, and LSCKVL while LSCCSW is "00", are valid for the color channel which uses Gain Factor Table 1.
		0	Table 1.
		1	Table 2.
		2	Table 3.
13-0	LSCH0	0-3FFFh	Lens center position (H0: H direction). Range: 0-16383

6.1.42 Lens Shading Correction - Center Position (V0) Register (LSCV0)

The lens shading correction - center position (V0) register (LSCV0) is shown in Figure 121 and described in Table 86.

Figure 121. Lens Shading Correction - Center Position (V0) Register (LSCV0)

15	14	13	0
Reserved		LSCV0	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 86. Lens Shading Correction - Center Position (V0) Register (LSCV0) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	LSCV0	0-3FFFh	Lens center position (V0: V direction). Range: 0-16383

6.1.43 Lens Shading Correction - Horizontal Coefficients Register (LSCKH)

The lens shading correction - horizontal coefficients register (LSCKH) is shown in Figure 122 and described in Table 87.

Figure 122. Lens Shading Correction - Horizontal Coefficients Register (LSCKH)

15	8	7	0
KHR		KHL	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 87. Lens Shading Correction - Horizontal Coefficients Register (LSCKH) Field Descriptions

Bit	Field	Value	Description
15-8	KHR	0-FFh	Horizontal-right coefficient (Khr). Khr is selected when (H > H0). Khr is U8Q7.
7-0	KHL	0-FFh	Horizontal-left coefficient (Khl). Khl is selected when (H < H0). Khl is U8Q7.

6.1.44 Lens Shading Correction - Vertical Coefficients Register (LSCKV)

The lens shading correction - vertical coefficients register (LSCKV) is shown in Figure 123 and described in Table 88.

Figure 123. Lens Shading Correction - Vertical Coefficients Register (LSCKV)

15	8	7	0
KVL		KVU	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 88. Lens Shading Correction - Vertical Coefficients Register (LSCKV) Field Descriptions

Bit	Field	Value	Description
15-8	KVL	0-FFh	Vertical-lower coefficient (Kvl). Kvl is selected when (V > V0). Kvl is U8Q7.
7-0	KVU	0-FFh	Vertical-upper coefficient (Kvu). Kvu is selected when (V < V0). Kvu is U8Q7.

6.1.45 Lens Shading Correction - Memory Control Register (LSCMEMCTL)

The lens shading correction - memory control register (LSCMEMCTL) is shown in Figure 124 and described in Table 89.

Figure 124. Lens Shading Correction - Memory Control Register (LSCMEMCTL)

15 5	4	3	2	1 0
Reserved	LSCMBSY	LSCMRD	LSCMARST	LSCMSL
R-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

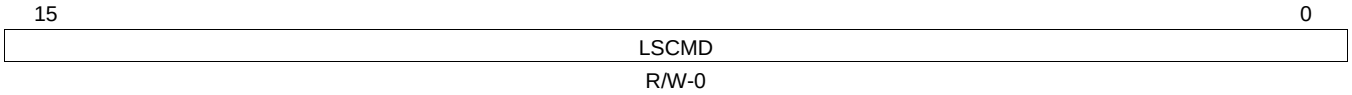
Table 89. Lens Shading Correction - Memory Control Register (LSCMEMCTL) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved.
4	LSCMBSY		Memory access busy flag. Set during memory configuration, when table updates are not allowed.
		0	Not busy.
		1	Busy.
3	LSCMRD		Memory read (for debug). Set LSCMRD and write any data to LSCMD. After LSCMBSY becomes 0, You'll be able to read memory data from LSCMQ. If LSCMARST is set, data of the address offset 0 can be read.
		0	Memory write.
		1	Memory read.
2	LSCMARST		Memory address reset. Write the gain factors for LUT address 0 and 1 to LSCMD with LSCMARST set. LSCMARST is automatically cleared if any of the data is written to LSCMD. Writing gain factors with LSCMARST cleared stores the data to the next half-word address.
		0	Increment the gain table address.
		1	Clear the gain table address to offset 0.
1-0	LSCMSL		Memory selection.
		0	Table 1.
		1	Table 2.
		2	Table 3.
		3	Reserved.

6.1.46 Lens Shading Correction - Memory Write Data Register (LSCMEMD)

The lens shading correction memory Write data register (LSCMEMD) is shown in Figure 125 and described in Table 90.

Figure 125. Lens Shading Correction - Memory Write Data Register (LSCMEMD)



LEGEND: R/W = Read/Write; -*n* = value after reset

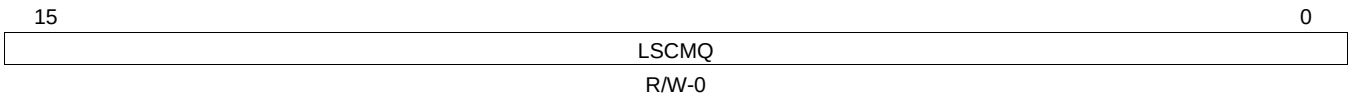
Table 90. Lens Shading Correction - Memory Write Data Register (LSCMEMD) Field Descriptions

Bit	Field	Value	Description
15-0	LSCMD	0-FFFFh	Memory write data. In case Gain Factor is U8Q8+1 (LSCGFMD = 00), a series of 2 Gain Factors can be stored at a table at once by writing 16bit data to LSCMD. U8Q8 + 1: Gain Factor(2N+1) & Gain Factor(2N) U16Q14: Gain Factor(N)

6.1.47 Lens Shading Correction - Memory Read Data Register (LSCMEMQ)

The lens shading correction - memory read data register (LSCMEMQ) is shown in Figure 126 and described in Table 91.

Figure 126. Lens Shading Correction - Memory Read Data Register (LSCMEMQ)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 91. Lens Shading Correction - Memory Read Data Register (LSCMEMQ) Field Descriptions

Bit	Field	Value	Description
15-0	LSCMQ	0-FFFFh	Memory read data (for debug purpose). Memory data can be read out from LSCMQ.

6.1.48 Defect Correction - Control Register (DFCCTL)

The defect correction - control register (DFCCTL) is shown in Figure 127 and described in Table 92.

Figure 127. Defect Correction - Control Register (DFCCTL)

15 11	10 8	7	6 5	4	3 1	0
Reserved	VDFLSFT	VDFCUDA	VDFCSL	VDFCEN	Reserved	GDFCEN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

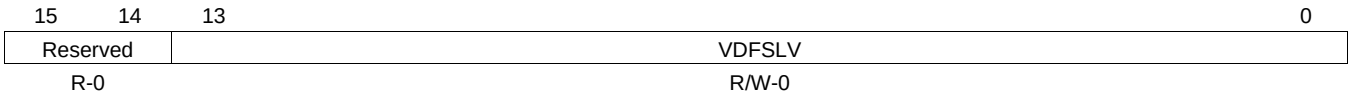
Table 92. Defect Correction - Control Register (DFCCTL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved.
10-8	VDFLSFT	0-7h	Vertical line defect level shift value. Defect Level (value to be subtracted from the data) is 8bit width, but can be up-shifted up to 6bits by VDFLSFT. Left shift value = VDFLSFT (Range: 0-6) Setting 7 to VDFLSFT is not allowed.
7	VDFCUDA		Vertical line defect correction upper pixels disable.
		0	The whole line is corrected.
		1	Pixels upper than the defect are not corrected.
6-5	VDFCSL		Vertical line defect correction mode select.
		0	(NORMAL) Defect level subtraction. Just fed through if data are saturating.
		1	(HORZINTERPOLIFSAT) Defect level subtraction. Horizontal interpolation ((I - 2) + (I + 2))/2 if data are saturating.
		2	(HORZINTERPOL) Horizontal interpolation ((I - 2) + (I + 2))/2.
		3	Reserved.
4	VDFCEN		Vertical line defect correction enable. This bit field is latched by VD.
		0	Off.
		1	On.
3-1	Reserved	0	Reserved.
0	GDFCEN		General defect correction enable. This bit field is latched by VD.
		0	Off.
		1	On.

6.1.49 Defect Correction - Vertical Saturation Level Register (DFCVSAT)

The defect correction - vertical saturation level register (DFCVSAT) is shown in Figure 128 and described in Table 93.

Figure 128. Defect Correction - Vertical Saturation Level Register (DFCVSAT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 93. Defect Correction - Vertical Saturation Level Register (DFCVSAT) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VDFSLV	0-3FFFh	Vertical line defect correction saturation level. VDFSLV is U14 (Range: 0-16383).

6.1.50 Defect Correction - Memory Control Register (DFCMEMCTL)

The defect correction - memory control register (DFCMEMCTL) is shown in Figure 129 and described in Table 94.

Figure 129. Defect Correction - Memory Control Register (DFCMEMCTL)

15	5	4	3	2	1	0
Reserved		DFCMCLR	Reserved	DFCMARST	DFCMRD	DFCMWR
R-0		R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 94. Defect Correction - Memory Control Register (DFCMEMCTL) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved.
4	DFCMCLR		Memory clear. Writing 1 to this bit clears the memory contents to all zero. It will be automatically cleared to 0 when the memory clear is completed.
		0	Memory clear complete.
		1	Clear memory.
3	Reserved	0	Reserved.
2	DFCMARST		Memory address reset.
			Setting DFCMWR or DFCMRD with LSCMARST set starts memory access to address offset 0. DFCMARST is automatically cleared if data transfer completes. Setting DFCMWR or DFCMRD with LSCMARST cleared starts memory access to the next address.
		0	Increment the memory address.
		1	Clear the memory address to offset 0.
1	DFCMRD		Memory read (for debug).
			Writing 1 to this bit starts reading from the memory. It will be automatically cleared when the data transfer is completed, and the data can be read from DFCMEM4_0.
		0	Memory read complete.
		1	Memory read.
0	DFCMWR		Memory write.
			Writing 1 to this bit starts writing to the memory. It will be automatically cleared when the data transfer is completed. DFCMEM4_0 should be set prior to the memory access.
		0	Memory write complete.
		1	Memory write.

6.1.51 Defect Correction - Set V Position Register (DFCMEM0)

The defect correction - set V position register (DFCMEM0) is shown in Figure 130 and described in Table 95.

Figure 130. Defect Correction - Set V Position Register (DFCMEM0)

15	12	11	0
Reserved		DFCMEM0	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 95. Defect Correction - Set V Position Register (DFCMEM0) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	DFCMEM0	0-1	Memory 0. Set V position of the defects.

6.1.52 Defect Correction - Set H Position Register (DFCMEM1)

The defect correction - set H position register (DFCMEM1) is shown in Figure 131 and described in Table 96.

Figure 131. Defect Correction - Set H Position Register (DFCMEM1)

15	12	11	0
Reserved		DFCMEM1	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 96. Defect Correction - Set H Position Register (DFCMEM1) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	DFCMEM1	0-1	Memory 1. Set H position of the defects.

6.1.53 Defect Correction - Set SUB1 Register (DFCMEM2)

The defect correction - set SUB1 register (DFCMEM2) is shown in Figure 132 and described in Table 97.

Figure 132. Defect Correction - Set SUB1 Register (DFCMEM2)

15	8	7	0
Reserved		DFCMEM2	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 97. Defect Correction - Set SUB1 Register (DFCMEM2) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	DFCMEM2	0-FFh	Memory 2. Set SUB1: Defect level of the Vertical line defect position (V = Vdefect). DFCMEM2 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.54 Defect Correction - Set SUB2 Register (DFCMEM3)

The defect correction - set SUB2 register (DFCMEM3) is shown in Figure 133 and described in Table 98.

Figure 133. Defect Correction - Set SUB2 Register (DFCMEM3)

15	8	7	0
Reserved		DFCMEM3	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 98. Defect Correction - Set SUB2 Register (DFCMEM3) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	DFCMEM3	0-FFh	Memory 3. Set SUB2: Defect level of the pixels upper than the Vertical line defect (V < Vdefect). DFCMEM3 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.55 Defect Correction - Set SUB3 Register (DFCMEM4)

The defect correction - set SUB3 register (DFCMEM4) is shown in Figure 134 and described in Table 99.

Figure 134. Defect Correction - Set SUB3 Register (DFCMEM4)

15	8	7	0
Reserved		DFCMEM4	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 99. Defect Correction - Set SUB3 Register (DFCMEM4) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	DFCMEM4	0-FFh	Memory 4 Set SUB3: Defect level of the pixels lower than the Vertical line defect (V > Vdefect). DFCMEM4 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.56 Color Space Converter Enable Register (CSCCTL)

The color space converter enable register (CSCCTL) is shown in Figure 135 and described in Table 100.

Figure 135. Color Space Converter Enable Register (CSCCTL)

15	0
CSCEN	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 100. Color Space Converter Enable Register (CSCCTL) Field Descriptions

Bit	Field	Value	Description
15-0	CSCEN		CSC enable.
		0	(DISABLE) disable.
		1	(ENABLE) enable.

6.1.57 Color Space Converter - Coefficients #0 Register (CSCM0)

The color space converter - coefficients #0 register (CSCM0) is shown in Figure 136 and described in Table 101.

Figure 136. Color Space Converter - Coefficients #0 Register (CSCM0)

15	8	7	0
CSCM01		CSCM00	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 101. Color Space Converter - Coefficients #0 Register (CSCM0) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM01	0-FFh	Color space conversion coefficient value M01. This value is S8Q5.
7-0	CSCM00	0-FFh	Color space conversion coefficient value M00. This value is S8Q5.

6.1.58 Color Space Converter - Coefficients #1 Register (CSCM1)

The color space converter - coefficients #1 register (CSCM1) is shown in Figure 137 and described in Table 102.

Figure 137. Color Space Converter - Coefficients #1 Register (CSCM1)

15	8	7	0
CSCM03		CSCM02	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 102. Color Space Converter - Coefficients #1 Register (CSCM1P) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM03	0-FFh	Color space conversion coefficient value M03. This value is S8Q5.
7-0	CSCM02	0-FFh	Color space conversion coefficient value M02. This value is S8Q5.

6.1.59 Color Space Converter - Coefficients #2 Register (CSCM2)

The color space converter - coefficients #2 register (CSCM2) is shown in Figure 138 and described in Table 103.

Figure 138. Color Space Converter - Coefficients #2 Register (CSCM2)

15	8	7	0
CSCM11		CSCM10	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 103. Color Space Converter - Coefficients #2 Register (CSCM2) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM11	0-FFh	Color space conversion coefficient value M11. This value is S8Q5.
7-0	CSCM10	0-FFh	Color space conversion coefficient value M10. This value is S8Q5.

6.1.60 Color Space Converter - Coefficients #3 Register (CSCM3)

The color space converter - coefficients #3 register (CSCM3) is shown in Figure 139 and described in Table 104.

Figure 139. Color Space Converter - Coefficients #3 Register (CSCM3)

15	8	7	0
CSCM13		CSCM12	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 104. Color Space Converter - Coefficients #3 Register (CSCM3) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM13	0-FFh	Color space conversion coefficient value M13. This value is S8Q5.
7-0	CSCM12	0-FFh	Color space conversion coefficient value M12. This value is S8Q5.

6.1.61 Color Space Converter - Coefficients #4 Register (CSCM4)

The color space converter - coefficients #4 register (CSCM4) is shown in Figure 140 and described in Table 105.

Figure 140. Color Space Converter - Coefficients #4 Register (CSCM4)

15	8	7	0
CSCM21		CSCM20	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 105. Color Space Converter - Coefficients #4 Register (CSCM4) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM21	0-FFh	Color space conversion coefficient value M21. This value is S8Q5.
7-0	CSCM20	0-FFh	Color space conversion coefficient value M20. This value is S8Q5.

6.1.62 Color Space Converter - Coefficients #5 Register (CSCM5)

The color space converter - coefficients #5 register (CSCM5) is shown in Figure 141 and described in Table 106.

Figure 141. Color Space Converter - Coefficients #5 Register (CSCM5)

15	8	7	0
CSCM23		CSCM22	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 106. Color Space Converter - Coefficients #5 Register (CSCM5) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM23	0-FFh	Color space conversion coefficient value M23. This value is S8Q5.
7-0	CSCM22	0-FFh	Color space conversion coefficient value M22. This value is S8Q5.

6.1.63 Color Space Converter - Coefficients #6 Register (CSCM6)

The color space converter - coefficients #6 register (CSCM6) is shown in Figure 142 and described in Table 107.

Figure 142. Color Space Converter - Coefficients #6 Register (CSCM6)

15	8	7	0
CSCM31		CSCM30	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 107. Color Space Converter - Coefficients #6 Register (CSCM6) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM31	0-FFh	Color space conversion coefficient value M31. This value is S8Q5.
7-0	CSCM30	0-FFh	Color space conversion coefficient value M30. This value is S8Q5.

6.1.64 Color Space Converter - Coefficients #7 Register (CSCM7)

The color space converter coefficients #7 register (CSCM7) is shown in Figure 143 and described in Table 108.

Figure 143. Color Space Converter - Coefficients #7 Register (CSCM7)

15	8	7	0
CSCM33		CSCM32	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 108. Color Space Converter - Coefficients #7 Register (CSCM7) Field Descriptions

Bit	Field	Value	Description
15-8	CSCM33	0-FFh	Color space conversion coefficient value M33. This value is S8Q5.
7-0	CSCM32	0-FFh	Color space conversion coefficient value M32. This value is S8Q5.

6.1.65 Data Offset Register (DATAOFST)

The data offset register (DATAOFST) is shown in Figure 144 and described in Table 109.

Figure 144. Data Offset Register (DATAOFST)

15	8	7	0
VOFST		HOFST	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 109. Data Offset Register (DATAOFST) Field Descriptions

Bit	Field	Value	Description
15-8	VOFST	0-FFh	V direction data offset for defect correction and lens shading correction. Range: 0-255.
7-0	HOFST	0-FFh	H direction data offset for defect correction and lens shading Correction. Range: 0-255.

6.2 Image Pipe Input Interface Registers (IPIPEIF)

The Image Pipe Input Interface registers are shown in Table 110.

Table 110. Image Pipe Input Interface Register Map (IPIPEIF)

Address	Acronym	Register Description	Section
0x01C7:0100	ENABLE	IPIPE I/F Enable	Section 6.2.1
0x01C7:0104	CFG	IPIPE I/F Configuration	Section 6.2.2
0x01C7:0108	PPLN	IPIPE I/F Interval of HD / Start pixel in HD	Section 6.2.3
0x01C7:010C	LPFR	IPIPE I/F Interval of VD / Start line in VD	Section 6.2.4
0x01C7:0110	HNUM	IPIPE I/F Number of valid pixels per line	Section 6.2.5
0x01C7:0114	VNUM	IPIPE I/F Number of valid lines per frame	Section 6.2.6
0x01C7:0118	ADDRU	IPIPE I/F Memory Address (Upper)	Section 6.2.7
0x01C7:011C	ADDRL	IPIPE I/F Memory Address (Lower)	Section 6.2.8
0x01C7:0120	ADOFS	IPIPE I/F Address offset of each line	Section 6.2.9
0x01C7:0124	RSZ	IPIPE I/F Horizontal Resizing Parameter	Section 6.2.10
0x01C7:0128	GAIN	IPIPE I/F Gain Parameter	Section 6.2.11

6.2.1 IPIPE I/F Enable Register (ENABLE)

The IPIPE I/F enable (ENABLE) register is shown in Figure 145 and described in Table 111.

Figure 145. IPIPE I/F Enable Register (ENABLE)

15	1	0
Reserved		ENABLE
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 111. IPIPE I/F Enable Register (ENABLE) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	ENABLE		IPIPE I/F Enable This register used to start the operation of SDRAM buffer memory read and generates SYNC signals. This register is available when INPSRC (CFG[3:2]) = 1, 2 or 3.
		0	Disable
		1	Enable

6.2.2 IPIPE I/F Configuration Register (CFG)

The IPIPE I/F configuration register (CFG) is shown in Figure 146 and described in Table 112.

Figure 146. IPIPE I/F Configuration Register (CFG)

15	14	13	11	10	9	8
Reserved		DATASFT		CLKSEL	IALAW	PACK8IN
R-0		R/W-2		R/W-0	R/W-0	R/W-0

7	6	4	3	2	1	0
AVGFILT	CLKDIV		INPSRC		DECM	ONESHOT
R/W-0	R/W-0		R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 112. IPIPE I/F Configuration Register (CFG) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved. Read as zero.
13-11	DATASFT		SDRAM Read Data Shift (0_6)
			This register is available when INPSRC = 1 or 2.
		0	Output data (13:0) = read data(15:2)
		1	Output data (13:0) = read data(14:1)
		2	Output data (13:0) = read data(13:0)
		3	Output data (13:0) = read data(12:0) & "0"
		4	Output data (13:0) = read data(11:0) & "00"
		5	Output data (13:0) = read data(10:0) & "000"
		6	Output data (13:0) = read data(9:0) & "0000"
10	CLKSEL		IPIPEIF & IPIPE Clock Select
			This register is available when INPSRC = 1 or 3. Should code "0" when INPSRC = 0 or 2.
		0	Pixel clock (PCLK)
		1	Divided SDRAM clock as per CLKDIV
9	IALAW		Inverse A-law Conversion
			Applies inverse A-law (8bit to 10bit) conversion to the SDRAM data.
			This register is available when INPSRC = 1 or 2.
		0	Inverse alaw off
		1	Inverse alaw on
8	PACK8IN		8-Bit Packed Mode
			When CCD raw data is stored in 8-bit packed mode, this register should code "1". This register is effective when INPSRC = 1 or 2.
		0	(NORMAL_16_BITS_PIXEL) 16 bits / pixel
		1	(PACK_8_BITS_PIXEL) 8 bits / pixel
7	AVGFILT		Averaging Filter
			It applies (1,2,1) filter for the RGB/YCbCr data.
		0	Off
		1	On

Table 112. IPIPE I/F Configuration Register (CFG) Field Descriptions (continued)

Bit	Field	Value	Description
6-4	CLKDIV		Clock Selection when Offline Mode (SDRAM Input Mode)
			IPIPEIF/IPIPE clock frequency = CLKDIV x VPSSCLK clock frequency
			This register is available when CLKSEL = 1
		0	1/2
		1	1/3
		2	1/4
		3	1/5
		4	1/6
		5	1/8
		6	1/16
		7	1/32
3-2	INPSRC		CCD/YCbCr Data Port Selection
		0	From CCD Controller
		1	From SDRAM (raw data)
		2	From CCD Controller & SDRAM (Darkframe)
		3	From SDRAM (YCbCr data)
1	DECM		Pixel Decimation
			Decimation rate defined by RSZ register
		0	No decimation
		1	Decimate
0	ONESHOT		One Shot Mode
			This register is available when INPSRC = 1 or 3.
		0	Continuous mode
		1	One shot mode

6.2.3 IPIPE I/F Interval of HD / Start pixel in HD Register (PPLN)

The PIPE I/F interval of HD /start pixel in HD register (PPLN) is shown in Figure 147 and described in Table 113.

Figure 147. PIPE I/F Interval of HD / Start pixel in HD Register (PPLN)

15 13	12 0
Reserved	PPLN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 113. PIPE I/F Interval of HD / Start pixel in HD Register (PPLN) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved. Read as zero.
12-0	PPLN	0-1FFFh	Case-1: Interval of Horizontal Sync (HD) Specifies the interval of horizontal sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Horizontal Sync (HD) Specifies the start pixel in horizontal sync. This register is available when INPSRC = 2

6.2.4 IPIPE I/F Interval of VD / Start line in VD Register (LPFR)

The IPIPE I/F interval of VD / start line in VD register (LPFR) is shown in Figure 148 and described in Table 114.

Figure 148. IPIPE I/F Interval of VD / Start line in VD Register (LPFR)

15 13	12 0
Reserved	LPFR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 114. IPIPE I/F Interval of VD / Start line in VD Register (LPFR) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved. Read as zero.
12-0	LPFR	0-1FFFh	Case-1: Interval of Vertical Sync (VD) Specifies the interval of vertical sync. This register is available when INPSRC = 1 or 3. Case-2: Start Pixel in Vertical Sync (VD) Specifies the start line in vertical sync. This register is available when INPSRC = 2

6.2.5 IPIPE I/F Number of valid pixels per line Register (HNUM)

The IPIPE I/F number of valid pixels per line register (HNUM) is shown in Figure 149 and described in Table 115.

Figure 149. IPIPE I/F Number of valid pixels per line Register (HNUM)

15 13	12 0
Reserved	HNUM
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 115. IPIPE I/F Number of valid pixels per line Register (HNUM) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	HNUM	0-1FFFh	The Number of Valid Pixel in a Line Specifies the number of valid pixel in a horizontal line. This register is available when INPSRC = 1, 2 or 3

6.2.6 IPIPE I/F Number of Valid Lines per Frame Register (VNUM)

The IPIPE I/F number of valid lines per frame (VNUM) is shown in Figure 150 and described in Table 116.

Figure 150. IPIPE I/F Number of Valid Lines per Frame Register (VNUM)

15 13	12 0
Reserved	VNUM
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 116. IPIPE I/F Number of Valid Lines per Frame Register (VNUM) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VNUM	0-1FFFh	The Number of Valid Lines in a Vertical Specifies the number of valid lines in a vertical. This register is available when INPSRC = 1, 2 or 3

6.2.7 IPIPE I/F Memory Address (Upper) Register (ADDRU)

The IPIPE I/F memory address (Upper) register (ADDRU) is shown in Figure 151 and described in Table 117.

Figure 151. IPIPE I/F Memory Address (Upper) Register (ADDRU)

15	7	6	0
Reserved		ADDRU	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 117. IPIPE I/F Memory Address (Upper) Register (ADDRU) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved.
6-0	ADDRU	0-7Fh	Memory Address - Upper This register is available when INPSRC = 1, 2 or 3.

6.2.8 IPIPE I/F Memory Address (Lower) Register (ADDRL)

The IPIPE I/F memory address (Lower) register (ADDRL) is shown in Figure 152 and described in Table 118.

Figure 152. IPIPE I/F Memory Address (Lower) Register (ADDRL)

15	0
ADDRL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 118. IPIPE I/F Memory Address (Lower) Register (ADDRL) Field Descriptions

Bit	Field	Value	Description
15-0	ADDRL	0-FFFFh	Memory Address - Lower Memory address lower 16-bits are specified in units of 32-bytes. This register is available when INPSRC = 1, 2 or 3.

6.2.9 IPIPE I/F Address Offset of Each Line Register (ADOFS)

The PIPE I/F address offset of each line (ADOFS) is shown in Figure 153 and described in Table 119.

Figure 153. IPIPE I/F Address Offset of Each Line Register (ADOFS)

15	9	8	0
Reserved		ADOFS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 119. IPIPE I/F Address Offset of Each Line Register (ADOFS) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved.
8-0	ADOFS	0-1FFh	The Address Offset of Each Line Specifies the offset address each start line is specified in units of 32-bytes. This register is available when INPSRC = 1, 2 or 3.

6.2.10 IPIPE I/F Horizontal Resizing Parameter Register (RSZ)

The IPIPE I/F Horizontal Resizing Parameter Register (RSZ) is shown in Figure 154 and described in Table 120.

Figure 154. IPIPE I/F Horizontal Resizing Parameter Register (RSZ)

15	7	6	0
Reserved		RSZ	
R-0		R/W-16	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 120. IPIPE I/F Horizontal Resizing Parameter Register (RSZ) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved. Read as zero.
6-0	RSZ	10h-70h	The Horizontal Resizing Parameter Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7).

6.2.11 IPIPE I/F Gain Parameter Register (GAIN)

The IPIPE I/F gain parameter register (GAIN) is shown in Figure 155 and described in Table 121.

Figure 155. IPIPE I/F Gain Parameter Register (GAIN)

15	10	9	0
Reserved		GAIN	
R-0		R/W-512	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 121. IPIPE I/F Gain Parameter Register (GAIN) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved. Read as zero.
9-0	GAIN	0-3FFh	Gain Parameter Specifies the gain parameter for IPIPE output data. The GAIN register can be configured within 0.00195(1/512) to 1.99805(1023/512) range. This gain default value is x1 gain. These bits don't influence Data of YCC.

6.3 Image Pipe Registers (IPIPE)

The Image Pipe registers are shown in Table 122.

Table 122. Image Pipe Registers (IPIPE)

Address	Acronym	Register Description	Section
Global Registers			
0x01C7:1000	IPIPE_EN	IPIPE Enable Register	Section 6.3.1
0x01C7:1004	IPIPE_MODE	One Shot Mode Register	Section 6.3.2
0x01C7:1008	IPIPE_DPATHS	Input/Output Data Paths Register	Section 6.3.3
0x01C7:100C	IPIPE_COLPAT	Color Pattern Register	Section 6.3.4
0x01C7:1010	IPIPE_VST	Vertical Start Position Register	Section 6.3.5
0x01C7:1014	IPIPE_VSZ	Vertical Processing Size Register	Section 6.3.6
0x01C7:1018	IPIPE_HST	Horizontal Start Position Register	Section 6.3.7
0x01C7:101C	IPIPE_HSZ	Horizontal Processing Size Register	Section 6.3.8
Gated Clock Enables			
0x01C7:1024	GCL_ARM	ARM Gated Clock Control Register	Section 6.3.9
0x01C7:1028	GCL_CCD	CCD Gated Clock Control Register	Section 6.3.10
0x01C7:102C	GCL_SDR	SDR Gated Clock Control Register	Section 6.3.11
Internal Memory Access			
0x01C7:1030	RAM_MODE	Internal Table Selection Register	Section 6.3.12
0x01C7:1034	RAM_ADR	Address Register	Section 6.3.13
0x01C7:1038	RAM_WDT	Write Data Register	Section 6.3.14
0x01C7:103C	RAM_RDT	Read Data Register	Section 6.3.15
Interrupts			
0x01C7:1040	IRQ_EN	Interrupt Enable Register	Section 6.3.16
0x01C7:1044	IRQ_RZA	Interval of IRQ-2 Register	Section 6.3.17
0x01C7:1048	IRQ_RZB	Interval of IRQ-3 Register	Section 6.3.18
Defect Correction			
0x01C7:104C	DFC_EN	Defect Correction Enable Register	Section 6.3.19
0x01C7:1050	DFC_SEL	Copy Method Selection (from Top or from Bottom) Register	Section 6.3.20
0x01C7:1054	DFC_ADR	Start Address in LUT Register	Section 6.3.21
0x01C7:1058	DFC_SIZ	Number of Available Entries in LUT Register	Section 6.3.22
Programmable Noise Filter			
0x01C7:105C	D2F_EN	2D Noise Filter Enable Register	Section 6.3.23
0x01C7:1060	D2F_CFG	Noise Filter Configuration Register	Section 6.3.24
0x01C7:1064	D2F_THR[32]	Noise Filter LUT Values (Threshold) Register	Section 6.3.25
0x01C7:10E4	D2F_STR[32]	Noise Filter LUT Values (Intensity) Register	Section 6.3.26
Pre-filter			
0x01C7:1164	PRE_EN	PreFilter Enable Register	Section 6.3.27
0x01C7:1168	PRE_TYP	PreFilter Type Register	Section 6.3.28
0x01C7:116C	PRE_SHF	Shift Value of Adaptive Gain Register	Section 6.3.29
0x01C7:1170	PRE_GAIN	Constant Gain or Adaptive Gain Slope Register	Section 6.3.30
0x01C7:1174	PRE_THR_G	Threshold G Register	Section 6.3.31
0x01C7:1178	PRE_THR_B	Threshold B Register	Section 6.3.32
0x01C7:117C	PRE_THR_1	Threshold 1 Register	Section 6.3.33
White Balance			
0x01C7:1180	WB2_DGN	Digital Gain Register	Section 6.3.34
0x01C7:1184	WB2_WG_R	White Balance Gain (Red) Register	Section 6.3.35
0x01C7:1188	WB2_WG_GR	White Balance Gain (GR) Register	Section 6.3.36

Table 122. Image Pipe Registers (IPIPE) (continued)

Address	Acronym	Register Description	Section
0x01C7:118C	WB2_WG_GB	White Balance Gain (GB) Register	Section 6.3.37
0x01C7:1190	WB2_WG_B	White Balance Gain (Blue) Register	Section 6.3.38
RGB to RGB Conversion (Include GAMMA Correction)			
0x01C7:11F4	RGB_MUL_RR	Matrix Coefficient RR Register	Section 6.3.39
0x01C7:11F8	RGB_MUL_GR	Matrix Coefficient GR Register	Section 6.3.40
0x01C7:11FC	RGB_MUL_BR	Matrix Coefficient BR Register	Section 6.3.41
0x01C7:1200	RGB_MUL_RG	Matrix Coefficient RG Register	Section 6.3.42
0x01C7:1204	RGB_MUL_GG	Matrix Coefficient GG Register	Section 6.3.43
0x01C7:1208	RGB_MUL_BG	Matrix Coefficient BG Register	Section 6.3.44
0x01C7:120C	RGB_MUL_RB	Matrix Coefficient RB Register	Section 6.3.45
0x01C7:1210	RGB_MUL_GB	Matrix Coefficient GB Register	Section 6.3.46
0x01C7:1214	RGB_MUL_BB	Matrix Coefficient BB Register	Section 6.3.47
0x01C7:1218	RGB_OFT_OR	R Output Offset Register	Section 6.3.48
0x01C7:121C	RGB_OFT_OG	G Output Offset Register	Section 6.3.49
0x01C7:1220	RGB_OFT_OB	B Output Offset Register	Section 6.3.50
0x01C7:1224	GMM_CFG	Gamma Correction Configuration Register	Section 6.3.51
RGB to YCbCr Conversion			
0x01C7:1228	YCC_ADJ	Luminance Adjustment (Contrast and Brightness) Register	Section 6.3.52
0x01C7:122C	YCC_MUL_RY	Matrix Coefficient RY Register	Section 6.3.53
0x01C7:1230	YCC_MUL_GY	Matrix Coefficient GY Register	Section 6.3.54
0x01C7:1234	YCC_MUL_BY	Matrix Coefficient BY Register	Section 6.3.55
0x01C7:1238	YCC_MUL_RCB	Matrix Coefficient RCb Register	Section 6.3.56
0x01C7:123C	YCC_MUL_GCB	Matrix Coefficient GCb Register	Section 6.3.57
0x01C7:1240	YCC_MUL_BCB	Matrix Coefficient BCb Register	Section 6.3.58
0x01C7:1244	YCC_MUL_RCR	Matrix Coefficient RCr Register	Section 6.3.59
0x01C7:1248	YCC_MUL_GCR	Matrix Coefficient GCr Register	Section 6.3.60
0x01C7:124C	YCC_MUL_BCR	Matrix Coefficient BCr Register	Section 6.3.61
0x01C7:1250	YCC_OFT_Y	Y Output Offset Register	Section 6.3.62
0x01C7:1254	YCC_OFT_CB	Cb Output Offset Register	Section 6.3.63
0x01C7:1258	YCC_OFT_CR	Cr Output Offset Register	Section 6.3.64
0x01C7:125C	YCC_Y_MIN	Saturation (Luminance Minimum) Register	Section 6.3.65
0x01C7:1260	YCC_Y_MAX	Saturation (Luminance Maximum) Register	Section 6.3.66
0x01C7:1264	YCC_C_MIN	Saturation (Chrominance Minimum) Register	Section 6.3.67
0x01C7:1268	YCC_C_MAX	Saturation (Chrominance Maximum) Register	Section 6.3.68
0x01C7:126C	YCC_PHS	Chrominance Position (for 422 Down Sampler) Register	Section 6.3.69
Edge Enhancer			
0x01C7:1270	YEE_EN	Edge Enhancer Enable Register	Section 6.3.70
0x01C7:1274	YEE_EMF	MedianNR Enable Register	Section 6.3.71
0x01C7:1278	YEE_SHF	HPF Shift Length Register	Section 6.3.72
0x01C7:127C	YEE_MUL_00	HPF Coefficient 00 Register	Section 6.3.73
0x01C7:1280	YEE_MUL_01	HPF Coefficient 01 Register	Section 6.3.74
0x01C7:1284	YEE_MUL_02	HPF Coefficient 02 Register	Section 6.3.75
0x01C7:1288	YEE_MUL_10	HPF Coefficient 10 Register	Section 6.3.76
0x01C7:128C	YEE_MUL_11	HPF Coefficient 11 Register	Section 6.3.77
0x01C7:1290	YEE_MUL_12	HPF Coefficient 12 Register	Section 6.3.78
0x01C7:1294	YEE_MUL_20	HPF Coefficient 20 Register	Section 6.3.79

Table 122. Image Pipe Registers (IPIPE) (continued)

Address	Acronym	Register Description	Section
0x01C7:1298	YEE_MUL_21	HPF Coefficient 21 Register	Section 6.3.80
0x01C7:129C	YEE_MUL_22	HPF Coefficient 22 Register	Section 6.3.81
False Color Suppression			
0x01C7:12A0	FCS_EN	Fault Color Suppression Enable Register	Section 6.3.82
0x01C7:12A4	FCS_TYP	Type Selection of HPF Register	Section 6.3.83
0x01C7:12A8	FCS_SHF_Y	Down Shift Size (HPF) Register	Section 6.3.84
0x01C7:12AC	FCS_SHF_C	Down Shift size (GAIN) Register	Section 6.3.85
0x01C7:12B0	FCS_THR	Threshold Register	Section 6.3.86
0x01C7:12B4	FCS_SGN	Intensity Register	Section 6.3.87
0x01C7:12B8	FCS_LTH	Lower Limit of Chroma Gain Register	Section 6.3.88
Resizer			
0x01C7:12BC	RSZ_SEQ	Processing Mode Register	Section 6.3.89
0x01C7:12C0	RSZ_AAL	Vertical Anti Aliasing Filter Register	Section 6.3.90
RSZ 0			
Resizer Rescale Parameters			
0x01C7:12C4	RSZ_EN	Resizer Enable Register	Section 6.3.91
0x01C7:12C8	RSZ_MODE	One Shot Mode Register	Section 6.3.92
0x01C7:12CC	RSZ_I_VST	Vertical Start Position of the Input Register	Section 6.3.93
0x01C7:12D0	RSZ_I_VSZ	Vertical Size of the Input Register	Section 6.3.94
0x01C7:12D4	RSZ_I_HST	Horizontal Start Position of the Input Register	Section 6.3.95
0x01C7:12D8	RSZ_O_VSZ	Vertical Size of the Output Register	Section 6.3.96
0x01C7:12DC	RSZ_O_HST	Horizontal Start Position of the Output Register	Section 6.3.97
0x01C7:12E0	RSZ_O_HSZ	Horizontal Size of the Output Register	Section 6.3.98
0x01C7:12E4	RSZ_V_PHS	Initial Phase of Vertical Resizing Process Register	Section 6.3.99
0x01C7:12E8	RSZ_V_PHS_O	Phase of Last Value in Previous Resize Process Register	Section 6.3.100
0x01C7:12EC	RSZ_V_DIF	Vertical Resize Parameter Register	Section 6.3.101
0x01C7:12F0	RSZ_V_SIZ_O	Actual Number of Output Lines Register	Section 6.3.102
0x01C7:12F4	RSZ_H_PHS	Initial Phase of Horizontal Resizing Process Register	Section 6.3.103
0x01C7:12F8	RSZ_H_DIF	Horizontal Resize Parameter Register	Section 6.3.104
0x01C7:12FC	RSZ_H_TYP	Interpolation Method for Horizontal Rescaling Register	Section 6.3.105
0x01C7:1300	RSZ_H_LSE	Selection of Horizontal LPF Intensity Register	Section 6.3.106
0x01C7:1304	RSZ_H_LPF	Horizontal LPF Intensity Register	Section 6.3.107
Resizer RGB Conversion Parameters			
0x01C7:1308	RSZ_RGB_EN	RGB Output Enable Register	Section 6.3.108
0x01C7:130C	RSZ_RGB_TYP	RGB Output Bit Mode (32 or 16 bit) Register	Section 6.3.109
0x01C7:1310	RSZ_RGB_BLD	YC422 to YC444 Conversion Method Register	Section 6.3.110
Resizer External Memory Parameters			
0x01C7:1314	RSZ_SDR_BAD_H	SDRAM Base Address MSB Register	Section 6.3.111
0x01C7:1318	RSZ_SDR_BAD_L	SDRAM Base Address LSB Register	Section 6.3.112
0x01C7:131C	RSZ_SDR_SAD_H	SDRAM Start Address MSB Register	Section 6.3.113
0x01C7:1320	RSZ_SDR_SAD_L	SDRAM Start Address LSB Register	Section 6.3.114
0x01C7:1324	RSZ_SDR_OFT	SDRAM Line Offset Register	Section 6.3.115
0x01C7:1328	RSZ_SDR_PTR_S	Start Line of SDRAM Pointer Register	Section 6.3.116
0x01C7:132C	RSZ_SDR_PTR_E	End line of SDRAM Pointer Register	Section 6.3.117
0x01C7:1330	RSZ_SDR_PTR_O	Output of Current Pointer Value (Read Only) Register	Section 6.3.118

Table 122. Image Pipe Registers (IPIPE) (continued)

Address	Acronym	Register Description	Section
RSZ 1			
Resizer Rescale Parameters			
0x01C7:1334	RSZ_EN	Resizer Enable Register	Section 6.3.91
0x01C7:1338	RSZ_MODE	One Shot Mode Register	Section 6.3.92
0x01C7:133C	RSZ_I_VST	Vertical Start Position of the Input Register	Section 6.3.93
0x01C7:1340	RSZ_I_VSZ	Vertical Size of the Input Register	Section 6.3.94
0x01C7:1344	RSZ_I_HST	Horizontal Start Position of the Input Register	Section 6.3.95
0x01C7:1348	RSZ_O_VSZ	Vertical Size of the Output Register	Section 6.3.96
0x01C7:134C	RSZ_O_HST	Horizontal Start Position of the Output Register	Section 6.3.97
0x01C7:1350	RSZ_O_HSZ	Horizontal Size of the Output Register	Section 6.3.98
0x01C7:1354	RSZ_V_PHS	Initial Phase of Vertical Resizing Process Register	Section 6.3.99
0x01C7:1358	RSZ_V_PHS_O	Phase of Last Value in Previous Resize Process Register	Section 6.3.100
0x01C7:135C	RSZ_V_DIF	Vertical Resize Parameter Register	Section 6.3.101
0x01C7:1360	RSZ_V_SIZ_O	Actual Number of Output Lines Register	Section 6.3.102
0x01C7:1364	RSZ_H_PHS	Initial Phase of Horizontal Resizing Process Register	Section 6.3.103
0x01C7:1368	RSZ_H_DIF	Horizontal Resize Parameter Register	Section 6.3.104
0x01C7:136C	RSZ_H_TYP	Interpolation Method for Horizontal Rescaling Register	Section 6.3.105
0x01C7:1370	RSZ_H_LSE	Selection of Horizontal LPF Intensity Register	Section 6.3.106
0x01C7:1374	RSZ_H_LPF	Horizontal LPF Intensity Register	Section 6.3.107
Resizer RGB Conversion Parameters			
0x01C7:1378	RSZ_RGB_EN	RGB Output Enable Register	Section 6.3.108
0x01C7:137C	RSZ_RGB_TYP	RGB Output Bit Mode (32 or 16 bit) Register	Section 6.3.109
0x01C7:1380	RSZ_RGB_BLD	YC422 to YC444 Conversion Method Register	Section 6.3.110
Resizer External Memory Parameters			
0x01C7:1384	RSZ_SDR_BAD_H	SDRAM Base Address MSB Register	Section 6.3.111
0x01C7:1388	RSZ_SDR_BAD_L	SDRAM Base Address LSB Register	Section 6.3.112
0x01C7:138C	RSZ_SDR_SAD_H	SDRAM Start Address MSB Register	Section 6.3.113
0x01C7:1390	RSZ_SDR_SAD_L	SDRAM Start Address LSB Register	Section 6.3.114
0x01C7:1394	RSZ_SDR_OFT	SDRAM Line Offset Register	Section 6.3.115
0x01C7:1398	RSZ_SDR_PTR_S	Start Line of SDRAM Pointer Register	Section 6.3.116
0x01C7:139C	RSZ_SDR_PTR_E	End line of SDRAM Pointer Register	Section 6.3.117
0x01C7:13A0	RSZ_SDR_PTR_O	Output of Current Pointer Value (Read Only) Register	Section 6.3.118
Boxcar (2d)			
0x01C7:13A4	BOX_EN	Boxcar Enable Register	Section 6.3.119
0x01C7:13A8	BOX_MODE	One Shot Mode Register	Section 6.3.120
0x01C7:13AC	BOX_TYP	Block Size (16x16 or 8x8) Register	Section 6.3.121
0x01C7:13B0	BOX_SHF	Down Shift Value of Input Register	Section 6.3.122
0x01C7:13B4	HST_EN	Histogram Enable Register	Section 6.3.123
0x01C7:13B8	HST_MODE	One Shot Mode Register	Section 6.3.124
0x01C7:13BC	HST_SEL	Histogram Source Select Register	Section 6.3.125
0x01C7:13C0	HST_PARA	Histogram Parameters Select Register	Section 6.3.126

Table 122. Image Pipe Registers (IPIPE) (continued)

Address	Acronym	Register Description	Section
Histogram Region Definitions			
Histogram Region 0			
0x01C7:13C4	HST_VST	Vertical Start Position Register	Section 6.3.127
0x01C7:13C8	HST_VSZ	Vertical Size Register	Section 6.3.128
0x01C7:13CC	HST_HST	Horizontal Start Position Register	Section 6.3.129
0x01C7:13D0	HST_HSZ	Horizontal Size Register	Section 6.3.130
Histogram Region 1			
0x01C7:13D4	HST_VST	Vertical Start Position Register	Section 6.3.127
0x01C7:13D8	HST_VSZ	Vertical Size Register	Section 6.3.128
0x01C7:13DC	HST_HST	Horizontal Start Position Register	Section 6.3.129
0x01C7:13E0	HST_HSZ	Horizontal Size Register	Section 6.3.130
Histogram Region 2			
0x01C7:13E4	HST_VST	Vertical Start Position Register	Section 6.3.127
0x01C7:13E8	HST_VSZ	Vertical Size Register	Section 6.3.128
0x01C7:13EC	HST_HST	Horizontal Start Position Register	Section 6.3.129
0x01C7:13F0	HST_HSZ	Horizontal Size Register	Section 6.3.130
Histogram Region 3			
0x01C7:13F4	HST_VST	Vertical Start Position Register	Section 6.3.127
0x01C7:13F8	HST_VSZ	Vertical Size Register	Section 6.3.128
0x01C7:13FC	HST_HST	Horizontal Start Position Register	Section 6.3.129
0x01C7:1400	HST_HSZ	Horizontal Size Register	Section 6.3.130

6.3.1 IPIPE Enable Register (IPIPE_EN)

The IPIPE enable register (IPIPE_EN) is shown in Figure 156 and described in Table 123.

Figure 156. IPIPE Enable Register (IPIPE_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 123. IPIPE Enable Register (IPIPE_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved
0	EN		The start flag of the IPIPE module.
			When EN is 1, the IPIPE module starts a processing from the next rising edge of the VD.
			If the processing mode of the IPIPE module is "one shot", the EN is cleared to 0 after the end of the processing area.
		0	Disable.
		1	Enable.

6.3.2 One Shot Mode Register (IPIPE_MODE)

The one shot mode register (IPIPE_MODE) is shown in Figure 157 and described in Table 124.

Figure 157. One Shot Mode Register (IPIPE_MODE)

15	2	1	0
Reserved		WRT	ONESHOT
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 124. One Shot Mode Register (IPIPE_MODE) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved
1	WRT		CAM_WEN mode selection.
			The mode selection of processing based on CAM_WEN signal. If WRT is 0, the IPIPE module ignores CAM_WEN signal and processes every image frame while IPIPE is enabled. If WRT = 1, the IPIPE only processes frames that while CAM_WEN is high. This bit should be cleared when the input timing is generated by the IPIPEIF (not from CCDC).
		0	Disable.
		1	Enable.
0	ONESHOT		One shot mode.
			The processing mode selection of the IPIPE module. Value 0 indicates the mode of "free run", value 1 indicates the mode of "one shot".
		0	Disable.
		1	Enable

6.3.3 Input/Output Data Paths Register (IPIPE_DPATHS)

The Input/Output data paths register (IPIPE_DPATHS) is shown in Figure 158 and described in Table 125.

Figure 158. Input/Output Data Paths Register (IPIPE_DPATHS)

15	3	2	1	0
Reserved		BYPASS	FMT	
R-0		R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 125. Input/Output Data Paths Register (IPIPE_DPATHS) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved
2	BYPASS		Enable RAW-Bypass mode through IPIPE.
			This mode enables passthru of RAW input for images up to 4096 pixels wide. This bit is valid only if FMT = 1 (Bayer input, bayer output).
		0	Raw passthru mode off.
		1	Raw passthru mode on.
0-1	FMT		Data Path through IPIPE.
		0	(RAW2YUV) Bayer input, YCbCr (or RGB) output.
		1	(RAW2RAW) Bayer input, Bayer output.
		2	(RAW2BOX) Bayer input, Boxcar output.
		3	(YUV2YUV) YCbCr (16bit) input, YCbCr (or RGB) output.

6.3.4 Color Pattern Register (IPIPE_COLPAT)

The color pattern register (IPIPE_COLPAT) is shown in Figure 159 and described in Table 126.

Figure 159. Color Pattern Register (IPIPE_COLPAT)

15 8	7 6	5 4	3 2	1 0
Reserved	OLOP	OLEP	ELOP	ELEP
R-0	R/W-3	R/W-2	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 126. Color Pattern Register (IPIPE_COLPAT) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-6	OLOP		Color of the odd line and odd pixel. This parameter is valid when IPIPE_DPATHS[FMT] is 0.
		0	(R) Red.
		1	(Gr) Green (red line).
		2	(Gb) Green (blue line).
		3	(B) Blue.
5-4	OLEP		Color of the odd line and even pixel. This parameter is valid when IPIPE_DPATHS[FMT] is 0.
		0	(R) Red.
		1	(Gr) Green (red line).
		2	(Gb) Green (blue line).
		3	(B) Blue.
3-2	ELOP		Color of the even line and odd pixel. This parameter is valid when IPIPE_DPATHS[FMT] is 0.
		0	(R) Red.
		1	(Gr) Green (red line).
		2	(Gb) Green (blue line).
		3	(B) Blue.
1-0	ELEP		Color of the even line and even pixel. This parameter is valid when IPIPE_DPATHS[FMT] is 0.
		0	(R) Red.
		1	(Gr) Green (red line).
		2	(Gb) Green (blue line).
		3	(B) Blue.

6.3.5 Vertical Start Position Register (IPIPE_VST)

The vertical start position register (IPIPE_VST) is shown in Figure 160 and described in Table 127.

Figure 160. Vertical Start Position Register (IPIPE_VST)

15 13	12 0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 127. Vertical Start Position Register (IPIPE_VST) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Vertical start position. The vertical position of the global frame from the rising edge of the VD. The IPIPE module will start an image processing from VAL line.

6.3.6 Vertical Processing Size Register (IPIPE_VSZ)

The vertical processing size register (IPIPE_VSZ) is shown in Figure 161 and described in Table 128.

Figure 161. Vertical Processing Size Register (IPIPE_VSZ)

15 13	12 0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

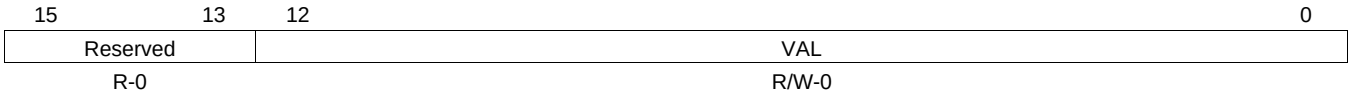
Table 128. Vertical Processing Size Register (IPIPE_VSZ) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Vertical processing size. The vertical size of the processing area. VAL[0] can not be written. The IPIPE module will process (VAL + 1) lines.

6.3.7 Horizontal Start Position Register (IPIPE_HST)

The horizontal start position register (IPIPE_HST) is shown in Figure 162 and described in Table 129.

Figure 162. Horizontal Start Position Register (IPIPE_HST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

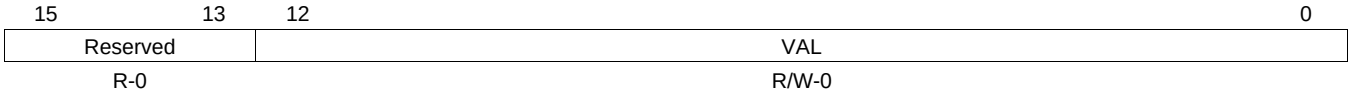
Table 129. Horizontal Start Position Register (IPIPE_HST) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Horizontal start position. The horizontal position of the global frame from the rising edge of the HD. The IPIPE module will start an image processing from VAL pixel.

6.3.8 Horizontal Processing Size Register (IPIPE_HSZ)

The horizontal processing size register (IPIPE_HSZ) is shown in Figure 163 and described in Table 130.

Figure 163. Horizontal Processing Size Register (IPIPE_HSZ)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 130. Horizontal Processing Size Register (IPIPE_HSZ) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Horizontal processing size. The horizontal size of the processing area. VAL[0] can not be written. The IPIPE module will process (VAL + 1) pixels.

6.3.9 ARM Gated Clock Control Register (GCL_ARM)

The ARM gated clock control register (GCL_ARM) is shown in Figure 164 and described in Table 131.

Figure 164. ARM Gated Clock Control Register (GCL_ARM)

15	1	0
Reserved		REG
R-0		R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 131. ARM Gated Clock Control Register (GCL_ARM) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	REG		IPIPE MMR clock enable.
			The on/off selection of the MMR interface clock which is used for ARM register accesses.
		0	Off
		1	On

6.3.10 CCD Gated Clock Control Register (GCL_CCD)

The CCD gated clock control register (GCL_CCD) is shown in Figure 165 and described in Table 132.

Figure 165. CCD Gated Clock Control Register (GCL_CCD)

15	3	2	1	0
Reserved		G2	G1	G0
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 132. CCD Gated Clock Control Register (GCL_CCD) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved
2	G2		IPIPE G2 clock enable.
			The on/off selection of the clock which is used for the IPIPE processing of "CFA" to "422", "Histogram".
		0	Off
		1	On
1	G1		IPIPE G1 clock enable.
			The on/off selection of the clock which is used for the IPIPE processing of "Defect Correction" to "White Balance".
		0	Off
		1	On
0	G0		IPIPE G0 clock enable.
			The on/off selection of the clock which is used for the IPIPE processing of "Boxcar".
		0	Off
		1	On

6.3.11 SDR Gated Clock Control Register (GCL_SDR)

The SDR gated clock control register (GCL_ARM) is shown in Figure 166 and described in Table 133.

Figure 166. SDR Gated Clock Control Register (GCL_SDR)

15	1	0
Reserved		RSZ
R-0		R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 133. SDR Gated Clock Control Register (GCL_SDR) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	RSZ		IPIPE RSZ clock enable. The on/off selection of the clock which is used for "Resize". The resizer operates in bypass mode when this is off.
		0	Off
		1	On

6.3.12 Internal Table Selection Register (RAM_MODE)

The internal table selection register (RAM_MODE) is shown in Figure 167 and described in Table 134.

Figure 167. Internal Table Selection Register (RAM_MODE)

15	14 7	6	5	4	3 0
WIT	Reserved	EXT	WDT	ADR	SEL
R-1	R-0	R/W-0	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 134. Internal Table Selection Register (RAM_MODE) Field Descriptions

Bit	Field	Value	Description
15	WIT		Internal wait flag.
			Value 0 indicates that the IPIPE module is busy. In this condition access to the RAM_xxx registers is prohibited.
		0	Busy.
		1	Not busy.
15-7	Reserved	0	Reserved.
6	EXT		Output selection of the IPIPE_NWAIT.
		0	Output.
		1	No output (Use WIT).
5	WDT		Write data enable. Value 0 indicates that RAM_WDT is written to the internal memory.
		0	Read only.
		1	Write.
4	ADR		Auto increment mode. Value 1 indicates that RAM_ADR adds to 1 after each memory access.
		0	Manual mode.
		1	Auto increment mode.
3-0	SEL		Memory selection.
		0	Histogram 0.
		1	Histogram 1.
		2	Reserved.
		3	Reserved.
		4	Defect correction.
		5	Gamma Red.
		6	Gamma Green.
		7	Gamma Blue.
		8	Gamma RGB all.
		9	Edge enhancer.

6.3.13 Address Register (RAM_ADR)

The address register (RAM_ADR) is shown in Figure 168 and described in Table 135.

Figure 168. Address Register (RAM_ADR)

15 13	12 0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 135. Address Register (RAM_ADR) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Address of an internal memory.

6.3.14 Write Data Register (RAM_WDT)

The write data register (RAM_WDT) is shown in Figure 169 and described in Table 136.

Figure 169. Write Data Register (RAM_WDT)

15 0
VAL
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 136. Write Data Register (RAM_WDT) Field Descriptions

Bit	Field	Value	Description
15-0	VAL	0-FFFFh	Write data value of an internal memory.

6.3.15 Read Data Register (RAM_RDT)

The read data register (RAM_RDT) is shown in Figure 170 and described in Table 137.

Figure 170. Read Data Register (RAM_RDT)

15 0
VAL
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 137. Read Data Register (RAM_RDT) Field Descriptions

Bit	Field	Value	Description
15-0	VAL	0-FFFFh	Read data value of an internal memory.

6.3.16 Interrupt Enable Register (IRQ_EN)

The interrupt enable register (IRQ_EN) is shown in Figure 171 and described in Table 138.

Figure 171. Interrupt Enable Register (IRQ_EN)

15	6	5	4	3	2	1	0
Reserved		INT5	INT4	INT3	INT2	INT1	INT0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

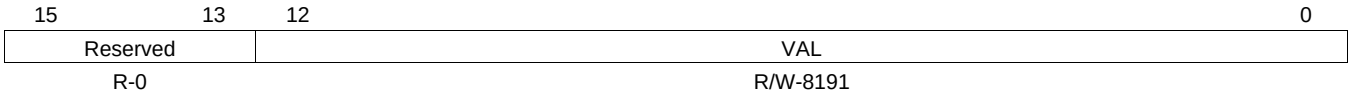
Table 138. Interrupt Enable Register (IRQ_EN) Field Descriptions

Bit	Field	Value	Description
15-6	Reserved	0	Reserved.
5	INT5		IRQ5 enable. Interrupt signal to indicate the beginning of the time period in which update of registers is allowed.
		0	Disable.
		1	Enable.
4	INT4		IRQ4 enable. Interrupt signal to indicate the completion of boundary signal calculator.
		0	Disable.
		1	Enable.
3	INT3		IRQ3 enable. Refer to IRQ_RZB.
		0	Disable.
		1	Enable.
2	INT2		IRQ2 enable. Refer to IRQ_RZA.
		0	Disable.
		1	Enable.
1	INT1		IRQ1 enable. Interrupt signal to indicate that output of a frame to SDRAM is finished, either in IPIPE mode or Boxcar mode.
		0	Disable.
		1	Enable.
0	INT0		IRQ0 enable. Interrupt signal at the last pixel output in image_pipe (completion of histogram).
		0	Disable.
		1	Enable.

6.3.17 Interval of IRQ-2 Register (IRQ_RZA)

The interval of IRQ-2 register (IRQ_RZA) is shown in Figure 172 and described in Table 139.

Figure 172. Interval of IRQ-2 Register (IRQ_RZA)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

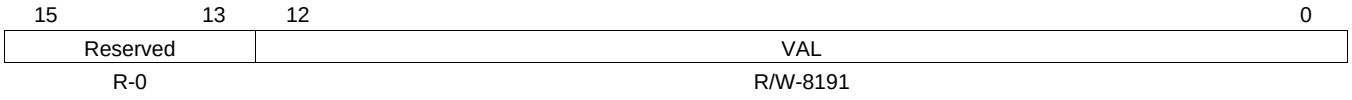
Table 139. Interval of IRQ-2 Register (IRQ_RZA) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Interval of IRQ_2. Interrupt signal at every (VAL + 1) lines of Resize and RGB output.

6.3.18 Interval of IRQ-3 Register (IRQ_RZB)

The interval of IRQ-3 register (IRQ_RZB) is shown in Figure 173 and described in Table 140.

Figure 173. Interval of IRQ-3 Register (IRQ_RZB)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 140. Interval of IRQ-3 Register (IRQ_RZB) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Interval of IRQ_3. Interrupt signal at every (VAL + 1) lines of Resize and RGB output.

6.3.19 Defect Correction Enable Register (DFC_EN)

The defect correction enable register (DFC_EN) is shown in Figure 174 and described in Table 141.

Figure 174. Defect Correction Enable Register (DFC_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 141. Defect Correction Enable Register (DFC_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Defect correction enable.
		0	Disable.
		1	Enable.

6.3.20 Copy Method Selection (from Top or from Bottom) Register (DFC_SEL)

The copy method selection (from top or from bottom) Register (DFC_SEL) is shown in Figure 175 and described in Table 142.

Figure 175. Copy Method Selection (from Top or from Bottom) Register (DFC_SEL)

15	1	0
Reserved		SEL
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 142. Copy Method Selection (from Top or from Bottom) Register (DFC_SEL) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	SEL		Copy method in vertical defect correction. Used when defect correction method for a pixel is set to option #7.
		0	From top.
		1	From bottom.

6.3.21 Start Address in LUT Register (DFC_ADR)

The start address in LUT register (DFC_ADR) is shown in Figure 176 and described in Table 143.

Figure 176. Start Address in LUT Register (DFC_ADR)

15	10	9	0
Reserved		ADR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 143. Start Address in LUT Register (DFC_ADR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	ADR	0-3FFh	Start Address in LUT.

6.3.22 Number of Available Entries in LUT Register (DFC_SIZ)

The number of available entries in LUT register (DFC_SIZ) is shown in Figure 177 and described in Table 144.

Figure 177. Number of Available Entries in LUT Register (DFC_SIZ)

15	10	9	0
Reserved		SIZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 144. Number of Available Entries in LUT Register (DFC_SIZ) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	SIZ	0-3FFh	Number of valid data in LUT.

6.3.23 2D Noise Filter Enable Register (D2F_EN)

The 2D noise filter enable register (D2F_EN) is shown in Figure 178 and described in Table 145.

Figure 178. 2D Noise Filter Enable Register (D2F_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 145. 2D Noise Filter Enable Register (D2F_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	SEL		Noise filter enable.
		0	Disable.
		1	Enable.

6.3.24 Noise Filter Configuration Register (D2F_CFG)

The noise filter configuration register (D2F_CFG) is shown in Figure 179 and described in Table 146.

Figure 179. Noise Filter Configuration Register (D2F_CFG)

15	4	3 2	1 0
Reserved	TYP	SHF	SPR
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

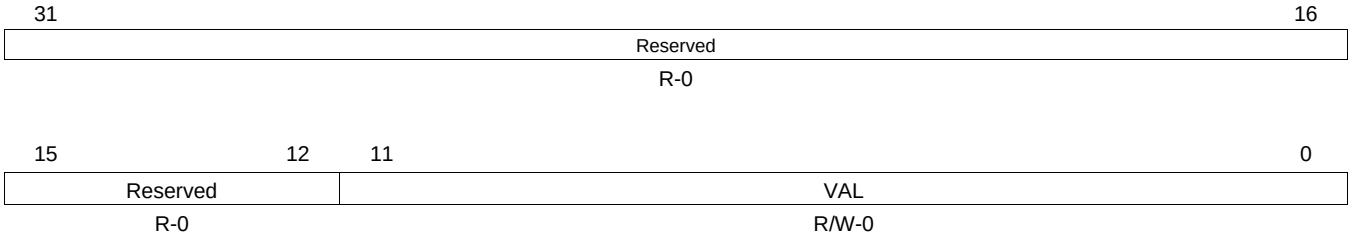
Table 146. Noise Filter Configuration Register (D2F_CFG) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved.
4	TYP		Sampling method of green pixels.
		0	Box (same as R or B).
		1	Diamond mode.
3-2	SHF	0-3	Down shift value in LUT reference address.
1-0	SPR	0-3	Spread value in noise filter algorithm.

6.3.25 Noise Filter LUT Values (Threshold) Register (D2F_THR[32])

The noise filter LUT values (Threshold) register (D2F_THR[32]) is shown in Figure 180 and described in Table 147.

Figure 180. Noise Filter LUT Values (Threshold) Register (D2F_THR[32])



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

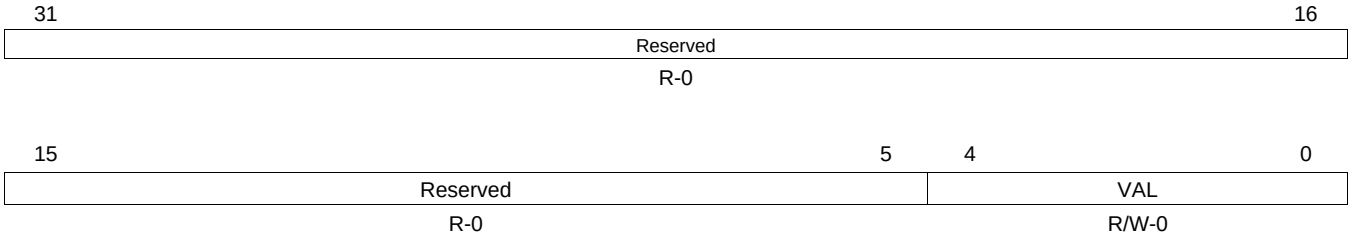
Table 147. Noise Filter LUT Values (Threshold) Register (D2F_THR[32]) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Threshold value in noise filter algorithm.

6.3.26 Noise Filter LUT Values (Intensity) Register (D2F_STR[32])

The noise filter LUT values (Intensity) register (D2F_STR[32]) is shown in Figure 181 and described in Table 148.

Figure 181. Noise Filter LUT Values (Intensity) Register (D2F_STR[32])



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 148. Noise Filter LUT Values (Intensity) Register (D2F_STR[32]) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved.
4-0	VAL	0-1Fh	Intensity value in noise filter algorithm. VAL needs to be equal to or less than 32.

6.3.27 PreFilter Enable Register (PRE_EN)

The PreFilter enable register (PRE_EN) is shown in Figure 182 and described in Table 149.

Figure 182. PreFilter Enable Register (PRE_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 149. PreFilter Enable Register (PRE_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		PreFilter enable.
		0	Disable.
		1	Enable.

6.3.28 PreFilter Type Register (PRE_TYP)

The PreFilter type register (PRE_TYP) is shown in Figure 183 and described in Table 150.

Figure 183. PreFilter Type Register (PRE_TYP)

15	4	3	2	1	0
Reserved		EN1	EN0	SEL1	SEL0
R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 150. PreFilter Type Register (PRE_TYP) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved.
3	EN1		Enable of Adaptive DotReduction.
		0	(DISABLE) only prefilter is applied.
		1	(ENABLE) DotReduction is applied after prefilter.
2	EN0		Enable of Adaptive PreFilter.
		0	(DISABLE) constant gain.
		1	(ENABLE) adaptive gain control.
1	SEL1		Averaging Method GS1 in PreFilter.
		0	(AVG4PIX) average of 4 pixels.
		1	(AVG2MEDPIX) average of 2 median pixels.
0	SEL0		Averaging Method GS2 in PreFilter.
		0	(AVG4PIX) average of 4 pixels.
		1	(AVG2MEDPIX) average of 2 median pixels.

6.3.29 Shift Value of Adaptive Gain Register (PRE_SHF)

The shift value of adaptive gain register (PRE_SHF) is shown in Figure 184 and described in Table 151.

Figure 184. Shift Value of Adaptive Gain Register (PRE_SHF)

15	4	3	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 151. Shift Value of Adaptive Gain Register (PRE_SHF) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved.
3-0	VAL	0-Fh	Downshift value in adaptive PreFilter algorithm.

6.3.30 Constant Gain or Adaptive Gain Slope Register (PRE_GAIN)

The constant gain or adaptive gain slope register (PRE_GAIN) is shown in Figure 185 and described in Table 152.

Figure 185. Constant Gain or Adaptive Gain Slope Register (PRE_GAIN)

15	8	7	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 152. Constant Gain or Adaptive Gain Slope Register (PRE_GAIN) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	VAL	0-FFh	Constant gain or adaptive gain slope. In constant gain mode (PRE_TYP[EN0]=0), VAL specifies the PreFilter gain. In adaptive PreFilter mode (PRE_TYP[EN0]=1), VAL specifies the slope in gain function.

6.3.31 Threshold G Register (PRE_THR_G)

The threshold G register (PRE_THR_G) is shown in Figure 186 and described in Table 153.

Figure 186. Threshold G Register (PRE_THR_G)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 153. Threshold G Register (PRE_THR_G) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Threshold (ThrG) in the adaptive PreFilter algorithm.

6.3.32 Threshold B Register (PRE_THR_B)

The threshold B register (PRE_THR_B) is shown in Figure 187 and described in Table 154.

Figure 187. Threshold B Register (PRE_THR_B)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 154. Threshold B Register (PRE_THR_B) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Threshold (ThrB) in the DotReduction.

6.3.33 Threshold 1 Register (PRE_THR_1)

The threshold 1 register (PRE_THR_1) is shown in Figure 188 and described in Table 155.

Figure 188. Threshold 1 Register (PRE_THR_1)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 155. Threshold 1 Register (PRE_THR_1) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Threshold (Thr1) in the adaptive PreFilter algorithm.

6.3.34 Digital Gain Register (WB2_DGN)

The digital gain register (WB2_DGN) is shown in Figure 189 and described in Table 156.

Figure 189. Digital Gain Register (WB2_DGN)

15	10	9	0
Reserved		DGAIN	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

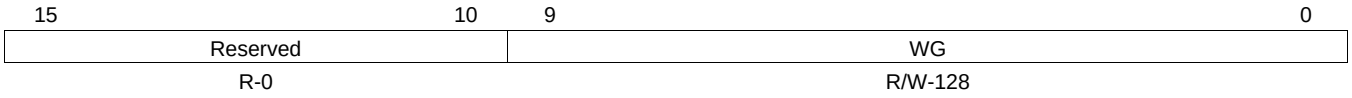
Table 156. Digital Gain Register (WB2_DGN) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	DGAIN	0-3FFh	Digital Gain. Value is in U10Q8.

6.3.35 White Balance Gain (Red) Register (WB2_WG_R)

The white balance gain (Red) register (WB2_WG_R) is shown in Figure 190 and described in Table 157.

Figure 190. White Balance Gain (Red) Register (WB2_WG_R)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

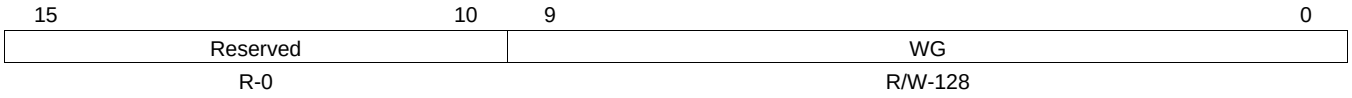
Table 157. White Balance Gain (Red) Register (WB2_WG_R) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	WG	0-3FFh	Red gain. Value is in U10Q7.

6.3.36 White Balance Gain (Gr) Register (WB2_WG_GR)

The white balance gain (Gr) register (WB2_WG_GR) is shown in Figure 191 and described in Table 158.

Figure 191. White Balance Gain (Gr) Register (WB2_WG_GR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 158. White Balance Gain (Gr) Register (WB2_WG_GR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	WG	0-3FFh	Gr gain. Value is in U10Q7.

6.3.37 White Balance Gain (Gb) Register (WB2_WG_GB)

The white balance gain (Gb) register (WB2_WG_GB) is shown in Figure 192 and described in Table 159.

Figure 192. White Balance Gain (Gb) Register (WB2_WG_GB)

15	10	9	0
Reserved		WG	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 159. White Balance Gain (Gb) Register (WB2_WG_GB) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	WG	0-3FFh	Gb gain. Value is in U10Q7.

6.3.38 White Balance Gain (Blue) Register (WB2_WG_B)

The white balance gain (Blue) register (WB2_WG_B) is shown in Figure 193 and described in Table 160.

Figure 193. White Balance Gain (Blue) Register (WB2_WG_B)

15	10	9	0
Reserved		WG	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 160. White Balance Gain (Blue) Register (WB2_WG_B) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	WG	0-3FFh	Blue gain. Value is in U10Q7.

6.3.39 Matrix Coefficient RR Register (RGB_MUL_RR)

The matrix coefficient RR register (RGB_MUL_RR) is shown in Figure 194 and described in Table 161.

Figure 194. Matrix Coefficient RR Register (RGB_MUL_RR)

15	12	11	0
Reserved		VAL	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 161. Matrix Coefficient RR Register (RGB_MUL_RR) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient RR. Value is in S12Q8.

6.3.40 Matrix Coefficient GR Register (RGB_MUL_GR)

The matrix coefficient GR register (RGB_MUL_GR) is shown in Figure 195 and described in Table 162.

Figure 195. Matrix Coefficient GR Register (RGB_MUL_GR)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 162. Matrix Coefficient GR Register (RGB_MUL_GR) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient GR. Value is in S12Q8.

6.3.41 Matrix Coefficient BR Register (RGB_MUL_BR)

The matrix coefficient BR register (RGB_MUL_BR) is shown in Figure 196 and described in Table 163.

Figure 196. Matrix Coefficient BR Register (RGB_MUL_BR)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 163. Matrix Coefficient BR Register (RGB_MUL_BR) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient BR. Value is in S12Q8.

6.3.42 Matrix Coefficient RG Register (RGB_MUL_RG)

The matrix coefficient RG register (RGB_MUL_RG) is shown in Figure 197 and described in Table 164.

Figure 197. Matrix Coefficient RG Register (RGB_MUL_RG)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 164. Matrix Coefficient RG Register (RGB_MUL_RG) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient RG. Value is in S12Q8.

6.3.43 Matrix Coefficient GG Register (RGB_MUL_GG)

The matrix coefficient GG register (RGB_MUL_GG) is shown in Figure 198 and described in Table 165.

Figure 198. Matrix Coefficient GG Register (RGB_MUL_GG)

15	12	11	0
Reserved		VAL	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 165. Matrix Coefficient GG Register (RGB_MUL_GG) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient GG. Value is in S12Q8.

6.3.44 Matrix Coefficient BG Register (RGB_MUL_BG)

The matrix coefficient BG register (RGB_MUL_BG) is shown in Figure 199 and described in Table 166.

Figure 199. Matrix Coefficient BG Register (RGB_MUL_BG)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 166. Matrix Coefficient BG Register (RGB_MUL_BG) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient BG. Value is in S12Q8.

6.3.45 Matrix Coefficient RB Register (RGB_MUL_RB)

The matrix coefficient RB register (RGB_MUL_RB) is shown in Figure 200 and described in Table 167.

Figure 200. Matrix Coefficient RB Register (RGB_MUL_RB)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 167. Matrix Coefficient RB Register (RGB_MUL_RB) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient RB. Value is in S12Q8.

6.3.46 Matrix Coefficient GB Register (RGB_MUL_GB)

The matrix coefficient GB register (RGB_MUL_GB) is shown in Figure 201 and described in Table 168.

Figure 201. Matrix Coefficient GB Register (RGB_MUL_GB)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

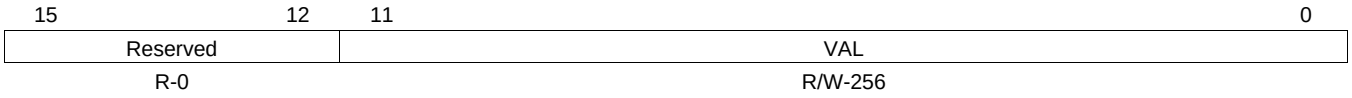
Table 168. Matrix Coefficient GB Register (RGB_MUL_GB) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient GB. Value is in S12Q8.

6.3.47 Matrix Coefficient BB Register (RGB_MUL_BB)

The matrix coefficient BB register (RGB_MUL_BB) is shown in Figure 202 and described in Table 169.

Figure 202. Matrix Coefficient BB Register (RGB_MUL_BB)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

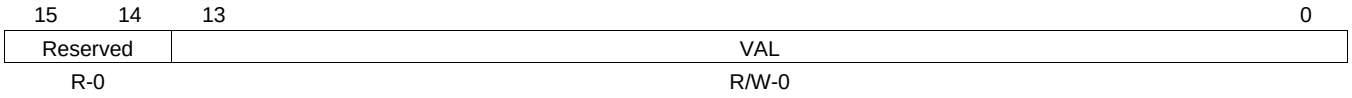
Table 169. Matrix Coefficient BB Register (RGB_MUL_BB) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Matrix coefficient BB. Value is in S12Q8.

6.3.48 R Output Offset Register (RGB_OFT_OR)

The R output offset register (RGB_OFT_OR) is shown in Figure 203 and described in Table 170.

Figure 203. R Output Offset Register (RGB_OFT_OR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 170. R Output Offset Register (RGB_OFT_OR) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Output offset value for R. Value is in S14Q0.

6.3.49 G Output Offset Register (RGB_OFT_OG)

The G output offset register (RGB_OFT_OG) is shown in Figure 204 and described in Table 171.

Figure 204. G Output Offset Register (RGB_OFT_OG)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 171. G Output Offset Register (RGB_OFT_OG) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Output offset value for G. Value is in S14Q0.

6.3.50 B Output Offset Register (RGB_OFT_OB)

The B output offset register (RGB_OFT_OB) is shown in Figure 205 and described in Table 172.

Figure 205. B Output Offset Register (RGB_OFT_OB)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 172. B Output Offset Register (RGB_OFT_OB) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Output offset value for B. Value is in S14Q0.

6.3.51 Gamma Correction Configuration Register (GMM_CFG)

The gamma correction configuration register (GMM_CFG) is shown in Figure 206 and described in Table 173.

Figure 206. Gamma Correction Configuration Register (GMM_CFG)

15	7	6	5	4	3	2	1	0
Reserved		SIZ		TBL	Reserved	BYPB	BYPG	BYPR
R-0		R/W-3		R/W-0	R-0	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 173. Gamma Correction Configuration Register (GMM_CFG) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved.
6-5	SIZ		Size of gamma table.
		0	128 words.
		1	256 words.
		2	Reserved.
		3	512 words.
4	TBL		Selection of gamma table.
		0	RAM.
		1	ROM.
3	Reserved	0	Reserved.
2	BYPB		Gamma correction mode for B.
		0	Not bypass.
		1	Bypass.
1	BYPG		Gamma correction mode for G.
		0	Not bypass.
		1	Bypass.
0	BYPR		Gamma correction mode for R.
		0	Not bypass.
		1	Bypass.

6.3.52 Luminance Adjustment (Contrast and Brightness) Register (YCC_ADJ)

The luminance adjustment (contrast and brightness) register (YCC_ADJ) is shown in Figure 207 and described in Table 174.

Figure 207. Luminance Adjustment (Contrast and Brightness) Register (YCC_ADJ)

15	8	7	0
BRT		CTR	
R/W-0		R/W-16	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 174. Luminance Adjustment (Contrast and Brightness) Register (YCC_ADJ) Field Descriptions

Bit	Field	Value	Description
15-8	BRT	0-FFh	Brightness. Offset value for brightness control.
7-0	CTR	0-FFh	Contrast. Multiplier coefficient for contrast control. Value is in U8Q4.

6.3.53 Matrix Coefficient RY Register (YCC_MUL_RY)

The matrix coefficient RY register (YCC_MUL_RY) is shown in Figure 208 and described in Table 175.

Figure 208. Matrix Coefficient RY Register (YCC_MUL_RY)

15	10	9	0
Reserved		VAL	
R-0		R/W-77	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 175. Matrix Coefficient RY Register (YCC_MUL_RY) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for RY. Value is in S10Q8.

6.3.54 Matrix Coefficient GY Register (YCC_MUL_GY)

The matrix coefficient GY register (YCC_MUL_GY) is shown in Figure 209 and described in Table 176.

Figure 209. Matrix Coefficient GY Register (YCC_MUL_GY)

15	10	9	0
Reserved		VAL	
R-0		R/W-150	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 176. Matrix Coefficient GY Register (YCC_MUL_GY) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for GY. Value is in S10Q8.

6.3.55 Matrix Coefficient BY Register (YCC_MUL_BY)

The matrix coefficient BY register (YCC_MUL_BY) is shown in Figure 210 and described in Table 177.

Figure 210. Matrix Coefficient BY Register (YCC_MUL_BY)

15	10	9	0
Reserved		VAL	
R-0		R/W-29	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 177. Matrix Coefficient BY Register (YCC_MUL_BY) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for BY. Value is in S10Q8.

6.3.56 Matrix Coefficient RCb Register (YCC_MUL_RCB)

The matrix coefficient RCb register (YCC_MUL_RCB) is shown in Figure 211 and described in Table 178.

Figure 211. Matrix Coefficient RCb Register (YCC_MUL_RCB)

15	10	9	0
Reserved		VAL	
R-0		R/W-981	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 178. Matrix Coefficient RCb Register (YCC_MUL_RCB) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for RCb. Value is in S10Q8.

6.3.57 Matrix Coefficient GCb Register (YCC_MUL_GCB)

The matrix coefficient GCb register (YCC_MUL_GCB) is shown in Figure 212 and described in Table 179.

Figure 212. Matrix Coefficient GCb Register (YCC_MUL_GCB)

15	10	9	0
Reserved		VAL	
R-0		R/W-939	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 179. Matrix Coefficient GCb Register (YCC_MUL_GCB) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for GCb. Value is in S10Q8.

6.3.58 Matrix Coefficient BCb Register (YCC_MUL_BCB)

The matrix coefficient BCb register (YCC_MUL_BCB) is shown in Figure 213 and described in Table 180.

Figure 213. Matrix Coefficient BCb Register (YCC_MUL_BCB)

15	10	9	0
Reserved		VAL	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 180. Matrix Coefficient BCb Register (YCC_MUL_BCB) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for BCb. Value is in S10Q8.

6.3.59 Matrix Coefficient RCr Register (YCC_MUL_RCR)

The matrix coefficient RCr register (YCC_MUL_RCR) is shown in Figure 214 and described in Table 181.

Figure 214. Matrix Coefficient RCr Register (YCC_MUL_RCR)

15	10	9	0
Reserved		VAL	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 181. Matrix Coefficient RCr Register (YCC_MUL_RCR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for RCr. Value is in S10Q8.

6.3.60 Matrix Coefficient GCr Register (YCC_MUL_GCR)

The matrix coefficient GCr register (YCC_MUL_GCR) is shown in Figure 215 and described in Table 182.

Figure 215. Matrix Coefficient GCr Register (YCC_MUL_GCR)

15	10	9	0
Reserved		VAL	
R-0		R/W-917	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 182. Matrix Coefficient GCr Register (YCC_MUL_GCR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for GCr. Value is in S10Q8.

6.3.61 Matrix Coefficient BCr Register (YCC_MUL_BCR)

The matrix coefficient BCr register (YCC_MUL_BCR) is shown in Figure 216 and described in Table 183.

Figure 216. Matrix Coefficient BCr Register (YCC_MUL_BCR)

15	10	9	0
Reserved		VAL	
R-0		R/W-1003	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 183. Matrix Coefficient BCr Register (YCC_MUL_BCR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	Matrix coefficient for BCr. Value is in S10Q8.

6.3.62 Y Output Offset Register (YCC_OFT_Y)

The Y output offset register (YCC_OFT_Y) is shown in Figure 217 and described in Table 184.

Figure 217. Y Output Offset Register (YCC_OFT_Y)

15	9	8	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 184. Y Output Offset Register (YCC_OFT_Y) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	VAL	0-1FFh	Y output offset. Value is in S9Q0.

6.3.63 Cb Output Offset Register (YCC_OFT_CB)

The Cb output offset register (YCC_OFT_CB) is shown in Figure 218 and described in Table 185.

Figure 218. Cb Output Offset Register (YCC_OFT_CB)

15	9	8	0
Reserved		VAL	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 185. Cb Output Offset Register (YCC_OFT_CB) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	VAL	0-1FFh	Cb output offset. Value is in S9Q0.

6.3.64 Cr Output Offset Register (YCC_OFT_CR)

The Cr output offset register (YCC_OFT_CR) is shown in Figure 219 and described in Table 186.

Figure 219. Cr Output Offset Register (YCC_OFT_CR)

15	9	8	0
Reserved		VAL	
R-0		R/W-128	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 186. Cr Output Offset Register (YCC_OFT_CR) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	VAL	0-1FFh	Cr output offset. Value is in S9Q0.

6.3.65 Saturation (Luminance Minimum) Register (YCC_Y_MIN)

The saturation (luminance minimum) register (YCC_Y_MIN) is shown in Figure 220 and described in Table 187.

Figure 220. Saturation (Luminance Minimum) Register (YCC_Y_MIN)

15	8	7	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 187. Saturation (Luminance Minimum) Register (YCC_Y_MIN) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	VAL	0-FFh	Minimum luminance value.

6.3.66 Saturation (Luminance Maximum) Register (YCC_Y_MAX)

The saturation (luminance maximum) register (YCC_Y_MAX) is shown in Figure 221 and described in Table 188.

Figure 221. Saturation (Luminance Maximum) Register (YCC_Y_MAX)

15	8	7	0
Reserved		VAL	
R-0		R/W-255	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 188. Saturation (Luminance Maximum) Register (YCC_Y_MAX) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	VAL	0-FFh	Maximum luminance value.

6.3.67 Saturation (Chrominance Minimum) Register (YCC_C_MIN)

The saturation (chrominance minimum) register (YCC_C_MIN) is shown in Figure 222 and described in Table 189.

Figure 222. Saturation (Chrominance Minimum) Register (YCC_C_MIN)

15	8	7	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 189. Saturation (Chrominance Minimum) Register (YCC_C_MIN) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	VAL	0-FFh	Minimum chrominance value.

6.3.68 Saturation (Chrominance Maximum) Register (YCC_C_MAX)

The saturation (chrominance maximum) register (YCC_C_MAX) is shown in Figure 223 and described in Table 190.

Figure 223. Saturation (Chrominance Maximum) Register (YCC_C_MAX)

15	8	7	0
Reserved		VAL	
R-0		R/W-255	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 190. Saturation (Chrominance Maximum) Register (YCC_C_MAX) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	VAL	0-FFh	Maximum chrominance value.

6.3.69 Chrominance Position (for 422 Down Sampler) Register (YCC_PHS)

The chrominance position (for 422 down sampler) register (YCC_PHS) is shown in Figure 224 and described in Table 191.

Figure 224. Chrominance Position (for 422 Down Sampler) Register (YCC_PHS)

15	1	0
Reserved	LPF	SEL
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 191. Chrominance Position (for 422 down sampler) Register (YCC_PHS) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved.
1	LPF		121_LPF enable for chrominance.
		0	Off.
		1	On.
0	POS		Phase position of the output of the chrominance.
			If IPIPE_DPATHS = 3 (YCbCr input), then the phase position of the INPUT of the Chrominance is selected by this register.
		0	(COSITING) same position with luminance.
		1	(CENTERING) the middle of the luminance.

6.3.70 Edge Enhancer Enable Register (YEE_EN)

The edge enhancer enable register (YEE_EN) is shown in Figure 225 and described in Table 192.

Figure 225. Edge Enhancer Enable Register (YEE_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 192. Edge Enhancer Enable Register (YEE_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Edge enhancer enable.
		0	Disable.
		1	Enable.

6.3.71 MedianNR Enable Register (YEE_EMF)

The MedianNR enable register (YEE_EMF) is shown in Figure 226 and described in Table 193.

Figure 226. MedianNR Enable Register (YEE_EMF)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 193. MedianNR Enable Register (YEE_EMF) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		MedianNR enable.
		0	Disable.
		1	Enable.

6.3.72 HPF Shift Length Register (YEE_SHF)

The HPF shift length register (YEE_SHF) is shown in Figure 227 and described in Table 194.

Figure 227. HPF Shift Length Register (YEE_SHF)

15	4	3	0
Reserved		SHF	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 194. HPF Shift Length Register (YEE_SHF) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved.
3-0	SHF	0-Fh	HPF shift length. Down shift length of high pass filter (HPF) in edge enhancer.

6.3.73 HPF Coefficient 00 Register (YEE_MUL_00)

The HPF coefficient 00 register (YEE_MUL_00) is shown in Figure 228 and described in Table 195.

Figure 228. HPF Coefficient 00 Register (YEE_MUL_00)

15	10	9	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

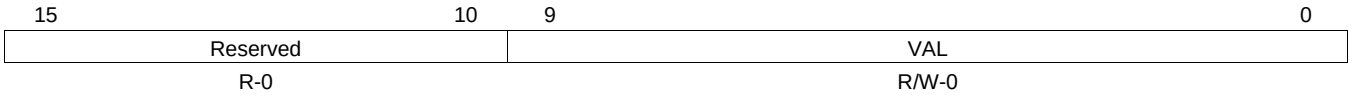
Table 195. HPF Coefficient 00 Register (YEE_MUL_00) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 00. Value is in S10Q0.

6.3.74 HPF Coefficient 01 Register (YEE_MUL_01)

The HPF coefficient 01 register (YEE_MUL_01) is shown in Figure 229 and described in Table 196.

Figure 229. HPF Coefficient 01 Register (YEE_MUL_01)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

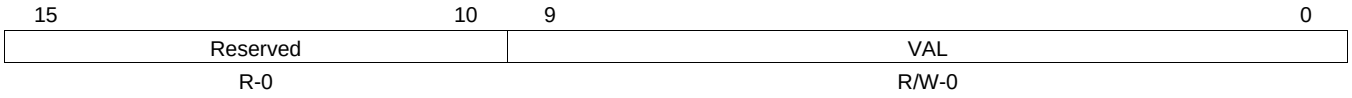
Table 196. HPF Coefficient 01 Register (YEE_MUL_01) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 01. Value is in S10Q0.

6.3.75 HPF Coefficient 02 Register (YEE_MUL_02)

The HPF coefficient 02 register (YEE_MUL_02) is shown in Figure 230 and described in Table 197.

Figure 230. HPF Coefficient 02 Register (YEE_MUL_02)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

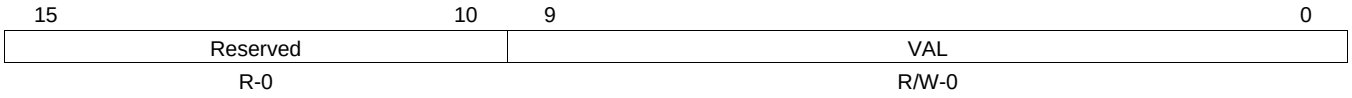
Table 197. HPF Coefficient 02 Register (YEE_MUL_02) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 02. Value is in S10Q0.

6.3.76 HPF Coefficient 10 Register (YEE_MUL_10)

The HPF coefficient 10 register (YEE_MUL_10) is shown in Figure 231 and described in Table 198.

Figure 231. HPF Coefficient 10 Register (YEE_MUL_10)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

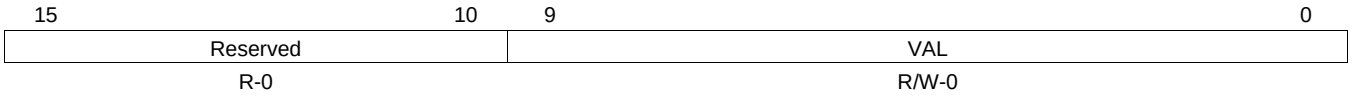
Table 198. HPF Coefficient 10 Register (YEE_MUL_10) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 10. Value is in S10Q0.

6.3.77 HPF Coefficient 11 Register (YEE_MUL_11)

The HPF coefficient 11 register (YEE_MUL_11) is shown in Figure 232 and described in Table 199.

Figure 232. HPF Coefficient 11 Register (YEE_MUL_11)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

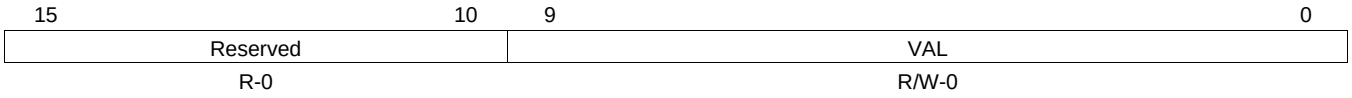
Table 199. HPF Coefficient 11 Register (YEE_MUL_11) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 11. Value is in S10Q0.

6.3.78 HPF Coefficient 12 Register (YEE_MUL_12)

The HPF coefficient 12 register (YEE_MUL_12) is shown in Figure 233 and described in Table 200.

Figure 233. HPF Coefficient 12 Register (YEE_MUL_12)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

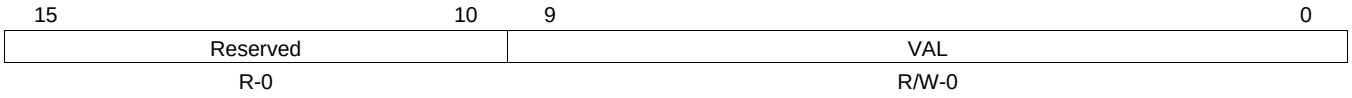
Table 200. HPF Coefficient 12 Register (YEE_MUL_12) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9-0	VAL	0-3FFh	HPF coefficient 12. Value is in S10Q0.

6.3.79 HPF Coefficient 20 Register (YEE_MUL_20)

The HPF coefficient 20 register (YEE_MUL_20) is shown in Figure 234 and described in Table 201.

Figure 234. HPF Coefficient 20 Register (YEE_MUL_20)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 201. HPF Coefficient 20 Register (YEE_MUL_20) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	VAL	0-3FFh	HPF coefficient 20. Value is in S10Q0.

6.3.80 HPF Coefficient 21 Register (YEE_MUL_21)

The HPF coefficient 21 register (YEE_MUL_21) is shown in Figure 235 and described in Table 202.

Figure 235. HPF Coefficient 21 Register (YEE_MUL_21)

15	10	9	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 202. HPF Coefficient 21 Register (YEE_MUL_21) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	VAL	0-3FFh	HPF coefficient 21. Value is in S10Q0.

6.3.81 HPF Coefficient 22 Register (YEE_MUL_22)

The HPF coefficient 22 register (YEE_MUL_22) is shown in Figure 236 and described in Table 203.

Figure 236. HPF Coefficient 22 Register (YEE_MUL_22)

15	10	9	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 203. HPF Coefficient 22 Register (YEE_MUL_22) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	VAL	0-3FFh	HPF coefficient 22. Value is in S10Q0.

6.3.82 Fault Color Suppression Enable Register (FCS_EN)

The fault color suppression enable register (FCS_EN) is shown in Figure 237 and described in Table 204.

Figure 237. Fault Color Suppression Enable Register (FCS_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 204. Fault Color Suppression Enable Register (FCS_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Fault color suppression enable.
		0	Disable.
		1	Enable.

6.3.83 Type selection of HPF Register (FCS_TYP)

The type selection of HPF Register (FCS_TYP) is shown in Figure 238 and described in Table 205.

Figure 238. Type selection of HPF Register (FCS_TYP)

15	3	2	0
Reserved		TYP	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 205. Type selection of HPF Register (FCS_TYP) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2-0	TYP		Type of HPF.
		0	Y.
		1	horizontal HPF.
		2	vertical HPF.
		3	2D HPF.
		4	2D HPF from edge enhancement.

6.3.84 Down Shift Size (HPF) Register (FCS_SHF_Y)

The down shift size (HPF) Register (FCS_SHF_Y) is shown in Figure 239 and described in Table 206.

Figure 239. Down Shift Size (HPF) Register (FCS_SHF_Y)

15	1	0
Reserved	SHF	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 206. Down Shift Size (HPF) Register (FCS_SHF_Y) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved.
1-0	SHF	0-3	Down shift value for HPF

6.3.85 Down Shift Size (GAIN) Register (FCS_SHF_C)

The Down Shift Size (GAIN) Register (FCS_SHF_C) is shown in Figure 240 and described in Table 207.

Figure 240. Down Shift Size (GAIN) Register (FCS_SHF_C)

15	3	2	0
Reserved		SHF	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 207. Down Shift Size (GAIN) Register (FCS_SHF_C) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2-0	SHF	0-7	Down shift value for GAIN function.

6.3.86 Threshold Register (FCS_THR)

The threshold register (FCS_THR) is shown in Figure 241 and described in Table 208.

Figure 241. Threshold Register (FCS_THR)

15	8	7	0
Reserved		THR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 208. Threshold Register (FCS_THR) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved.
8-0	THR	0-1FFh	Threshold of the suppression gain.

6.3.87 Intensity Register (FCS_SGN)

The Intensity Register (FCS_SGN) is shown in Figure 242 and described in Table 209.

Figure 242. Intensity Register (FCS_SGN)

15	8	7	0
Reserved		SGN	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 209. Intensity Register (FCS_SGN) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved.
8-0	SGN	0-1FFh	Intensity of the color suppression.

6.3.88 Lower Limit of Chroma Gain Register (FCS_LTH)

The lower limit of chroma gain register (FCS_LTH) is shown in Figure 243 and described in Table 210.

Figure 243. Lower Limit of Chroma Gain Register (FCS_LTH)

15	9	8	0
Reserved		LIM	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 210. Lower Limit of Chroma Gain Register (FCS_LTH) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	LIM	0-1FFh	Lower limit of chroma gain. Range: 0= LIM =256.

6.3.89 Processing Mode Register (RSZ_SEQ)

The processing mode register (RSZ_SEQ) is shown in Figure 244 and described in Table 211.

Figure 244. Processing Mode Register (RSZ_SEQ)

15	5	4	3	2	1	0
Reserved		CRV	VRV	HRV	TMM	SEQ
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 211. Processing Mode Register (RSZ_SEQ) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved.
4	CRV		Chroma sampling point change.
		0	Chroma sampling point is not changed.
		1	Chroma sampling point is changed from odd-numbered pixels to even-number pixels. The pixel the left end is removed and the pixel at the right end is duplicated.
3	VRV		Vertical reversal of output image.
		0	Processed lines are output in the order of input (normal operation) in vertical direction.
		1	The order of output data is flipped top to bottom.
2	HRV		Horizontal reversal of output image.
		0	Processed pixels are output in the order of input (normal operation) in horizontal direction.
		1	The order of output data is flipped left to right.
1	TMM		Terminal condition of vertical processing.
		0	Output line number confined mode (normal mode). The module continues output of resized image until the number of output lines reaches the value set by RZA_O_VSZ and RZB_O_VSZ.
		1	Input line number confined mode. The modules continues output of resized image until the input number of input lines reads the value set by RZA_I_VSZ and RZB_I_VSZ. The numbers of output lines are output to RZA_V_SIZ_O and RZB_V_SIZ_O.
0	SEQ		Operation mode of vertical processing.
		0	Normal mode. The module clears register values and internal buffer values at VSYNC.
		1	Continuous mode. Resizer holds values from the previous operation. This mode may only be used in combination with input line number confined mode (TMM).

6.3.90 Vertical Anti aliasing Filter Register (RSZ_AAL)

The vertical anti aliasing filter register (RSZ_AAL) is shown in Figure 245 and described in Table 212.

Figure 245. Vertical Anti aliasing Filter Register (RSZ_AAL)

15	1	0
Reserved		AAL
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 212. Vertical Anti aliasing Filter Register (RSZ_AAL) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	AAL		Vertical anti aliasing filter enable.
		0	Disable.
		1	Enable.

6.3.91 Resizer Enable Register (RSZ_EN)

The resizer enable register (RSZ_EN) is shown in Figure 246 and described in Table 213.

Figure 246. Resizer Enable Register (RSZ_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 213. Resizer Enable Register (RSZ_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Resizer enable.
		0	Disable.
		1	Enable.

6.3.92 One Shot Mode Register (RSZ_MODE)

The one shot mode register (RSZ_MODE) is shown in Figure 247 and described in Table 214.

Figure 247. One Shot Mode Register (RSZ_MODE)

15	1	0
Reserved		OST
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 214. One Shot Mode Register (RSZ_MODE) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	OST		One shot mode enable.
		0	Continuous mode.
		1	One shot mode.

6.3.93 Vertical Start Position of the Input Register (RSZ_I_VST)

The Vertical Start Position of the Input Register (RSZ_I_VST) is shown in Figure 248 and described in Table 215.

Figure 248. Vertical Start Position of the Input Register (RSZ_I_VST)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

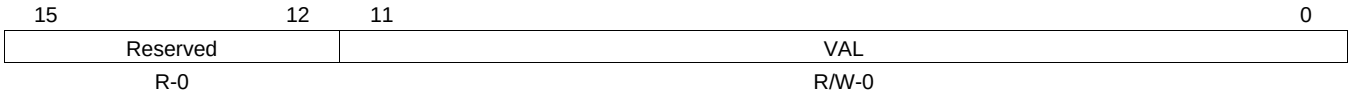
Table 215. Vertical Start Position of the Input Register (RSZ_I_VST) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Vertical start position of image processing. After IPIPE_VST, the VAL line is processed as the first line in each image.

6.3.94 Vertical Size of the Input Register (RSZ_I_VSZ)

The vertical size of the input register (RSZ_I_VSZ) is shown in Figure 249 and described in Table 216.

Figure 249. Vertical Size of the Input Register (RSZ_I_VSZ)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

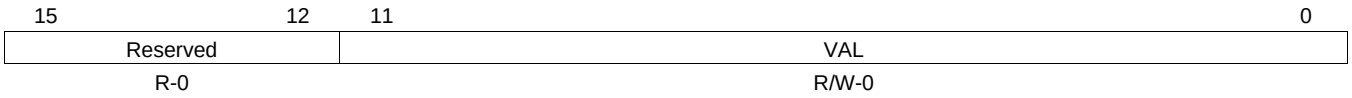
Table 216. Vertical Size of the Input Register (RSZ_I_VSZ) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Number of input lines. This value is used only in input line confined mode. (RSZ_SEQ[TMM] at 0108h). The number of input lines is (VAL + 1).

6.3.95 Horizontal Start Position of the Input Register (RSZ_I_HST)

The horizontal start position of the input register (RSZ_I_HST) is shown in Figure 250 and described in Table 217.

Figure 250. Horizontal Start Position of the Input Register (RSZ_I_HST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 217. Horizontal Start Position of the Input Register (RSZ_I_HST) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Horizontal start position of image processing. (RSZ_I_HST[0] is held low so this value must be even). After IPIPE_HST, the VAL pixel is processed as the first pixel.

6.3.96 Vertical Size of the Output Register (RSZ_O_VSZ)

The vertical size of the output register (RSZ_O_VSZ) is shown in Figure 251 and described in Table 218.

Figure 251. Vertical Size of the Output Register (RSZ_O_VSZ)

15 12	11 0
Reserved	VAL
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 218. Vertical Size of the Output Register (RSZ_O_VSZ) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Vertical size of the output image. The number of output lines is (VAL + 1). (RSZ_O_VSZ[0] is held high so this value must be odd).

6.3.97 Horizontal Start Position of the Output Register (RSZ_O_HST)

The horizontal start position of the output register (RSZ_O_HST) is shown in Figure 252 and described in Table 219.

Figure 252. Horizontal Start Position of the Output Register (RSZ_O_HST)

15 12	11 0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

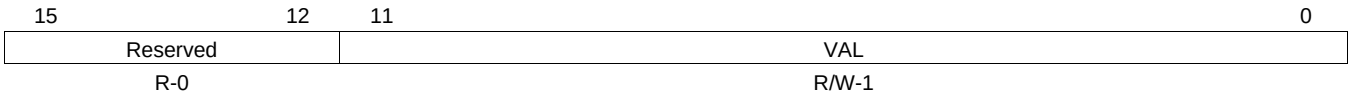
Table 219. Horizontal Start Position of the Output Register (RSZ_O_HST) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Horizontal position of the first pixel to be output in processed image. The first VAL pixels of the resized area in each line are discarded, and the next pixel becomes the first to be output. (RSZ_O_HST[0] is held low so this value must be even).

6.3.98 Horizontal Size of the Output Register (RSZ_O_HSZ)

The horizontal size of the output register (RSZ_O_HSZ) is shown in Figure 253 and described in Table 220.

Figure 253. Horizontal Size of the Output Register (RSZ_O_HSZ)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

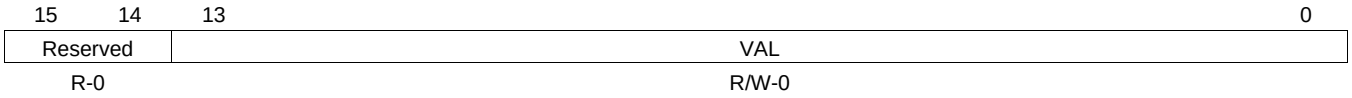
Table 220. Horizontal Size of the Output Register (RSZ_O_HSZ) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Horizontal size of output image. The number of pixel in each line is (VAL + 1). RSZ[0]:Value must be lower than 1344 except in RAW passthu mode. RSZ[1]:Value must be lower than 640. (RSZ_O_HSZ[0] is held high so this value must be odd).

6.3.99 Initial Phase of Vertical Resizing Process Register (RSZ_V_PHS)

The initial phase of vertical resizing process register (RSZ_V_PHS) is shown in Figure 254 and described in Table 221.

Figure 254. Initial Phase of Vertical Resizing Process Register (RSZ_V_PHS)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 221. Initial Phase of Vertical Resizing Process Register (RSZ_V_PHS) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process. (Should be set to zero except in Frame Division Mode-H). Valid range: 0-8191.

6.3.100 Phase of Last Value in Previous Resize Process Register (RSZ_V_PHS_O)

The phase of last value in previous resize process register (RSZ_V_PHS_O) is shown in Figure 255 and described in Table 222.

Figure 255. Phase of Last Value in Previous Resize Process Register (RSZ_V_PHS_O)

15	14	13	0
Reserved		VAL	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 222. Phase of Last Value in Previous Resize Process Register (RSZ_V_PHS_O) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Phase value of the last line in the previous resizing process. This value is only valid in input line number confined mode ((RSZ_SEQ[TMM] at 0x0108).

6.3.101 Vertical Resize Parameter Register (RSZ_V_DIF)

The vertical resize parameter register (RSZ_V_DIF) is shown in Figure 256 and described in Table 223.

Figure 256. Vertical Resize Parameter Register (RSZ_V_DIF)

15	14	13	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

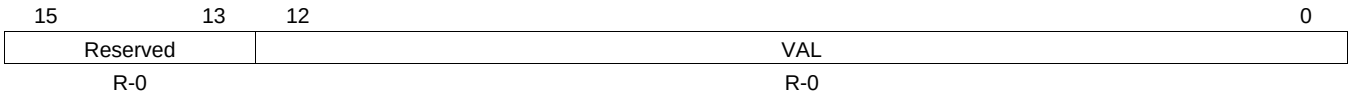
Table 223. Vertical Resize Parameter Register (RSZ_V_DIF) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Vertical resize parameter. The actual resizing ratio is 256/VAL.

6.3.102 Actual Number of Output Lines Register (RSZ_V_SIZ_O)

The actual number of output lines register (RSZ_V_SIZ_O) is shown in Figure 257 and described in Table 224.

Figure 257. Actual Number of Output Lines Register (RSZ_V_SIZ_O)



LEGEND: R = Read only; -*n* = value after reset

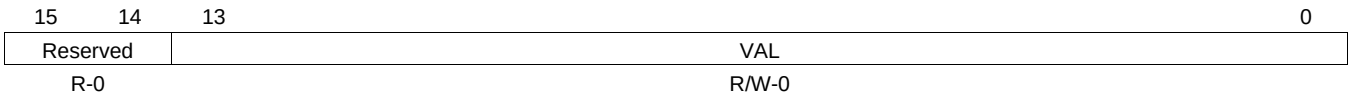
Table 224. Actual Number of Output Lines Register (RSZ_V_SIZ_O) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Number of actually produced lines in the previous resizing process.

6.3.103 Initial Phase of Horizontal Resizing Process Register (RSZ_H_PHS)

The initial phase of horizontal resizing process register (RSZ_H_PHS) is shown in Figure 258 and described in Table 225.

Figure 258. Initial Phase of Horizontal Resizing Process Register (RSZ_H_PHS)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 225. Initial Phase of Horizontal Resizing Process Register (RSZ_H_PHS) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Initial value for the phase value in horizontal resizing process. (Should be set to zero except in Frame Division Mode-V). Valid range: 0-8192.

6.3.104 Horizontal Resize Parameter Register (RSZ_H_DIF)

The horizontal resize parameter register (RSZ_H_DIF) is shown in Figure 259 and described in Table 226.

Figure 259. Horizontal Resize Parameter Register (RSZ_H_DIF)

15	14	13	0
Reserved		VAL	
R-0		R/W-256	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 226. Horizontal Resize Parameter Register (RSZ_H_DIF) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	VAL	0-3FFFh	Horizontal resize parameter. The actual resizing ratio is 256/VAL.

6.3.105 Interpolation Method for Horizontal Rescaling Register (RSZ_H_TYP)

The interpolation method for horizontal rescaling register (RSZ_H_TYP) is shown in Figure 260 and described in Table 227.

Figure 260. Interpolation Method for Horizontal Rescaling Register (RSZ_H_TYP)

15	1	0
Reserved		TYP
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 227. Interpolation Method for Horizontal Rescaling Register (RSZ_H_TYP) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	TYP		Selection of resizing method in horizontal direction.
		0	4-tap cubic convolution.
		1	2-tap linear interpolation.

6.3.106 Selection of Horizontal LPF Intensity Register (RSZ_H_LSE)

The selection of horizontal LPF intensity register (RSZ_H_LSE) is shown in Figure 261 and described in Table 228.

Figure 261. Selection of Horizontal LPF Intensity Register (RSZ_H_LSE)

15	1	0
Reserved		SEL
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 228. Selection of Horizontal LPF Intensity Register (RSZ_H_LSE) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	SEL		Selection of the intensity value for horizontal low pass filtering.
		0	Use an internally calculated value.
		1	Use the value set by the register (RSZ_H_LPF).

6.3.107 Horizontal LPF Intensity Register (RSZ_H_LPF)

The horizontal LPF intensity register (RSZ_H_LPF) is shown in Figure 262 and described in Table 229.

Figure 262. Horizontal LPF Intensity Register (RSZ_H_LPF)

15	8	7	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 229. Horizontal LPF Intensity Register (RSZ_H_LPF) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	VAL	0-FFh	Intensity parameter for horizontal low pass filtering. Used when RZA_H_LSE is high.

6.3.108 RGB Output Enable Register (RSZ_RGB_EN)

The RGB output enable register (RSZ_RGB_EN) is shown in Figure 263 and described in Table 230.

Figure 263. RGB Output Enable Register (RSZ_RGB_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 230. RGB Output Enable Register (RSZ_RGB_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		RGB output enable.
		0	Disable.
		1	Enable.

6.3.109 RGB Output Bit Mode (32 or 16 bit) Register (RSZ_RGB_TYP)

The RGB output bit mode (32 or 16 bit) register (RSZ_RGB_TYP) is shown in Figure 264 and described in Table 231.

Figure 264. RGB Output Bit Mode (32 or 16 bit) Register (RSZ_RGB_TYP)

15	2	1	0
Reserved	MSK1	MSK0	TYP
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

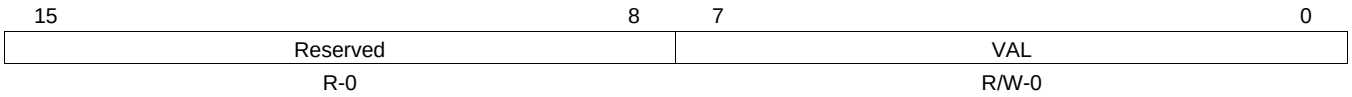
Table 231. RGB Output Bit Mode (32 or 16 bit) Register (RSZ_RGB_TYP) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2	MSK1		Enable masking of the last 2 pixels.
		0	(NOMASK) output the last 2 pixels.
		1	(MASKLAST2) mask the last 2 pixels (do not output).
1	MSK0		Enable masking of the first 2 pixels.
		0	(NOMASK) output the first 2 pixels.
		1	(MASKFIRST2) mask the first 2 pixels (do not output).
0	TYP		16bit/32bit output selection.
		0	(OUTPUT32BITS) 32 bit output; alpha + R + G + B (8 bit each).
		1	(OUTPUT16BITS) 16 bit output; R(5bit) + G(6bit) + B(5bit).

6.3.110 YC422 to YC444 Conversion Method Register (RSZ_RGB_BLD)

The YC422 to YC444 conversion method register (RSZ_RGB_BLD) is shown in Figure 265 and described in Table 232.

Figure 265. YC422 to YC444 Conversion Method Register (RSZ_RGB_BLD)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

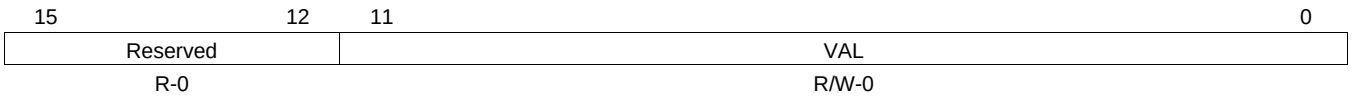
Table 232. YC422 to YC444 Conversion Method Register (RSZ_RGB_BLD) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved.
7-0	VAL	0-FFh	The alpha value used in 32_bit output mode.

6.3.111 SDRAM Base Address MSB Register (RSZ_SDR_BAD_H)

The SDRAM base address MSB register (RSZ_SDR_BAD_H) is shown in Figure 266 and described in Table 233.

Figure 266. SDRAM Base Address MSB Register (RSZ_SDR_BAD_H)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 233. SDRAM Base Address MSB Register (RSZ_SDR_BAD_H) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	The upper 11 bits of the first address in the allowed memory space in buffer memory or SDRAM.

6.3.112 SDRAM Base Address LSB Register (RSZ_SDR_BAD_L)

The SDRAM base address LSB register (RSZ_SDR_BAD_L) is shown in Figure 267 and described in Table 234.

Figure 267. SDRAM Base Address LSB Register (RSZ_SDR_BAD_L)

15	0
VAL	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 234. SDRAM Base Address LSB Register (RSZ_SDR_BAD_L) Field Descriptions

Bit	Field	Value	Description
15-0	VAL	0-FFFFh	The lower 16 bits of the first address in the allowed memory space in buffer memory or SDRAM. In Resize mode, the lowest 2 bits should be 00 when horizontal reversal mode ((RSZ_SEQ[HRV] at 0x0108) is off. These 2 bits should be 11 when horizontal reversal mode is on. In RGB output mode, the lowest 5 bits must be 00000.

6.3.113 SDRAM Start Address MSB Register (RSZ_SDR_SAD_H)

The SDRAM start address MSB register (RSZ_SDR_SAD_H) is shown in Figure 268 and described in Table 235.

Figure 268. SDRAM Start Address MSB Register (RSZ_SDR_SAD_H)

15	12	11	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

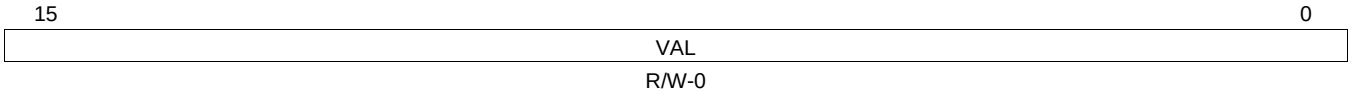
Table 235. SDRAM Start Address MSB Register (RSZ_SDR_SAD_H) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	The higher 11 bits of the first address of output in buffer memory or SDRAM.

6.3.114 SDRAM Start Address LSB Register (RSZ_SDR_SAD_L)

The SDRAM start address LSB register (RSZ_SDR_SAD_L) is shown in Figure 269 and described in Table 236.

Figure 269. SDRAM Start Address LSB Register (RSZ_SDR_SAD_L)



LEGEND: R/W = Read/Write; -*n* = value after reset

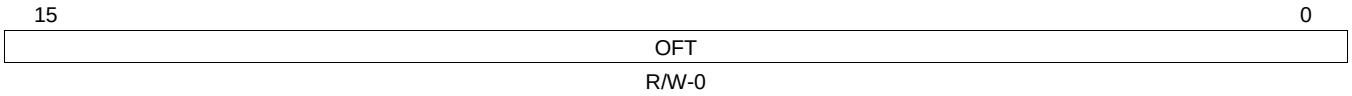
Table 236. SDRAM Start Address LSB Register (RSZ_SDR_SAD_L) Field Descriptions

Bit	Field	Value	Description
15-0	VAL	0-FFFFh	The lower 16 bits of the first address of output in buffer memory or SDRAM. In Resize mode, The lowest 2 bits should be 00 when horizontal reversal mode (RSZ_SEQ[HRV] at 0x0108) is off. These 2 bits should be 11 when horizontal reversal mode is on. In RGB output mode, the lowest 5 bits must be 00000.

6.3.115 SDRAM Line Offset Register (RSZ_SDR_OFT)

The SDRAM line offset register (RSZ_SDR_OFT) is shown in Figure 270 and described in Table 237.

Figure 270. SDRAM Line Offset Register (RSZ_SDR_OFT)



LEGEND: R/W = Read/Write; -*n* = value after reset

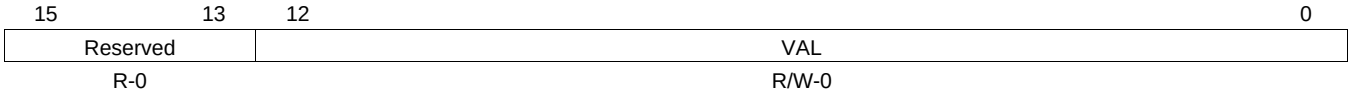
Table 237. SDRAM Line Offset Register (RSZ_SDR_OFT) Field Descriptions

Bit	Field	Value	Description
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes). The first address of each output line should be SAD+(line+OFT). Examples are shown below. line 0: address = SAD + (0 × OFT) line 1: address = SAD + (1 × OFT) line 2: address = SAD + (2 × OFT) line 3: address = SAD + (3 × OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.3.116 Start Line of SDRAM Pointer Register (RSZ_SDR_PTR_S)

The start line of SDRAM pointer register (RSZ_SDR_PTR_S) is shown in Figure 271 and described in Table 238.

Figure 271. Start Line of SDRAM Pointer Register (RSZ_SDR_PTR_S)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 238. Start Line of SDRAM Pointer Register (RSZ_SDR_PTR_S) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when RZA_SAD=RZA_BAD. In RGB output mode, this value should be multiple of 4 (the lowest two bits be 00).

6.3.117 End Line of SDRAM Pointer Register (RSZ_SDR_PTR_E)

The end line of SDRAM pointer register (RSZ_SDR_PTR_E) is shown in Figure 272 and described in Table 239.

Figure 272. End Line of SDRAM Pointer Register (RSZ_SDR_PTR_E)

15 13	12 0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 239. End Line of SDRAM Pointer Register (RSZ_SDR_PTR_E) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL = 0x0003h line 0: address = SAD + (0 × OFT) line 1: address = SAD + (1 × OFT) line 2: address = SAD + (2 × OFT) line 3: address = SAD + (3 × OFT) line 4: address = SAD + (0 × OFT) <= (Returned to the first address) line 5: address = SAD + (1 × OFT) line 6: address = SAD + (2 × OFT) line 7: address = SAD + (3 × OFT) line 8: address = SAD + (0 × OFT) <= (Returned to the first address) line 9: address = SAD + (1 × OFT) line 10: address = SAD + (2 × OFT) line 11: address = SAD + (3 × OFT) In RGB output mode, this value should be multiple of 4 (the lowest two bits be 00) to ensure that the end of SDRAM region is aligned with line size.

6.3.118 Output of Current Pointer Value (Read Only) Register (RSZ_SDR_PTR_O)

The output of current pointer value (read only) register (RSZ_SDR_PTR_O) is shown in Figure 273 and described in Table 240.

Figure 273. Output of Current Pointer Value (Read Only) Register (RSZ_SDR_PTR_O)

15 13	12 0
Reserved	VAL
R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 240. Output of Current Pointer Value (Read Only) Register (RSZ_SDR_PTR_O) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Vertical position of the last line of the previous resizing process in the memory space. This value is not valid in RGB output mode.

6.3.119 Boxcar Enable Register (BOX_EN)

The boxcar enable register (BOX_EN) is shown in Figure 274 and described in Table 241.

Figure 274. Boxcar Enable Register (BOX_EN)

15 1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 241. Boxcar Enable Register (BOX_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Boxcar enable.
		0	Disable.
		1	Enable.

6.3.120 One Shot Mode Register (BOX_MODE)

The one shot mode register (BOX_MODE) is shown in Figure 275 and described in Table 242.

Figure 275. One Shot Mode Register (BOX_MODE)

15	1	0
Reserved		OST
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 242. One Shot Mode Register (BOX_MODE) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	OST		One shot mode enable.
		0	Continuous mode.
		1	One shot mode.

6.3.121 Block Size (16 x 16 or 8 x 8) Register (BOX_TYP)

The block size (16 × 16 or 8 × 8) register (BOX_TYP) is shown in Figure 276 and described in Table 243.

Figure 276. Block Size (16x16 or 8x8) Register (BOX_TYP)

15	1	0
Reserved		SEL
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 243. Block Size (16x16 or 8x8) Register (BOX_TYP) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	SEL		Block size in boxcar sampling.
		0	8 × 8
		1	16 × 16

6.3.122 Down Shift Value of Input Register (BOX_SHF)

The down shift value of input register (BOX_SHF) is shown in Figure 277 and described in Table 244.

Figure 277. Down Shift Value of Input Register (BOX_SHF)

15	3	2	0
Reserved		VAL	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 244. Down Shift Value of Input Register (BOX_SHF) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2-0	VAL	0-7	Down shift value of input data (range: 0-4).

6.3.123 Histogram Enable Register (HST_EN)

The histogram enable register (HST_EN) is shown in Figure 278 and described in Table 245.

Figure 278. Histogram Enable Register (HST_EN)

15	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

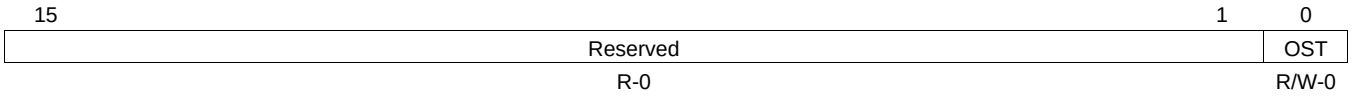
Table 245. Histogram Enable Register (HST_EN) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EN		Histogram enable.
		0	Disable.
		1	Enable.

6.3.124 One Shot Mode Register (HST_MODE)

The one shot mode register (HST_MODE) is shown in Figure 279 and described in Table 246.

Figure 279. One Shot Mode Register (HST_MODE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

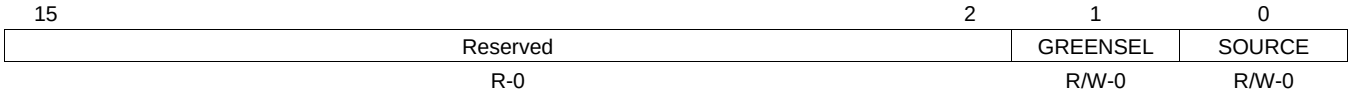
Table 246. One Shot Mode Register (HST_MODE) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	OST		One shot mode enable.
		0	Continuous mode.
		1	One shot mode.

6.3.125 Histogram Source Select Register (HST_SEL)

The histogram source select register (HST_SEL) is shown in Figure 280 and described in Table 247.

Figure 280. Histogram Source Select Register (HST_SEL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 247. Histogram Source Select Register (HST_SEL) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved.
1	GREENSEL		Green sampling selection.
		0	Gr is collected.
		1	Gb is collected.
0	SOURCE		Input selection.
		0	From horizontal defect correction (R/Gr/Gb/B).
		1	From RGB2YUV (RGB input + Y output).

6.3.126 Histogram Parameters Select Register (HST_PARA)

The histogram parameters select register (HST_PARA) is shown in Figure 281 and described in Table 248.

Figure 281. Histogram Parameters Select Register (HST_PARA)

15	14	13	12	11	8	7	6	5	4	3	2	1	0
Reserved		BIN		SHF		COL3	COL2	COL1	COL0	RGN3	RGN2	RGN1	RGN0
R-0		R/W-0		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

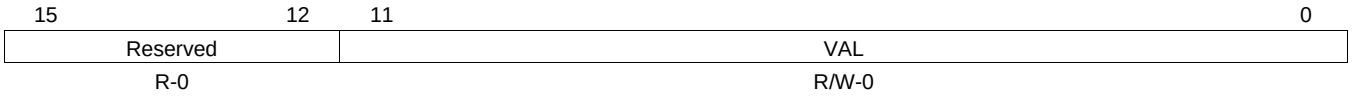
Table 248. Histogram Parameters Select Register (HST_PARA) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-12	BIN		Number of bins.
		0	32 bins.
		1	64 bins.
		2	128 bins.
		3	256 bins.
11-8	SHF	0-Fh	Shift length of input data.
7	COL3		Color 3 enable.
		0	Disable.
		1	Enable.
6	COL2		Color 2 enable.
		0	Disable.
		1	Enable.
5	COL1		Color 1 enable.
		0	Disable.
		1	Enable.
4	COL0		Color 0 enable.
		0	Disable.
		1	Enable.
3	RGN3		Region 3 enable.
		0	Disable.
		1	Enable.
2	RGN2		Region 2 enable.
		0	Disable.
		1	Enable.
1	RGN1		Region 1 enable.
		0	Disable.
		1	Enable.
0	RGN0		Region 0 enable.
		0	Disable.
		1	Enable.

6.3.127 Vertical Start Position Register (HST_VST)

The vertical start position register (HST_VST) is shown in Figure 282 and described in Table 249.

Figure 282. Vertical Start Position Register (HST_VST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

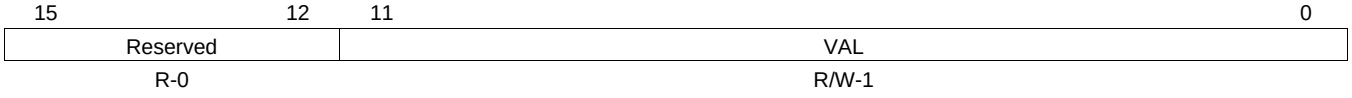
Table 249. Vertical Start Position Register (HST_VST) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Vertical start position of the region from the IPIPE_VST. The region will start the Histogram processing from VAL line. (HST_VST[0] is held low so this value must be even).

6.3.128 Vertical Size Register (HST_VSZ)

The vertical size register (HST_VSZ) is shown in Figure 283 and described in Table 250.

Figure 283. Vertical Size Register (HST_VSZ)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

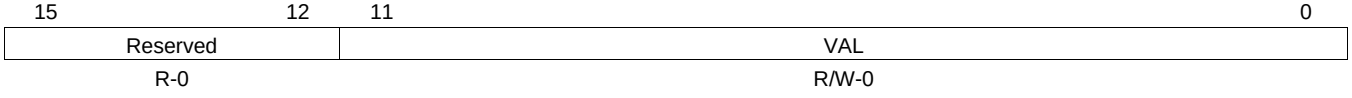
Table 250. Vertical Size Register (HST_VSZ) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Vertical size of the region. This value must be greater than 0. (0 is not allowed). The Histogram processing of the region will process (VAL + 1) lines. (HST_VSZ[0] is held high so this value must be odd).

6.3.129 Horizontal Start Position Register (HST_HST)

The horizontal start position register (HST_HST) is shown in Figure 284 and described in Table 251.

Figure 284. Horizontal Start Position Register (HST_HST)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 251. Horizontal Start Position Register (HST_HST) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-0	VAL	0-FFFh	Horizontal start position of the region from the IPIPE_HST. The region will start the "Histogram" processing from VAL pixel. (HST_HST[0] is held low so this value must be even).

6.3.130 Horizontal Size Register (HST_HSZ)

The horizontal size register (HST_HSZ) is shown in Figure 285 and described in Table 252.

Figure 285. Horizontal Size Register (HST_HSZ)

15	12	11	0
Reserved		VAL	
R-0		R/W-1	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 252. Horizontal Size Register (HST_HSZ) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved. Read as zero.
11-0	VAL	0-FFFh	Horizontal size of the region This value must be greater than 0. (0 is not allowed). The "Histogram" processing of the region will process (VAL + 1) pixels. HST_HSZ[0] is held high so this value must be odd.

6.4 Hardware 3A Registers (H3A)

The Hardware 3A Registers (H3A) are shown in Table 253.

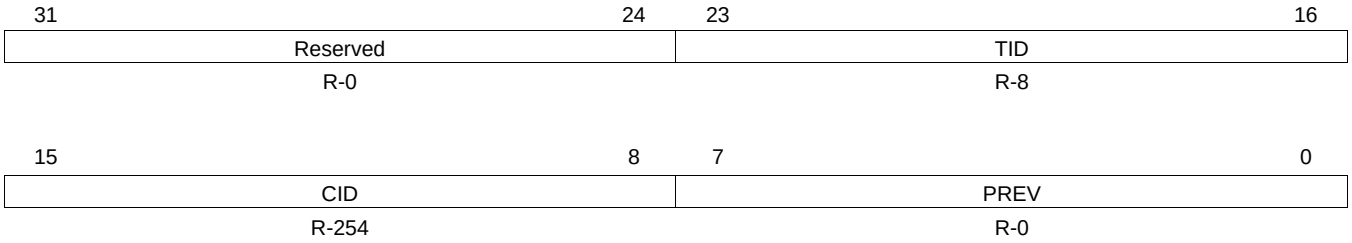
Table 253. Hardware 3A Register Map (H3A)

Address	Acronym	Register Description	Section
0x01C7:0080	PID	Peripheral Revision and Class Information	Section 6.4.1
0x01C7:0084	PCR	Peripheral Control Register	Section 6.4.2
0x01C7:0088	AFPAX1	Setup for the AF Engine Paxel Configuration	Section 6.4.3
0x01C7:008C	AFPAX2	Setup for the AF Engine Paxel Configuration	Section 6.4.4
0x01C7:0090	AFPAXSTART	Start Position for AF Engine Paxels	Section 6.4.5
0x01C7:0094	AFIIRSH	Start Position for IIRSH	Section 6.4.6
0x01C7:0098	AFBUFST	SDRAM/DDRAM Start Address for AF Engine	Section 6.4.7
0x01C7:009C	AFCOEF010	IIR Filter Coefficient Data for SET 0	Section 6.4.8
0x01C7:00A0	AFCOEF032	IIR Filter Coefficient Data for SET 0	Section 6.4.9
0x01C7:00A4	AFCOEFF054	IIR Filter Coefficient Data for SET 0	Section 6.4.10
0x01C7:00A8	AFCOEFF076	IIR Filter Coefficient Data for SET 0	Section 6.4.11
0x01C7:00AC	AFCOEFF098	IIR Filter Coefficient Data for SET 0	Section 6.4.12
0x01C7:00B0	AFCOEFF0010	IIR Filter Coefficient Data for SET 0	Section 6.4.13
0x01C7:00B4	AFCOEF110	IIR Filter Coefficient Data for SET 1	Section 6.4.14
0x01C7:00B8	AFCOEF132	IIR Filter Coefficient Data for SET 1	Section 6.4.15
0x01C7:00BC	AFCOEFF154	IIR Filter Coefficient Data for SET 1	Section 6.4.16
0x01C7:00C0	AFCOEFF176	IIR Filter Coefficient Data for SET 1	Section 6.4.17
0x01C7:00C4	AFCOEFF198	IIR Filter Coefficient Data for SET 1	Section 6.4.18
0x01C7:00C8	AFCOEFF1010	IIR Filter Coefficient Data for SET 1	Section 6.4.19
0x01C7:00CC	AEWWIN1	Configuration for AE/AWB Windows	Section 6.4.20
0x01C7:00D0	AEWINSTART	Start Position for AE/AWB Windows	Section 6.4.21
0x01C7:00D4	AEWINBLK	Start Position and Height for Black Line of AE/AWB Windows	Section 6.4.22
0x01C7:00D8	AEWSUBWIN	Configuration for Subsample Data in AE/AWB Window	Section 6.4.23
0x01C7:00DC	AEWBUFST	SDRAM/DDRAM Start Address for AE/AWB Engine Output Data	Section 6.4.24
0x01C7:00E0	RSDR_ADDR	SDRAM/DDRAM Read Address	Section 6.4.25
0x01C7:00E4	RADR_OFFSET	SDRAM/DDRAM Line Offset	Section 6.4.26
0x01C7:00E8	SDR_FRSIZE	Frame Size for SDRAM Read Data	Section 6.4.27

6.4.1 Peripheral Revision and Class Information Register (PID)

The peripheral ID register (PID) is shown in Figure 286 and described in Table 254.

Figure 286. Peripheral Revision and Class Information Register (PID)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 254. Peripheral ID Register (PID) Field Description

Bit	Field	Value	Description
31-24	Reserved	0	Reserved. Read as zero.
23-16	TID	0-FFh	Peripheral Identification H3A (AF, AE, and AWB)
15-8	CID	0-FFh	Class Identification VPFE module
7-0	PREV	0-FFh	Peripheral Revision Number Initial Revision

6.4.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 287 and described in Table 255.

Figure 287. Peripheral Control Register (PCR)

31	24
AVE2LMT	
R/W-1023	

23	22	21	2 0	19	18	17	16
AVE2LMT		SDR_FETCH_EN	INP_WIDTH	INP_SRC	BUSYAEAWB	AEW_ALAW_EN	AEW_EN
R/W-1023		R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

15	14	13	11	10	8
BUSYAF	FVMODE	RGBPOS		MED_TH	
R-0	R/W-0	R/W-0		R/W-255	

7	3	2	1	0
MED_TH		AF_MED_EN	AF_ALAW_EN	AF_EN
R/W-255		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 255. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-22	AVE2LMT	0-7Fh	AE/AWB Saturation Limit This is the value that all sub sampled pixels in the AE/AWB engine are compared to. If the data is greater or equal to this data then the block is considered saturated.
21	SDR_FETCH_EN		SDRAM Fetch Enable This bit is used in SDRAM input mode. Set to 1 to begin SDRAM fetch for a frame. Upon completion of frame, it is self-cleared to zero and must then be set to 1 again to initiate the processing of another frame.
		0	SDRAM fetch is not active
		1	Start SDRAM Fetch for 1 frame
20	INP_WIDTH		Input Width
		0	8-bit packed data (4 pix/ 32 bits)
		1	10-bit data (2 pix/32 bits)
19	INP_SRC		Input Source
		0	CCDC (sensor) input
		1	SDRAM input
18	BUSYAEAWB	0-1	Busy bit for AE/AWB
17	AEW_ALAW_EN		AE/AWB A-law Enable
		0	Disable AE/AWB A-law table
		1	Enable AE/AWB A-law table
16	AEW_EN		AE/AWB Enable
		0	Disable AE/AWB Engine
		1	Enable AE/AWB Engine
15	BUSYAF	0-1	Busy bit for AF

Table 255. Peripheral Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description
14	FVMODE		Focus Value Accumulation Mode
		0	Sum Mode
		1	Peak Mode
13-11	RGBPOS		Red, Green, and blue pixel location in the AF windows
		0	GR and GB as Bayer pattern
		1	RG and GB as Bayer pattern
		2	GR and BG as Bayer pattern
		3	RG and BG as Bayer pattern
		4	GG and RB as custom pattern
		5	RB and GG as custom pattern
10-3	MED_TH	0-FFh	Median filter threshold
2	AF_MED_EN		Auto Focus Median filter Enable If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not in the valid region. Therefore the paxel start/end and IIR filter start positions should not be set within the 1st and last 2 pixels.
		0	Disable Auto Focus median filter
		1	Enable Auto Focus median filter
1	AF_ALAW_EN		Auto Focus A-law table Enable
		0	Disable Auto Focus A-law table
		1	Enable Auto Focus A-law table
0	AF_EN		Auto Focus Enable
		0	Disable Auto Focus Engine
		1	Enable Auto Focus Engine

6.4.3 Setup for the AF Engine Paxel Configuration Register (AFPAX1)

The AF engine paxel configuration register (AFPAX1) is shown in Figure 288 and described in Table 256.

Figure 288. Setup for the AF Engine Paxel Configuration Register (AFPAX1)

31	23	22	16
Reserved		PAXW	
R-0		R/W-0	

15	7	6	0
Reserved		PAXH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 256. Setup for the AF Engine Paxel Configuration Register (AFPAX1) Field Descriptions

Bit	Field	Value	Description
31-23	Reserved	0	Reserved. Read as zero.
22-16	PAXW	0-7Fh	AF Engine Paxel Width The width of the paxel is the value of this register plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
15-7	Reserved	0	Reserved. Read as zero.
6-0	PAXH	0-7Fh	AF Engine Paxel Height The height of the paxel is the value of this register plus 1 multiplied by 2 with a final value of 2-256 (even)

6.4.4 Setup for the AF Engine Paxel Configuration Register (AFPAX2)

The setup for the AF engine paxel configuration register (AFPAX2) is shown in Figure 289 and described in Table 257.

Figure 289. Setup for the AF Engine Paxel Configuration Register (AFPAX2)

31	17	16
Reserved		AFINCV
R-0		R/W-0

15	13	12	6	5	0
AFINCV		PAXVC		PAXHC	
R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 257. Setup for the AF Engine Paxel Configuration Register (AFPAX2) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved. Read as zero.
16-13	AFINCV	0-Fh	AF Engine Line Increments Number of lines to increment in a Paxel plus 1 multiplied by 2. Incrementing the line in a paxel is always done on a line pair due to the fact that the RGB pattern falls in two lines. If all the lines are to be processed, this field should be set to zero, and thus line count is incremented by 2 following a line pair. Thus, the number of lines that can be skipped between two processed line pairs is 0-30 (even). The starting two lines in a paxel are first processed before this field is applied.
12-6	PAXVC	0-7Fh	AF Engine Vertical Paxel Count The number of paxels in the vertical direction plus 1. The maximum number of vertical paxels in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	PAXHC	0-3Fh	AF Engine Horizontal Paxel Count The number of paxels in the horizontal direction plus 1. It is illegal to set a number that is greater than 35 (total of 36 paxels in the horizontal direction).

6.4.5 Start Position for AF Engine Paxels Register (AFPAXSTART)

The start position for AF engine paxels register (AFPAXSTART) is shown in Figure 290 and described in Table 258.

Figure 290. Start Position for AF Engine Paxels Register (AFPAXSTART)

31	28	27	16
Reserved		PAXSH	
R-0		R/W-0	

15	12	11	0
Reserved		PAXSV	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 258. Start Position for AF Engine Paxels Register (AFPAXSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	PAXSH	0-FFFh	AF Engine Paxel Horizontal Start Position Range: 2-4094 PAXSH must be equal to or greater than IIRSH + 2 (must be even).
15-12	Reserved	0	Reserved. Read as zero.
11-0	PAXSV	0-FFFh	AF Engine Paxel Vertical Start Position Range: 0-4095 Sets the vertical line for the first paxel.

6.4.6 Start Position for IIRSH Register (AFIIRSH)

The start position for IIRSH register (AFIIRSH) is shown in Figure 291 and described in Table 259.

Figure 291. Start Position for IIRSH Register (AFIIRSH)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		IIRSH	
R-0		R/W-0	

LEGEND: R = Read only; -*n* = value after reset

Table 259. Start Position for IIRSH Register (AFIIRSH) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved. Read as zero.
11-0	INITX	0-FFFh	AF Engine IIR Horizontal Start Position Range: 0-4094 When the horizontal position of a line equals this value, the shift registers are cleared on the next pixel (must be even).

6.4.7 SDRAM/DDRAM Start Address for AF Engine Register (AFBUFST)

The SDRAM/DDRAM start address for AF engine register (AFBUFST) is shown in Figure 292 and described in Table 260.

Figure 292. SDRAM/DDRAM Start Address for AF Engine Register (AFBUFST)

31	0
AFBUST	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 260. SDRAM/DDRAM Start Address for AF Engine Register (AFBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AFBUST	0-FFFF FFFFh	AF Engine SDRAM/DDRAM Start Address The starting location in the SDRAM/DDRAM. The 6 LSB are ignored, address should be on a 64-byte boundary **Note**: This field can be altered even when the AF is busy. Change will take place only for the next frame. However, reading this register will always give the latest value.

6.4.8 IIR Filter Coefficient Data for SET 0 Register (AFCOEF010)

The IIR filter coefficient data for SET 0 register (AFCOEF010) is shown in Figure 293 and described in Table 261.

Figure 293. IIR Filter Coefficient Data for SET 0 Register (AFCOEF010)

31	28	27	16
Reserved		COEFF1	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF0	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 261. IIR Filter Coefficient Data for SET 0 Register (AFCOEF010) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF1	0-FFFh	AF Engine IIR Filter Coefficient #1 (Set 0) The range is signed -32 ≤ value ≤ 31 + 63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF0	0-FFFh	AF Engine IIR Filter Coefficient #0 (Set 0) The range is signed -32 ≤ value ≤ 31 + 63/64

6.4.9 IIR Filter Coefficient Data for Set 0 Register (AFCOEF032)

The IIR filter coefficient data for Set 0 register (AFCOEF032) is shown in Figure 294 and described in Table 262.

Figure 294. IR Filter Coefficient Data for Set 0 Register (AFCOEF032)

31	28	27	16
Reserved		COEFF3	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF2	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 262. IR Filter Coefficient Data for Set 0 Register (AFCOEF032) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF3	0-FFFh	AF Engine IIR filter Coefficient #3 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.

Table 262. IR Filter Coefficient Data for Set 0 Register (AFCOEF032) Field Descriptions (continued)

Bit	Field	Value	Description
11-0	COEFF2	0-FFFh	AF Engine IIR filter Coefficient #2 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64

6.4.10 IIR Filter Coefficient Data for SET 0 Register (AFCOEFF054)

The IIR filter coefficient data for SET 0 register (AFCOEFF054) is shown in Figure 295 and described in Table 263.

Figure 295. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF054)

31	28	27	16
Reserved		COEFF5	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF4	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 263. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF054) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF5	0-3FFFh	AF Engine IIR filter Coefficient #5 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF4	0-3FFFh	AF Engine IIR filter Coefficient #4 (Set 0) The range is signed -32 ≤ value ≤31 +63/64

6.4.11 IIR Filter Coefficient Data for SET 0 Register (AFCOEFF076)

The IIR filter coefficient data for SET 0 register (AFCOEFF076) is shown in Figure 296 and described in Table 264.

Figure 296. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF076)

31	28	27	16
Reserved		COEFF7	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF6	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 264. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF076) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF7	0-FFFh	AF Engine IIR filter Coefficient #7 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF6	0-FFFh	AF Engine IIR filter Coefficient #6 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64

6.4.12 IIR Filter Coefficient Data for SET 0 Register (AFCOEFF098)

The IIR filter coefficient data for SET 0 register (AFCOEFF098) is shown in Figure 297 and described in Table 265.

Figure 297. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF098)

31	28	27	16
Reserved		COEFF9	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF8	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 265. Lens Center (LD) Register (CENTER) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF9	0-FFFh	AF Engine IIR filter Coefficient #9 (Set 0) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF8	0-FFFh	AF Engine IIR filter Coefficient #8 (Set 0) The range is signed -32 ≤ value ≤31 +63/64

6.4.13 IIR Filter Coefficient Data for SET 0 Register (AFCOEFF0010)

The IIR filter coefficient data for SET 0 register (AFCOEFF0010) is shown in Figure 298 and described in Table 266.

Figure 298. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF0010)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		COEFF10	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 266. IIR Filter Coefficient Data for SET 0 Register (AFCOEFF0010) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF10	0-FFFh	AF Engine IIR filter Coefficient #10 (Set 0) The range is signed -32 ≤ value ≤31 + 63/64

6.4.14 IIR Filter Coefficient Data for SET 1 Register (AFCOEF110)

The IIR filter coefficient data for SET 1 register (AFCOEF110) is shown in Figure 299 and described in Table 267.

Figure 299. IIR Filter Coefficient Data for SET 1 Register (AFCOEF110)

31	28	27	16
Reserved		COEFF1	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF0	
R-0		R/W-0	

LEGEND: R = Read only; -*n* = value after reset

Table 267. IIR Filter Coefficient Data for SET 1 Register (AFCOEF110) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF1	0-FFFh	AF Engine IIR Filter Coefficient #1(Set 1) The range is signed -32 ≤ value ≤ 31 + 63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF0	0-FFFh	AF Engine IIR Filter Coefficient #0 (Set 1) The range is signed -32 ≤ value ≤ 31 + 63/64

6.4.15 IIR Filter Coefficient Data for SET 1 Register (AFCOEF132)

The IIR filter coefficient data for SET 1 register (AFCOEF132) is shown in Figure 300 and described in Table 268.

Figure 300. IIR Filter Coefficient Data for SET 1 Register (AFCOEF132)

31	28	27	16
Reserved		COEFF3	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF2	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 268. IIR Filter Coefficient Data for SET 1 Register (AFCOEF132) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF3	0-FFFh	AF Engine IIR filter Coefficient #3 (Set 1) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.

Table 268. IIR Filter Coefficient Data for SET 1 Register (AFCOEF132) Field Descriptions (continued)

Bit	Field	Value	Description
11-0	COEFF2	0-FFFh	AF Engine IIR filter Coefficient #2 (Set 1) The range is signed -32 ≤ value ≤ 31 +63/64

6.4.16 IIR Filter Coefficient Data for SET 1 Register (AFCOEFF154)

The IIR filter coefficient data for SET 1 register (AFCOEFF154) is shown in Figure 301 and described in Table 269.

Figure 301. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF154)

31	28	27	16
Reserved		COEFF5	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF4	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 269. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF154) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF5	0-FFFh	AF Engine IIR filter Coefficient #5 (Set 1) The range is signed -32 ≤value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF4	0-FFFh	AF Engine IIR Filter Coefficient #4 (Set 1) The range is signed -32 ≤ value ≤31 +63/64

6.4.17 IIR Filter Coefficient Data for SET 1 Register (AFCOEFF176)

The IIR filter coefficient data for SET 1 register (AFCOEFF176) is shown in Figure 302 and described in Table 270.

Figure 302. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF176)

31	28	27	16
Reserved		COEFF7	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF6	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 270. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF176) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.

Table 270. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF176) Field Descriptions (continued)

Bit	Field	Value	Description
27-16	COEFF7	0-FFFh	AF Engine IIR Filter Coefficient #7 (Set 1) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF6	0-FFFh	AF Engine IIR Filter Coefficient #6 (Set 1) The range is signed -32 ≤ value ≤ 31 +63/64

6.4.18 IIR Filter Coefficient Data for SET 1 Register (AFCOEFF198)

The IIR filter coefficient data for SET 1 register (AFCOEFF198) is shown in Figure 303 and described in Table 271.

Figure 303. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF198)

31	28	27	16
Reserved		COEFF9	
R-0		R/W-0	

15	12	11	0
Reserved		COEFF8	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 271. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF198) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	COEFF9	0-FFFh	AF Engine IIR Filter Coefficient #9 (Set 1) The range is signed -32 ≤ value ≤ 31 +63/64
15-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF8	0-FFFh	AF Engine IIR Filter Coefficient #8 (Set 1) The range is signed -32 ≤ value ≤31 +63/64

6.4.19 IIR Filter Coefficient Data for SET 1 Register (AFCOEFF1010)

The IIR filter coefficient data for SET 1 register (AFCOEFF1010) is shown in Figure 304 and described in Table 272.

Figure 304. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF1010)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		COEFF10	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

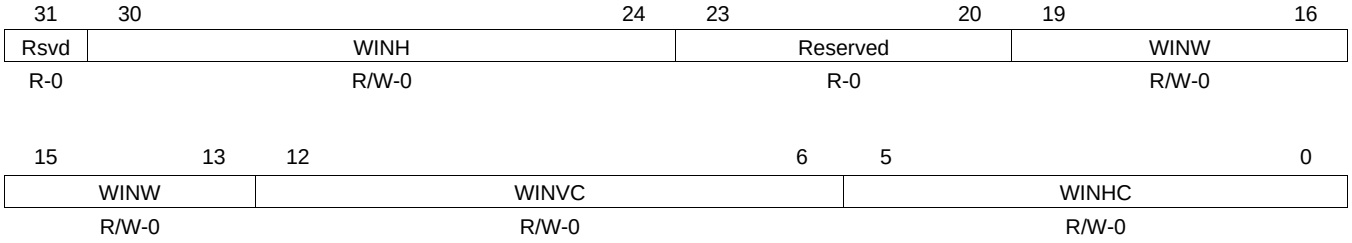
Table 272. IIR Filter Coefficient Data for SET 1 Register (AFCOEFF1010) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved. Read as zero.
11-0	COEFF10	0-FFFh	AF Engine IIR filter Coefficient #10 (Set 1) The range is signed -32 ≤ value ≤31 + 63/64

6.4.20 Configuration for AE/AWB Windows Register (AEWWIN1)

The configuration for AE/AWB windows register (AEWWIN1) is shown in Figure 305 and described in Table 273.

Figure 305. Configuration for AE/AWB Windows Register (AEWWIN1)



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 273. Configuration for AE/AWB Windows Register (AEWWIN1) Field Descriptions

Bit	Field	Value	Description
31	Reserved	0	Reserved. Read as zero.
30-24	WINH	0-7Fh	AE/AWB Engine Window Height This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-256 (even).
23-20	Reserved	0	Reserved. Read as zero.
19-13	WINW	0-7Fh	AE/AWB Engine Window Width This specifies the window width in an even number of pixels, the window width is the value plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
12-6	WINVC	0-7Fh	AE/AWB Engine Vertical Window Count The number of windows in the vertical direction plus 1. The maximum number of vertical windows in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	WINHC	0-3Fh	AE/AWB Engine Horizontal Window Count The number of horizontal windows plus 1. The maximum number of horizontal windows is 35 plus 1 (36). The minimum number of windows should be 2 (valid range for the field is 1-35).

6.4.21 Start Position for AE/AWB Windows Register (AEWINSTART)

The start position for AE/AWB windows register (AEWINSTART) is shown in Figure 306 and described in Table 274.

Figure 306. Start Position for AE/AWB Windows Register (AEWINSTART)

31	28	27	16
Reserved		WINSV	
R-0		R/W-0	

15	12	11	0
Reserved		WINSH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 274. Start Position for AE/AWB Windows Register (AEWINSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position Sets the first line for the first window. Range 0-4095
15-12	Reserved	0	Reserved. Read as zero.
11-0	WINSH	0-FFFh	AE/AWB Engine Horizontal Window Start Position Sets the horizontal position for the first window on each line. Range: 0-4095

6.4.22 Start Position and Height for Black Line of AE/AWB Windows Register (AEWINBLK)

The start position and height for black line of AE/AWB windows register (AEWINBLK) is shown in Figure 307 and described in Table 275.

Figure 307. Start Position and Height for Black Line of AE/AWB Windows Register (AEWINBLK)

31	28	27	16
Reserved		WINSV	
R-0		R/W-0	

15	7	6	0
Reserved		WINH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 275. Start Position and Height for Black Line of AE/AWB Windows Register (AEWINBLK) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved. Read as zero.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position for single black line of windows. Sets the first line for the first window. Range: 0 - 4095 **Note**: the horizontal start and the horizontal number of windows will be similar to the regular windows.
15-7	Reserved	0	Reserved. Read as zero.
6-0	WINH	0-7Fh	AE/AWB Engine Window Height for the single black line of windows. This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2 - 256 (must be even).

6.4.23 Configuration for Subsample Data in AE/AWB Window Register (AEWSUBWIN)

The configuration for subsample data in AE/AWB window register (AEWSUBWIN) is shown in Figure 308 and described in Table 276.

Figure 308. Configuration for Subsample Data in AE/AWB Window Register (AEWSUBWIN)

31	16
Reserved	
R-0	

15 12	11 8	7 4	3 0
Reserved	AEWINCV	Reserved	AEWINCH
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 276. Configuration for Subsample Data in AE/AWB Window Register (AEWSUBWIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved. Read as zero.
11-8	AEWINCV	0-Fh	AE/AWB Engine Vertical Sampling Point Increment Sets vertical distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.
7-4	Reserved	0	Reserved. Read as zero.
3-0	AEWINCH	0-Fh	AE/AWB Engine Horizontal Sampling Point Increment Sets horizontal distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.

6.4.24 SDRAM/DDRAM Start Address for AE/AWB Engine Output Data Register (AEWBUFST)

The SDRAM/DDRAM start address for AE/AWB engine output data register (AEWBUFST) is shown in Figure 309 and described in Table 277.

Figure 309. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data Register (AEWBUFST)

31	0
AEWBUFST	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 277. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data Register (AEWBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AEWBUFST	0-FFFF FFFFh	AE/AWB Engine SDRAM/DDRAM Start Address The starting location in the SDRAM/DDRAM for the AE/AWB data. The 6 LSB are ignored, address should be on a 64-byte boundary **Note**: This field can be altered even when the AE/AWB is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.4.25 SDRAM/DDRAM Read Address for AE/AWB Engine Register (RSDR_ADDR)

The SDRAM/DDRAM read address for AE/AWB engine register (RSDR_ADDR) is shown in Figure 310 and described in Table 278.

Figure 310. SDRAM/DDRAM Read Address for AE/AWB Engine Register (RSDR_ADDR)

31	0
RADR	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

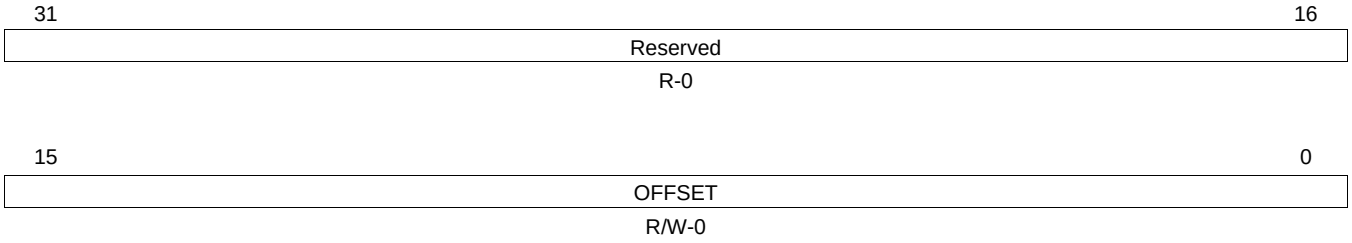
Table 278. SDRAM/DDRAM Read Address for AE/AWB Engine Register (RSDR_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	RADR	0-FFFF FFFFh	Read Address Specifies the initial address of the frame that is to be fetched from SDRAM. The lower 5 bits of this register are always treated as zeroes - the starting address should be 32-byte aligned. **Note**: This field can be altered even when the H3A is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.4.26 Line Offset for the Read Data Register (RADR_OFFSET)

The line offset for the read data register (RADR_OFFSET) is shown in Figure 311 and described in Table 279.

Figure 311. Line Offset for the Read Data Register (RADR_OFFSET)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

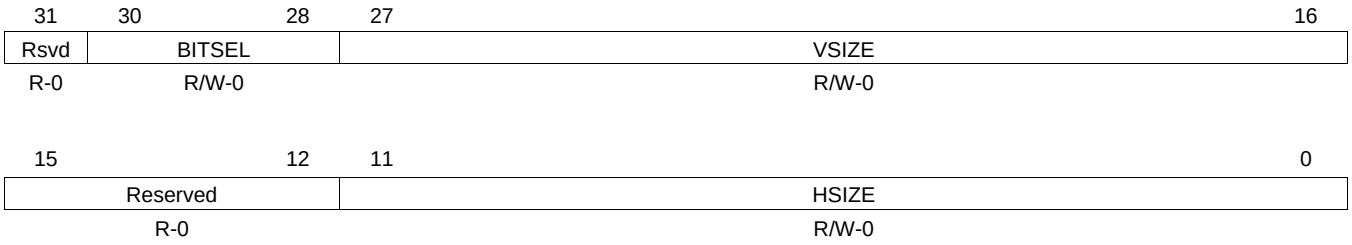
Table 279. Line Offset for the Read Data Register (RADR_OFFSET) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. Read as zero.
15-0	OFFSET	0-FFFFh	Line offset Specifies the offset for each line relative to the previous line. The lower 5 bits of this register are always treated as zeroes - the offset should be 32-byte aligned. **Note**: This field can be altered even when the H3A is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.4.27 Frame Size for SDRAM Read Data Register (SDR_FRSIZE)

The frame size for SDRAM read data register (SDR_FRSIZE) is shown in Figure 312 and described in Table 280.

Figure 312. Frame Size for SDRAM Read Data Register (SDR_FRSIZE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 280. Frame Size for SDRAM Read Data Register (SDR_FRSIZE) Field Descriptions

Bit	Field	Value	Description
31	Reserved	0	Reserved. Read as zero.
30-28	BITSEL		Bit Selection
			10 bits from 16 bit SDRAM word
		0	(BITS9_0) 9:0 from 15:0 input
		1	(BITS10_1) 10:1 from 15:0 input
		2	(BITS11_2) 11:2 from 15:0 input
		3	(BITS12_3) 12:3 from 15:0 input
		4	(BITS13_4) 13:4 from 15:0 input
		5	(BITS14_5) 14:5 from 15:0 input
		6	(BITS15_6) 15:6 from 15:0 input
		7	Reserved
27-16	VSIZE	0-FFFh	Number of lines to fetch from SDRAM for the frame
15-12	Reserved	0	Reserved. Read as zero.
11-0	HSIZE	0-7Fh	Number of pixels to fetch for each line for SDRAM The number of bytes to fetch depends on whether input source is 8-bits or 10-bits.

6.5 VPSS Buffer Logic Registers (VPSSBL)

The VPSS Buffer Logic Registers (VPSSBL) are shown in Table 281.

Table 281. VPSS Buffer Logic Register Map (VPSSBL)

Address	Acronym	Register Description	Section
0x01C7:0800	PID	Peripheral Revision and Class Information	Section 6.5.1
0x01C7:0804	PCR	Peripheral Control Register	Section 6.5.2
0x01C7:080C	INTSTAT	Interrupt Status Register	Section 6.5.3
0x01C7:0810	INTSEL	Interrupt Selection Register	Section 6.5.4
0x01C7:0814	EVTSEL	Event Selection Register	Section 6.5.5
0x01C7:0818	MEMCTRL	Shared Memory Master Select	Section 6.5.6

6.5.1 Peripheral Revision and Class Information Register (PID)

The peripheral revision and class information register (PID) is shown in Figure 313 and described in Table 282.

Figure 313. Peripheral Revision and Class Information Register (PID)

31	24	23	16
Reserved		TID	
R-0		R-1	

15	8	7	0
CID		PREV	
R-251		R-1	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 282. Peripheral ID Register (PID) Field Description

Bit	Field	Value	Description
31-24	Reserved	0	Reserved. Read as zero.
23-16	TID	0-FFh	Peripheral Identification VPSSBL
15-8	CID	0-FFh	Class Identification VPSS module
7-0	PREV	0-FFh	Peripheral Revision N umber Initial Revision

6.5.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 314 and described in Table 283.

Figure 314. Peripheral Control Register (PCR)

31	16
Reserved	
R-0	

15	7	6	5	4	3	2	0
Reserved		WBLCTRL	RBLCTRL		Rsvd	CPRIORITY	
R/W-0		R/W-0	R/W-0		R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 283. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Read as zero.
6	WBLCTRL		Select DDR2/mDDR controller Write Master
		0	IPIPE
		1	Reserved
5-4	RBLCTRL		Select DDR2/mDDR controller Read Master
		0	IPIPEIF
		1	Reserved
		2	H3A
3	Reserved	0	Read as zero.
2-0	CPRIORITY	0-7	Sets Priority of VPSS
			Should be set to highest priority (0) for best performance

6.5.3 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 315 and described in Table 284.

Figure 315. Interrupt Status Register (INTSTAT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved			IPIPE_IN T5	IPIPE_INT4	IPIPE_INT3	IPIPE_INT2	IPIPE_INT1
R-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
IPIPE_INT0	IPIPEIFINT	OSDINT	VENCINT	H3AINT	CCDC_VDINT2	CCDC_VDINT1	CCDC_VDINT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 284. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved. Read as zero.
12	IPIPE_INT5		Set when IPIPE_INT5 is triggered, clear by writing 1.
		1	Clear bit
11	IPIPE_INT4		Set when IPIPE_INT4 is triggered, clear by writing 1.
		1	Clear bit
10	IPIPE_INT3		Set when IPIPE_INT3 is triggered, clear by writing 1.
		1	Clear bit
9	IPIPE_INT2		Set when IPIPE_INT2 is triggered, clear by writing 1.
		1	Clear bit
8	IPIPE_INT1		Set when IPIPE_INT1 is triggered, clear by writing 1.
		1	Clear bit
7	IPIPE_INT0		Set when IPIPE_INT0 is triggered, clear by writing 1.
		1	Clear bit
6	IPIPEIFINT		Set when IPIPEIFINT is triggered, clear by writing 1.
		1	Clear bit
5	OSDINT		Set when OSDINT is triggered, clear by writing 1.
		1	Clear bit
4	VENCINT		Set when VENCINT is triggered, clear by writing 1.
		1	Clear bit
3	H3AINT		Set when H3AINT is triggered, clear by writing 1.
		1	Clear bit
2	CCDC_VDINT2		Set when CCDC_VDINT2 is triggered, clear by writing 1.
		1	Clear bit
1	CCDC_VDINT1		Set when CCDC_VDINT1 is triggered, clear by writing 1.
		1	Clear bit
0	CCDC_VDINT0		Set when CCDC_VDINT0 is triggered, clear by writing 1.
		1	Clear bit

6.5.4 Interrupt Selection Register (INTSEL)

The interrupt selection register (INTSEL) is shown in Figure 316 and described in Table 285.

Figure 316. Interrupt Selection Register (INTSEL)

31 28	27 24	23 20	19 16
INTSEL7	INTSEL6	INTSEL5	INTSEL4
R/W-7	R/W-6	R/W-5	R/W-4

15 12	11 8	7 4	3 0
INTSEL3	INTSEL2	INTSEL1	INTSEL0
R/W-3	R/W-2	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 285. Interrupt Selection Register (INTSEL) Field Descriptions

Bit	Field	Value	Description
31-28	INTSEL7		Selects the interrupt for vpss_int[7]
		0	CCDC VDINT0
		1	CCDC VDINT1
		2	CCDC VDINT2
		3	H3AINT
		4	VENCINT
		5	OSDINT
		6	IPIPEIFINT
		7	IPIPE_INT0_HST
		8	IPIPE_INT1_SDR
		9	IPIPE_INT2_RZA
		10	IPIPE_INT3_RZB
		12	IPIPE_INT5_MMR
27-24	INTSEL6	0-Fh	Selects the interrupt for vpss_int[6]
23-20	INTSEL5	0-Fh	Selects the interrupt for vpss_int[5]
19-16	INTSEL4	0-Fh	Selects the interrupt for vpss_int[4]
15-12	INTSEL3	0-Fh	Selects the interrupt for vpss_int[3]
11-8	INTSEL2	0-Fh	Selects the interrupt for vpss_int[2]
7-4	INTSEL1	0-Fh	Selects the interrupt for vpss_int[1]
3-0	INTSEL1	0-Fh	Selects the interrupt for vpss_int[1]

6.5.5 Event Selection Register (EVTSEL)

The event selection register (EVTSEL) is shown in Figure 317 and described in Table 286.

Figure 317. Event Selection Register (EVTSEL)

31 28	27 24	23 20	19 16
EVTSEL3	EVTSEL2	EVTSEL1	EVTSEL0
R-13	R/W-11	R/W-8	R/W-3

15 4	3 0
Reserved	INTSEL8
R-0	R/W-8

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 286. Event Selection Register (EVTSEL) Field Descriptions

Bit	Field	Value	Description
31-28	EVTSEL3		Selects the event for vpss_evt[3]
		0	CCDC VDINT0
		1	CCDC VDINT1
		2	CCDC VDINT2
		3	H3AINT
		4	VENCINT
		5	OSDINT
		6	IPIPEIFINT
		7	IPIPE_INT0_HST
		8	IPIPE_INT1_SDR
		9	IPIPE_INT2_RZA
		10	IPIPE_INT3_RZB
		12	IPIPE_INT5_MMR
27-24	EVTSEL2	0-Fh	Selects the event for vpss_evt[2]
23-20	EVTSEL1	0-Fh	Selects the event for vpss_evt[1]
19-16	EVTSEL0	0-Fh	Selects the event for vpss_evt[0]
15-4	Reserved	0	Reserved. Read as zero.
3-0	INTSEL8	0-Fh	Selects the interrupt for vpss_int[8]

6.5.6 Shared Memory Master Select Register (MEMCTRL)

The shared memory master select register (MEMCTRL) is shown in Figure 318 and described in Table 287.

Figure 318. Shared Memory Master Select Register (MEMCTRL)

31	16
Reserved	
R-0	

15	3	2	1	0
Reserved		IPIPE_WD_EN	RSZ_CTRL	DFCCTRL
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 287. Shared Memory Master Select Register (MEMCTRL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. Read as zero.
2	IPIPE_WD_EN		IPIPE Write Address Word Enable
			Enable the IPIPE to write to any addresses. When disabled, the IPIPE can only write to 32-byte starting addresses.
		0	Enable
		1	Disable
1	RSZ_CTRL		Resizer Memory Select
		0	IPIPE
		1	Reserved
0	DFCCTRL		Defect Correction Memory Select
		0	IPIPE
		1	CCDC

6.6 VPSS Clock Control Registers (VPSSCLK)

The VPSS Clock Control Registers (VPSSCLK) are shown in Table 288.

Table 288. VPSS Clock Control Register Map (VPSSCLK)

Address	Acronym	Register Description	Section
0x01C7:0000	PID	Peripheral Revision and Class Information	Section 6.6.1
0x01C7:0004	CLKCTRL	VPSS Clock Control Register	Section 6.6.2

6.6.1 Peripheral Revision and Class Information Register (PID)

The peripheral ID register (PID) is shown in Figure 319 and described in Table 289.

Figure 319. Peripheral Revision and Class Information Register (PID)

31	24	23	16
Reserved		TID	
R-0		R-1	

15	8	7	0
CID		PREV	
R-255		R-1	

LEGEND: R = Read only; -*n* = value after reset

Table 289. Peripheral ID Register (PID) Field Description

Bit	Field	Value	Description
31-24	Reserved	0	Reserved. Read as zero.
23-16	TID	0-FFh	Peripheral Identification VPSS
15-8	CID	0-FFh	Class Identification VPSS module
7-0	PREV	0-FFh	Peripheral Revision Number Initial Revision

6.6.2 VPSS Clock Control Register (CLKCTRL)

The VPSS clock control register (CLKCTRL) is shown in Figure 320 and described in Table 290.

Figure 320. VPSS Clock Control Register (CLKCTRL)

31	8
Reserved	
R-0	

7	6	5	4	3	2	1	0
Reserved	CCDC_CLK	IPIPE_CLK	H3A_CLK	Reserved	VENC_CLKSEL	Reserved	VPBE_CLK
R-0	R/W-1	R/W-1	R/W-1	R-0	R/W-0	R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 290. VPSS Clock Control Register (CLKCTRL) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Reserved. Read as zero.
6	CCDC_CLK		CCDC Clock Enable
		0	Clock off
		1	Clock on
5	IPIPE_CLK		IPIPE Clock Enable
		0	Clock off
		1	Clock on
4	H3A_CLK		H3A Clock Enable
		0	Clock off
		1	Clock on
3	Reserved	0	Reserved. Read as zero.
2	VENC_CLKSEL		Select Clock for VENC
		0	enc clk
		1	enc clk/2
1	Reserved	0	Reserved. Read as zero.
0	VPBE_CLK		VPBE Clock Enable
		0	Clock off
		1	Clock on

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