

TMS320DM357 DMSoC General-Purpose Input/Output (GPIO)

User's Guide



Literature Number: SPRUG31A
August 2010

Preface	6
1 Introduction	9
1.1 Purpose of the Peripheral	9
1.2 Features	9
1.3 Functional Block Diagram	9
1.4 Industry Standard(s) Compliance Statement	9
2 Peripheral Architecture	10
2.1 Clock Control	10
2.2 Signal Descriptions	10
2.3 GPIO Register Structure	10
2.4 Using a GPIO Signal as an Output	12
2.5 Using a GPIO Signal as an Input	13
2.6 Reset Considerations	13
2.7 Interrupt Support	14
2.8 EDMA Event Support	16
2.9 Power Management	16
2.10 Emulation Considerations	16
3 Registers	17
3.1 Peripheral Identification Register (PID)	18
3.2 GPIO Interrupt Per-Bank Enable Register (BINTEN)	19
3.3 GPIO Direction Registers (DIR _n)	20
3.4 GPIO Output Data Register (OUT_DATA _n)	21
3.5 GPIO Set Data Register (SET_DATA _n)	22
3.6 GPIO Clear Data Register (CLR_DATA _n)	23
3.7 GPIO Input Data Register (IN_DATA _n)	25
3.8 GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG _n)	27
3.9 GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIG _n)	29
3.10 GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIG _n)	31
3.11 GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG _n)	33
3.12 GPIO Interrupt Status Register (INTSTAT _n)	35
Appendix A Revision History	37

List of Figures

1	GPIO Peripheral Block Diagram.....	10
2	Peripheral Identification Register (PID).....	18
3	GPIO Interrupt Per-Bank Enable Register (BINTEN).....	19
4	GPIO Banks 0 and 1 Direction Register (DIR01)	20
5	GPIO Banks 2 and 3 Direction Register (DIR23)	20
6	GPIO Bank 4 Direction Register (DIR4)	20
7	GPIO Banks 0 and 1 Output Data Register (OUT_DATA01).....	21
8	GPIO Banks 2 and 3 Output Data Register (OUT_DATA23).....	21
9	GPIO Bank 4 Output Data Register (OUT_DATA4)	21
10	GPIO Banks 0 and 1 Set Data Register (SET_DATA01)	22
11	GPIO Banks 2 and 3 Set Data Register (SET_DATA23)	22
12	GPIO Bank 4 Set Data Register (SET_DATA4).....	22
13	GPIO Banks 0 and 1 Clear Data Register (CLR_DATA01).....	23
14	GPIO Banks 2 and 3 Clear Data Register (CLR_DATA23).....	23
15	GPIO Bank 4 Clear Data Register (CLR_DATA4)	23
16	GPIO Banks 0 and 1 Input Data Register (IN_DATA01).....	25
17	GPIO Banks 2 and 3 Input Data Register (IN_DATA23).....	25
18	GPIO Bank 4 Input Data Register (IN_DATA4)	25
19	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (SET_RIS_TRIG01)	27
20	GPIO Banks 2 and 3 Set Rising Edge Interrupt Register (SET_RIS_TRIG23)	27
21	GPIO Bank 4 Set Rising Edge Interrupt Register (SET_RIS_TRIG4).....	27
22	GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG01).....	29
23	GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG23).....	29
24	GPIO Bank 4 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG4)	29
25	GPIO Banks 0 and 1 Set Falling Edge Interrupt Register (SET_FAL_TRIG01)	31
26	GPIO Banks 2 and 3 Set Falling Edge Interrupt Register (SET_FAL_TRIG23)	31
27	GPIO Bank 4 Set Falling Edge Interrupt Register (SET_FAL_TRIG4).....	31
28	GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG01).....	33
29	GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG23).....	33
30	GPIO Bank 4 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG4)	33
31	GPIO Banks 0 and 1 Interrupt Status Register (INTSTAT01)	35
32	GPIO Banks 2 and 3 Interrupt Status Register (INTSTAT23)	35
33	GPIO Bank 4 Interrupt Status Register (INTSTAT4)	35

List of Tables

1	GPIO Register Bits and Banks Associated With GPIO Pins.....	11
2	GPIO Interrupts to the ARM CPU	14
3	GPIO Synchronization Events to the EDMA.....	16
4	General-Purpose Input/Output (GPIO) Registers	17
5	Peripheral Identification Register (PID) Field Descriptions	18
6	GPIO Interrupt Per-Bank Enable Register (BINTEN) Field Descriptions	19
7	GPIO Direction Register (DIR _n) Field Descriptions.....	20
8	GPIO Output Data Register (OUT_DATA _n) Field Descriptions	21
9	GPIO Set Data Register (SET_DATA _n) Field Descriptions.....	22
10	GPIO Clear Data Register (CLR_DATA _n) Field Descriptions	24
11	GPIO Input Data Register (IN_DATA _n) Field Descriptions	26
12	GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG _n) Field Descriptions	28
13	GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIG _n) Field Descriptions	30
14	GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIG _n) Field Descriptions.....	32
15	GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG _n) Field Descriptions	34
16	GPIO Interrupt Status Register (INTSTAT _n) Field Descriptions	36
17	Document Revision History	37

Read This First

About This Manual

Describes the general-purpose input/output (GPIO) peripheral in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
 - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
 - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM357 Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

[SPRUG06](#) — TMS320DM357 DMSoC Video Processing Back End (VPBE) User's Guide. Describes the video processing back end (VPBE) in the TMS320DM357 Digital Media System-on-Chip (DMSoC) video processing subsystem. Included in the VPBE is the video encoder, on-screen display, and digital LCD controller.

[SPRUG25](#) — TMS320DM357 DMSoC ARM Subsystem Reference Guide. Describes the ARM subsystem in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the video processing subsystem, and a majority of the peripherals and external memories.

[SPRUG26](#) — TMS320DM357 DMSoC Universal Asynchronous Receiver/Transmitter (UART) User's Guide. This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

[SPRUG27](#) — TMS320DM357 DMSoC Inter-Integrated Circuit (I2C) Peripheral User's Guide. Describes the inter-integrated circuit (I2C) peripheral in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

- [SPRUG28](#) — *TMS320DM357 DMSoC 64-Bit Timer User's Guide.*** Describes the operation of the software-programmable 64-bit timer in the TMS320DM357 Digital Media System-on-Chip (DMSoC). Timer 0 and Timer 1 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.
- [SPRUG29](#) — *TMS320DM357 DMSoC Serial Peripheral Interface (SPI) User's Guide.*** Describes the serial peripheral interface (SPI) in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.
- [SPRUG30](#) — *TMS320DM357 DMSoC Host Port Interface (HPI) Reference Guide.*** This document describes the host port interface in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The HPI provides a parallel port interface through which an external host processor can directly access the TMS320DM357 DMSoC processor's resources (configuration and program/data memories).
- [SPRUG31](#) — *TMS320DM357 DMSoC General-Purpose Input/Output (GPIO) User's Guide.*** Describes the general-purpose input/output (GPIO) peripheral in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.
- [SPRUG32](#) — *TMS320DM357 DMSoC Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide.*** Describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.
- [SPRUG33](#) — *TMS320DM357 DMSoC Asynchronous External Memory Interface (EMIF) User's Guide.*** Describes the asynchronous external memory interface (EMIF) in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.
- [SPRUG34](#) — *TMS320DM357 DMSoC Enhanced Direct Memory Access (EDMA) Controller User's Guide.*** Describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The EDMA3 controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.
- [SPRUG35](#) — *TMS320DM357 DMSoC Audio Serial Port (ASP) User's Guide.*** Describes the operation of the audio serial port (ASP) audio interface in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.
- [SPRUG36](#) — *TMS320DM357 DMSoC Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide.*** Discusses the ethernet media access controller (EMAC) and physical layer (PHY) device management data input/output (MDIO) module in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The EMAC controls the flow of packet data from the DMSoC to the PHY. The MDIO module controls PHY configuration and status monitoring.

[SPRUG37](#) — TMS320DM357 DMSoC Pulse-Width Modulator (PWM) Peripheral User's Guide.

Describes the pulse-width modulator (PWM) peripheral in the TMS320DM357 Digital Media System-on-Chip (DMSoC).

[SPRUG38](#) — TMS320DM357 DMSoC DDR2 Memory Controller User's Guide. Describes the DDR2 memory controller in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The DDR2 memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices.

[SPRUG39](#) — TMS320DM357 DMSoC Video Processing Front End (VPFE) User's Guide. Describes the video processing front end (VPFE) in the TMS320DM357 Digital Media System-on-Chip (DMSoC) video processing subsystem. Included in the VPFE is the preview engine, CCD controller, resizer, histogram, and hardware 3A (H3A) statistic generator.

[SPRUGH2](#) — TMS320DM357 DMSoC Peripherals Overview Reference Guide. This document provides an overview of the peripherals in the TMS320DM357 Digital Media System-on-Chip (DMSoC).

[SPRUGH3](#) — TMS320DM357 DMSoC Universal Serial Bus Controller User's Guide. This document describes the universal serial bus (USB) controller in the TMS320DM357 Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

General-Purpose Input/Output (GPIO)

1 Introduction

The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

1.1 Purpose of the Peripheral

Most system on a chip (SoC) devices require some general-purpose input/output (GPIO) functionality in order to interact with other components in the system using low-speed interface pins. The control and use of the GPIO capability on this device is grouped together in the GPIO peripheral and is described in the following sections.

1.2 Features

The GPIO peripheral consists of the following features.

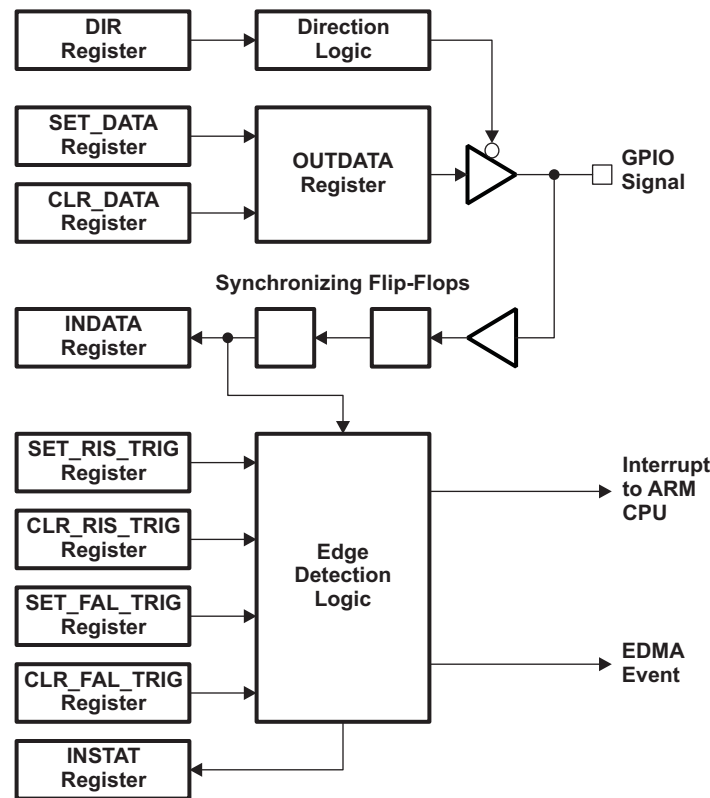
- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers
 - Output register can be read to reflect output drive status.
 - Input register can be read to reflect pin status.
- Some GPIO signals can be used as interrupt sources with configurable edge detection.

1.3 Functional Block Diagram

[Figure 1](#) shows a block diagram of the GPIO peripheral.

1.4 Industry Standard(s) Compliance Statement

The GPIO peripheral connects to external devices. While it is possible that the software implements some standard connectivity protocol over GPIO, the GPIO peripheral itself is not compliant with any such standards.

Figure 1. GPIO Peripheral Block Diagram


2 Peripheral Architecture

The following sections describe the GPIO peripheral.

2.1 Clock Control

The input clock to the GPIO peripheral is the SYSCLK5 chip-level clock. SYSCLK5 represents PLL1 divided by 6. The maximum operation speed for the GPIO peripheral is 10 MHz.

2.2 Signal Descriptions

The DM357 device supports up to 71 GPIO signals. GPIO[53:0] are 1.8V I/O signals. GPIOV33_[16:0] are 3.3V I/O signals. For information on the package pinout of each GPIO signal, refer to the device data manual.

2.3 GPIO Register Structure

The GPIO signals are grouped into banks of 16 signals per bank.

The GPIO configuration registers are organized as one 32-bit register per pair of banks. When there are an odd number of banks, the upper 16-bit of registers for the last pair are reserved and have no effect. For the interrupt configuration, the registers associated with GPIO signals that do not support interrupt capability are also reserved and have no effect. [Table 1](#) shows the banks and register control bit information associated with each GPIO pin on the device. The table can be used to locate the register bits that control each GPIO signal. For detailed information on the GPIO registers, see [section 3](#).

Table 1. GPIO Register Bits and Banks Associated With GPIO Pins

GPIO Signal	Bank Number	Register Pair Number	Register Field Number	Bit Number
GPIO0	0	register_name01	field_name0	Bit 0
GPIO1	0	register_name01	field_name1	Bit 1
GPIO2	0	register_name01	field_name2	Bit 2
GPIO3	0	register_name01	field_name3	Bit 3
GPIO4	0	register_name01	field_name4	Bit 4
GPIO5	0	register_name01	field_name5	Bit 5
GPIO6	0	register_name01	field_name6	Bit 6
GPIO7	0	register_name01	field_name7	Bit 7
GPIO8	0	register_name01	field_name8	Bit 8
GPIO9	0	register_name01	field_name9	Bit 9
GPIO10	0	register_name01	field_name10	Bit 10
GPIO11	0	register_name01	field_name11	Bit 11
GPIO12	0	register_name01	field_name12	Bit 12
GPIO13	0	register_name01	field_name13	Bit 13
GPIO14	0	register_name01	field_name14	Bit 14
GPIO15	0	register_name01	field_name15	Bit 15
GPIO16	1	register_name01	field_name16	Bit 16
GPIO17	1	register_name01	field_name17	Bit 17
GPIO18	1	register_name01	field_name18	Bit 18
GPIO19	1	register_name01	field_name19	Bit 19
GPIO20	1	register_name01	field_name20	Bit 20
GPIO21	1	register_name01	field_name21	Bit 21
GPIO22	1	register_name01	field_name22	Bit 22
GPIO23	1	register_name01	field_name23	Bit 23
GPIO24	1	register_name01	field_name24	Bit 24
GPIO25	1	register_name01	field_name25	Bit 25
GPIO26	1	register_name01	field_name26	Bit 26
GPIO27	1	register_name01	field_name27	Bit 27
GPIO28	1	register_name01	field_name28	Bit 28
GPIO29	1	register_name01	field_name29	Bit 29
GPIO30	1	register_name01	field_name30	Bit 30
GPIO31	1	register_name01	field_name31	Bit 31
GPIO32	2	register_name23	field_name32	Bit 0
GPIO33	2	register_name23	field_name33	Bit 1
GPIO34	2	register_name23	field_name34	Bit 2
GPIO35	2	register_name23	field_name35	Bit 3
GPIO36	2	register_name23	field_name36	Bit 4
GPIO37	2	register_name23	field_name37	Bit 5
GPIO38	2	register_name23	field_name38	Bit 6
GPIO39	2	register_name23	field_name39	Bit 7
GPIO40	2	register_name23	field_name40	Bit 8
GPIO41	2	register_name23	field_name41	Bit 9
GPIO42	2	register_name23	field_name42	Bit 10
GPIO43	2	register_name23	field_name43	Bit 11
GPIO44	2	register_name23	field_name44	Bit 12
GPIO45	2	register_name23	field_name45	Bit 13
GPIO46	2	register_name23	field_name46	Bit 14
GPIO47	2	register_name23	field_name47	Bit 15

Table 1. GPIO Register Bits and Banks Associated With GPIO Pins (continued)

GPIO Signal	Bank Number	Register Pair Number	Register Field Number	Bit Number
GPIO48	3	<i>register_name23</i>	<i>field_name48</i>	Bit 16
GPIO49	3	<i>register_name23</i>	<i>field_name49</i>	Bit 17
GPIO50	3	<i>register_name23</i>	<i>field_name50</i>	Bit 18
GPIO51	3	<i>register_name23</i>	<i>field_name51</i>	Bit 19
GPIO52	3	<i>register_name23</i>	<i>field_name52</i>	Bit 20
GPIO53	3	<i>register_name23</i>	<i>field_name53</i>	Bit 21
GPIOV33_0	3	<i>register_name23</i>	<i>field_name54</i>	Bit 22
GPIOV33_1	3	<i>register_name23</i>	<i>field_name55</i>	Bit 23
GPIOV33_2	3	<i>register_name23</i>	<i>field_name56</i>	Bit 24
GPIOV33_3	3	<i>register_name23</i>	<i>field_name57</i>	Bit 25
GPIOV33_4	3	<i>register_name23</i>	<i>field_name58</i>	Bit 26
GPIOV33_5	3	<i>register_name23</i>	<i>field_name59</i>	Bit 27
GPIOV33_6	3	<i>register_name23</i>	<i>field_name60</i>	Bit 28
GPIOV33_7	3	<i>register_name23</i>	<i>field_name61</i>	Bit 29
GPIOV33_8	3	<i>register_name23</i>	<i>field_name62</i>	Bit 30
GPIOV33_9	3	<i>register_name23</i>	<i>field_name63</i>	Bit 31
GPIOV33_10	4	<i>register_name4</i>	<i>field_name64</i>	Bit 0
GPIOV33_11	4	<i>register_name4</i>	<i>field_name65</i>	Bit 1
GPIOV33_12	4	<i>register_name4</i>	<i>field_name66</i>	Bit 2
GPIOV33_13	4	<i>register_name4</i>	<i>field_name67</i>	Bit 3
GPIOV33_14	4	<i>register_name4</i>	<i>field_name68</i>	Bit 4
GPIOV33_15	4	<i>register_name4</i>	<i>field_name69</i>	Bit 5
GPIOV33_16	4	<i>register_name4</i>	<i>field_name70</i>	Bit 6

2.4 Using a GPIO Signal as an Output

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an output signal.

2.4.1 Configuring a GPIO Output Signal

To configure a given GPIO signal as an output, clear the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see [Section 3](#).

2.4.2 Controlling the GPIO Output Signal State

There are three registers that control the output state driven on a GPIO signal configured as an output:

- GPIO set data register (SET_DATA) controls driving GPIO signals high
- GPIO clear data register (CLR_DATA) controls driving GPIO signals low
- GPIO output data register (OUT_DATA) contains the current state of the output signals

Reading SET_DATA, CLR_DATA, and OUT_DATA returns the output state not necessarily the actual signal state (since some signals may be configured as inputs). The actual signal state is read using the GPIO input data register (IN_DATA) associated with the desired GPIO signal. IN_DATA contains the actual logic state on the external signal.

For detailed information on these registers, see [Section 3](#).

2.4.2.1 Driving a GPIO Output Signal High

To drive a GPIO signal high, use one of the following methods:

- Write a logic 1 to the bit in SET_DATA associated with the desired GPIO signal(s) to be driven high. Bit positions in SET_DATA containing logic 0 do not affect the state of the associated output signals.
- Modify the bit in OUT_DATA associated with the desired GPIO signal by using a read-modify-write operation. The logic states driven on the GPIO output signals match the logic values written to all bits in OUT_DATA.

For GPIO signals configured as inputs, the values written to the associated SET_DATA, CLR_DATA, and OUT_DATA bits have no effect.

2.4.2.2 Driving a GPIO Output Signal Low

To drive a GPIO signal low, use one of the following methods:

- Write a logic 1 to the bit in CLR_DATA associated with the desired GPIO signal(s) to be driven low. Bit positions in CLR_DATA containing logic 0 do not affect the state of the associated output signals.
- Modify the bit in OUT_DATA associated with the desired GPIO signal by using a read-modify-write operation. The logic states driven on the GPIO output signals match the logic values written to all bits in OUT_DATA.

For GPIO signals configured as inputs, the values written to the associated SET_DATA, CLR_DATA, and OUT_DATA bits have no effect.

2.5 Using a GPIO Signal as an Input

GPIO signals are configured to operate as inputs or outputs by writing the appropriate value to the GPIO direction register (DIR). This section describes using the GPIO signal as an input signal.

2.5.1 Configuring a GPIO Input Signal

To configure a given GPIO signal as an input, set the bit in DIR that is associated with the desired GPIO signal. For detailed information on DIR, see [Section 3](#).

2.5.2 Reading a GPIO Input Signal

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA).

- For GPIO signals configured as inputs, reading IN_DATA returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA returns the output value being driven by the device.

Some signals may utilize open-drain output buffers for wired-logic operations. For open-drain GPIO signals, reading IN_DATA returns the wired-logic value on the signal (which will not be driven by the device alone). Information on any signals using open-drain outputs is available in the device data manual.

To use GPIO input signals as interrupt sources, see section [Section 2.7](#).

2.6 Reset Considerations

The GPIO peripheral has two reset sources: software reset and hardware reset.

2.6.1 Software Reset Considerations

A software reset (such as a reset initiated through the emulator) does not modify the configuration and state of the GPIO signals.

2.6.2 Hardware Reset Considerations

A hardware reset does reset the GPIO configuration and data registers to their default states; therefore, affecting the configuration and state of the GPIO signals.

2.7 Interrupt Support

The GPIO peripheral can send an interrupt event to the ARM.

2.7.1 Interrupt Events and Requests

A subset of the GPIO signals can also be configured to generate interrupts. The DM357 supports interrupts from single GPIO signals, interrupts from banks of GPIO signals, or both. The interrupt mapping from the GPIO peripheral to the ARM CPU is shown in [Table 2](#).

Table 2. GPIO Interrupts to the ARM CPU

Interrupt Source	Acronym	ARM Interrupt Number
GPIO0	GPIO0	48
GPIO1	GPIO1	49
GPIO2	GPIO2	50
GPIO3	GPIO3	51
GPIO4	GPIO4	52
GPIO5	GPIO5	53
GPIO6	GPIO6	54
GPIO7	GPIO7	55
GPIO Bank 0	GPIOBNK0	56
GPIO Bank 1	GPIOBNK1	57
GPIO Bank 2	GPIOBNK2	58
GPIO Bank 3	GPIOBNK3	59
GPIO Bank 4	GPIOBNK4	60

2.7.2 Enabling GPIO Interrupt Events

GPIO interrupt events are enabled in banks of 16 by setting the appropriate bit(s) in the GPIO interrupt per-bank enable register (BINTEN). For example, to enable bank 0 interrupts (events from GPIO[15-0]), set bit 0 in BINTEN; to enable bank 3 interrupts (events from GPIO[63-48]), set bit 3 in BINTEN.

For detailed information on BINTEN, see [Section 3](#).

2.7.3 Configuring GPIO Interrupt Edge Triggering

Each GPIO interrupt source can be configured to generate an interrupt on the GPIO signal rising edge, falling edge, both edges, or neither edge (no event). The edge detection is synchronized to the GPIO peripheral module clock.

The following four registers control the configuration of the GPIO interrupt edge detection:

- The GPIO set rising edge interrupt register (SET_RIS_TRIG) enables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO clear rising edge interrupt register (CLR_RIS_TRIG) disables GPIO interrupts on the occurrence of a rising edge on the GPIO signal.
- The GPIO set falling edge interrupt register (SET_FAL_TRIG) enables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.
- The GPIO clear falling edge interrupt register (CLR_FAL_TRIG) disables GPIO interrupts on the occurrence of a falling edge on the GPIO signal.

To configure a GPIO interrupt to occur only on rising edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG

To configure a GPIO interrupt to occur only on falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_FAL_TRIG

To configure a GPIO interrupt to occur on both the rising and falling edges of the GPIO signal:

- Write a logic 1 to the associated bit in SET_RIS_TRIG
- Write a logic 1 to the associated bit in SET_FAL_TRIG

To disable a specific GPIO interrupt:

- Write a logic 1 to the associated bit in CLR_RIS_TRIG
- Write a logic 1 to the associated bit in CLR_FAL_TRIG

For detailed information on these registers, see [Section 3](#).

Note that the direction of the GPIO signal does not have to be an input for the interrupt event generation to work. When a GPIO signal is configured as an output, the software can change the GPIO signal state and, in turn, generate an interrupt. This can be useful for debugging interrupt signal connectivity.

2.7.4 GPIO Interrupt Status

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTAT). Pending GPIO interrupts are indicated with a logic 1 in the associated bit position; interrupts that are not pending are indicated with a logic 0.

For individual GPIO interrupts that are directly routed to the ARM subsystem, the interrupt status can be read by reading the associated interrupt flag in the CPU. For the GPIO bank interrupts, INTSTAT can be used to determine which GPIO interrupt occurred. It is the responsibility of software to ensure that all pending GPIO interrupts are appropriately serviced.

Pending GPIO interrupt flags can be cleared by writing a logic 1 to the associated bit position in INTSTAT.

For detailed information on INTSTAT, see [Section 3](#).

2.7.5 Interrupt Multiplexing

No GPIO interrupts are multiplexed with other interrupt functions on the DM357.

2.8 EDMA Event Support

The GPIO peripheral can provide synchronization events to the EDMA. The EDMA events supported on this device are listed in [Table 3](#).

Table 3. GPIO Synchronization Events to the EDMA

Interrupt Source	EDMA Synchronization Event Number
GPIO0	32
GPIO1	33
GPIO2	34
GPIO3	35
GPIO4	36
GPIO5	37
GPIO6	38
GPIO7	39
GPIO Bank 0	40
GPIO Bank 1	41
GPIO Bank 2	42
GPIO Bank 3	43
GPIO Bank 4	44

2.9 Power Management

The GPIO peripheral can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the GPIO peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM357 DMSoC ARM Subsystem Reference Guide* ([SPRUG25](#)).

When the GPIO peripheral is placed in a low-power state by the PSC, the interrupt generation capability is suspended until the GPIO peripheral is removed from the low-power state. While in the low-power state, the GPIO signals configured as outputs are maintained at their state prior to the GPIO peripheral entering the low-power state.

2.10 Emulation Considerations

The GPIO peripheral is not affected by emulation suspend events (such as halts and breakpoints).

3 Registers

Table 4 lists the memory-mapped registers for the general-purpose input/output (GPIO). See the device-specific data manual for the memory address of these registers.

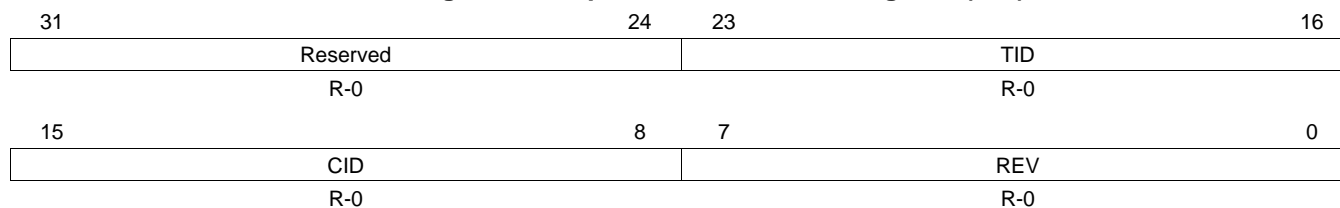
Table 4. General-Purpose Input/Output (GPIO) Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral Identification Register	Section 3.1
8h	BINTEN	GPIO Interrupt Per-Bank Enable Register	Section 3.2
GPIO Banks 0 and 1			
10h	DIR01	GPIO Banks 0 and 1 Direction Register	Section 3.3
14h	OUT_DATA01	GPIO Banks 0 and 1 Output Data Register	Section 3.4
18h	SET_DATA01	GPIO Banks 0 and 1 Set Data Register	Section 3.5
1Ch	CLR_DATA01	GPIO Banks 0 and 1 Clear Data Register	Section 3.6
20h	IN_DATA01	GPIO Banks 0 and 1 Input Data Register	Section 3.7
24h	SET_RIS_TRIG01	GPIO Banks 0 and 1 Set Rising Edge Interrupt Register	Section 3.8
28h	CLR_RIS_TRIG01	GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register	Section 3.9
2Ch	SET_FAL_TRIG01	GPIO Banks 0 and 1 Set Falling Edge Interrupt Register	Section 3.10
30h	CLR_FAL_TRIG01	GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register	Section 3.11
34h	INTSTAT01	GPIO Banks 0 and 1 Interrupt Status Register	Section 3.12
GPIO Banks 2 and 3			
38h	DIR23	GPIO Banks 2 and 3 Direction Register	Section 3.3
3Ch	OUT_DATA23	GPIO Banks 2 and 3 Output Data Register	Section 3.4
40h	SET_DATA23	GPIO Banks 2 and 3 Set Data Register	Section 3.5
44h	CLR_DATA23	GPIO Banks 2 and 3 Clear Data Register	Section 3.6
48h	IN_DATA23	GPIO Banks 2 and 3 Input Data Register	Section 3.7
4Ch	SET_RIS_TRIG23	GPIO Banks 2 and 3 Set Rising Edge Interrupt Register	Section 3.8
50h	CLR_RIS_TRIG23	GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register	Section 3.9
54h	SET_FAL_TRIG23	GPIO Banks 2 and 3 Set Falling Edge Interrupt Register	Section 3.10
58h	CLR_FAL_TRIG23	GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register	Section 3.11
5Ch	INTSTAT23	GPIO Banks 2 and 3 Interrupt Status Register	Section 3.12
GPIO Bank 4			
60h	DIR4	GPIO Bank 4 Direction Register	Section 3.3
64h	OUT_DATA4	GPIO Bank 4 Output Data Register	Section 3.4
68h	SET_DATA4	GPIO Bank 4 Set Data Register	Section 3.5
6Ch	CLR_DATA4	GPIO Bank 4 Clear Data Register	Section 3.6
70h	IN_DATA4	GPIO Bank 4 Input Data Register	Section 3.7
74h	SET_RIS_TRIG4	GPIO Bank 4 Set Rising Edge Interrupt Register	Section 3.8
78h	CLR_RIS_TRIG4	GPIO Bank 4 Clear Rising Edge Interrupt Register	Section 3.9
7Ch	SET_FAL_TRIG4	GPIO Bank 4 Set Falling Edge Interrupt Register	Section 3.10
80h	CLR_FAL_TRIG4	GPIO Bank 4 Clear Falling Edge Interrupt Register	Section 3.11
84h	INTSTAT4	GPIO Bank 4 Interrupt Status Register	Section 3.12

3.1 Peripheral Identification Register (PID)

The peripheral identification register (PID) contains identification data (type, class, and revision) for the peripheral. PID is shown in [Figure 2](#) and described in [Table 5](#).

Figure 2. Peripheral Identification Register (PID)



LEGEND: R = Read only; -n = value after reset

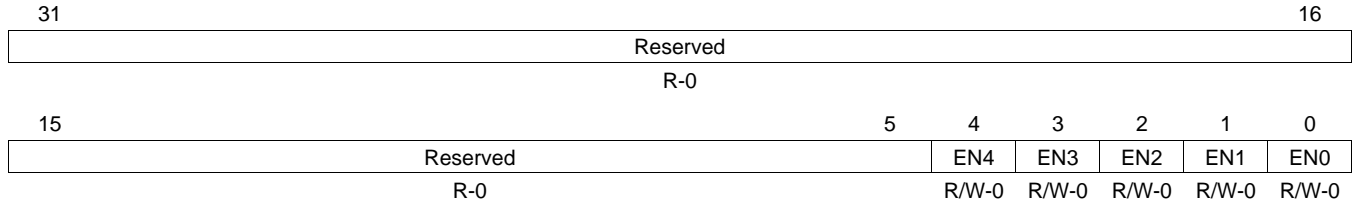
Table 5. Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-Fh	Identifies type of peripheral.
15-8	CID	0-Fh	Identifies class of peripheral.
7-0	REV	0-Fh	Identifies revision of peripheral.

3.2 GPIO Interrupt Per-Bank Enable Register (BINTEN)

The GPIO interrupt per-bank enable register (BINTEN) is shown in [Figure 3](#) and described in [Table 6](#). For information on which GPIO signals are associated with each bank, see [Table 1](#).

Figure 3. GPIO Interrupt Per-Bank Enable Register (BINTEN)



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. GPIO Interrupt Per-Bank Enable Register (BINTEN) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	EN4	0	Bank 4 interrupts are disabled.
		1	Bank 4 interrupts are enabled.
3	EN3	0	Bank 3 interrupts are disabled.
		1	Bank 3 interrupts are enabled.
2	EN2	0	Bank 2 interrupts are disabled.
		1	Bank 2 interrupts are enabled.
1	EN1	0	Bank 1 interrupts are disabled.
		1	Bank 1 interrupts are enabled.
0	EN0	0	Bank 0 interrupts are disabled.
		1	Bank 0 interrupts are enabled.

3.3 GPIO Direction Registers (DIR_{*n*})

The GPIO direction register (DIR_{*n*}) determines if GPIO pin *n* in GPIO bank *I* is an input or an output. Each of the GPIO banks may have up to 16 GPIO pins. By default, all the GPIO pins are configured as inputs (bit value = 1). The GPIO direction register (DIR01) is shown in Figure 4, DIR23 is shown in Figure 5, DIR4 is shown in Figure 6, and described in Table 7. See Table 1 to determine the DIR_{*n*} bit associated with each GPIO bank and pin number.

Figure 4. GPIO Banks 0 and 1 Direction Register (DIR01)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR31	DIR30	DIR29	DIR28	DIR27	DIR26	DIR25	DIR24	DIR23	DIR22	DIR21	DIR20	DIR19	DIR18	DIR17	DIR16
R/W-1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR15	DIR14	DIR13	DIR12	DIR11	DIR10	DIR9	DIR8	DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
R/W-1															

LEGEND: R/W = Read/Write; -*n* = value after reset

Figure 5. GPIO Banks 2 and 3 Direction Register (DIR23)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR63	DIR62	DIR61	DIR60	DIR59	DIR58	DIR57	DIR56	DIR55	DIR54	DIR53	DIR52	DIR51	DIR50	DIR49	DIR48
R/W-1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR47	DIR46	DIR45	DIR44	DIR43	DIR42	DIR41	DIR40	DIR39	DIR38	DIR37	DIR36	DIR35	DIR34	DIR33	DIR32
R/W-1															

LEGEND: R/W = Read/Write; -*n* = value after reset

Figure 6. GPIO Bank 4 Direction Register (DIR4)

31	Reserved														16
R-0															
15	Reserved							7	6	5	4	3	2	1	0
R-0							DIR70	DIR69	DIR68	DIR67	DIR66	DIR65	DIR64		
R-0							R/W-1								

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. GPIO Direction Register (DIR_{*n*}) Field Descriptions

Bit	Field	Value	Description
31-16	DIR _{<i>n</i>}	0 1	Direction of GPIO pin <i>n</i> . The DIR _{<i>n</i>} bit is used to control the direction (output = 0, input = 1) of pin <i>n</i> on GPIO bank 2 <i>I</i> + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3. GPIO pin <i>n</i> is an output. GPIO pin <i>n</i> is an input.
15-0	DIR _{<i>n</i>}	0 1	Direction of GPIO pin <i>n</i> . The DIR _{<i>n</i>} bit is used to control the direction (output = 0, input = 1) of pin <i>n</i> on GPIO bank 2 <i>I</i> . This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. GPIO pin <i>n</i> is an output. GPIO pin <i>n</i> is an input.

3.4 GPIO Output Data Register (OUT_DATA n)

The GPIO output data register (OUT_DATA n) determines the value driven on the corresponding GPIO pin n in GPIO bank l , if the pin is configured as an output (DIR n = 0). Writes do not affect pins not configured as GPIO outputs. The bits in OUT_DATA n are set or cleared by writing directly to this register. A read of OUT_DATA n returns the value of the register not the value at the pin (that might be configured as an input). The GPIO output data register (OUT_DATA01) is shown in Figure 7, OUT_DATA23 is shown in Figure 8, OUT_DATA4 is shown in Figure 9, and described in Table 8. See Table 1 to determine the OUT_DATA n bit associated with each GPIO bank and pin number.

Figure 7. GPIO Banks 0 and 1 Output Data Register (OUT_DATA01)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT31	OUT30	OUT29	OUT28	OUT27	OUT26	OUT25	OUT24	OUT23	OUT22	OUT21	OUT20	OUT19	OUT18	OUT17	OUT16
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R/W-0															

LEGEND: R/W = Read/Write; - n = value after reset

Figure 8. GPIO Banks 2 and 3 Output Data Register (OUT_DATA23)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT63	OUT62	OUT61	OUT60	OUT59	OUT58	OUT57	OUT56	OUT55	OUT54	OUT53	OUT52	OUT51	OUT50	OUT49	OUT48
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT47	OUT46	OUT45	OUT44	OUT43	OUT42	OUT41	OUT40	OUT39	OUT38	OUT37	OUT36	OUT35	OUT34	OUT33	OUT32
R/W-0															

LEGEND: R/W = Read/Write; - n = value after reset

Figure 9. GPIO Bank 4 Output Data Register (OUT_DATA4)

31	Reserved														16
R-0															
15	Reserved							7	6	5	4	3	2	1	0
R-0								OUT70	OUT69	OUT68	OUT67	OUT66	OUT65	OUT64	
R-0								R/W-0							

LEGEND: R/W = Read/Write; R = Read only; - n = value after reset

Table 8. GPIO Output Data Register (OUT_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	OUT n	0 1	Output drive state of GPIO pin n . The OUT n bit is used to drive the output (low = 0, high = 1) of pin n on GPIO bank $2l + 1$ only when pin n is configured as an output (DIR n = 0). The OUT n bit is ignored when GPIO pin n is configured as an input. This bit field configures the GPIO pins on GPIO banks 1 and 3. GPIO pin n is driven low. GPIO pin n is driven high.
15-0	OUT n	0 1	Output drive state of GPIO pin n . The OUT n bit is used to drive the output (low = 0, high = 1) of pin n on GPIO bank $2l$ only when pin n is configured as an output (DIR n = 0). The OUT n bit is ignored when GPIO pin n is configured as an input. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. GPIO pin n is driven low. GPIO pin n is driven high.

3.5 GPIO Set Data Register (SET_DATA n)

The GPIO set data register (SET_DATA n) controls driving high the corresponding GPIO pin n in GPIO bank l , if the pin is configured as an output (DIR n = 0). Writes do not affect pins not configured as GPIO outputs. The bits in SET_DATA n are set or cleared by writing directly to this register. A read of the SET n bit returns the output drive state of the corresponding GPIO pin n . The GPIO set data register (SET_DATA01) is shown in Figure 10, SET_DATA23 is shown in Figure 11, SET_DATA4 is shown in Figure 12, and described in Table 9. See Table 1 to determine the SET_DATA n bit associated with each GPIO bank and pin number.

Figure 10. GPIO Banks 0 and 1 Set Data Register (SET_DATA01)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET31	SET30	SET29	SET28	SET27	SET26	SET25	SET24	SET23	SET22	SET21	SET20	SET19	SET18	SET17	SET16
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET15	SET14	SET13	SET12	SET11	SET10	SET9	SET8	SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
R/W-0															

LEGEND: R/W = Read/Write; - n = value after reset

Figure 11. GPIO Banks 2 and 3 Set Data Register (SET_DATA23)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET63	SET62	SET61	SET60	SET59	SET58	SET57	SET56	SET55	SET54	SET53	SET52	SET51	SET50	SET49	SET48
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET47	SET46	SET45	SET44	SET43	SET42	SET41	SET40	SET39	SET38	SET37	SET36	SET35	SET34	SET33	SET32
R/W-0															

LEGEND: R/W = Read/Write; - n = value after reset

Figure 12. GPIO Bank 4 Set Data Register (SET_DATA4)

31	Reserved														16
R-0															
15	Reserved							7	6	5	4	3	2	1	0
R-0								SET70	SET69	SET68	SET67	SET66	SET65	SET64	
R-0								R/W-0							

LEGEND: R/W = Read/Write; R = Read only; - n = value after reset

Table 9. GPIO Set Data Register (SET_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	SET n	0 1	Set output drive state of GPIO pin n . The SET n bit is used to set the output of pin n on GPIO bank $2l + 1$ only when pin n is configured as an output (DIR n = 0). The SET n bit is ignored when GPIO pin n is configured as an input. Writing a 1 to the SET n bit sets the output drive state of the corresponding GPIO pin n ; reading the SET n bit returns the output drive state of the corresponding GPIO pin n . This bit field configures the GPIO pins on GPIO banks 1 and 3. No effect. Set GPIO pin n output to 1.
15-0	SET n	0 1	Set output drive state of GPIO pin n . The SET n bit is used to set the output of pin n on GPIO bank $2l$ only when pin n is configured as an output (DIR n = 0). The SET n bit is ignored when GPIO pin n is configured as an input. Writing a 1 to the SET n bit sets the output drive state of the corresponding GPIO pin n ; reading the SET n bit returns the output drive state of the corresponding GPIO pin n . This bit field configures the GPIO pins on GPIO banks 0, 2, and 4. No effect. Set GPIO pin n output to 1.

3.6 GPIO Clear Data Register (CLR_DATAn)

The GPIO clear data register (CLR_DATAn) controls driving low the corresponding GPIO pin *n* in GPIO bank *l*, if the pin is configured as an output (DIR*n* = 0). Writes do not affect pins not configured as GPIO outputs. The bits in CLR_DATAn are set or cleared by writing directly to this register. A read of the CLR*n* bit returns the output drive state of the corresponding GPIO pin *n*. The GPIO clear data register (CLR_DATA01) is shown in Figure 13, CLR_DATA23 is shown in Figure 14, CLR_DATA4 is shown in Figure 15, and described in Table 10. See Table 1 to determine the CLR_DATAn bit associated with each GPIO bank and pin number.

Figure 13. GPIO Banks 0 and 1 Clear Data Register (CLR_DATA01)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR31	CLR30	CLR29	CLR28	CLR27	CLR26	CLR25	CLR24	CLR23	CLR22	CLR21	CLR20	CLR19	CLR18	CLR17	CLR16
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR15	CLR14	CLR13	CLR12	CLR11	CLR10	CLR9	CLR8	CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
R/W-0															

LEGEND: R/W = Read/Write; -*n* = value after reset

Figure 14. GPIO Banks 2 and 3 Clear Data Register (CLR_DATA23)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR63	CLR62	CLR61	CLR60	CLR59	CLR58	CLR57	CLR56	CLR55	CLR54	CLR53	CLR52	CLR51	CLR50	CLR49	CLR48
R/W-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR47	CLR46	CLR45	CLR44	CLR43	CLR42	CLR41	CLR40	CLR39	CLR38	CLR37	CLR36	CLR35	CLR34	CLR33	CLR32
R/W-0															

LEGEND: R/W = Read/Write; -*n* = value after reset

Figure 15. GPIO Bank 4 Clear Data Register (CLR_DATA4)

31	Reserved														16
R-0															
15	Reserved						7	6	5	4	3	2	1	0	
R-0							CLR70	CLR69	CLR68	CLR67	CLR66	CLR65	CLR64		
R-0							R/W-0								

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. GPIO Clear Data Register (CLR_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	CLR n	0 1	<p>Clear output drive state of GPIO pin n. The CLRn bit is used to clear the output of pin n on GPIO bank $2/ + 1$ only when pin n is configured as an output (DIR$n = 0$). The CLRn bit is ignored when GPIO pin n is configured as an input. Writing a 1 to the CLRn bit clears the output drive state of the corresponding GPIO pin n; reading the CLRn bit returns the output drive state of the corresponding GPIO pin n. This bit field configures the GPIO pins on GPIO banks 1 and 3.</p> <p>No effect.</p> <p>Clear GPIO pin n output to 0.</p>
15-0	CLR n	0 1	<p>Clear output drive state of GPIO pin n. The CLRn bit is used to clear the output of pin n on GPIO bank $2/$ only when pin n is configured as an output (DIR$n = 0$). The CLRn bit is ignored when GPIO pin n is configured as an input. Writing a 1 to the CLRn bit clears the output drive state of the corresponding GPIO pin n; reading the CLRn bit returns the output drive state of the corresponding GPIO pin n. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.</p> <p>No effect.</p> <p>Clear GPIO pin n output to 0.</p>

3.7 GPIO Input Data Register (IN_DATA n)

The current state of the GPIO signals is read using the GPIO input data register (IN_DATA n).

- For GPIO signals configured as inputs, reading IN_DATA n returns the state of the input signal synchronized to the GPIO peripheral clock.
- For GPIO signals configured as outputs, reading IN_DATA n returns the output value being driven by the device.

The GPIO input data register (IN_DATA01) is shown in Figure 16, IN_DATA23 is shown in Figure 17, IN_DATA4 is shown in Figure 18, and described in Table 11. See Table 1 to determine the IN_DATA n bit associated with each GPIO bank and pin number.

Figure 16. GPIO Banks 0 and 1 Input Data Register (IN_DATA01)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN31	IN30	IN29	IN28	IN27	IN26	IN25	IN24	IN23	IN22	IN21	IN20	IN19	IN18	IN17	IN16
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
R-0															

LEGEND: R = Read only; - n = value after reset

Figure 17. GPIO Banks 2 and 3 Input Data Register (IN_DATA23)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN63	IN62	IN61	IN60	IN59	IN58	IN57	IN56	IN55	IN54	IN53	IN52	IN51	IN50	IN49	IN48
R-0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN47	IN46	IN45	IN44	IN43	IN42	IN41	IN40	IN39	IN38	IN37	IN36	IN35	IN34	IN33	IN32
R-0															

LEGEND: R = Read only; - n = value after reset

Figure 18. GPIO Bank 4 Input Data Register (IN_DATA4)

31															16
Reserved															
R-0															
15							7	6	5	4	3	2	1	0	
Reserved							IN70	IN69	IN68	IN67	IN66	IN65	IN64		
R-0							R-0								

LEGEND: R = Read only; - n = value after reset

Table 11. GPIO Input Data Register (IN_DATA n) Field Descriptions

Bit	Field	Value	Description
31-16	IN n		Status of GPIO pin n . Reading the IN n bit returns the state of pin n on GPIO bank $2I + 1$. This bit field returns the status of the GPIO pins on GPIO banks 1 and 3.
		0	GPIO pin n is logic low.
		1	GPIO pin n is logic high.
15-0	IN n		Status of GPIO pin n . Reading the IN n bit returns the state of pin n on GPIO bank $2I$. This bit field returns the status of the GPIO pins on GPIO banks 0, 2 and 4.
		0	GPIO pin n is logic low.
		1	GPIO pin n is logic high.

3.8 GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIGn)

The GPIO set rising edge interrupt register (SET_RIS_TRIGn) enables a rising edge on the GPIO pin to generate a GPIO interrupt. The GPIO set rising edge interrupt register (SET_RIS_TRIG01) is shown in [Figure 19](#), SET_RIS_TRIG23 is shown in [Figure 20](#), SET_RIS_TRIG4 is shown in [Figure 21](#), and described in [Table 12](#). See [Table 1](#) to determine the SET_RIS_TRIGn bit associated with each GPIO bank and pin number.

Figure 19. GPIO Banks 0 and 1 Set Rising Edge Interrupt Register (SET_RIS_TRIG01)

31	30	29	28	27	26	25	24
SETRIS31	SETRIS30	SETRIS29	SETRIS28	SETRIS27	SETRIS26	SETRIS25	SETRIS24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SETRIS23	SETRIS22	SETRIS21	SETRIS20	SETRIS19	SETRIS18	SETRIS17	SETRIS16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SETRIS15	SETRIS14	SETRIS13	SETRIS12	SETRIS11	SETRIS10	SETRIS9	SETRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETRIS7	SETRIS6	SETRIS5	SETRIS4	SETRIS3	SETRIS2	SETRIS1	SETRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 20. GPIO Banks 2 and 3 Set Rising Edge Interrupt Register (SET_RIS_TRIG23)

31	30	29	28	27	26	25	24
SETRIS63	SETRIS62	SETRIS61	SETRIS60	SETRIS59	SETRIS58	SETRIS57	SETRIS56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SETRIS55	SETRIS54	SETRIS53	SETRIS52	SETRIS51	SETRIS50	SETRIS49	SETRIS48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SETRIS47	SETRIS46	SETRIS45	SETRIS44	SETRIS43	SETRIS42	SETRIS41	SETRIS40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETRIS39	SETRIS38	SETRIS37	SETRIS36	SETRIS35	SETRIS34	SETRIS33	SETRIS32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 21. GPIO Bank 4 Set Rising Edge Interrupt Register (SET_RIS_TRIG4)

31							16
Reserved							
R-0							
15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved	SETRIS70	SETRIS69	SETRIS68	SETRIS67	SETRIS66	SETRIS65	SETRIS64
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. GPIO Set Rising Edge Interrupt Register (SET_RIS_TRIG_n) Field Descriptions

Bit	Field	Value	Description
31-16	SETRIS _n		Enable rising edge interrupt detection on GPIO pin <i>n</i> . Reading the SETRIS _n bit returns the state of pin <i>n</i> on GPIO bank 2 l + 1. This bit field configures the GPIO pins on GPIO banks 1 and 3.
		0	No effect.
		1	Interrupt is caused by a low-to-high transition on GPIO pin <i>n</i> .
15-0	SETRIS _n		Enable rising edge interrupt detection on GPIO pin <i>n</i> . Reading the SETRIS _n bit returns the state of pin <i>n</i> on GPIO bank 2 l . This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.
		0	No effect.
		1	Interrupt is caused by a low-to-high transition on GPIO pin <i>n</i> .

3.9 GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIGn)

The GPIO clear rising edge interrupt register (CLR_RIS_TRIGn) disables a rising edge on the GPIO pin from generating a GPIO interrupt. The GPIO clear rising edge interrupt register (CLR_RIS_TRIG01) is shown in Figure 22, CLR_RIS_TRIG23 is shown in Figure 23, CLR_RIS_TRIG4 is shown in Figure 24, and described in Table 13. See Table 1 to determine the CLR_RIS_TRIGn bit associated with each GPIO bank and pin number.

Figure 22. GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG01)

31	30	29	28	27	26	25	24
CLRRIS31	CLRRIS30	CLRRIS29	CLRRIS28	CLRRIS27	CLRRIS26	CLRRIS25	CLRRIS24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLRRIS23	CLRRIS22	CLRRIS21	CLRRIS20	CLRRIS19	CLRRIS18	CLRRIS17	CLRRIS16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLRRIS15	CLRRIS14	CLRRIS13	CLRRIS12	CLRRIS11	CLRRIS10	CLRRIS9	CLRRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRRIS7	CLRRIS6	CLRRIS5	CLRRIS4	CLRRIS3	CLRRIS2	CLRRIS1	CLRRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 23. GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG23)

31	30	29	28	27	26	25	24
CLRRIS63	CLRRIS62	CLRRIS61	CLRRIS60	CLRRIS59	CLRRIS58	CLRRIS57	CLRRIS56
R/W-10	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLRRIS55	CLRRIS54	CLRRIS53	CLRRIS52	CLRRIS51	CLRRIS50	CLRRIS49	CLRRIS48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLRRIS47	CLRRIS46	CLRRIS45	CLRRIS44	CLRRIS43	CLRRIS42	CLRRIS41	CLRRIS40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRRIS39	CLRRIS38	CLRRIS37	CLRRIS36	CLRRIS35	CLRRIS34	CLRRIS33	CLRRIS32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 24. GPIO Bank 4 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG4)

31							16
Reserved							
R-0							
15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved	CLRRIS70	CLRRIS69	CLRRIS68	CLRRIS67	CLRRIS66	CLRRIS65	CLRRIS64
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. GPIO Clear Rising Edge Interrupt Register (CLR_RIS_TRIG_n) Field Descriptions

Bit	Field	Value	Description
31-16	CLRRIS _n		Disable rising edge interrupt detection on GPIO pin <i>n</i> . Reading the CLRRIS _n bit returns the complement state of pin <i>n</i> on GPIO bank $2I + 1$. This bit field configures the GPIO pins on GPIO banks 1 and 3.
		0	No effect.
		1	No interrupt is caused by a low-to-high transition on GPIO pin <i>n</i> .
15-0	CLRRIS _n		Disable rising edge interrupt detection on GPIO pin <i>n</i> . Reading the CLRRIS _n bit returns the complement state of pin <i>n</i> on GPIO bank $2I$. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.
		0	No effect.
		1	No interrupt is caused by a low-to-high transition on GPIO pin <i>n</i> .

3.10 GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIG_n)

The GPIO set falling edge interrupt register (SET_FAL_TRIG_n) enables a falling edge on the GPIO pin to generate a GPIO interrupt. The GPIO set falling edge interrupt register (SET_FAL_TRIG01) is shown in [Figure 25](#), SET_FAL_TRIG23 is shown in [Figure 26](#), SET_FAL_TRIG4 is shown in [Figure 27](#), and described in [Table 14](#). See [Table 1](#) to determine the SET_FAL_TRIG_n bit associated with each GPIO bank and pin number.

Figure 25. GPIO Banks 0 and 1 Set Falling Edge Interrupt Register (SET_FAL_TRIG01)

31	30	29	28	27	26	25	24
SETFAL31	SETFAL30	SETFAL29	SETFAL28	SETFAL27	SETFAL26	SETFAL25	SETFAL24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SETFAL23	SETFAL22	SETFAL21	SETFAL20	SETFAL19	SETFAL18	SETFAL17	SETFAL16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SETFAL15	SETFAL14	SETFAL13	SETFAL12	SETFAL11	SETFAL10	SETFAL9	SETFAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETFAL7	SETFAL6	SETFAL5	SETFAL4	SETFAL3	SETFAL2	SETFAL1	SETFAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 26. GPIO Banks 2 and 3 Set Falling Edge Interrupt Register (SET_FAL_TRIG23)

31	30	29	28	27	26	25	24
SETFAL63	SETFAL62	SETFAL61	SETFAL60	SETFAL59	SETFAL58	SETFAL57	SETFAL56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
SETFAL55	SETFAL54	SETFAL53	SETFAL52	SETFAL51	SETFAL50	SETFAL49	SETFAL48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
SETFAL47	SETFAL46	SETFAL45	SETFAL44	SETFAL43	SETFAL42	SETFAL41	SETFAL40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
SETFAL39	SETFAL38	SETFAL37	SETFAL36	SETFAL35	SETFAL34	SETFAL33	SETFAL32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 27. GPIO Bank 4 Set Falling Edge Interrupt Register (SET_FAL_TRIG4)

31							16
Reserved							
R-0							
15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved	SETFAL70	SETFAL69	SETFAL68	SETFAL67	SETFAL66	SETFAL65	SETFAL64
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. GPIO Set Falling Edge Interrupt Register (SET_FAL_TRIG n) Field Descriptions

Bit	Field	Value	Description
31-16	SETFAL n	0	No effect.
		1	Interrupt is caused by a high-to-low transition on GPIO pin n .
15-0	SETFAL n	0	No effect.
		1	Interrupt is caused by a high-to-low transition on GPIO pin n .

3.11 GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIGn)

The GPIO clear falling edge interrupt register (CLR_FAL_TRIG n) disables a falling edge on the GPIO pin from generating a GPIO interrupt. The GPIO clear falling edge interrupt register (CLR_FAL_TRIG01) is shown in Figure 28, CLR_FAL_TRIG23 is shown in Figure 29, CLR_FAL_TRIG4 is shown in Figure 30, and described in Table 15. See Table 1 to determine the CLR_FAL_TRIG n bit associated with each GPIO bank and pin number.

Figure 28. GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG01)

31	30	29	28	27	26	25	24
CLRFAL31	CLRFAL30	CLRFAL29	CLRFAL28	CLRFAL27	CLRFAL26	CLRFAL25	CLRFAL24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLRFAL23	CLRFAL22	CLRFAL21	CLRFAL20	CLRFAL19	CLRFAL18	CLRFAL17	CLRFAL16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLRFAL15	CLRFAL14	CLRFAL13	CLRFAL12	CLRFAL11	CLRFAL10	CLRFAL9	CLRFAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRFAL7	CLRFAL6	CLRFAL5	CLRFAL4	CLRFAL3	CLRFAL2	CLRFAL1	CLRFAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 29. GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG23)

31	30	29	28	27	26	25	24
CLRFAL63	CLRFAL62	CLRFAL61	CLRFAL60	CLRFAL59	CLRFAL58	CLRFAL57	CLRFAL56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
CLRFAL55	CLRFAL54	CLRFAL53	CLRFAL52	CLRFAL51	CLRFAL50	CLRFAL49	CLRFAL48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
CLRFAL47	CLRFAL46	CLRFAL45	CLRFAL44	CLRFAL43	CLRFAL42	CLRFAL41	CLRFAL40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
CLRFAL39	CLRFAL38	CLRFAL37	CLRFAL36	CLRFAL35	CLRFAL34	CLRFAL33	CLRFAL32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; -n = value after reset

Figure 30. GPIO Bank 4 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG4)

31							16
Reserved							
R-0							
15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved	CLRFAL70	CLRFAL69	CLRFAL68	CLRFAL67	CLRFAL66	CLRFAL65	CLRFAL64
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. GPIO Clear Falling Edge Interrupt Register (CLR_FAL_TRIG n) Field Descriptions

Bit	Field	Value	Description
31-16	CLRFAL n		Disable falling edge interrupt detection on GPIO pin n . Reading the CLRFAL n bit returns the complement state of pin n on GPIO bank $2l + 1$. This bit field configures the GPIO pins on GPIO banks 1 and 3.
		0	No effect.
		1	No interrupt is caused by a high-to-low transition on GPIO pin n .
15-0	CLRFAL n		Disable falling edge interrupt detection on GPIO pin n . Reading the CLRFAL n bit returns the complement state of pin n on GPIO bank $2l$. This bit field configures the GPIO pins on GPIO banks 0, 2, and 4.
		0	No effect.
		1	No interrupt is caused by a high-to-low transition on GPIO pin n .

3.12 GPIO Interrupt Status Register (INTSTAT_n)

The status of GPIO interrupt events can be monitored by reading the GPIO interrupt status register (INTSTAT_n). In the associated bit position, pending GPIO interrupts are indicated with a logic 1 and GPIO interrupts that are not pending are indicated with a logic 0. The GPIO interrupt status register (INTSTAT01) is shown in Figure 31, INTSTAT23 is shown in Figure 32, INTSTAT4 is shown in Figure 33, and described in Table 16. See Table 1 to determine the INTSTAT_n bit associated with each GPIO bank and pin number.

Figure 31. GPIO Banks 0 and 1 Interrupt Status Register (INTSTAT01)

31	30	29	28	27	26	25	24
STAT31	STAT30	STAT29	STAT28	STAT27	STAT26	STAT25	STAT24
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
23	22	21	20	19	18	17	16
STAT23	STAT22	STAT21	STAT20	STAT19	STAT18	STAT17	STAT16
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
15	14	13	12	11	10	9	8
STAT15	STAT14	STAT13	STAT12	STAT11	STAT10	STAT9	STAT8
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
7	6	5	4	3	2	1	0
STAT7	STAT6	STATSTAT5	STAT4	STAT3	STAT2	STAT1	STAT0
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit (writing 0 has no effect); -n = value after reset

Figure 32. GPIO Banks 2 and 3 Interrupt Status Register (INTSTAT23)

31	30	29	28	27	26	25	24
STAT63	STAT62	STAT61	STAT60	STAT59	STAT58	STAT57	STAT56
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
23	22	21	20	19	18	17	16
STAT55	STAT54	STAT53	STAT52	STAT51	STAT50	STAT49	STAT48
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
15	14	13	12	11	10	9	8
STAT47	STAT46	STATSTAT45	STAT44	STAT43	STAT42	STAT41	STAT40
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0
7	6	5	4	3	2	1	0
STAT39	STAT38	STAT37	STAT36	STAT35	STAT34	STAT33	STAT32
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit (writing 0 has no effect); -n = value after reset

Figure 33. GPIO Bank 4 Interrupt Status Register (INTSTAT4)

31							16
Reserved							
R-0							
15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved	STAT70	STAT69	STAT68	STAT67	STAT66	STAT65	STAT64
R-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear bit (writing 0 has no effect); -n = value after reset

Table 16. GPIO Interrupt Status Register (INTSTAT n) Field Descriptions

Bit	Field	Value	Description
31-16	STAT n	0 1	<p>Interrupt status of GPIO pin n. The STATn bit is used to monitor pending GPIO interrupts on pin n of GPIO bank $2l + 1$. This bit field returns the status of GPIO pins on GPIO banks 1 and 3. Write a 1 to the STATn bit to clear the STATn bit; a write of 0 has no effect.</p> <p>No pending interrupt on GPIO pin n.</p> <p>Pending interrupt on GPIO pin n.</p>
15-0	STAT n	0 1	<p>Interrupt status of GPIO pin n. The STATn bit is used to monitor pending GPIO interrupts on pin n of GPIO bank $2l$. This bit field returns the status of GPIO pins on GPIO banks 0, 2, and 4. Write a 1 to the STATn bit to clear the STATn bit; a write of 0 has no effect.</p> <p>No pending interrupt on GPIO pin n.</p> <p>Pending interrupt on GPIO pin n.</p>

Appendix A Revision History

[Table 17](#) lists the changes made since the previous version of this document.

Table 17. Document Revision History

Reference	Additions/Modifications/Deletions
Table 2	Changed ARM Interrupt Number for GPIO Bank 4.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps