WHITE PAPER

Texas Instruments

Optimizing Power Consumption in DSP Designs

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Executive Summary

Determining the optimum power consumption for a DSP system is important but has been traditionally difficult to achieve. Using advanced process technology and chip design expertise, TI has provided new methods for controlling power consumption in its TMS320C55x™ line of power-efficient DSPs. DSP/BIOS™ real-time kernel-managed low-power modes and voltage and frequency scaling are among the techniques that give system designers some degree of control over power consumption in different design scenarios. In addition, power consumption spreadsheets provide more exact information, and advanced tools enable developers to first profile, then optimize the power consumption of their C55x DSP designs. By combining these resources with power-efficient design techniques, developers can create systems that save space, dissipate less heat, extend operation between battery charges, and promote reliability for end-product users.

Optimizing power consumption is an important design goal for systems based on digital signal processors (DSPs), but it is a goal that is often difficult to achieve. Today, DSP-based equipments often combine applications that were previously separate, and each application may have multiple operating modes. Developing a power profile for such a device, let alone the entire complex system, is very difficult. Designers need the best information available, as well as techniques and tools that can help them optimize power consumption within the specific application.

Recognizing this need, TI has developed more advanced methods for reducing power consumption in its line of TMS320C55x™ DSPs, using both chip design and manufacturing processes. On-chip power optimization techniques now offer more granular control and more power-saving modes. C55x™ DSP-based development tools give designers more insight into how their systems consume power and provide techniques for lowering power consumption via on-chip hardware. And TI's DSP/BIOS™ real-time operating system incorporates power management features that coordinate low-power operation and timing among the many on-chip functions, giving developers greater control over power-saving techniques. When these built-in features and tools are used in combination with a well-planned system design, power consumption in a DSP system can be reduced dramatically.

Low Power Matters

Low power consumption is important for all DSP systems, though the reasons vary somewhat by application. In grid-powered systems, lowering the power decreases operating expenses, increases reliability and allows compact design that permits more functionality to be packed into the same space, with less need for fans and other cooling techniques. In critical applications such as high-definition medical imaging, heat can even cause operating problems, defeating the purpose of the equipment, so low power dissipation is essential.

In portable electronic systems, low power consumption helps minimize size and weight while maximizing the life of the battery between charges. Smaller batteries can be used, further reducing the scale of the system. Lower power also helps keep

portable systems from becoming hot during prolonged use. Cellphones, PDAs, MP3 players, digital still and video cameras, electronic instruments–these and other handheld devices can all become smaller, run cooler and operate longer between charges with lower power consumption.

Understanding Power Profiles and Chip Resources

The first step toward reducing power in any type of system is understanding how the system is used, and how that usage affects power consumption. A cellphone, for instance, spends a great deal of its time waiting for a call, but relatively little time during the call. An MP3 player, on the other hand, is normally either on, and in active operation, or off. Other systems, line-powered as well as portable, have different profiles of standby and active operation.

Understanding this profile can help the designer in choosing a power-efficient processor, since the fundamental CMOS technology of a DSP can greatly affect power consumption in a specific type of application. Advanced CMOS processes are based on high-performance transistors that run at extremely low voltages, and TI is an industry leader in tailoring the transistors in its processes to the needs of individual DSP applications. Depending on the intended application, the transistors can either minimize power consumption by clamping quiescent current, or maximize performance, though with slightly greater current leakage. TI DSPs that are designed for applications with long standby times, such as cellphones, keep quiescent current to a minimum with low-leakage transistors, while those products that are designed for high-performance applications that are always active favor faster-switching transistors.

System usage also involves the responsiveness of the system to events and, thus, the latency when circuitry is powered on. Some delay is expected on initial power-up, and a lesser delay is acceptable when a system wakes from a standby mode. But users generally expect immediate response from a system that is in active operation, so that on-chip functions cannot be too deeply asleep at these times. Two considerations enter here: first, some functions can be shut down more completely than others, especially during standby periods, but also during active operation. Second, the more granularity the processor offers in controlling its power modes, the more the designer can tailor power consumption to the operating profile of the system.

Power-efficient C55x™ DSP chip designs take into account these considerations by creating power domains that enable the application to disconnect the clock inputs to functions that are not in use. Just as a processing core can enter a sleep mode, where it performs no operations until it is awakened by an interrupt, so peripherals and memory blocks can be put to sleep until needed. The transistors in the unclocked functions lose no

power except for quiescent current, and the wake-up delay required for resuming the clock is minimal. As system designers consider the usage profiles of their products, they also need to be aware of how much control C55x™ DSPs give them, as well as how much control the chips handle automatically, over individual clock functions.

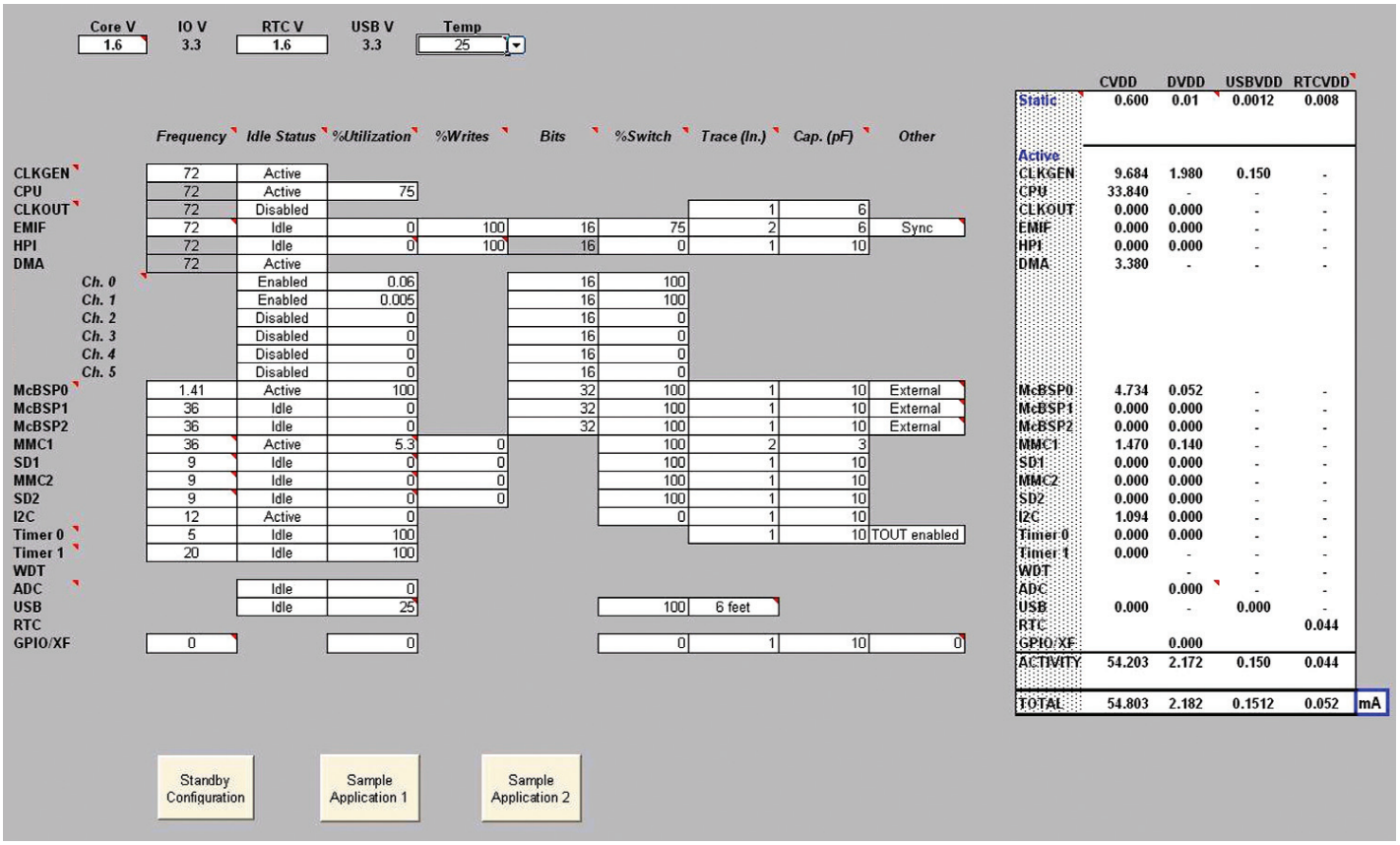
An additional power-conserving feature of C55x DSPs is the ability to scale the core voltage and frequency. If the DSP can reduce the core clock rate and still meet its processing requirements, a proportional savings in active power consumption results. And when lower frequencies are accompanied by lower operating voltages, the additional power savings can be significant. Voltages and frequencies can be scaled at startup for all system operations, or they can be controlled dynamically through software as the application needs change, providing an important means for cutting power consumption during off-peak processing intervals.

Getting the Right Power Information

Multiple cores, applications and power modes can make estimating power for complex DSP systems very difficult. Traditional methods of determining power were based on information such as the maximum current figure from the device data sheet, current draw per cycle or instruction (mA/MHz, mA/MIPS) and test cases, often synthetic, for the entire chip. Although useful for gross estimates, these methods are not acceptable for estimating the power consumed by a DSP in a complex system, where the cores, peripherals and on-chip memory may be turned on and off independently according to changes in the applications and operating modes. Designers need visibility into the power consumed by different functions on the chip in real applications because realistic power information enables them to estimate more accurately the effects of different implementations, and even to determine how an application affects power consumption on different platforms.

What TI offers is a modular approach to power estimation that divides the device into subsystems, then exercises each subsystem independently. Once maximum and idle power figures are established for each of the on-chip functions, it is possible to create a power consumption curve for each by interpolation. Then, when the level of operation of each function is specified, the resulting power figures derived from the individual curves can be summed to provide a realistic estimate for the entire device.

Figure 1 shows a power estimation spreadsheet based on this type of approach. The spreadsheet breaks down a C55x DSP into its subsystems, accepts user-supplied parameters, and returns a device power estimate. As the spreadsheet indicates, a valid estimate is based on user-supplied information that reflects a good understanding of system usage, including factors such as data width, frequency, supply voltage and the percentage of the available bandwidth for peripherals that is in use.



Core V	IO V	RTC V	USB V	Temp
1.6	3.3	1.6	3.3	25

	Frequency	Idle Status	%Utilization	%Writes	Bits	%Switch	Trace (In.)	Cap. (pF)	Other
CLKGEN	72	Active							
CPU	72	Active	75						
CLKOUT	72	Disabled					1	6	
EMIF	72	Idle	0	100	16	75	2	6	Sync
HPI	72	Idle	0	100	16	0	1	10	
DMA	72	Active							
Ch. 0		Enabled	0.06		16	100			
Ch. 1		Enabled	0.005		16	100			
Ch. 2		Disabled	0		16	0			
Ch. 3		Disabled	0		16	0			
Ch. 4		Disabled	0		16	0			
Ch. 5		Disabled	0		16	0			
McBSP0	1.41	Active	100		32	100	1	10	External
McBSP1	36	Idle	0		32	100	1	10	External
McBSP2	36	Idle	0		32	100	1	10	External
MMC1	36	Active	5.3	0		100	2	3	
SD1	9	Idle	0	0		100	1	10	
MMC2	9	Idle	0	0		100	1	10	
SD2	9	Idle	0	0		100	1	10	
I2C	12	Active	0			0	1	10	
Timer 0	5	Idle	100				1	10	TOUT enabled
Timer 1	20	Idle	100						
WDT									
ADC		Idle	0						
USB		Idle	25			100	6 feet		
RTC									
GPIO/XF	0		0			0	1	10	0

	CVDD	DVDD	USBVDD	RTCVDD	
Static	0.600	0.01	0.0012	0.008	
Active					
CLKGEN	9.684	1.980	0.150	-	
CPU	33.840	-	-	-	
CLKOUT	0.000	0.000	-	-	
EMIF	0.000	0.000	-	-	
HPI	0.000	0.000	-	-	
DMA	3.380	-	-	-	
McBSP0	4.734	0.052	-	-	
McBSP1	0.000	0.000	-	-	
McBSP2	0.000	0.000	-	-	
MMC1	1.470	0.140	-	-	
SD1	0.000	0.000	-	-	
MMC2	0.000	0.000	-	-	
SD2	0.000	0.000	-	-	
I2C	1.094	0.000	-	-	
Timer 0	0.000	0.000	-	-	
Timer 1	0.000	-	-	-	
WDT		-	-	-	
ADC		0.000	-	-	
USB	0.000	-	0.000	-	
RTC				0.044	
GPIO/XF		0.000			
ACTIVITY	54.203	2.172	0.150	0.044	
TOTAL	54.803	2.182	0.1512	0.052	mA

Figure 1. Power estimation spreadsheet.

Designing for Low Power Consumption

Power-conscious design techniques help the DSP developer take full advantage of a valid power estimate. At the system level, the designer should select components carefully and keep their number as low as possible. In addition, the designer should consider which unused components can be powered down at times, especially during standby operation. Use of board-level memory is also a power drain, since it has to energize both memory chips and board traces. Whenever possible, the application should use the DSP internal memory, keeping high-bandwidth memory on-chip and reserving external memory for low-speed, occasional access. Off-chip non-volatile memory may be required for booting, but may be powered down after startup. Software should be optimized for performance in order to reduce the code's footprint in memory and the number of instruction fetches. Tighter code makes better use of the cache and internal instruction buffers, and if the program runs faster, that reduces the system's time in active mode.

The most device-specific power reductions take advantage of the built-in hardware capabilities in the C55x™ DSPs. From startup on, the application can idle domains that are not in use, limiting peripheral power consumption to only those I/Os that are needed

at a given time. Normally, the application will control the domains directly at boot time; then, later, the DSP core can run a background loop that checks for functions that are not needed and turns them off. If the application uses these techniques, the device's sleep modes can minimize the power drains of the core and chip domains during idle times.

The architecture of the C55x™ DSP allows the core voltage and frequency (V/F) to be scaled at boot time, if the total performance required does not equal the full capabilities of the device. V/F scaling can also be dynamically invoked during run time if, say, the system alternates among applications that have different performance loads. For V/F scaling, the design has to provide external control of the DSP's supply voltage, as well as software control built into the background loop. Since frequency scaling slows the core's operation, the designer should consider the timing of dependent operations in designing the application.

Power Management in the OS

Changing the power requirements of the C55x DSP dynamically, whether through V/F scaling or through low-power modes, is facilitated by TI's DSP/BIOS™ real-time operating system (RTOS). A power management (PM) module within the RTOS implements boot-time power savings and coordinates the various low-power operations throughout the system. Core frequency scaling can affect the timing of subsystem operations, so the PM has the capability to scale the DSP's chip clock after a frequency scaling operation. If the OS clock accuracy is not important to the application or if the user wishes to conserve code space, this PM capability can be disabled. Additionally, the user can enable or disable the PM function that automatically idles clocks when threads are blocked. In its coordinating role, the PM provides a registry for power event notifications so that clients can register to be notified when specific power management events occur. Because of the complexity of the system, the PM supports multiple client instances and allows clients to have delayed completion of events.

The PM also exports a library of application program interfaces (APIs) that enable software control of the chip's low-power techniques. Through the APIs, the application can gate clocks, activate sleep modes and safely manage the transitions between setpoints for V/F scaling. Setpoints are valid combinations of core voltage and operating frequency. The power management library ensures that changes between setpoints are made safely. Figure 2 on the following page shows how setpoints govern the timing of V/F scaling. Because the voltage and frequency scaling implementation is specific to the DSP and voltage regulator used in the design, the PM APIs support setpoint and latency queries and configurations, and the PM library can be rebuilt.

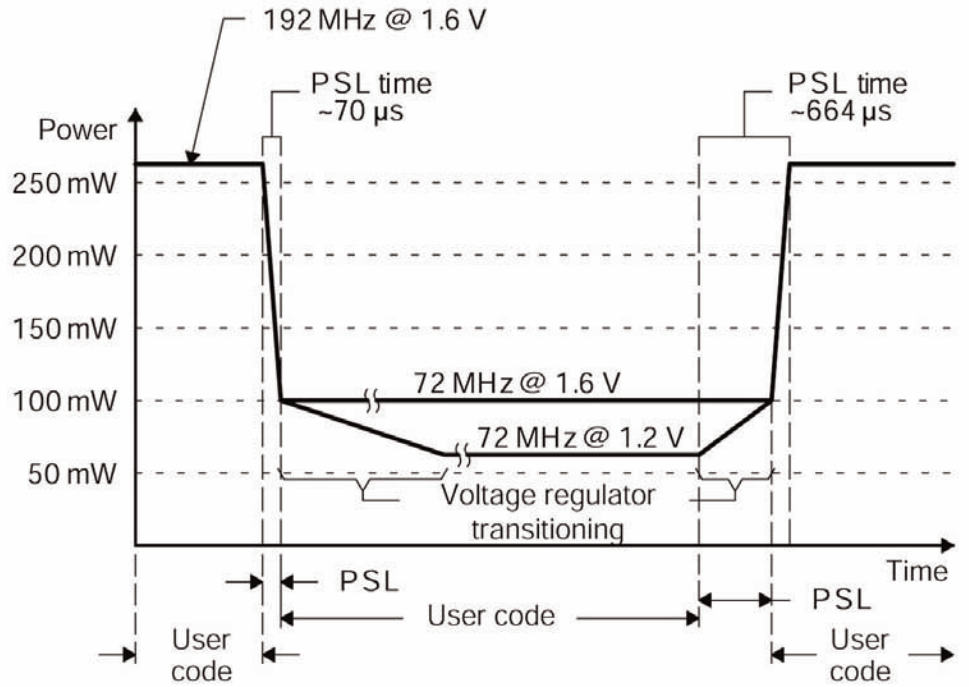


Figure 2. Voltage and frequency scaling with setpoints.

The TMS320C55x™ Power Optimization DSK

Dealing effectively with all of these techniques requires tools that are designed for power management. Paralleling its other areas of DSP tool development, TI has introduced power optimization tools that provide visibility and ease of use to help simplify system analysis and speed time-to-market. The tools work with the C55x™ DSP embedded and RTOS power management techniques while providing test features such as meters, scope waveforms, channel calibration, test code, event triggering and so forth. With these capabilities in hand, the designer has a feedback mechanism that enables evaluation of how alternate implementations affect power consumption. Figure 3 shows how the power optimization tools fit into the code development cycle.

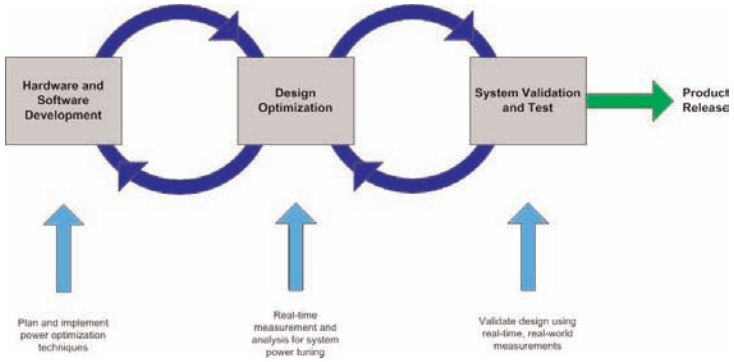


Figure 3. Power optimization and code development.

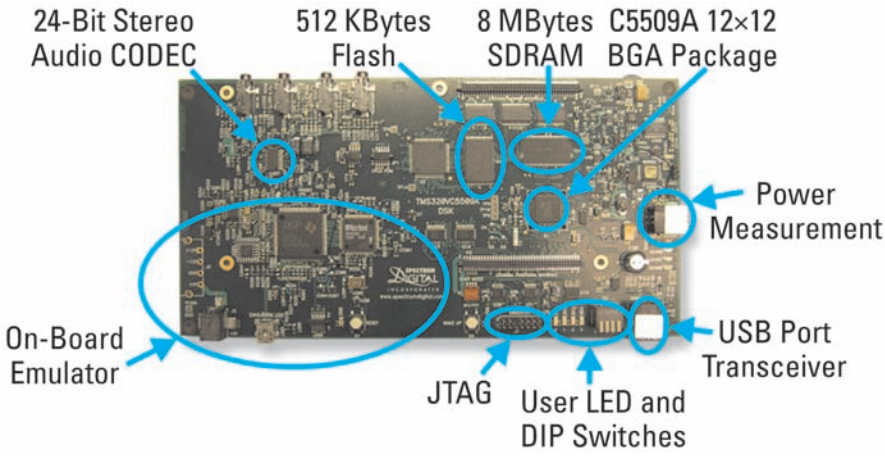


Figure 4. C55x power optimization DSK hardware.

TI brings together the hardware, software and tools for power-efficient DSP design with the C55x™ Power Optimization DSP Starter Kit (DSK), part number TMDSDSK5509. The DSK hardware, shown in Figure 4, includes a Spectrum Digital™ evaluation module (EVM) with the following features:

- Power-efficient TMS320C5509A DSP
- 16-MB SDRAM
- USB interface
- AIC23 stereo codec
- Support for SD and other media interfaces
- On-board XDS510™ JTAG controller for emulation
- Daughter card and expansion port connectors
- USB power measurement hardware

TI software for the DSK includes the Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS™ RTOS, compiler, assembler, linker, foundation software and chip support library. All of these tools and basic software building blocks help simplify the task of designing a DSP system for evaluation, then carrying it through the complete development cycle into production.

From the DSK board, the USB power measurement port connects to a PC via a power analyzer board supplied by National Instruments. Based on NI's USB data acquisition (DAQ) design, the power analyzer includes a 14-bit analog-to-digital converter (ADC) sampling at 40 kilosamples per second, four analog inputs to measure board current and monitor triggering, and eight digital inputs for frequency detection and core voltage selection. Operating on the PC is NI's Windows®-based, ready-to-run LABView™ virtual instrumentation for power optimization, along with driver and application software. In addition to

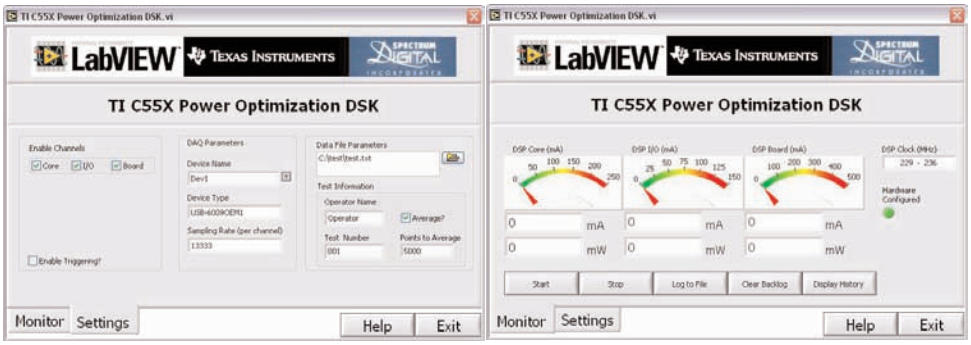


Figure 5. TMS320C55x™ DSK LABView™ software GUI.

offering utilities for set-up and configuration, the NI application software includes the Channel Calibration Wizard, which provides end-to-end calibration from sensor to software, thus improving measurement accuracy. Additional NI tools for graphical programming and measurement, as well as free source code for customization, can be added as needed to the NI power optimization instrumentation. Figure 5 shows the graphical user interface of the DSK power optimization software.

In using the DSK for profiling power, the designer can simply set start and stop trigger points using the Code Composer Studio™ IDE. Since the DSP trigger points also trigger the DAQ power analyzer, that power consumption can be measured and displayed by the LABView software. The integrated hardware and tools of the DSK help developers evaluate the power consumption of the C55x™ DSP in different design scenarios, saving them time as they determine the best overall mix of low power consumption and high performance for their systems.

Designing for Power from the Beginning

Power optimization is sometimes treated as an afterthought in DSP system development, but it should not be. The earlier it is considered in the development cycle, the better, especially in complex systems with multiple applications and operating modes. In handheld systems, low power consumption is usually a major requirement in order to extend battery operating time, but even line-powered systems need to keep heat dissipation and operating costs down by drawing less current. In order to optimize power consumption, a designer needs to understand the power profile of the system, then turn to an information resource that takes into account all of the major system functions in deriving a power estimate.

TMS320C55x™ DSPs, which are based on power-efficient CMOS processes, integrate hardware techniques such as granularly defined low-power modes and voltage and frequency scaling. APIs make these techniques readily available to the application for control through the DSP/BIOS™ RTOS, and test tools help the designer evaluate different implementations for power consumption. With all of these resources available, there is no longer any reason not to design for power from the very beginning of the development cycle.

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