Technical Article
Factory Automation Design Made Simple with Multiprotocol Industrial Ethernet Systems

Thomas Mauer

Factory automation equipment – sensors, actuators, drives and programmable logic controllers (PLCs) – supports industrial Ethernet protocols such as EtherCAT, Profinet, EtherNet Industrial Protocol (EtherNet/IP) and Sercos, each one exchangeable by loading a different software image onto the hardware platform.

Multiprotocol industrial Ethernet systems reduce manufacturing costs in the hardware development cycle, reducing bill-of-materials costs by requiring fabrication of only a single printed circuit board, thereby accelerating time to market. Manufacturers can offer field devices such as digital input modules or servo drives for factory automation using different industrial Ethernet protocols.

Architectures such as TI's programmable real-time unit industrial communications subsystem (PRU-ICSS) can support industrial Ethernet speeds of 1,000 Mbps for field devices – especially with the new Time-Sensitive Networking (TSN) protocol.

Industrial Ethernet System Architecture

Figure 1 shows the main components within an industrial Ethernet field device that exchanges process data with a PLC and other field devices. Two Ethernet ports support a line or ring Ethernet topology, meaning that the Ethernet cables connect a PLC to a line of field devices without an Ethernet switch.
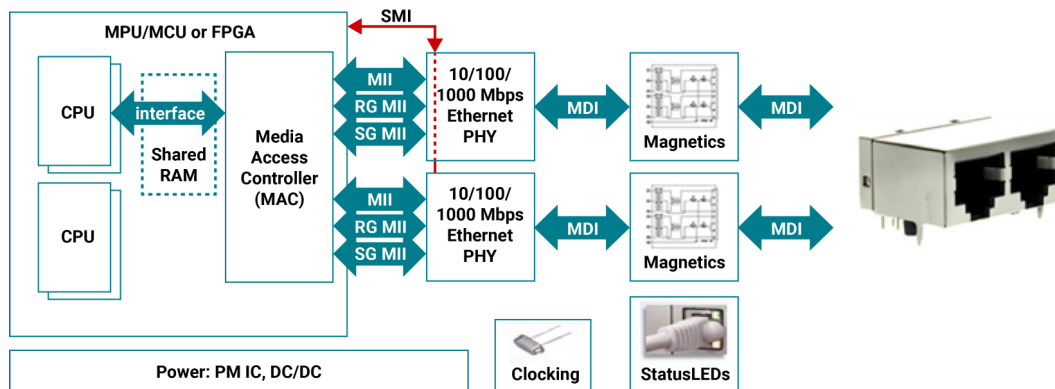

Figure 1. Industrial Ethernet Field Device System Block Diagram

From the RJ45 connector, the Medium Dependent Interface (MDI) connects to magnetics that provide an isolation barrier to other devices before the Ethernet frame enters the Ethernet physical layer (PHY) transceiver.

The PHY converts the Ethernet frame from analog to digital (receiver) and digital to analog (transmitter) and outputs the digital bitstream over Media Independent Interface (MII), Reduced Gigabit Media Independent Interface (RGMII) or Serial Gigabit Media Independent Interface (SGMII).

The PHY plays an important role in industrial Ethernet – as important as the media access controller (MAC). Depending on the MDI, the PHY has to support copper media with different pairs (one pair for T1 single-pair Ethernet, two pairs for 100-Mbps Ethernet or four pairs for 1,000-Mbps Ethernet). Some industrial Ethernet networks also support fiber, which is more resilient against electromagnetic compatibility (EMC) and electromagnetic interference disturbances in challenging industrial environments.

Next, the MII stream of Ethernet bytes enters the MAC. The MAC is responsible for the industrial Ethernet protocol and is an important functional block for multiprotocol industrial Ethernet support.

Because each industrial Ethernet protocol has a unique way of handling the industrial Ethernet frame when extracting and inserting process data, the MAC processing method must be changed for each protocol. An application-specific integrated circuit solution such as a MAC is typically fixed to a single protocol and does not have multiprotocol capability. A multiprotocol-capable MAC must support various methods of Ethernet frame processing, such as on the fly, cut-through, frame preemption, and store and forward.

The MAC makes the process data from the PLC available to the central processing unit (CPU) through an interface. When the MAC is a physically separate device, this interface is slow (Serial Peripheral Interface [SPI] or I^{2}C, or a memory-mapped external bus). When the MAC and CPU are integrated, shared high-speed memory handles the interface and synchronizes the process data between the MAC and CPU.

The CPU performs various tasks. Each industrial Ethernet protocol requires a software stack that interacts with the MAC in order to exchange process data. A field device uses this process data for controlling digital inputs and outputs or controlling the speed and rotation of a servo drive.

When the system contains multiple CPUs, it is common practice to split the workload where the industrial Ethernet stack runs on its own CPU and the industrial application operates on a different CPU.

It is possible to run different kinds of operating systems (OSs) on the CPU cores – a high-level OS (HLOS) such as Linux or real-time Linux, or a real-time OS (RTOS) such as Free-RTOS or no-OS.

The TI Sitara™ Family Solutions and TI Ethernet PHYs for Multiprotocol Industrial Ethernet

The Sitara™ processor family supports a programmable MAC with its integrated PRU-ICSS peripheral. The PRU loads at run time with firmware from one of the industrial Ethernet protocols. The Sitara AM6442 as seen in Figure 2, AM2434 and AM2434 support 1,000-Mbps protocols such as TSN. The PRU-ICSS also operates as a standard Ethernet MAC and two-port Ethernet switch.
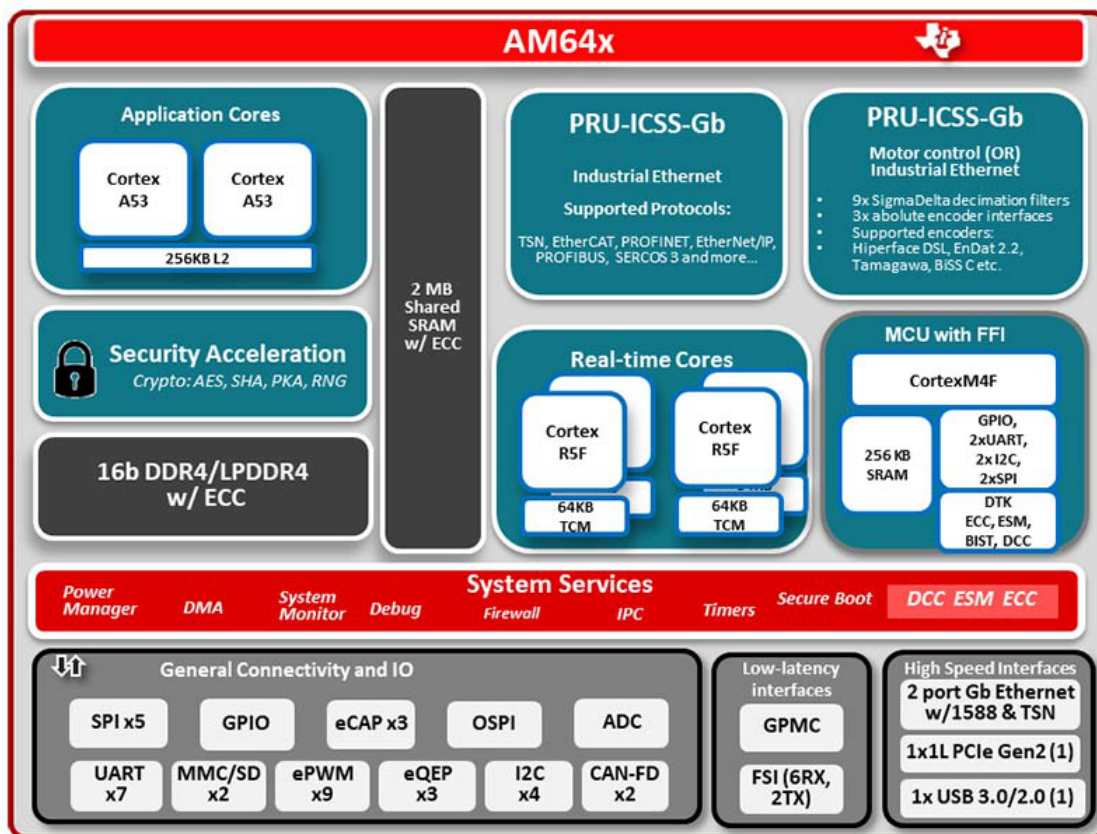

Figure 2. The Sitara AM6442 Processor Solution with PRU-ICSS for Multiprotocol Industrial Ethernet Support

The Sitara processor family's ability to support multiple instances of PRU-ICSS enables industrial peripherals such as position encoders (EnDAT 2.2, HIPERFACE digital servo link [DSL], Bidirectional Serial Synchronous [BiSS]); pulse-width modulation (PWM); and a sigma-delta decimation filter for external isolated analog-to-digital converters. Servo drives use such peripherals.

Sitara processors also integrate various functions used by industrial applications, including ADC, SPI, I^2C and general-purpose memory controllers. The system-on-chip also has internal shared memory to exchange process data between the MAC and CPU.

As seen in Figure 3, the Sitara processor family has multiple Arm® Cortex®-A53 cores for HLOSs, Arm Cortex-R5F cores for RTOS or bare-metal applications, and PRU-ICSS for the industrial Ethernet MAC.
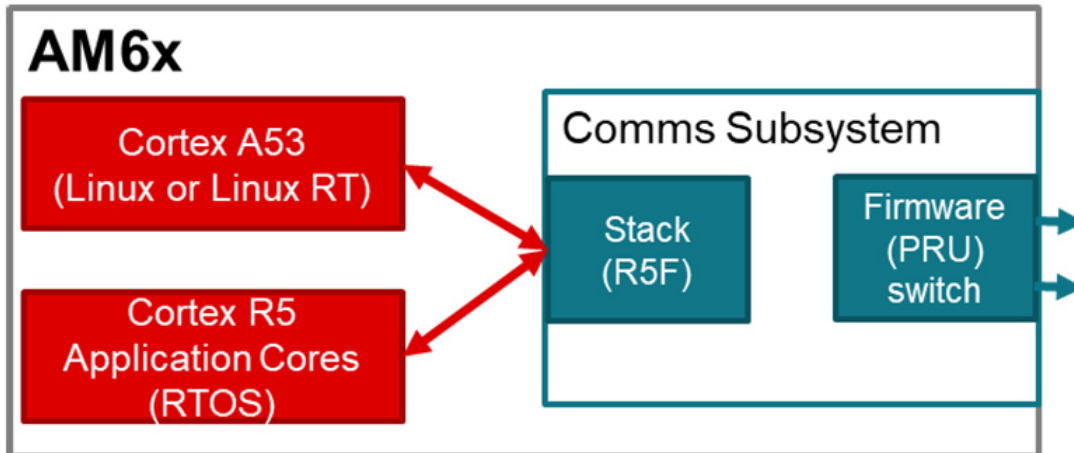
Figure 3. Multicore Processing with an RTOS, HLOS and Firmware

The integration of a programmable MAC approach supports different frame-handling methods required for multiprotocol industrial Ethernet, with the application processor on a single chip. Fast process data exchange between the processor and MAC is possible through the high-speed internal memory interface, and the family offers scalable processor cores.

TI offers evaluation modules (EVMs) for the Sitara processor family with Ethernet PHY solutions using either the DP83867 or DP83869 Ethernet PHY transceivers.

Additional Resources
- Learn more about industrial protocols for 100 Mbps and 1,000 Mbps Ethernet in the AM64x and AM24x software development kit (SDK).
- Learn more about PRU-ICSS industrial software for Sitara processors and integrated industrial protocols available.
- Read more on TI's industrial communications academy
- Check out the Sitara AM64x EVM.
- Order the AM243x Arm-based MCU general-purpose LaunchPad™ development kit.

IMPORTANT NOTICE AND DISCLAIMER