Technical Article

Increasing Power Density with an Integrated GaN Solution

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Gallium nitride (GaN) is a popular topic in the power electronics industry, as it enables designs such as 80 Plus titanium power supplies, 3.8-kW/L electric vehicle (EV) onboard chargers and EV charging stations. In many applications, GaN replaces traditional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) given its ability to drive higher power density and efficiency. But because of its electrical properties and the performance that it enables, designing with GaN has a different set of challenges than silicon.

Several different types of GaN FETs exist with different device structures – depletion mode (d-mode), enhancement mode (e-mode) and cascade to cathode (cascode) – and each has its own accompanying gate-driver and system requirements. In this article, I will break down the most important considerations for designing with different types of GaN FETs to improve power density in your system design. I will also review how integrating functions such as a gate driver and voltage supply regulation can significantly simplify your overall design.

Anatomy of a GaN FET

Each GaN power switch must be paired with an appropriate gate driver. (Otherwise, you could experience a pop and puff of smoke when testing at the bench!) GaN devices can have uniquely sensitive gates, as they are not classical MOSFETs, but are instead high-electron-mobility transistors (HEMTs). The cross section of a HEMT, shown in Figure 1, appears similar to a MOSFET; however, current does not flow through the full substrate or buffer layer, but instead flows through a two-dimensional electron gas layer.

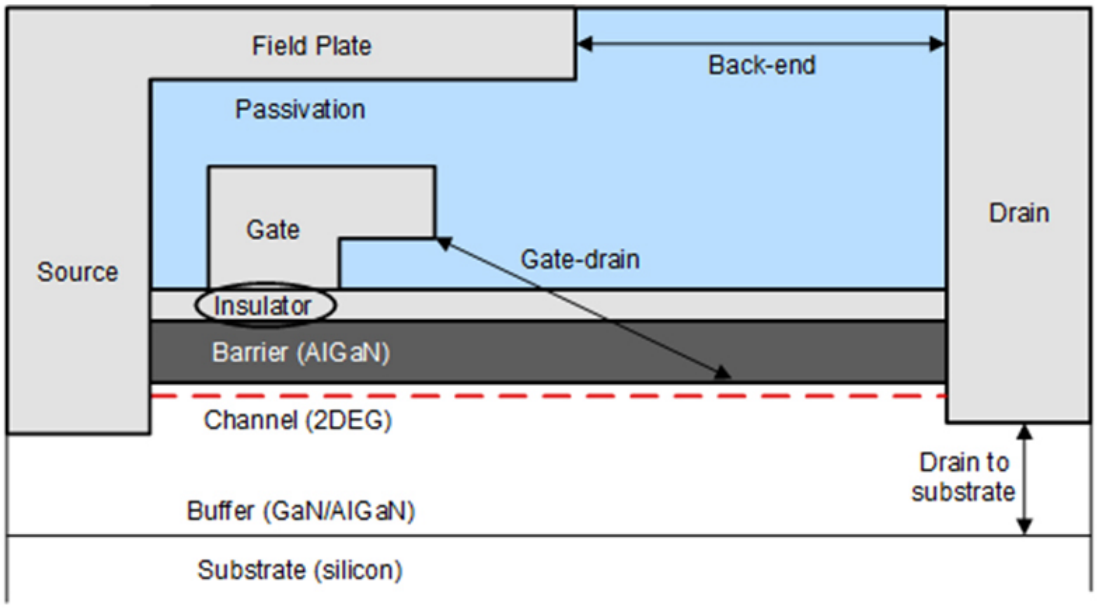

Figure 1. Cross-section of the Lateral Structure of GaN FETs

Incorrect gate control of a GaN FET will cause a breakdown of the insulative layer, barrier or other structural elements; the device will not only fail during that system condition, but it is likely also permanently damaged. This level of sensitivity necessitates a review of different types of GaN devices and their broad needs. HEMTs also do not have the traditional doped FET structure that forms p-n junctions, which then cause body diodes.

This means that there are no internal diodes that can break down or cause unwanted behavior during operation such as reverse recovery.

Gate-driver and Bias-supply Considerations

E-mode GaN FETs look very similar to the e-mode silicon FETs that you may already have experience with. A positive voltage of 1.5 V to 1.8 V will begin to turn on the FET, with most operating conditions specified for 6-V gate threshold operation. However, most e-mode GaN devices have a maximum gate threshold of 7 V, which when violated will likely result in permanent damage.

Because traditional silicon gate drivers may not offer proper voltage regulation or cannot handle the high common-mode transient immunity in a GaN-based design, many designers choose a gate driver such as the LMG1210-Q1, which TI designed specifically for use with a GaN FET. This device offers a gate-drive voltage of 5 V, regardless of supply voltage. Traditional gate drivers would need very tight regulation of the gate driver's bias supply so that they do not overstress the GaN FET. A cascode GaN FET, shown in Figure 2, is a compromise for ease of use compared to e-mode GaN FETs.

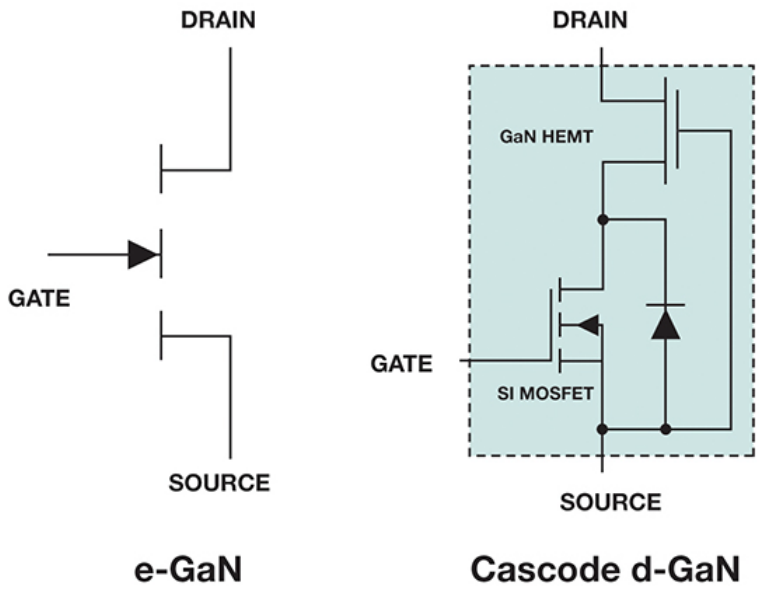

Figure 2. Symbols for E-mode and Cascode D-mode GaN FETs

The GaN FET is a d-mode device, which means that it is normally on, and requires a negative gate threshold to turn the device off. This is extremely problematic for a power switch, so most manufacturers add a 30-V silicon FET in series with the GaN FET for sale as one package. The gate of the GaN FET connects to the source of the silicon FET, and applies the turnon and turnoff gate pulses to the gate of the silicon FET.

The biggest benefit of this approach is that traditional isolated gate drivers such as the UCC5350-Q1 drive the silicon FET, eliminating many gate-driver and bias-supply concerns. The biggest downsides of cascode GaN FETs are higher output capacitance for the FET and susceptibility to reverse recovery given the presence of a body diode. The output capacitance of the silicon FET adds on to that of the GaN FET, resulting in a 20% increase, which means >20% increased switching losses compared to other GaN solutions. And during reverse conduction, the body diode of the silicon FET conducts current and undergoes reverse recovery when the voltage polarity flips.

Cascode GaN FETs operate at slew rates of 70 V/ns (compared to 150 V/ns for other GaN solutions) in order to guard against avalanche breakdown of the silicon FET, increasing switching overlap losses. Although cascode GaN FETs are simpler to design with, they limit the achievable performance.

Integration Offers an Easier Solution

The integration of a gate driver with built-in bias-supply regulation and a d-mode GaN FET solves many of the design challenges of e-mode and cascode GaN FETs. For example, the LMG3522R030-Q1, a 650-V 30-mΩ GaN device, has an integrated gate driver and power management features that enables higher power density and efficiency while reducing the risks and engineering effort required. Since the GaN FET is d-mode, there is a silicon FET integrated in series with the GaN FET. But the big difference versus cascode GaN FETs is that the integrated gate driver can directly drive the gate of the GaN FET, while the silicon FET performs the role of a normally-off enable switch at power-up. This approach, known as direct drive, eliminates the most pressing issues of cascode GaN FETs, such as higher output capacitance, reverse-recovery susceptibility and avalanche breakdown of the silicon FET in series. The gate driver integrated in the LMG3522R030-Q1 enables very low switching overlap losses, enabling the GaN FET to operate at a switching frequency as high as 2.2 MHz and eliminating the risk of pairing a GaN FET with the wrong gate driver. Figure 3 shows an example of a half-bridge configuration using integrated LMG3522R030-Q1 GaN FETs.

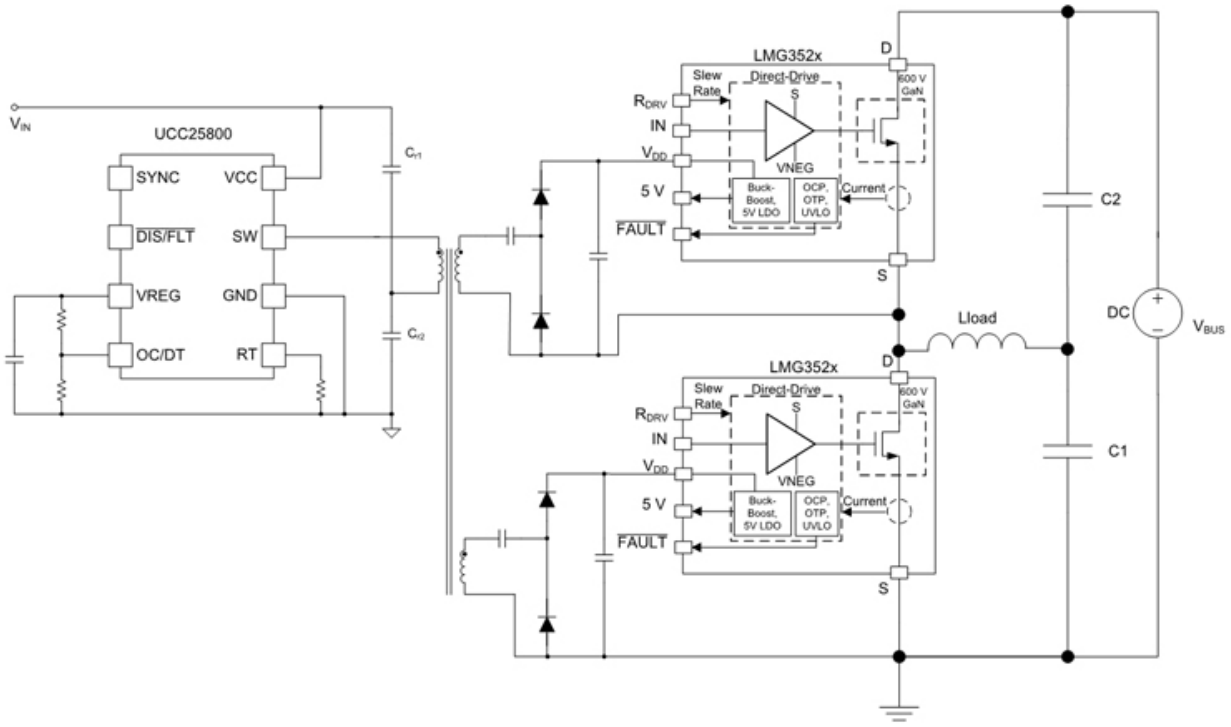

Figure 3. Simplified GaN Half-bridge Configuration Using the UCC25800-Q1 Transformer Driver and Two LMG3522R030-Q1 GaN FETs

The integrated driver shrinks solution size, enabling a power-dense system. Integrating a buck-boost converter also means that the LMG3522R030-Q1 can operate with a 9-V to 18-V unregulated power supply, which significantly reduces bias-supply requirements. To enable a compact and lower-cost system solution, you could combine the LMG3522R030-Q1 with an ultra-low electromagnetic interference transformer driver such as the UCC25800-Q1, which has open-loop inductor-inductor-capacitor control with multiple secondary-side windings. Alternatively, a highly integrated, compact bias power supply such as UCC14240-Q1 DC/DC module can supply the device locally, resulting in a low-profile design with a small printed circuit board footprint.

Conclusion

With the right gate driver and bias supply, GaN devices can help you achieve system-level benefits such as a switching speed of 150 V/ns, reduced switching losses and a smaller magnetics size for high-power systems across industrial and automotive applications. Integrated GaN solutions simplify many of your device-level challenges so that you can focus on the wider system.

Additional Resources

Check out these white papers:

- "Optimizing GaN Performance With an Integrated Driver."
- "Direct Drive Configuration for GaN Devices."
- "Understanding the Trade-Offs and Technologies to Increase Power Density.

View our reference designs:

- 3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density
- 6.6-kW three-phase, three-level ANPC inverter/PFC bidirectional power stage reference design

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