Technical Article

What You Need to Know about Input Bias Current – and Why

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One of my standard interview questions for new college graduates is to describe the non-ideal aspects of an operational amplifier (op amp). While most candidates start with open-loop gain, offset voltage, bandwidth and noise, only a few mention input bias current. Even experienced circuit designers often have questions about input bias current and its effects. In this post, I'll answer some of these questions and hopefully clear up some misconceptions.

Q: What Is Input Bias Current?

A: The term "input bias current" (I_B) in datasheets – for both op amps and fully differential amplifiers (FDAs) – refers to the DC currents flowing into or out of the amplifier's input pins to create a defined operating point during normal operation, as shown in Figure 1.

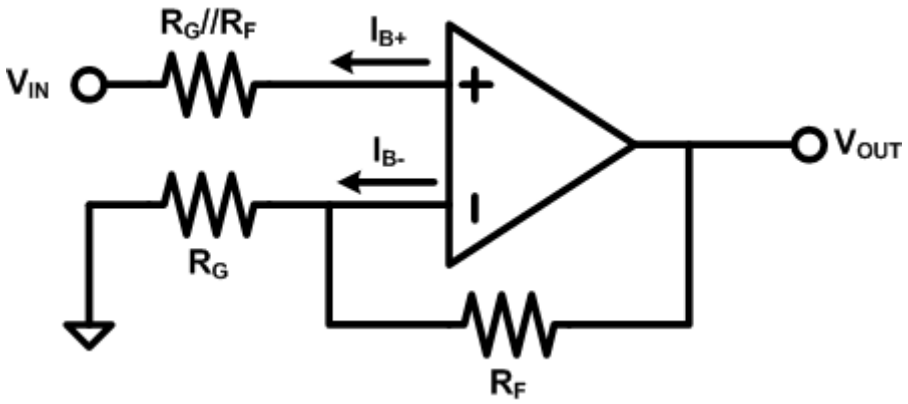

Figure 1. Definition of Input Bias Current for a Simple PNP Input Stage

Because a MOSFET requires very little DC gate current to operate, the input bias current of a CMOS amplifier is dominated by leakage from electrostatic discharge (ESD) protection cells and other secondary circuits connected to the inputs. The magnitude of this leakage current is small – on the order of picoamps (pA). Since the inputs of bipolar junction transistor (BJT) amplifiers require base currents for proper bias, however, the BJT input bias current is a lot larger – on the order of microamps (µA). Hence, input bias current is an important issue for BJT amplifiers.

Q: Why Do You Need BJT-input Amplifiers?

A: Since CMOS amplifiers have almost negligible input bias currents, why do you even need BJT amplifiers? The answer is that a BJT has much larger transconductance (g_m) compared to a CMOS transistor at the same quiescent current. In addition, matching between BJTs is also a lot better, and so is its flicker (or 1/f noise). All three advantages are crucial for high-speed precision amplifiers; hence, BJT inputs are ubiquitous in high-performance op amps and FDAs.

Q: How Do You Evaluate the Effects of Input Bias Currents?

A: While using amplifiers with significant input bias currents often requires some additional design considerations, you might be surprised to find how little they actually affect system performance. Once you understand the effects of input bias current, you can weigh the benefits of a BJT-input amplifier against these effects.

Let's investigate the effects of input bias currents using the FDA circuit shown in Figure 2. The THS4551 is the newest addition to TI's family of precision analog-to-digital converter (ADC) drivers. The THS4551 features not only 150MHz bandwidth on 1.35mA I_q, but also ±2µV/°C max V_{OS} drift, as shown in Table 1. The BJT-input architecture enables such performance but creates a notable I_B.

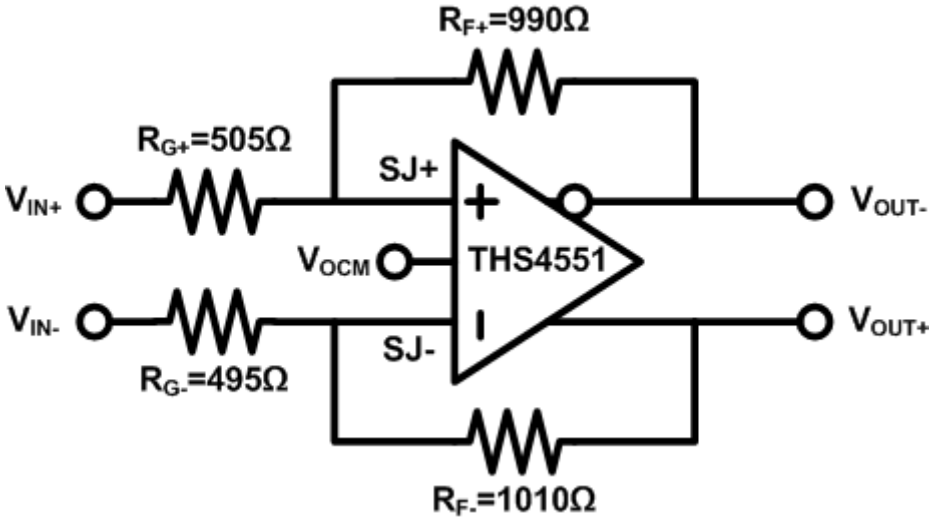

Figure 2. THS4551 FDA Circuit with 1% Resistors

Table 1. Key Input-referred DC Parameters of the THS4551

V_{IO}	Input-referred offset voltage	T_A = 25°C	–175	±50	175	µV
		T_A = 0°C to +70°C	–225		265	
		T_A = –40°C to +85°C	–295		295	
		T_A = –40°C to +125°C	–295		375	
	Input offset voltage drift(4)	T_A = –40°C to +125°C (DGK package)	–2.0	±0.45	2.0	µV/°C
I_{IB}	Input bias current (positive current out of node)	T_A = 25°C	0.55	1.0	1.5	µA
		T_A = 0°C to +70°C	0.41		1.75	
		T_A = –40°C to +85°C	0.2		1.83	
		T_A = –40°C to +125°C	0.2		2.05	
	Input bias current drift(4)	T_A = –40°C to +125°C (DGK package)	2	3.3	5.5	nA/°C
I_{OS}	Input offset current	T_A = 25°C	–50	±10	50	nA
		T_A = 0°C to +70°C	–57		63	
		T_A = –40°C to +85°C	–68		67	
		T_A = –40°C to +125°C	–68		78	
	Input offset current drift(4)	T_A = –40°C to +125°C (DGK package)	–280	±70	280	pA/°C

Focusing on the mathematically simplest case, let's first assume that the FDAs are always connected with symmetrical feedback elements, since this leads to minimum signal conversion from the common-mode errors to the differential output.

You can calculate the "output referred" offset voltage V_{OOS} in two steps. First, find the amplifier's positive and negative summing-junction voltages using Equation 1:

$$V_{SJ\pm} = I_{B\pm} \times Z_{SJ\pm} = I_{B\pm} \times (R_{G\pm} || R_{F\pm}) \qquad (1)$$

Then, use Equation 2 to calculate V_{OUT} based on the gain from the summing junction to the output, which is the noise gain:

$$V_{OUT\mp} = V_{SJ\pm} \times NG_{\pm} = V_{SJ\pm} \times \left(1 + \frac{R_{F\pm}}{R_{G\pm}}\right) = V_{SJ\pm} \times \left(\frac{R_{F\pm}}{R_{G\pm}||R_{F\pm}}\right) \quad (2)$$

Combining Equations 1 and 2 together, you can calculate V_{OOS} at the output as the difference between these two output voltages with Equation 3:

$$V_{OUT\mp} = I_{B\pm} \times (R_{G\pm}||R_{F\pm}) \times \left(\frac{R_{F\pm}}{R_{G\pm}||R_{F\pm}}\right) = I_{B\pm} \times R_{F\pm}$$

$$V_{OOS} = (I_{B+} \times R_{F+}) - (I_{B-} \times R_{F-}) \quad (3)$$

The output V_{OOS} is simply the difference between the input bias currents on each side, multiplied by their respective feedback-resistor values (R_F). The gain resistor (R_G) has dropped out of the V_{OOS} equation. Intuitively, this is because a small R_G, which would have reduced the impact of I_B on the summing-junction voltage, also increases the noise gain from summing junction to output, and the two effects cancel each other.

Let's use the circuit in Figure 2 and the specs of the THS4551 in Table 1 to calculate the worst-case output V_{OOS} from each contributing factor (input V_{OS}, I_B and I_{OS}), listed in Table 2.

Table 2. THS4551 Output Referred Offset Voltage Terms for R_F=1kΩ, 1%

Contributing factor	25°C max error	Worst gain to output	Worst-case contribution to output V_{OOS} (µV)	Gained up by
Input V_{OS}	±175µV	3.04V/V	±532	Noise gain
$I_{B\pm}$	1.5µA	±20Ω	±30	Feedback resistor mismatch
I_{OS}	±50nA	1.01kΩ	±50.5	Feedback resistor

Now, let's look at four cases for different resistor values and tolerances in the circuit. For two values of R_F (1kΩ and 5kΩ) and two tolerances (1% and 0.1%), Table 3 shows the results.

Table 3. THS4551 Output Referred Offset Voltage Terms for Different R_F Choices

Case	RF (kΩ)	RF tolerance (%)	Worse-case output V_{OOS} terms (µV)		
			V_{OS}	$I_{B\pm}$	I_{OS}
1	1	1	±532	±30	±50.5
2	1	0.1	±526	±3	±50.1
3	5	1	±532	±150	±252.5
4	5	0.1	±526	±15	±250.3

Similarly, Table 4 shows the results for the output-offset drift.

Table 4. THS4551 Output Referred Offset Drift Terms for Different R_F Choices

Case	RF (kΩ)	RF tolerance (%)	Worse-case output V_{OOS} drift terms (µV/°C)		
			V_{OS}	$I_{B\pm}$	I_{OS}
1	1	1	±6.1	±0.11	±0.283
2	1	0.1	±6	±0.01	±0.28
3	5	1	±6.1	±0.55	±1.41
4	5	0.1	±6	±0.06	±1.4

A couple of takeaways:

- A well-designed BJT-input FDA or op amp should be able to handle several kilo-ohms of R_F without much effect on DC performance.
- When DC performance is a concern, consider improving the resistor R_F and R_G tolerances to 0.1%, which is a simple and inexpensive method to mitigate the negative effects of I_B.

Q: What about Input-current Noise?

A: Most of this post is about the impact of I_B and I_{OS} on offset voltage and offset-voltage drift. Another important effect of input current is added noise. Luckily, noise is just a time-varying offset, so you can calculate the effect of noise just as you calculated the effect of offset. For example, the output-voltage noise due to the input-current noise is simply

Another issue worth mentioning is internal input-bias cancellation. Various cancellation techniques can usually reduce I_B from the level of microamps to nanoamps. The I_{OS} will also be reduced, although not nearly as much. However, these cancellation techniques usually increase input-current noise due to uncorrelated noise from the cancellation current. So if noise limits your system's performance, input-bias cancellation is likely not the right choice.

Conclusion

Compared to CMOS-input amplifiers, BJT-input op amps and FDAs offer many benefits: higher bandwidth at lower power, lower voltage noise and 1/f noise, and better DC precision. They come with one catch, however: higher input bias currents. With careful design, you can evaluate and mitigate the negative effects of the higher input bias currents.

What is your experience dealing with issues due to input bias current? I have only scratched the surface of I_B effects, and haven't mentioned many secondary issues. What more do you want to know? Log in below and leave a comment.

Additional Resources

- Read more about the THS4551 and learn about the equations involving FDA offset calculations.
- Check out this module on input bias current from TI Precision Labs.
- Learn about TI's entire portfolio of high-speed op amps and explore related technical resources.

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