TPS65921 USB Charger Detection

ABSTRACT

The TPS65921 has a USB charger detection system. This document intends to clarify the use of this feature.

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1 Introduction

The TPS65921 has a USB connection monitoring system that can determine if a USB100 or USB500 is connected.

- USB100: Refers to standard downstream port (SDP)
- USB500: Refers to charging downstream port (CDP) or dedicated charging port (DCP)

This document explains how use this capability.

2 Requirement Before Starting a USB Charger Detection

2.1 TPS65921 State

The USB charger detection Finite State-Machine (FSM) works only when the TPS65921 is in ACTIVE or SLEEP state (SYSACTIV = high, corresponding to the NRESPWRON signal).

2.2 VBUS Presence

For the USB charger detection to function, the USB_P signal must be High (VBUS presence with 10ms debounce).

USB_P status can be read in bit 4 of the USB_DTCT_CTRL register.

2.2.1 USB_DTCT_CTRL Register

Table 1. USB_DTCT_CTRL

I2C address	0x4A		
Register address	0x76	**Instance**	ACCESSORY_VINTDIG
Description	Battery charger controller (BCC) status bits		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	USB_500	USB_100	USB_P_STS	USB_DET_STS		USB_SW_CHRG_CTRL_EN	USB_HW_CHRG_DET_EN

Bits	Field Name	Description	Type	Reset
7	RESERVED		RORreturns0s	0
6	USB_500	Can be write-only when USB_SW_CHRG_CTRL_EN is set to 1. Set USB500_P signal. Status of FSM USB500_P when USB_SW_CHRG_CTRL_EN is disabled and USB_HW_CHRG_DET_EN set to 1.	RW	0
5	USB_100	Can be write-only when USB_SW_CHRG_CTRL_EN is set to 1. Set USB100_P signal. Status of FSM USB100_P when USB_SW_CHRG_CTRL_EN is disabled and USB_HW_CHRG_DET_EN set to 1.	RW	0
4	USB_P_STS	Status of USBVBUS_PRES signal with 10 ms debounce time. When set to 1, USB FSM is active according to enable bit setting.	RO	0
3:2	USB_DET_STS	Status of USB charger presence and USB charger type. Read 0x0: 00 => No USB charger detected. Read 0x1: 01 => 100-mA charger detected. Read 0x2: 10 => 500-mA charger detected. Read 0x3: 11 => Undefined.	RO	0x0
1	USB_SW_CHRG_CTRL_EN	Let the software control USB current sources and comparator outputs directly through register. USB dedicated FSM for detection is bypassed if this bit is set to 1.	RW	0
0	USB_HW_CHRG_DET_EN	Software enable of USB hardware FSM for USB detection. Enable automatic charger detection (used to enable CHGD IBIAS block). Once enabled, the USB_CHG_TYPE interrupt is generated once a USB 100-mA or USB 500-mA charger is detected.	RW	0

2.3 USB Transceiver Configuration

Software must configure the power resources and USB transceiver.

To access the USB registers, VUSB3P1, VUSB1P8, VUSP1P5 must be ON.

Dedicated DP/DM (15k) pulldowns have been added in the charger detection analog block. They are physically distinct from DP/DM (15k) pulldowns in the USB PHY block controlled by the OTG_CTRL[1] DPPULLDOWN and OTG_CTRL[2] DMPULLDOWN bits.

In ACTIVE and SLEEP states, the DPPULLDOWN and DMPULLDOWN bits in the OTG_CTRL register are 1 by default.

To avoid any detection error, software must ensure that the USB transceiver is not driving the DP and DM pins by setting the FUNC_CTRL[4:3] OPMODE bit field to 0x1 (nondriving) before initiating charger detection.

Setting the USB transceiver in nondriving mode automatically disables the DPPULLDOWN and DMPULLDOWN bits. Also, the USB PHY can be powered down before starting USB charger detection (the USB PHY can be powered down by setting the PHY_PWR_CTRL[0] PHYPWD bit to 1). Powering down the USB PHY is not mandatory, however, because setting the FUNC_CTRL[4:3] OPMODE bit field to 0x1 is already sufficient to avoid charger detection conflict.

2.3.1 VUSB1V5_DEV_GRP Register

Table 2. VUSB1V5_DEV_GRP

I2C address	0x4B		
Register address	0xCC	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB1V5 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

2.3.2 VUSB1V8_DEV_GRP Register

Table 3. VUSB1V8_DEV_GRP

I2C address	0x4B		
Register address	0xCF	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB1V8 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

2.3.3 VUSB3V1_DEV_GRP Register

Table 4. VUSB3V1_DEV_GRP

I2C address	0x4B		
Register address	0xD2	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB3V1 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device group 000: Belongs to no device group 001: Belongs to P1 device group 010: Belongs to P2 device group 011: Belongs to P1 and P2 device groups 100: Belongs to P3 device group 101: Belongs to P1 and P3 device groups 110: Belongs to P2 and P3 device groups 111: Belongs to all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the WARMRESET state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the WARMRESET state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

2.3.4 FUNC_CTRL Register

Table 5. FUNC_CTRL

I2C address	0x48		
Register address	0x04	**Instance**	USB
Description	Controls UTMI function settings of the PHY.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	RESERVED		RO	0
6	SUSPENDM	Active low PHY suspend. Put PHY into low-power mode. In low-power mode the PHY powers down all blocks except the full-speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically sets this bit to 1 when low-power mode is exited.	RW	1
5	RESET	Active high transceiver reset. Does not reset the ULPI interface or ULPI register set. Once set, the PHY asserts the DIR signal and resets the UTMI core. When the reset is complete, the PHY deasserts DIR and clears this bit. After deasserting DIR, the PHY reasserts DIR and sends an RX command update. **Note:** This bit is auto-cleared; this explains why it cannot be read at 1.	RW	0
4:3	OPMODE	Select the required bit encoding style during transmit: 0x0: Normal operation 0x1: Nondriving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved	RW	0x0
2	TERMSELECT	Controls the internal 1.5-kΩ pullup resistor and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown, and DmPulldown.	RW	0
1:0	XCVRSELECT	Select the required transceiver speed.	RW	0x1

2.3.5 PHY_PWR_CTRL Register

Table 6. PHY_PWR_CTRL

I2C address	0x48		
Register address	0xFD	**Instance**	USB
Description	Controls the PHY state. It can be access only through I2C.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PHYPWD

Bits	Field Name	Description	Type	Reset
7	RESERVED		RO	0
6	RESERVED		RO	0
5	RESERVED		RO	0
4	RESERVED		RO	0
3	RESERVED		RO	0
2	RESERVED		RO	0
1	RESERVED		RO	0
0	PHYPWD	Power down entire PHY. 0b: Normal state 1b: Power down	RW	0

3 Enabling USB Charger Detection FSM

To enable the USB charger detection FSM, the following accesses must be performed:

1. Set USB_SW_CHRG_CTRL_EN (set bit 1 of USB_DTCT_CTRL to 1).
2. Set USB_HW_CHRG_DET_EN and unset USB_SW_CHRG_CTRL_EN (set bit 1 and bit 0 of USB_DTCT_CTRL to 1).

4 Reading USB Charger Detection Result

An interrupt occurs once a charger is detected. The INT1 line is pulled down and bit 0 of the ACCISR1 register is set to logic 1. Set this bit to 1 to release the interrupt line.

The detection result can be read in the USB_DET_STS[1:0] bit field of the USB_DTCT_CTRL register.

4.1 ACCISR1 Register

Table 7. ACCISR1

I2C address	0x4A		
Register address	0x79	**Instance**	ACCESSORY_VINTDIG
Description	The INTERRUPT STATUS ISR1A REGISTER is used to determine which monitoring function interrupt triggered the interrupt line PO_BCI_SIH_INT1_N request. When a bit in this register is set to 1, it indicates that the corresponding monitoring function is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR1 REGISTER. When a bit in this register is set to 1 then the corresponding interrupt line is released. If the user sets a bit in this register to 0, the value remains unchanged. The INTERRUPT STATUS ISR1 REGISTER is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED							USB_CHRG_TYPE_ISR1

Bits	Field Name	Description	Type	Reset
7:1	RESERVED		RO	0x00
0	USB_CHRG_TYPE_ISR1	Interrupt USB_CHG_TYPE is generated once automatic detection detects a USB 100-mA or USB 500-mA charger. This interrupt is only available when: Write 0: No impact; register keeps its value Read 0: No interrupt set Read 1: Interrupt set Write 1: When set to 1, the corresponding line is released	RW	0

5 Stopping Charger Detection

Software must stop the charger detection such that the timing complies with the USB connect ECN TSVLD_CON_PWD specification of 1 s.

To stop the detection, set USB_HW_CHRG_DET_EN to 0 (set bit 0 of USB_DTCT_CTRL to 0)

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