Powering OMAP™3 With TPS65950: Design-In Guide

User's Guide

Literature Number: SWCU056C
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Powering OMAP™3 With TPS65950: Design-In Guide

1 Introduction

This document describes the system hardware implementation for the OMAP3530 device and the TPS65950 companion [power integrated circuit (IC). The document concentrates on the power connectivity for the processor and the companion power IC. The document also briefly explains some other specifics related to power, such as the boot modes and the power-up sequence.

1.1 Purpose

The purpose of this system hardware implementation document is to describe the system design of the OMAP3530-TPS65950 solution

1.2 Audience

This document is for an audience using the OMAP3530 with the TPS65950 companion power IC for any application.

1.3 References

Table 1 lists reference documents that support this document.

Table 1. Reference Documents

Document	Rev
OMAP35xx Technical Reference Manual (SPRUF98)	
OMAP3530 Data Manual	
TPS65950 Technical Reference Manual (SWCU050)	
TPS65950 Data Manual (SWCS032)	

2 System

This document describes the hardware interconnection between the OMAP3530 and its TPS65950 companion power IC.

2.1 Platform

The platform that supports the system is built on the OMAP3530 and the TPS65950 companion chip:

- The OMAP3530 is the first device in TI's OMAP™ 3 architecture to combine mobile entertainment with high-performance productivity applications:
  - First processor with advanced Superscalar ARM® Cortex™-A8 reduced instruction set computer (RISC) core, enabling 3x gain in performance
  - First processor designed in 65-nm complementary metal oxide semiconductor (CMOS) process technology, adding processing performance
  - Image/video/audio (IVA) 2+ accelerator, enabling multistandard (MPEG-4, WMV9, RealVideo®, H263, H264) encoding/decoding at D1 (720 x 480 pixels) 30 frames per second (fps)
  - Integrated image signal processor (ISP) for faster, higher-quality image capture and lower system cost
  - Leverage of SmartReflex™ technologies for advanced power reduction
  - M-shield™ mobile security enhanced with ARM TrustZone™ support
  - High-level operating system (HLOS) support for customizable interface
- The TPS65950 IC is an integrated power-management IC for applications powered by Li-Ion or Li-Ion polymer batteries or Li-Ion batteries with cobalt-Ni-manganese anodes. It is a generic companion chip that can be connected to an application processor. It contains buck converters, low-dropout regulators (LDOs), a charger module, an entire audio module with digital filters, input amplifiers, and output class-D amplifiers. The TPS65950 IC provides several additional functions, such as a high-speed (HS) universal serial bus (USB) physical layer (PHY) transceiver.

2.2 Overview of Connectivity

Figure 1 is an overview of top-level connectivity.

Figure 1. Top-Level Connectivity

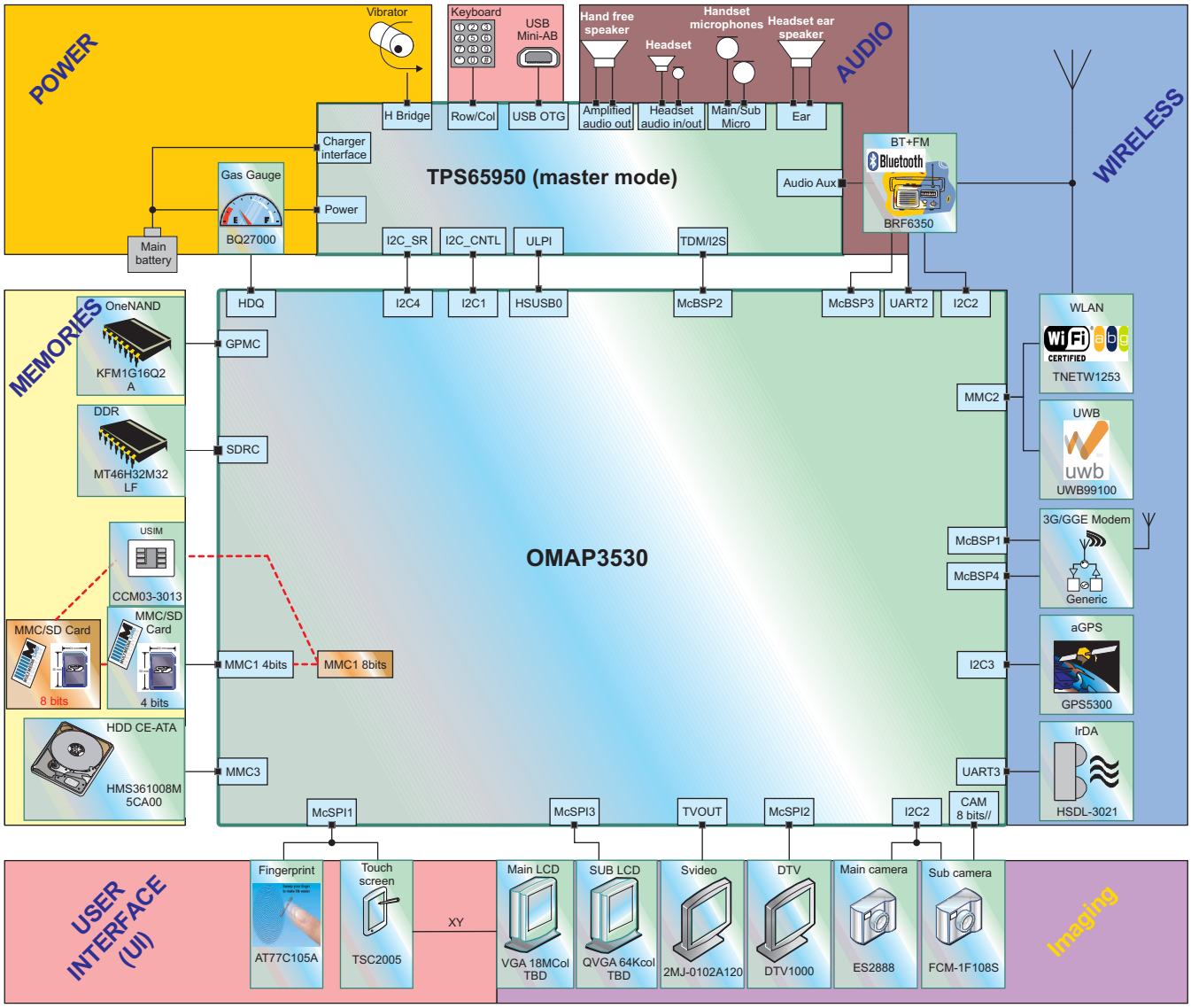


Figure 1 shows the complete capability and connections for a typical OMAP3 architecture platform. This document does not describe all the peripherals for OMAP3 design. This document concentrates on the power connections for OMAP using the companion IC.

3 System Interconnect

This section describes the interconnections within the system, outlining for each function the power and clock requirements. Whenever applicable, design constraints and limitations are given.

3.1 Platform

The platform, or host system, is composed of the OMAP3530 and the TPS65950 companion IC. The following sections describe the connections in the host system only. Information about the specific functions supported by the platform is in their respective sections.

3.1.1 Features

The TPS65950 companion IC is the system clock manager:

- It generates a 32-kHz clock from a crystal or an external sine wave and delivers a square digital waveform to the entire system.
- It collects all the high-frequency clock requests from the system and forwards the demand to the system clock source.
- It buffers the high-frequency clock from the source and delivers a square digital waveform to the entire applicative system.

3.1.1.1 Power-On and Reset Management

The TPS65950 companion IC is the system power-on and reset manager:

- A push-button debouncing starts the state-machine (master configuration).
- It controls the reset release of the OMAP3530.
- It controls the warm reset steps when instructed to do so by the OMAP3530 or the user.
- It can control power-on of an auxiliary subsystem.

3.1.1.2 Power Management

The TPS65950 companion IC is the system power manager:

- It integrates several power supplies (DCDC/SMPS or LDO types) to meet the system demands in terms of currents and voltages.
- It is the processor power companion, providing all required power supplies and power-management functions (dynamic voltage scaling, SmartReflex) to the OMAP3530. SmartReflex is controlled through a dedicated HS inter-integrated circuit (I2C™) link.
- It can control the activation of additional power resources (external LDOs).

3.1.1.3 System Management

TPS65950 modes of operation and states are entirely configurable through register access using the HS I^2C configuration interface. Additionally, the TPS65950 IC implements:

- Several functional interrupts that can be routed to one or two targets
- Internal and external signal monitoring, with the analog-to-digital conversions requested by software or by hardware
- Secure software access protocols for digital rights management (DRM)

3.1.2 Block Diagram

Figure 2 is a block diagram of platform interconnections.

Figure 2. Platform Interconnections

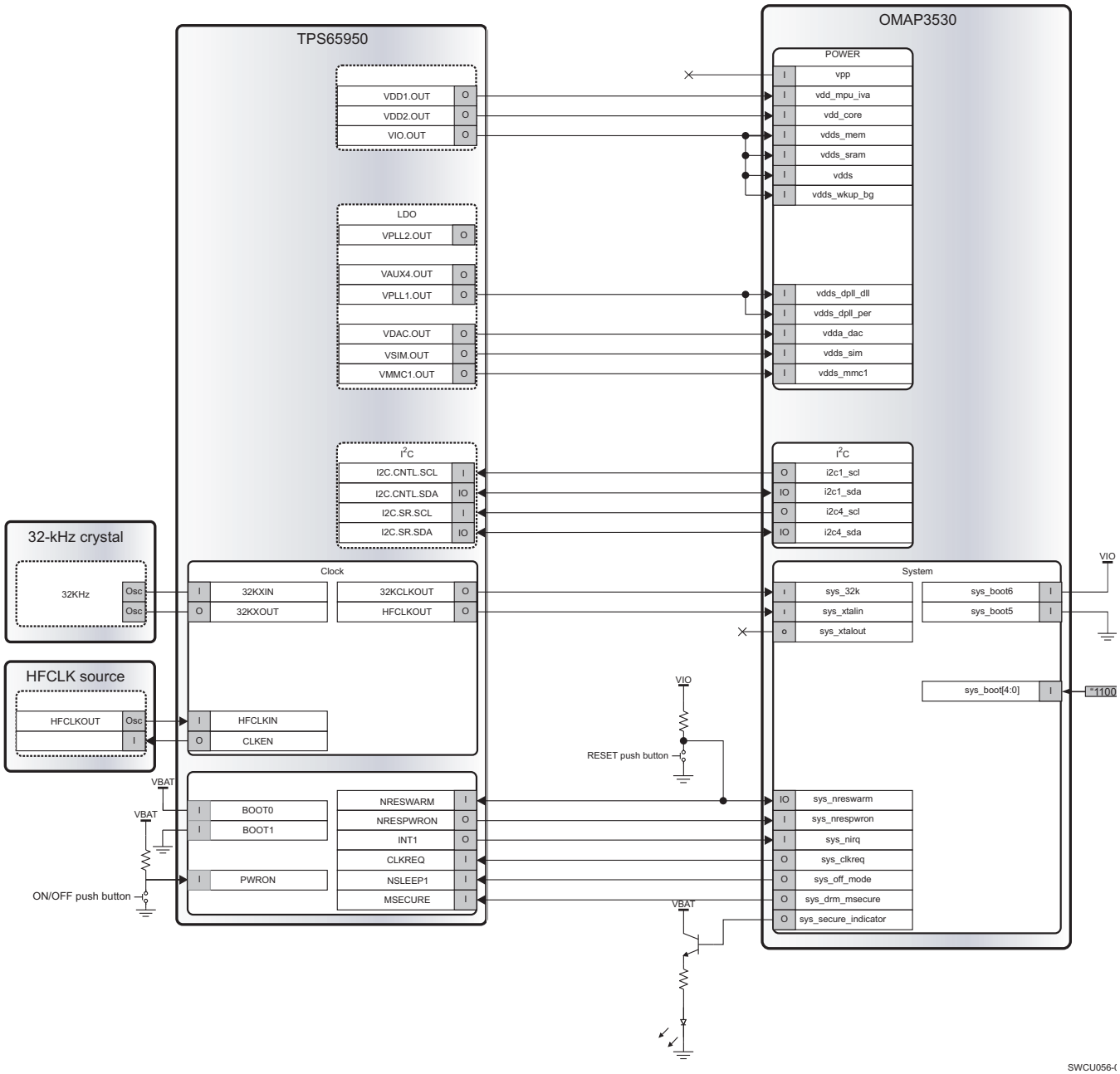


Figure 2 is an overview of power, clocks, and reset management connections. For detailed power connections, see Figure 3.

3.1.3 Controls and Data Interconnections

Table 2 lists the platform controls and data interconnections.

Table 2. Platform Controls and Data Interconnections

Signal ID	Mode	Ball	Power Domain	Dir	Signal ID	Mode Ball	Power Domain
OMAP3530					TPS65950		
sys_nreswarm	0	AF24	VDDS1		NRESWARM	B13	IO_1P8
sys_nrespwron	0	AH25	VDDS1		NRESPWRON	A13	IO_1P8

Table 2. Platform Controls and Data Interconnections (continued)

Signal ID	Mode	Ball	Power Domain	Dir	Signal ID	Mode Ball	Power Domain
sys_nirq	0	AF26	VDDS1		INT1	F10	IO_1P8
sys_clkreq	0	AF25	VDDS1		CLKREQ	G10	IO_1P8
sys_off_mode	0	AF22	VDDS1		NSLEEP1	P7	IO_1P8
sys_drm_msecure	1	AF9	VDDS1		MSECURE	H8	IO_1P8
OMAP3530					Push button		
sys_nreswarm	0	AF24	VDDS1		NRESWARM		

3.1.4 Boot Pin Interconnections

The TPS65950 companion IC has the following boot pin connections:

- BOOT0 pin is tied to 1.
- BOOT1 pin is tied to ground.

3.1.5 Power Requirements

Table 3 lists the platform power requirements.

Table 3. Platform Power Requirements

Signal ID	Type	Vmin	Vnom	Vmax	Domain
VBAT	Input	2.7	3.6	4.5	Battery pack positive terminal
CP.IN	Input	2.7	3.6	4.5	USB charge pump
VAUX12S.IN	Input	2.7	3.6	4.5	VAUX1/2 and VSIM
VPLLA3R.IN	Input	2.7	3.6	4.5	VPLL1/2, VAUX3, and VRTC
VAUX4.IN	Input	2.7	3.6	4.5	VAUX4
VMMC1.IN	Input	2.7	3.6	4.5	VMMC1
VMMC2.IN	Input	2.7	3.6	4.5	VMMC2
VDAC.IN	Input	2.7	3.6	4.5	VDAC and VINTANA1/2
VDD1.IN	Input	2.7	3.6	4.5	VDD1
VDD2.IN	Input	2.7	3.6	4.5	VDD2
VIO.IN	Input	2.7	3.6	4.5	VIO
VBAT.USB	Input	2.7	3.6	4.5	USB LDOs
VAC	Input	2.7	3.6	4.5	Charger
VBUS	Input	2.7	3.6	4.5	USB supply

3.1.6 Clock Requirements

Table 4 lists the clock requirements for the TPS65950 companion IC.

Table 4. Platform Clock Requirements

Pad	Clock Frequency		Stability	Duty Cycle
32KXIN 32KXOUT	32.768 kHz	Crystal	±30 ppm	40%/60%
		Square wave	–	45%/55%
		Sine wave	–	–
HFCLKIN	19.2 MHz, 26 MHz, 38.4 MHz	Square wave	±150 PPM	–
		Sine wave	–	–

3.1.7 Constraints and Limitations

3.1.7.1 I^2C Bus

The I^2C interfaces are HS interfaces. Consequently, the I^2C clock signal can reach 3.4 MHz. This indication must be considered in the case of connecting other I^2C devices not necessarily compliant with that standard.

3.1.7.2 Msecure

If used, Msecure must be driven by OMAP3530 software to allow or prevent writing in the TPS65950 real-time clock (RTC) register and hash tables. If unused, the TPS65950 MSECURE pin must be tied to VIO. For instance, sys_secure_indicator can be used to indicate Msecure activation by driving an LED.

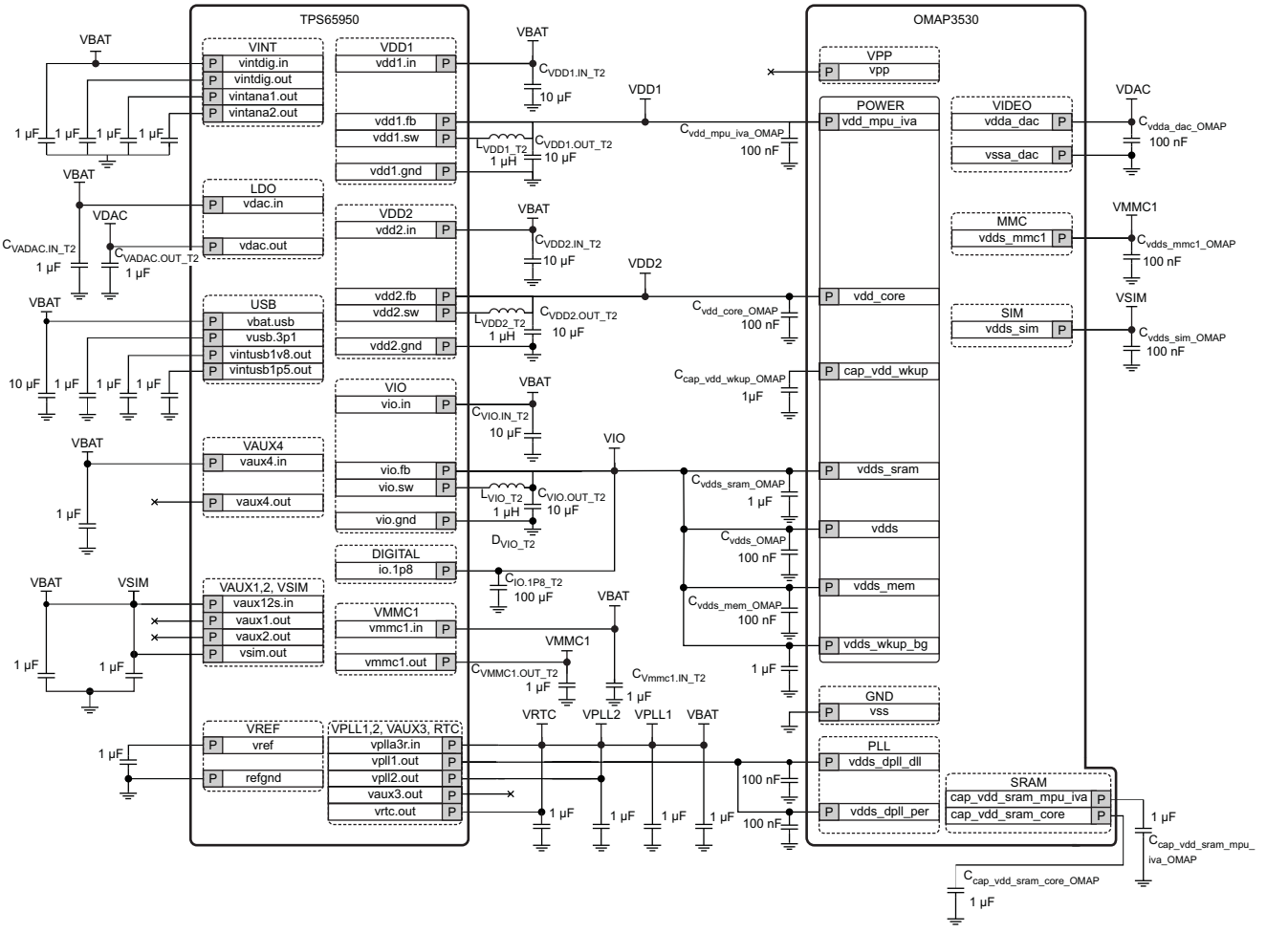
3.2 Power Distribution

3.2.1 Platform Power Distribution

3.2.1.1 Block Diagram

Figure 3 shows the platform power supply, based on the OMAP3530 application processor and the TPS65950 power IC chip.

Figure 3. TPS65950-OMAP3530 Platform Power Distribution



3.2.1.2 Resources

Table 5 lists the TPS65950 power resources.

Table 5. TPS65950 Power Resources

Signal ID	Type	Vrange/Vlist	Step/Accuracy	Imax
VDD1_OUT	SMPS	0.6 to 1.45 V	12.5 mV	1.2 A
VDD2_OUT	SMPS	0.6 to 1.45 V	12.5 mV	600 mA
VIO_OUT	SMPS	1.8, 1.85 V	4%	600 mA
VDAC_OUT	LDO	1.2, 1.3, 1.8 V	3%	70 mA
VPLL1_OUT	LDO	1.0, 1.2, 1.3, 1.8, 2.8, 3.0 V	3%	40 mA
VPLL2.OUT	LDO	0.7, 1.0, 1.2, 1.3, 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15	3%	100 mA
VMMC1_OUT	LDO	1.85, 2.85, 3.0, 3.15 V	3%	220 mA
VMMC2_OUT	LDO	1.0, 1.2, 1.3, 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15 V	3%	100 mA
VSIM_OUT	LDO	1.0, 1.2, 1.3, 1.8, 2.8, 3.0 V	3%	50 mA
VAUX1_OUT	LDO	1.5, 1.8, 2.5, 2.8, 3 V	3%	200 mA
VAUX2_OUT	LDO	1.3, 1.5, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.3, 2.4, 2.5, 2.8 V	3%	100 mA
VAUX3_OUT	LDO	1.5, 1.8, 2.5, 2.8, 3.0 V	3%	200 mA
VAUX4_OUT	LDO	0.7, 1, 1.2, 1.3, 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15 V	3%	100 mA

Additional resources are described in relevant SID sections.

3.2.1.3 Distribution Summary

Table 6 lists the power distribution.

Table 6. Power Distribution

Signal ID	Vnom	Imax	Dir	Signal ID	Imax
TPS65950				OMAP3530	
VDD1	0.6 to 1.45 V	1100 mA		vdd_mpu_iva	1200 mA
VDD2	0.6 to 1.45 V	600 mA		vdd_core	600 mA
VIO	1.8 and 1.85 V	600 mA		vdds_sram	41 mA
				vdds	63 mA
				vdds_mem	37 mA
				vdds_wkup_bg	6 (25 mA in emul mode)
				Total	**147 mA**
VDAC	1.2 to 1.8 V	70 mA		vdda_dac	65 mA
VMMC1	1.85 or 3.15 V	220 mA		vdds_mmc1	60 mA
VPLL1	1, 1.2, 1.3, 1.8 V	40 mA		vdds_dpll_dll	25 mA
				vdds_dpll_per	15 mA
				Total	**40 mA**

NOTE:

- If any LDO is not used, the corresponding output pin must be left floating.
- If any DCDC is not used, the corresponding output pin must be floating and the feedback pin must be grounded.

3.2.1.4 Constraints and Limitations

- The power traces from the TPS65950 companion IC to the OMAP3530 must be large enough to supply the maximum current required by OMAP. Avoid thin traces on supply lines. Choose short and wide traces whenever possible.
- All digital, CLK, RF lines must be far from power traces to avoid any noise coupling effect.
- Put the via to GND very close to the GND pad of the decoupling capacitor (in the pad if possible).
- The supply trace coming from the TPS65950 companion IC must go first to the decoupling capacitor and then to the relevant OMAP3530 power ball.
- The decoupling capacitors must be placed as near as possible of the TPS65950 companion IC and OMAP power balls.
- Ideally, place the decoupling capacitor in the same layer as the chip, to avoid any additional parasitic inductor causes by vias.

For more information about layout, see the TPS65950 Layout Guide (SWCU055).

4 System Modes

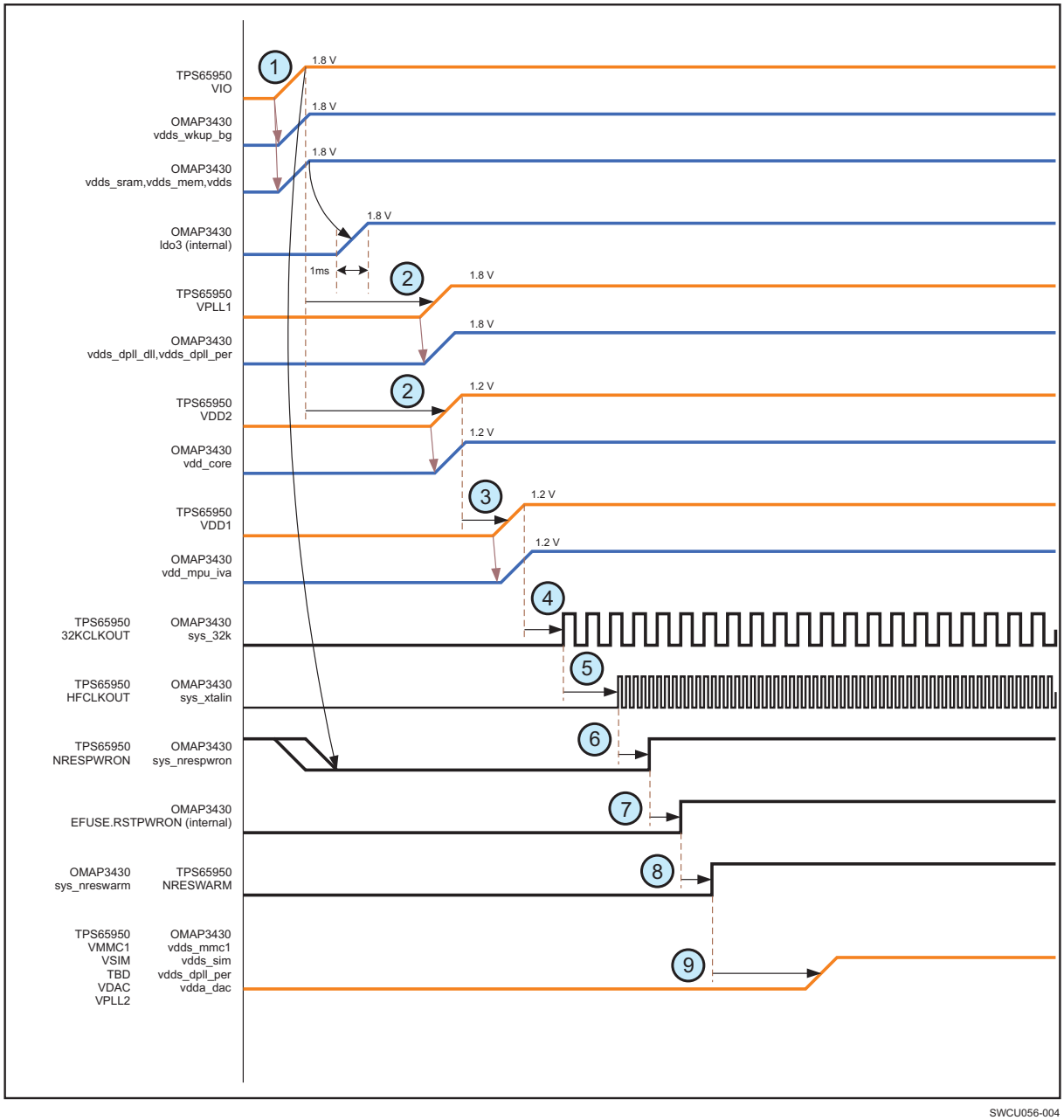
4.1 Power Up and Reset

4.1.1 Platform Power-up and Reset Sequence

4.1.1.1 Platform Power-up Sequence

Figure 4 shows the platform power-up sequence.

Figure 4. Platform Power-Up Sequence Chronogram



SWCU056-004

The power-up sequence includes the following main steps:

1. TPS65950 VIO is ramped up:
   (a) The vdds_wkup_bg, vdds_mem, vdds_sram, and vdds balls of the OMAP3530 are supplied.

(b) The OMAP3530 internal LDO (LDO3) ramps up.

(c) sys_nrespwron is asserted low.

2. TPS65950 VPLL1 and VDD2 ramp up:
   (a) The OMAP3530 vdds_dpll_dll, vdds_dpll_per, and vdd_core balls are supplied.
   (b) Wait for VDD2 stabilization.
3. TPS65950 VDD1 is ramped up:
   (a) The vdd_mpu_iva ball of OMAP3530 is supplied.
   (b) Wait for VDD1 stabilization.
4. The 32-kHz clock is delivered by the TPS65950 IC: The OMAP3530 reset manager holds the entire device under reset.
5. The HF clock is provided by the TPS65950 IC: The HF clock is gated by the OMAP3530 power, reset, and clock management (PRCM) module.
6. NRESPWRON is released by the TPS65950 IC: OMAP3530 boots (sys_nrespwron can be released as soon as the vdds_dpll_dll power rail is stabilized and sys_xtalin and sys_32k are stabilized).
7. The OMAP3530 performs an eFuse check.
8. The OMAP3530 releases sys_nreswarm.
9. Auxiliary TPS65950 ICs are switched on by software on demand.

4.1.1.2 Platform Power-off Sequence

The TPS65950 power-off sequence includes the following steps:

1. System reset. sys_nrespwron is asserted by the TPS65950 IC and the HF clock is stopped.
2. All power resources of the TPS65950 IC are switched off.

4.2 Boot

4.2.1 TPS65950 Boot Description

The TPS65950 IC acts as the master power IC for the OMAP3530 platform. The TPS65950 IC has two possible boot modes when used with the OMAP3530 processor: master mode and slave mode. These two modes can be configured by two hardware input pins as shown in Table 7.

Table 7. TPS65950 Boot Modes

Boot Mode	BOOT0	BOOT1
Master	1	0
Slave	1	1

In master mode, the TPS65950 IC accepts a power-on button and controls the other power ICs in the system. The master power IC decides to power up or down the system. In slave mode, the TPS65950 IC is controlled by another device in the system with a digital signal on the PWRON input.

4.2.2 Boot Process Mode (BOOT0 Signal)

The TPS65950 IC can experience two different behaviors at booting, depending on the BOOT0 signal. This signal sets three different parameters:

- The boot core voltage delivered by the TPS65950 IC
- The power sequence
- The DVFS control protocol

In this system, the TPS65950 IC is set in C0.21 boot process mode (BOOT0 = 1). This implies:

- Boot core voltage is 1.2 V.
- The power-up sequence is VIO first, then VDD1 and VDD2.

- The DVFS protocol is SmartReflex.

4.3 Resets and Clocks

4.3.1 Resets

Following are the reset functions available on this device. TPS65950 is the system power-on and reset manager:

- A push-button debouncing starts its state-machine (master configuration). The pin controlling this function is the PWRON pad.
- It controls the reset release of the applicative part of OMAP3430. The pin controlling this function is the nRESPWRON pad.
- It controls the warm reset steps when instructed to do so by the processor or the user. The pin controlling this function is the nWARMRESET pad.
- It can optionally control the power on of an auxiliary subsystem (additional power-on manager such as the RF subsystem power IC). The pin controlling this function can be REGEN, SYSEN, or any other power resource.

4.3.1.1 PWRON

The PWRON signal is activated by a push button when the device is in master mode. In master mode, the voltage on this input is the battery voltage. PWRON can also be driven by a digital signal when the device boots up in slave mode. In slave mode, PWRON is activated when driven high by the master power IC.

In some specific user cases, a push button is not essential. In this case, PWRON can be connected to the battery supply. If this is done, then connecting the battery supply on the VBAT pin acts as the power-on event. Care must be taken to ensure that the battery supply is stable and more than the threshold. The threshold for the VBAT trigger to power on the device is 3.2 V ± 100 mV.

4.3.1.2 nRESPWRON

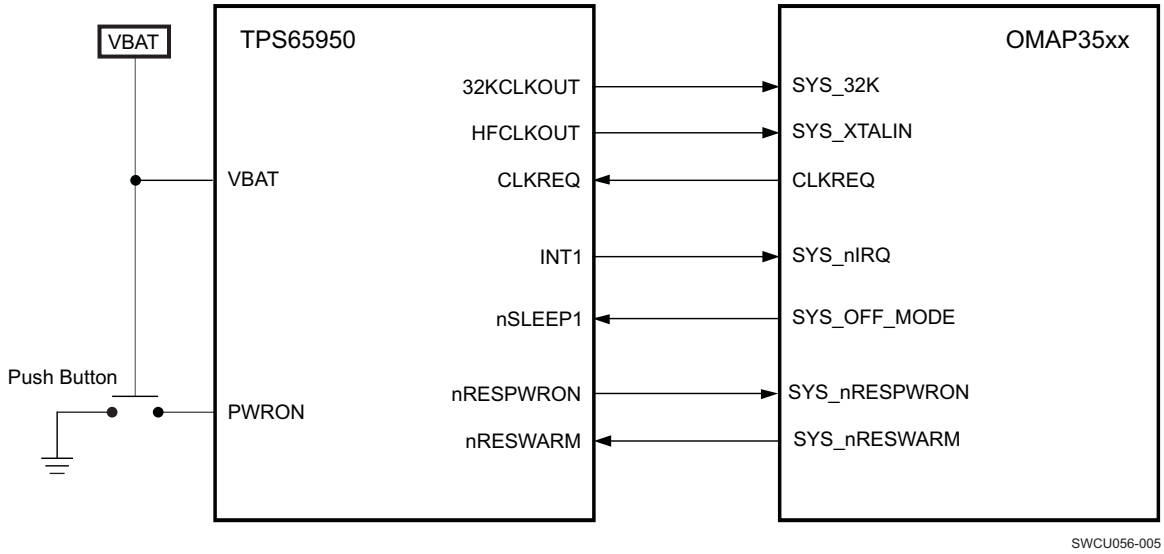
The nRESPWRON output signal is the reset signal delivered to the OMAP processor at power-on reset (POR) when the core voltages and input/output (I/O) supplies are correctly set up. See the power up sequence diagram shown in Figure 4.

4.3.1.3 nWARMRESET

nRESWARM is an active low input reset signal to the device. Depending on the application, this signal can be connected to a reset button, an RC cell, or the warm reset output of the OMAP application processor.

This reset signal can be used to put the device into a known stable state. For the warm reset signal to be functional there should be a predefined sequence programmed in the device memory. For details about this sequence,see the TRM.

Figure 5. Reset and Control Connections



NOTE: If the system does not power up correctly and REGEN keeps toggling, try grounding the TEST.RESET pin. On some platforms keeping TEST.REST floating created instability.

4.3.1.4 Resetting the System

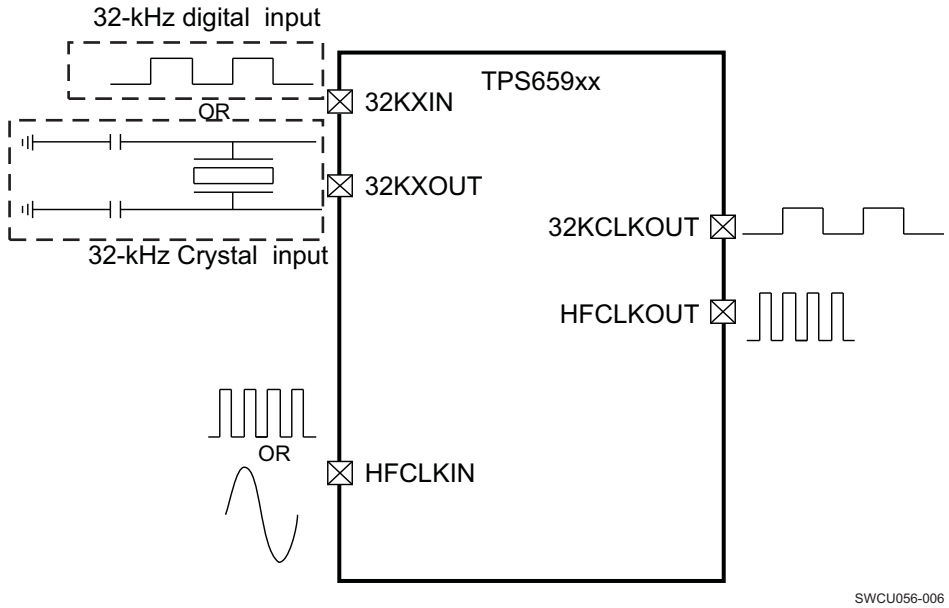
There are two resets available on TPS65950: NRESPWRON and NRESWARM. NRESPWRON is an output from TPS65950 that at initial power-on de-asserts and takes OMAP out of reset. This reset must not be used to reset OMAP asynchronously. If an external circuit is used to assert NRESPWRON to reset OMAP, then this assertion causes OMAP to reset and it may cause the platform to be unstable. When OMAP resets, it de-asserts (drives low) SYS_OFF_MODE signal. If TPS65950 is programmed with a SLEEP sequence, then driving this signal low will change the DCDC output signals as programmed in the sequence. If the DCDC reduces to a level where it cannot power-up OMAP core domains, then the system will hang or be in a weird undefined state.

To avoid the above behavior it is recommended that OMAP and TPS65950 be reset using the warm reset feature on both devices. OMAP warm reset can be configured as an input. If external logic drives the warm reset low on both OMAP and TPS65950, then both devices would be reset without abnormal behavior. Ensure that HFCLK is maintained during a warm reset.

4.3.2 Clocks

This section provides information about the slow and fast clock requirements for the device.

Figure 6. System Clock Connections



4.3.2.1 Slow Clock (32KHz)

The 32-kHz clock (32.768 kHz) circuit can function with either an externally supplied digital signal or a quartz crystal. The 32-kHz clock drives the real-time clock (RTC), which is used by the device for various functions.

Regardless of whether the device 32-kHz oscillator circuit runs directly from a crystal or from an external 32-kHz signal, the device buffers the resulting 32-kHz signal and provides it as 32KCLKOUT, which can be provided externally to the application processor or other devices. The default mode of the 32KCLKOUT signal is active, but it can be disabled.

Table 8. 32-kHz Clock Specifications

Pad	Clock Frequency		Stability	Duty Cycle
32KXIN, 32KXOUT	32.768 kHz	Crystal	± 30 ppm	40% / 60%
		Square wave	–	45% / 55%
		Sine wave	–	–

4.3.2.2 High-Frequency Clock

HFCLKIN is the high-frequency input clock. It can be a square- or sine-wave input clock. If a square-wave clock is provided, it is recommended to switch the block to bypass mode to avoid loading the clock.

The high-frequency clock circuit does not modify the input clock characteristics. It acts as a slicer when a sine wave oscillator is used. If a square wave is supplied at the clock inputs then the clock slicer should be in the bypass mode. In any case, the oscillator clock characteristics are not degraded due to this circuit. For complete compatibility of the clock characteristics ensure that the input high-frequency clock satisfies the OMAP clock requirements.

NOTE: Ensure that the external HF oscillator has a start-up time of less than 5.3 ms. At initial power up the internal design has a default timer that enables HFCLK to OMAP. If HFCLK is not provided to OMAP before nRESPWRON goes high then the system does not function correctly. If the delay cannot be met, a workaround would be to delay the nRESPWRON signal using an external supervisory.

4.4 TPS659xx Power Management Features

The OMAP3 applications processor has various power management features that are supported by the TPS659xx devices. Each power resource on the TPS659xx can be controlled individually or as groups for efficient power management with the OMAP3 applications processor. The power resources can be configured in multiple states.

The resources operating states can be categorized as follows:

- ACTIVE: The power resource is supplying the nominal voltage with full load current capability.
- SLEEP: The power resource is supplying the nominal output voltage with low power consumption but with a low current capability.
- OFF: The output voltage is not maintained and the power consumption is practically zero volts.

These three states can be controlled by the OMAP processor, either through the inter-integrated circuit (I^2C™) bus or using the external control signals, such as the nSLEEP1, nSLEEP2, and CLKREQ.

4.4.1 State Control Using nSLEEP1, nSLEEP2, and CLKREQ Signals

TPS65950 provides the possibility to group its resources into three processorgroups – P1, P2, and P3.

The goal is to group all resources required by the same processor into one group so that their states (ON, OFF, SLEEP) can be changed in unison upon request.

Processor group 1 (P1) is typically used for all resources associated with the application processor, in this case OMAP35xx; processor group 2 (P2) typically contains all resources associated with the modem (if applicable) while processor group 3 (P3) contains the resources associated with peripherals or clock system.

Each resource (such as a power supply, a clock, or an output signal) of TPS65950 can be allocated to none, one, two, or all three processor groups. This allocation is user-programmable; a default allocation exists which depends on the boot mode.

If different resources are allocated to more than one processor group and these processor groups request the resource to be in different states (ON, SLEEP, or OFF) then the resource always enters the highest required state. For instance, if a resource is allocated to P1 and P2, P1 requests ON state and P2 requests SLEEP state, then the resource enters ON state. Conversely, if a resource is not allocated to any processor group it is always in OFF state.

The state control signals nSLEEP1, nSLEEP2, and CLKREQ are used to trigger the execution of state transitions for P1, P2, and P3 respectively.

4.4.2 Power Management Techniques

4.4.2.1 Direct Control Software Scaling Mode (Using VSEL)

Every power resource on the TPS659xx can be controlled for different voltage levels. The OMAP3 application processor can send I^2C commands to set various voltage levels on the power resources. Depending on the voltage and frequency requirement, software can command TPS659xx power resource to change voltage levels accordingly.

This technique can be used for the LDOs on this IC. To control and manage the DCDC output levels it is best to use the SmartReflex technique explained in Section 4.4.2.3.

4.4.2.2 DVFS (Using VMODE)

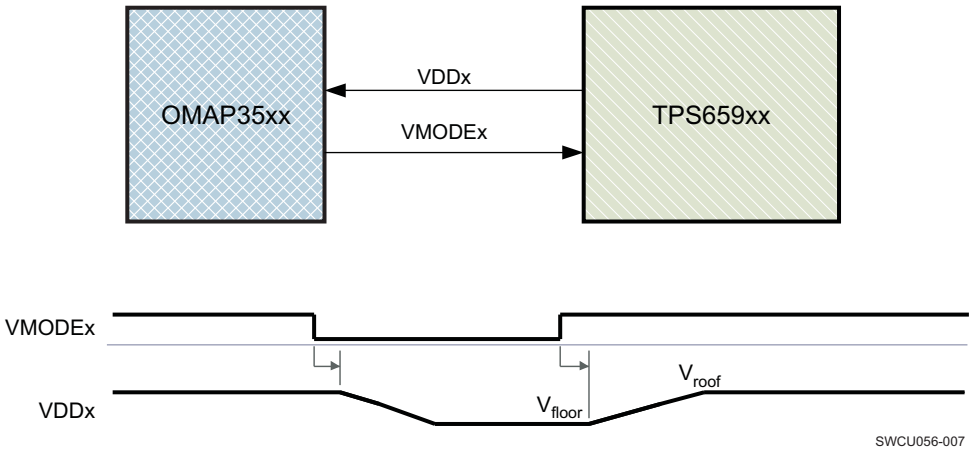
TPS659XX can automatically set the supply voltage of two of its switch mode power supplies (SMPSs), VDD1 and VDD2, to two different levels – V_{ROOF} (the higher level) and V_{FLOOR} (the lower level). This option is disabled by default and can be enabled independently for VDD1 and VDD2 by two dedicated status bits.

The setting of V_{ROOF} and V_{FLOOR} is independent for DCDC1 and DCDC2; that is, different V_{ROOF} and V_{FLOOR} levels can be programmed for DCDC1 and DCDC2. Four dedicated registers are used to set these voltage levels – VDD1_VFLOOR, VDD1_VROOF, VDD2_VFLOOR, and VDD2_VROOF. These registers are programmed through I^2C.

The supply voltage selected depends on the input level of the associated voltage control pin. The VMODE1 pin controls the output voltage of the VDD1 supply while the VMODE2 pin controls the output voltage of the VDD2 supply.

If the VMODE pin is high then the associated power resource supplies V_{ROOF}; if VMODE is low it supplies V_{FLOOR}.

Figure 7. DVFS Control using VMODE pin



4.4.2.3 SmartReflex

With SmartReflex, it is possible to meet a specific frequency performance from a strong silicon device at a much lower voltage than from a weaker silicon device. SmartReflex takes advantage of this by lowering the supply voltage, resulting in lower active and leakage power.

The TPS659xx family of devices supports Class3 SmartReflex. This provides dynamic voltage management for two DCDC switching supplies (VDD1 and VDD2) powering the OMAP3 core supplies, VDD_MPU and VDD_CORE. This hardware technique provides excellent power savings.

SmartReflex is disabled by default. It can be enabled by setting the DC-to-DC_GLOBAL_CFG[SMARTREFLEX_ENABLE] bit to 1. Further control of the voltage level can be done by configuring the VDD1_SR_CONTROL and VDD2_SR_CONTROL registers.

The communication for SmartReflex commands is done through the dedicated I^2C interface (I2C4 on OMAP35xx and I2C.SR on TPS659xx). The OMAP35xx processor acts as the master controller for adjusting the VDD1 and VDD2 power supplies on TPS659xx.

This technique yields the maximum power savings on the system.

4.5 Audio

The audio module for this family of devices exists on the TPS65950 and the TPS65930. TPS65950 has two input amplifiers and multiple analog output options (Class-D, headset, ear, predriver). TPS65930 has one input amplifier and one analog output (predriver).

Figure 8 and Figure 9 show the input and output options available with TPS65950.

Figure 8. Analog Input Options for Audio

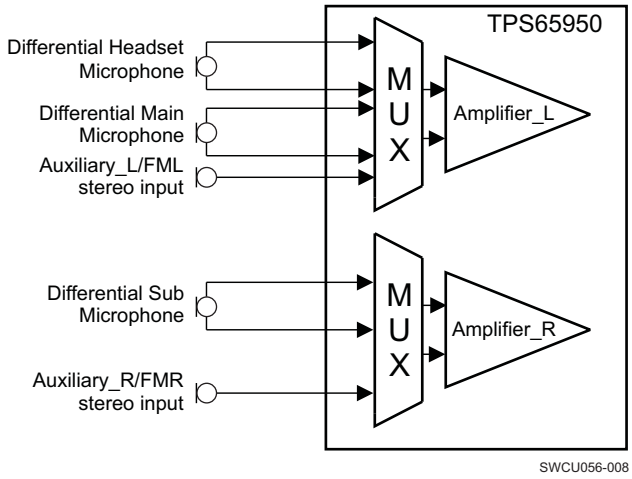


Figure 9. Analog Output Options for Audio

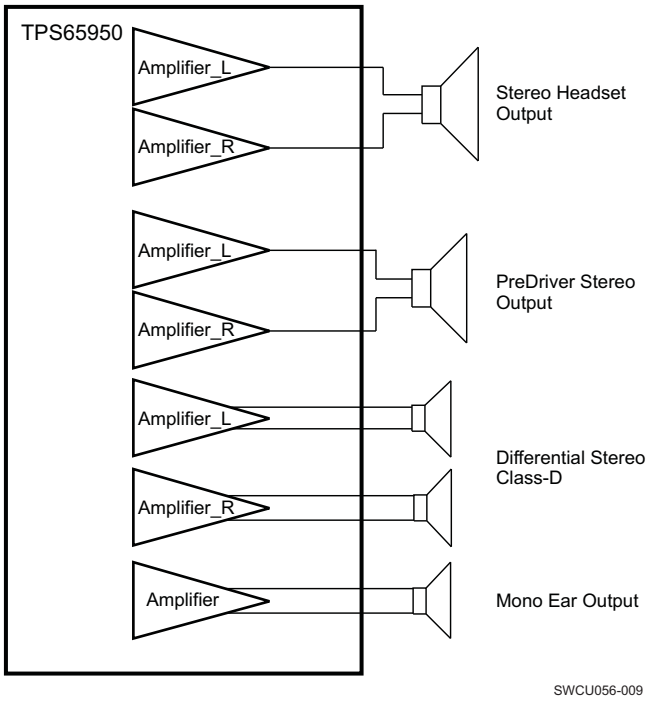
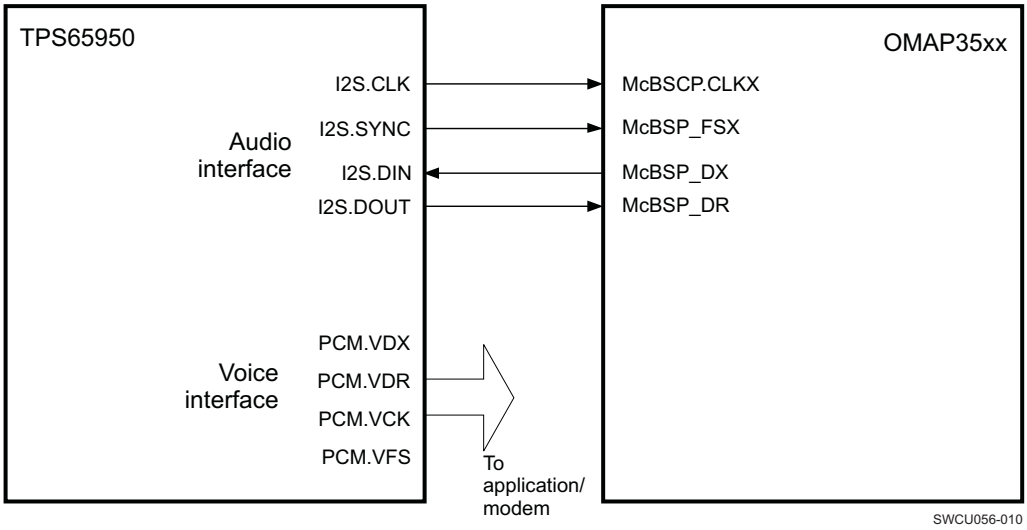


Figure 10 shows a typical connection between TPS65950 and OMAP35xx application processor.

Figure 10. Example Connection Between TPS65950 Audio and OMAP35xx

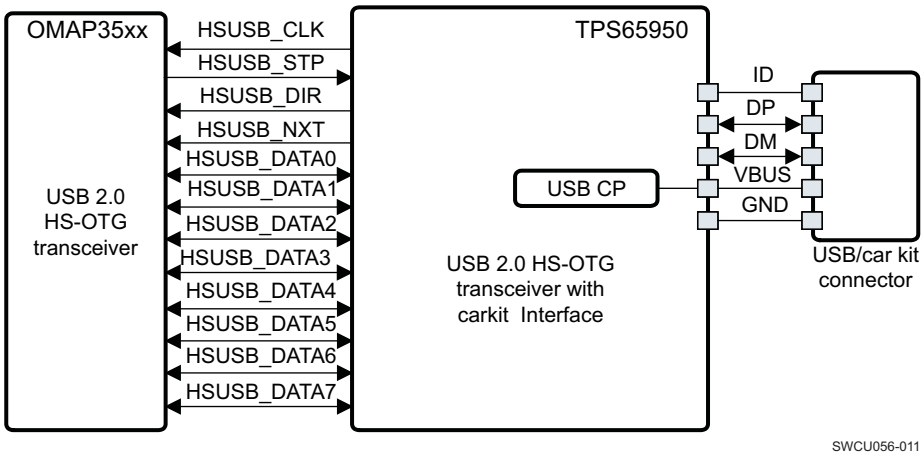


4.6 USB

The TPS659xx includes a universal serial bus (USB) on-the-go (OTG) transceiver with CEA and MCPC carkit interfaces. It supports USB 480Mbps high-speed (HS), 12 Mbps full-speed (FS), and 1.5Mbps low-speed (LS) through a 4-pin UTMI+ low pin interface (ULPI).

The device includes a charge pump capable of supplying a typical 4.8-V, 100-mA output. The USB interface can be configured in several modes. For details, see the technical reference manual.

Figure 11. Connection Between TPS65950 USB and OMAP35xx



NOTE: In case there is a need to use an external 5-V supply for larger current needs then one can use an external supply; however, the VBUS pin from the device must be connected to the VBUS pad on the USB connector.

This is necessary for the internal comparators of the USB module to support the correct functioning in OTG mode and VBUS detection.

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