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Abstract

Improving the performance of semiconductor devices has increased per-device power consumption, but not allowable junction temperatures. Historically, thermal-resistance measurements have been made in a variety of ways that have not been explained thoroughly. The advantages of the JEDEC 51 method (JESD 51) are explained and compared with other methods used to determine thermal resistance of semiconductor devices.

Introduction

Even with lower voltage levels, the steady increase in logic clock speed and gate count has resulted in device parasitic heat loss that would have been almost unbelievable just a few years ago. Some leading-edge processors must dissipate as much as a small incandescent room light. This offers significant challenges to system-level designers, particularly because allowable junction temperatures are not increasing. Conversely, in some technologies, junction temperatures must be maintained lower than could previously be allowed due to reliability concerns with newer metal systems and smaller geometries.

Historically, one tool that system designers have used to compare devices and determine operating junction temperatures are properties published by semiconductor manufacturers that specify the ability of device packages to dissipate junction-generated heat away from the surface of the silicon die. Although relatively simple in concept, these thermal-resistance values are sometimes misunderstood and misused, partly because manufacturers rarely publish how they are measured and what they represent physically.

Without this knowledge, the advantages of the new JEDEC 51 method (JESD 51) of measuring thermal impedance cannot be appreciated. This application report begins with an explanation of how thermal-impedance values have been obtained historically, and then describes the advantages of the newer JESD 51 method.

Background

Thermal resistance in a solid is much like electrical resistance in that the steady-state defining equation is:

$$\Delta T \text{ across solid} = R_T \times \text{heat (watts) conducted through solid}$$

or

$$R_T = \frac{\Delta T}{W} \quad \text{(usually expressed in °C/W)} \qquad (1)$$

Where R_T is thermal resistance of a material.

That is, a measured temperature, ΔT, across a solid would mean $\Delta T/R_T$ watts of power passes through it.

Figure 1 shows a simplified two-dimensional diagram of resistance to heat flow from the junctions on a die surface to the surface of the package.

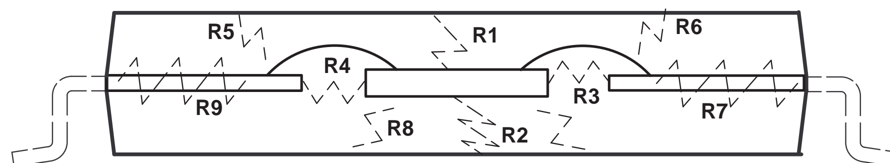


Figure 1. Representation of the Distributed Resistance to Thermal Dissipation in a Device

Rl, R2, etc., are the equivalent thermal resistances from the die surface to a section of the package. Because thermal resistance in a solid depends on material properties, length of path, and cross-sectional area of the path, each section of the package contributes a unique thermal resistance. Thermal power dissipation from die surface to the surface of the package can be calculated by:

$$\text{Overall power dissipated} = (T_J - T_S1)/R1) + (T_J - T_S7)/(R3 + R7) + \ldots (T_J - T_{SN})/(R_N) \quad \textbf{(2)}$$

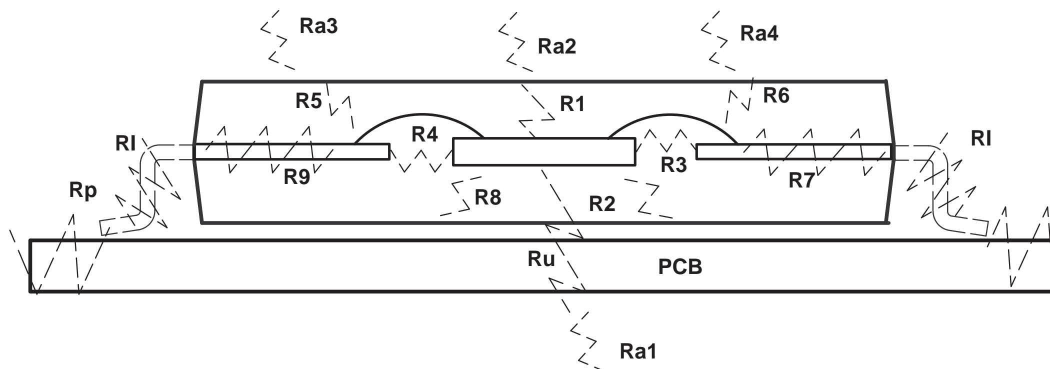
Where:

T_S l...T_S n = package surface temperatures at the exterior locations shown
T_J = average junction temperature at the surface of the die
Rl...Rn = distributed thermal resistances for each section of the package

The smaller the overall package thermal resistance becomes, the better able a package is to conduct heat away from the die surface.

If the ability of a package to conduct heat from the die to the outside surface were all that is required to predict junction temperatures, semiconductor manufacturers could provide accurate thermal resistance using finite-element analysis (FEA) or equivalent discrete models. Unfortunately, external factors, such as airflow and spacing from the printed circuit board (PCB), can affect package thermal resistance much more than the package construction itself.

Figure 2 shows the effects of external factors on thermal resistance of an assembled device.



Ral...Ran = thermal resistance of the air around the device
Ru = thermal resistance of whatever is under the package (e.g., thermal grease and air gap)
Rl = lead thermal resistance
Rp = PCB thermal resistance, etc.

Figure 2. Representation of Distributed Thermal Resistance With External Factors Added

Table 1 shows the effects of environment on junction temperature.

Table 1. Selected Thermal-Resistance Values

MATERIAL	THERMAL RESISTIVITY °C • m/W
Copper (lead frame)	0.003
Silicon (die)	0.007
Ceramic	0.055
Mold compound (plastic case)	1.59 to .7468
Thermal grease	2
FR 4 (PWB)	3.5
Air	38.2

These values most often are published inversely (as conductivity), but are listed here as resistive to be consistent with the way overall package thermal resistance is expressed.

These values are for thermal conduction only. Actual thermal analysis involves conduction, convection, and radiation, all of which are calculated differently and can be estimated accurately only by dedicated FEA using empirical data. For the purpose of explaining package thermal resistance, a simplified resistor model is used here.

Because the external resistances of the surrounding air, PCB, thermal grease, etc. are in series with the package resistance, factors external to the package affect junction temperature significantly. If a package has an overall thermal resistance equivalent to Equation 1 and Figure 1 of about 14°C/W after adding in the external resistive factors, such as the surrounding air (equivalent to Figure 2), a thermal resistance of 40°C/W, or higher, could be expected.

This presents a problem to device manufacturers who want to provide thermal information about their packages because external factors are not known at package thermal characterization. As a solution, semiconductor manufacturers historically have provided two types of resistance values: θ_{JC} (resistance from junction to case) and θ_{JA} and θ_{JMA} in an attempt to account for end-use environments.

Junction-to-Case Thermal Resistance

θ_{JC} is, approximately, the ability of a device to dissipate heat in an ideal environment, that is, mounted with an infinite or temperature-controlled heat sink. However, test methods used to determine θ_{JC} have varied in the past and proper use of this value depends on which method was used to determine the specified value.

Military Standard

Description

Instructions for determining θ_{JC} for military products are specified in MIL-STD-883 Method 1012.1. θ_{JC} determined using this method defines the ability of a device to dissipate heat if it is mounted on a temperature-controlled heat sink.

To establish a temperature reference on the surface of the die, the temperature-dependent forward bias voltage of a bipolar junction is calibrated at constant bias current for several different temperatures in an oven. This can be an unused junction on the device, but usually a special die for thermal characterization is assembled in the package being tested (see Figure 3).

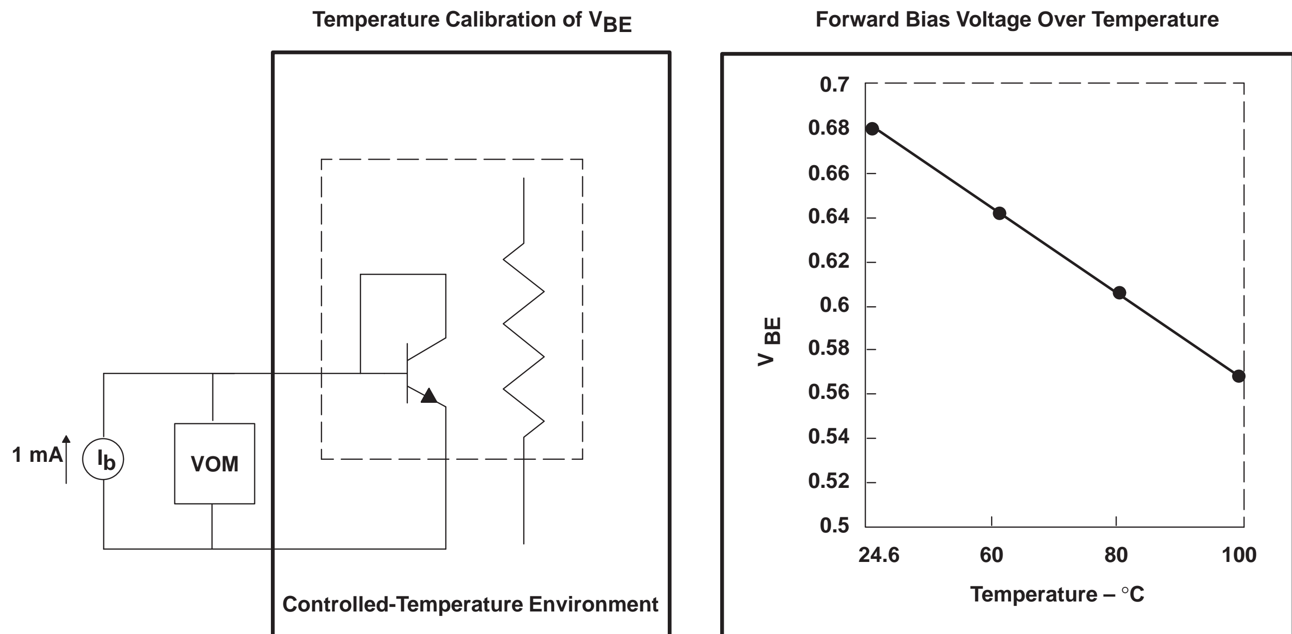


Figure 3. Die Schematic for Thermal Characterization

The device is then placed on a copper heat sink that is maintained at a constant temperature, using thermal grease to ensure the best possible conductivity. A thermocouple is inserted through the heat sink and is pressed against the underside of the package nearest the device to record package surface temperature. MIL-STD-883 Method 1012.1 specifies that the thermocouple be placed on the hottest part of the case (see Figure 4).

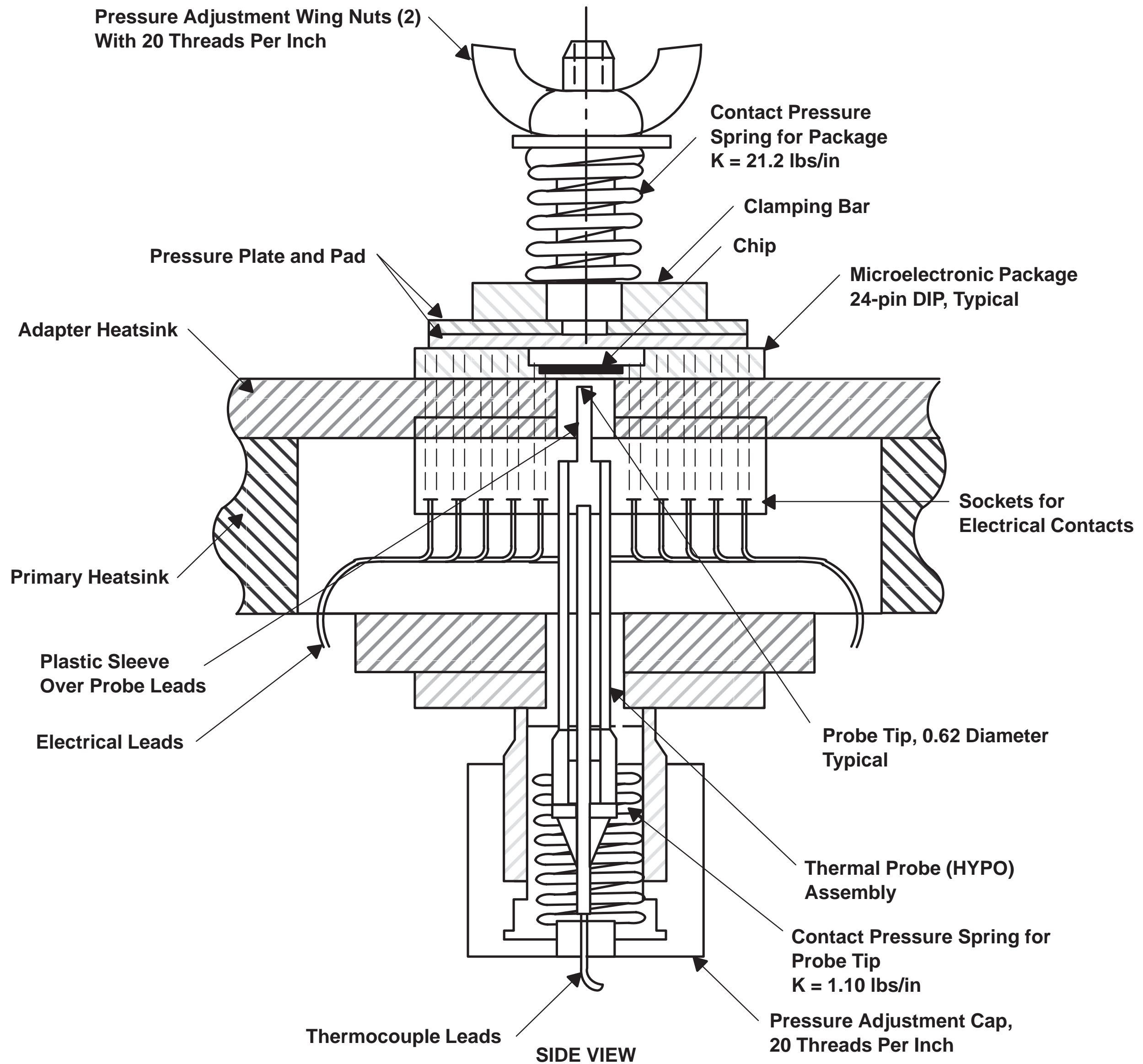


Figure 4. Military θ_{JC} Test Configuration as Illustrated in MIL-STD-883 Method 1012.1

With some amount of power applied to the power-dissipating elements on the die, the forward bias voltage is measured after temperature has stabilized and the surface temperature of the die determined. θ_{JC} is then calculated using the formula:

$$\theta_{JC} = \frac{\text{Die surface temperature} - \text{Package surface temperature}}{\text{Power applied}} \quad (3)$$

Package surface temperature is the temperature recorded by the thermocouple pressed against the underside of the package. Die surface temperature is the temperature derived from the previously calibrated forward bias voltage. Power applied is the product of voltage and current applied to the die resistive network (bias current is small enough to be ignored).

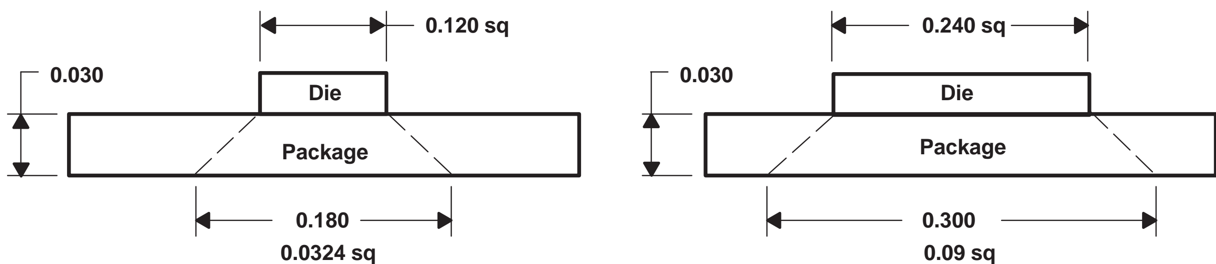
Use

The configuration in Figure 4 represents, as nearly as possible, an ideal heat sink placed directly under the die. It does not comprehend any other heat sink position, nor does it include any additional cooling, such as air flow. With the heat sink maintained at a constant temperature during testing, MIL-STD-883 Method 1012.1 provides a more nearly ideal θ_{JC} than if the device were mounted on a passive heat slug.

Assembly designers often use θ_{JC} measured in this way to approximate junction temperatures at circuit conception. If the unit is to be mounted on a surface with known thermal properties, such as a thermal rail, and all heat is assumed to be taken out along this path, estimation of junction temperature is straightforward.

Because many military applications are enclosed, with heat extraction through a heat sink on the bottom of the device case to a thermal rail (in the same configuration as the test), a thermocouple attached to the *measured* package surface can be used to estimate realistic junction temperatures in the assembled system. A thermocouple applied in this manner gives erroneous results if no heat sink is used or the in-use configuration differs from the test configuration.

By far, the largest variation potential in θ_{JC} values measured in this manner is the size of the die used in the test. With two of the standard thermal die sizes available, unidirectional heat flow from a finite source fans out at approximately a 45-degree angle in an isotropic material (see Figure 5).



All dimensions are in inches.

Figure 5. Small-Die and Large-Die Dissipation Areas

The larger die dissipates power over an area three times that of the smaller die, thus the heat dissipated by the large-die device is about one-third that of the smaller die.

This is not as much of a problem as it may seem at first because test-die sizes are chosen to match the size of the device die. It does explain though, why smaller packages, and, therefore, smaller die, have significantly higher θ_{JC} values when measured using MIL-STD-883 Method 1012.1. In addition, several devices of slightly varying die size may use the same package, causing slight deviations from published thermal-resistance values.

Default values of θ_{JC} that are significantly higher than if the package were measured have been published in miltary standards. Therefore, if a particular package type has not been characterized by a manufacturer, the default values are used and may cause some military thermal-resistance values to seem extraordinarily high.

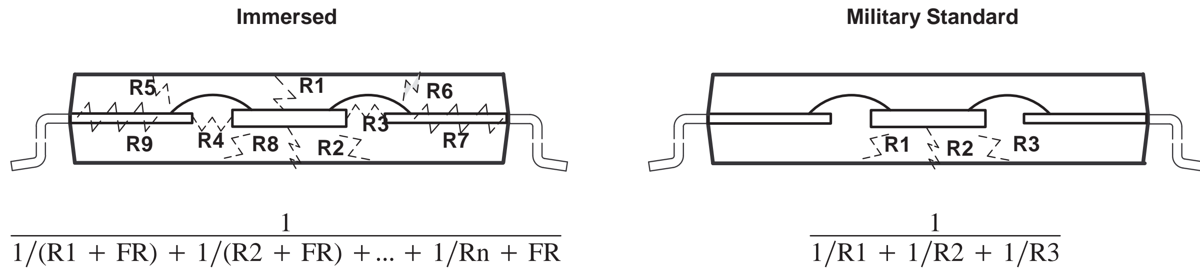
Although ceramic is a much better thermal conductor than most organics, military semiconductor users occasionally are confused by the fact that plastic packages sometimes have lower published θ_{JC} (and θ_{JA}, discussed later in this application report) values than equivalent ceramic-package devices. The root of this paradox is not in the package materials, but in different methods of characterizing θ_{JC}.

Simulated Infinite Heat Sink

Description

One historical method of characterizing θ_{JC} is similar to that used for military devices, but the device is immersed in an agitated, electrically insulating fluorinert fluid rather than sitting on a heat sink. This test method is an attempt to measure directly the overall thermal resistance of a package. Even though the thermal resistance of the fluorinert is poor, this method emulates, to some extent, an infinite heat sink on all parts of the package.

Figure 6 shows the practical difference between a simulated infinite heat sink and the military-standard method.



$$\frac{1}{1/(R1 + FR) + 1/(R2 + FR) + ... + 1/Rn + FR}$$

$$\frac{1}{1/R1 + 1/R2 + 1/R3}$$

Where:

FR = fluid thermal resistance exterior to the package

Figure 6. Simulated Infinite Heat Sink vs Military-Standard Method

The parallel resistance net, composed of the entire package as opposed to only the bottom section, explains why a package made of thermally inferior material, such as plastic instead of ceramic, sometimes can have lower published thermal resistance values.

Use

Thermal resistance determined in this way is best used for comparison purposes only (with other similarly measured devices). Thermal resistance cannot be used to approximate junction temperatures prior to component assembly and power up because all of the package surface is used to extract heat during this test and it is impossible to know how the package will be affected by the system environment.

Other θ_{JC} and θ_{JC}-Like Determinations

There is no universal standard for θ_{JC}, so it has been determined in various ways. For instance, some package vendors use FEA models to determine thermal performance of their packages. In this category, θ_{JC} has been calculated from the die surface to the most remote part of the package, as well as calculated from resistance meshes similar to equation 1.

A newer method, differentiated by the designator Ψ_{JT} is defined by EIA/JESD 51-2. This method entails measuring case temperature using a fine-gage thermocouple glued to the top of the package during operation on a PCB. This allows a more accurate calculation of system-level *in situ* junction temperatures because it more closely replicates typical end-use conditions[1].

Semiconductor data sheets typically are published using consistent thermal-resistance-measuring techniques as described here, but, if thermal information is obtained from a third party, such as a package vendor, it is important to understand their definition of θ_{JC}.

θ_{JA} and θ_{JMA} Prior to JEDEC Method 51

Description

θ_{JA} is a measure of the ability of a device to dissipate heat while operating in open air without a heat sink. Recently, JEDEC has refined the terminology for open-air testing so that, if the test is performed in still air, it is properly termed θ_{JA}. If performed in a wind tunnel with calibrated air velocity, it is called θ_{JMA}. Before this refinement, all types of open-air testing usually were labeled θ_{JA}. Due to the lack of standardized methodology, this general description also has led to differing methods and results.

Military Ceramic

There is no specific requirement in military specifications to provide θ_{JA} or θ_{JMA}, but as is typical of military testing, when θ_{JA} is published, usually it is determined by the most conservative interpretation. For example, TI Military Semiconductor Group tests θ_{JA} with a unit suspended in open air under a 1×1×1-foot cover with no air flow. Because air is a very good insulator, the thermal resistance values produced are worst case. At times, this is troublesome because a device that would be usable if provided the added heat-dissipative capabilities of a PCB mount, might be eliminated during preliminary consideration due to deceptively high junction temperatures derived from a highly conservative value of θ_{JA}. Devices suspended in air can have θ_{JA} values two or more times that of mounted units, depending on device configuration.

Plastic

θ_{JA} values for plastic-package devices have been characterized in environmental conditions considered by the manufacturer to be adequate for in-use junction-temperature estimation. This can vary from suspended in air, mounted on boards, sitting on countertops, or inserted in sockets.

Use

Generally, θ_{JA} is used as a comparison tool between package types. For preliminary estimates of on-board junction-temperature, derating curves are derived from θ_{JA} using the formula in Equation 4.

$$\text{Maximum device power} = \frac{\text{Maximum junction temperature allowed} - \text{Estimated ambient temperature}}{\theta_{JA}} \tag{4}$$

θ_{JA} can be considered worst case if measured in open air, in a socket, or, possibly, as nominal if measured mounted on a PCB. PCB trace dimensions, device orientation, air turbulence and method of measuring air velocity, proximity of the ambient temperature thermocouple, and enclosure size, if any, are additional factors that can change the θ_{JA} value.

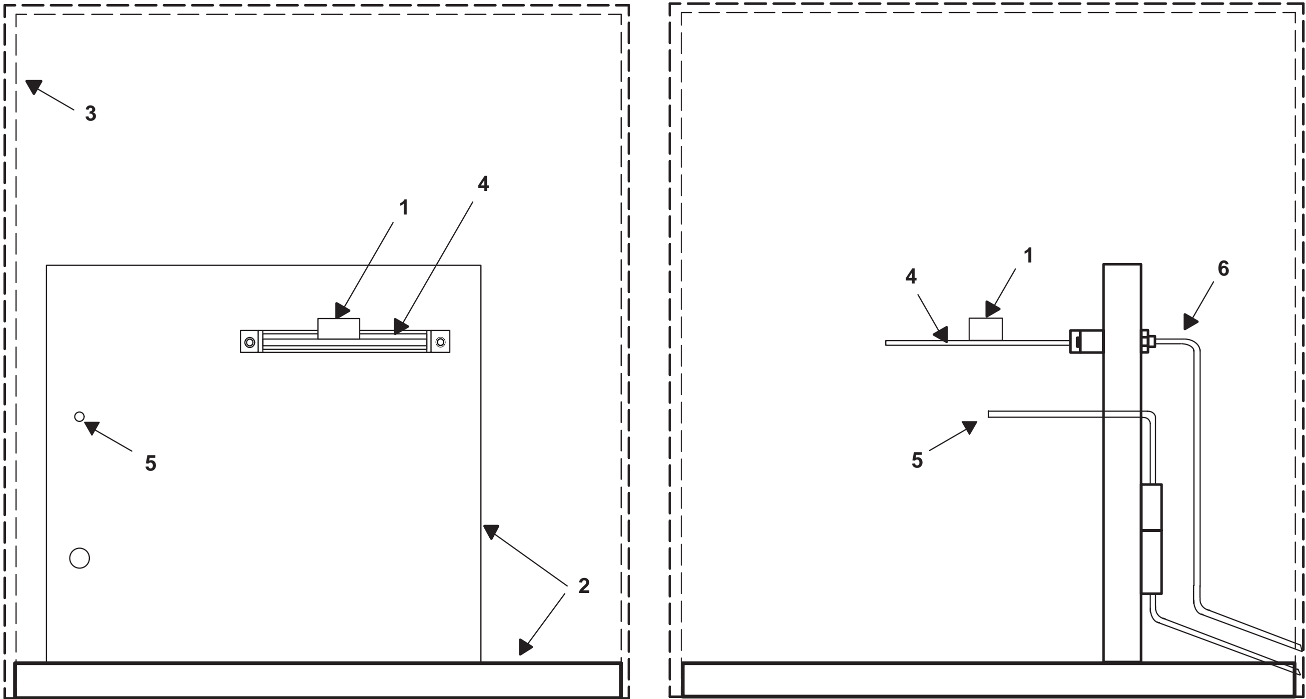
Junction and maximum allowable ambient temperatures often are calculated from θ_{JA} by device product engineers, but this can be a very conservative approach if θ_{JA} is measured in open air with no conduction to a PCB. Experiments have shown that 85% of the heat produced by the die in a typical package is dissipated from the test board[2].

Conversely, this calculation may result only in nominal to optimistic values if θ_{JA} was measured mounted on a PCB, particularly if the PCB has thermal vias or power planes. Unfortunately, semiconductor manufacturers often do not publish how their thermal-resistance values were determined.

Characterizing θ_{JA} Using JEDEC Method 51

JEDEC Method 51 provides the semiconductor industry a method of eliminating the most troublesome aspect of θ_{JA} characterization: inconsistency. In addition, this test method emulates a slightly conservative, but realistic, system-level environment for junction-temperature estimations.

Method 51 enforces rigid environmental requirements, controlling parameters that contributed previously to resistance variability. Figure 7 shows the test fixture for the still-air portion of the test.



1. Unit under test
2. Insulating suport of specific dimensions
3. Insulating 1’ x 1’ x 1’ cover
4. PCB of specific dimensions without planes or thermal vias; trace size and length, connector type and board material and construction defined. (see Note A)
5. Thermocouple used to record ambient temperature; location defined by JEDEC
6. Test leads

NOTE: Although EIA/JEDEC Standard 51-3 (August 1998) lists only the board described here (no planes or thermal vias) there is another board design pending publication that has four layers and two power planes. Because the currently published board is called low effective thermal-conductivity test board, the power-plane design could be considered a high- or higher-conductivity test board. This board is used by many companies.

Figure 7. JEDEC Method 51 Test Setup for Still-Air Portion of the Test

JEDEC has explicitly defined all parameters because studies indicated surprising thermal effects of the environment, in addition to parameters mentioned previously. For example, one study shows that PCB trace length can affect measured θ_{JA} on a plastic package almost as much as the presence or absence of a 500 lf/m airflow[1].

Also, FEA modeling evaluations have shown that this methodology is sufficiently controlled so that only one package configuration need be measured. Other packages of the same material and configuration, but different size, can then be characterized by FEA using parameters determined from the measured unit.

Because a large portion of the heat generated by a die surface is conducted to the PCB, this arrangement provides a much more consistent and realistic value of θ_{JA} between characterization laboratories than any of the previous methods. In addition, junction-temperature calculations based on this method of characterization provide a good conservative nominal first-pass value.

The new JEDEC method of measuring θ_{JA} does not provide junction temperatures from case temperature as θ_{JC} or the newer Ψ_{JT} provide, so these values, or an equivalent, continue to be required data-sheet entries. Presumably, ambiguous characterization methods, such as immersion, will be replaced by defined methods similar to military θ_{JC} or Ψ_{JT}.

Summary

The primary purpose of this application report is to inform users of thermal-resistance values and derating curves of hidden variabilities in historical values and to emphasize the importance of inquiring into test methodology before using the results. In addition, an explanation of the inconsistencies in measurements between manufacturers and package types has been provided. New JEDEC methods have potential for greatly improving the accuracy and reliability of semiconductor-package thermal characterization.

This application report also explains the rationale behind TI’s conversion to the new JEDEC standard. TI provides θ_{JC} per MIL-STD-883 method 1012.1 for military parts, and adds the more realistic JEDEC method. TI commercial plastic devices have been characterized using the JEDEC method since 1995.

Acknowledgment

The author of this application report is R. A. Pauley.

References

1. JEDEC Standard 51
2. *K-Factor Test-Board Design Impact on Thermal Impedance Measurements*, literature number SCAA022A