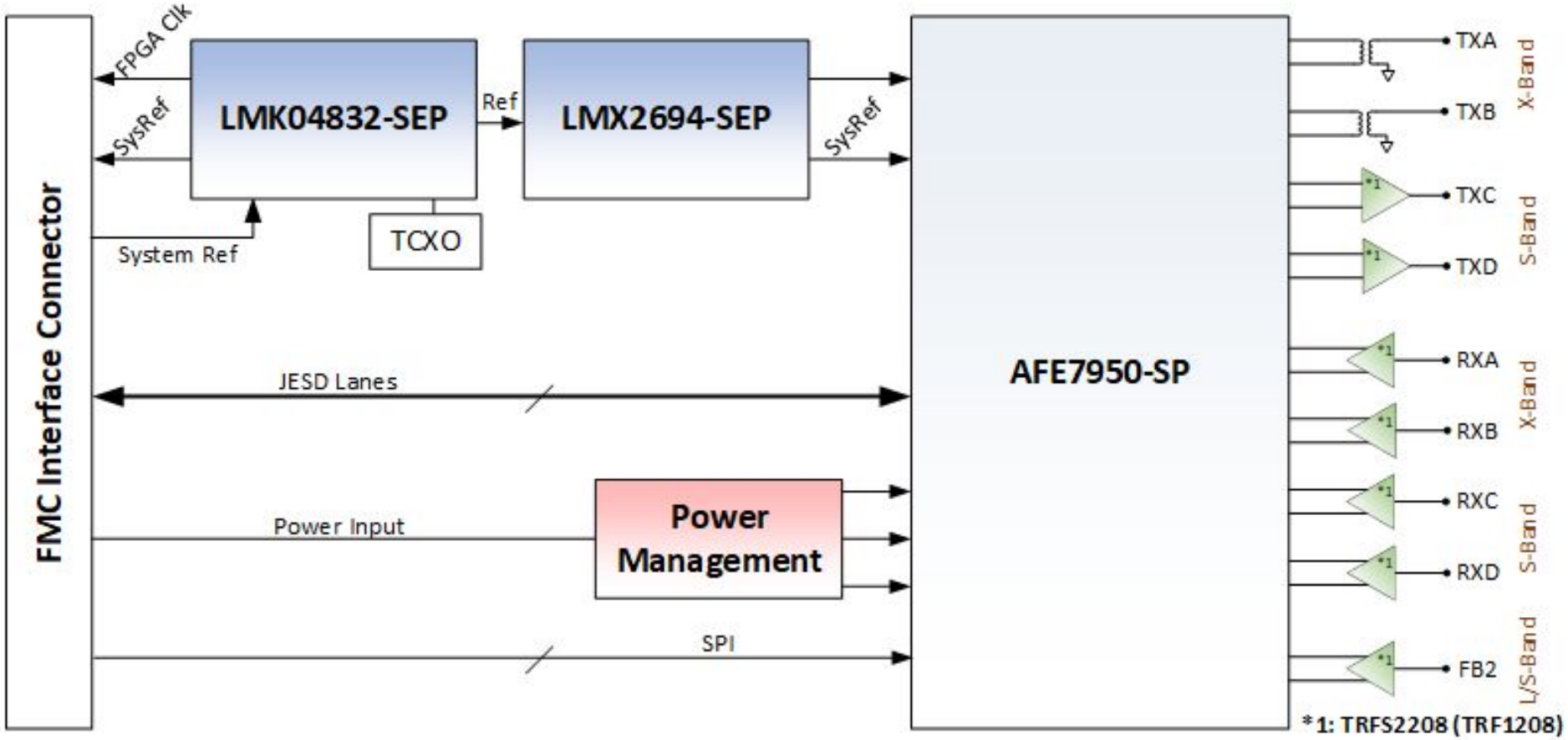
AFE7950-SP
4T4R1F Reference Design



Logo1
PCB
LOGO
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PCB
LOGO
Logo4

Orderable:		Designed for:	Mod. Date: 11/29/2022
TID #:		Project Title:	
Number:	Rev:	Sheet Title: Block Diagram	
SVN Rev: Not in version control		Assembly Variant: Proto	Sheet 1 of 11
Drawn By: Avinash N		File: CoverSheet.SchDoc	Size: C
Engineer:		Contact:	

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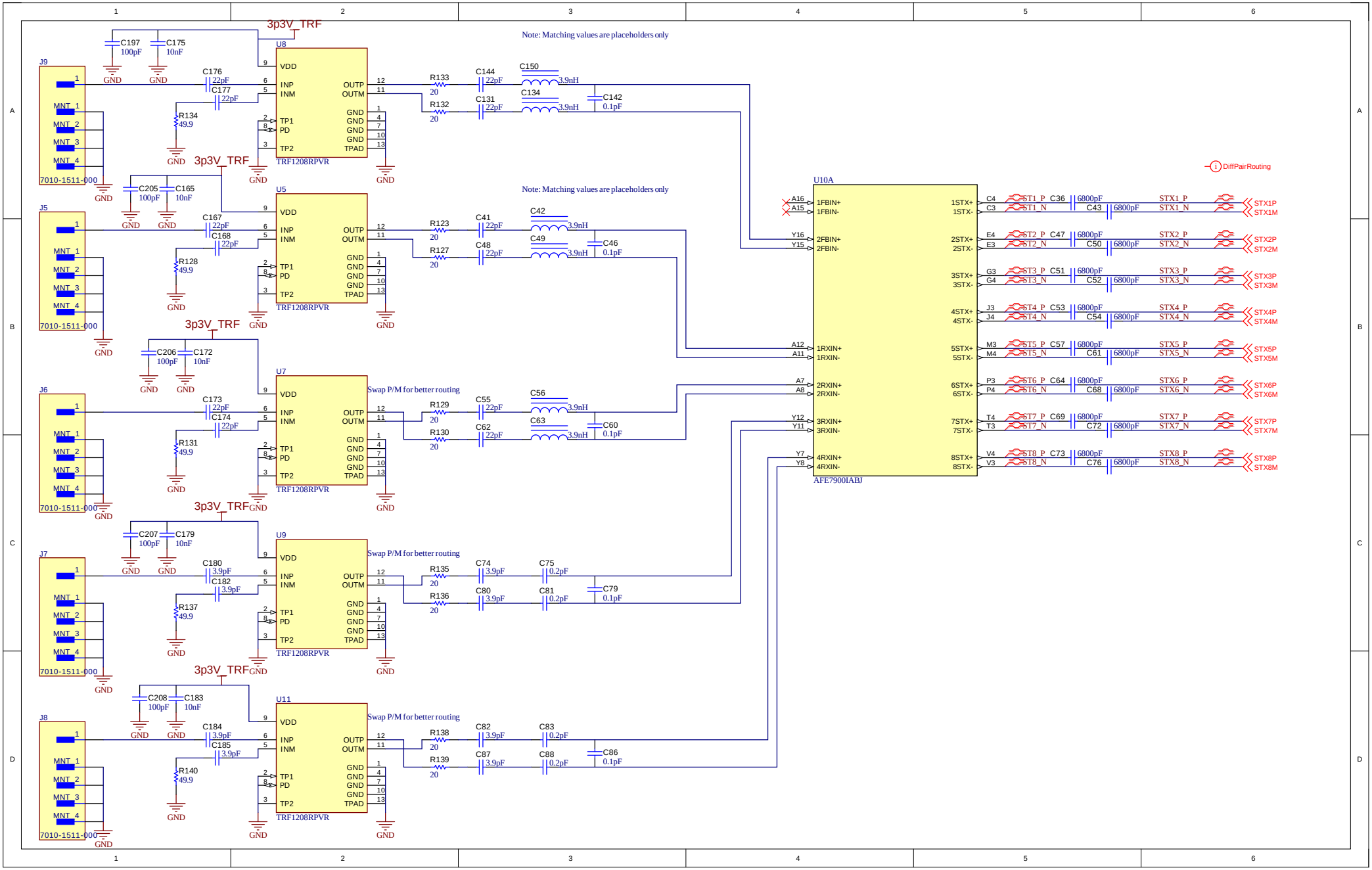
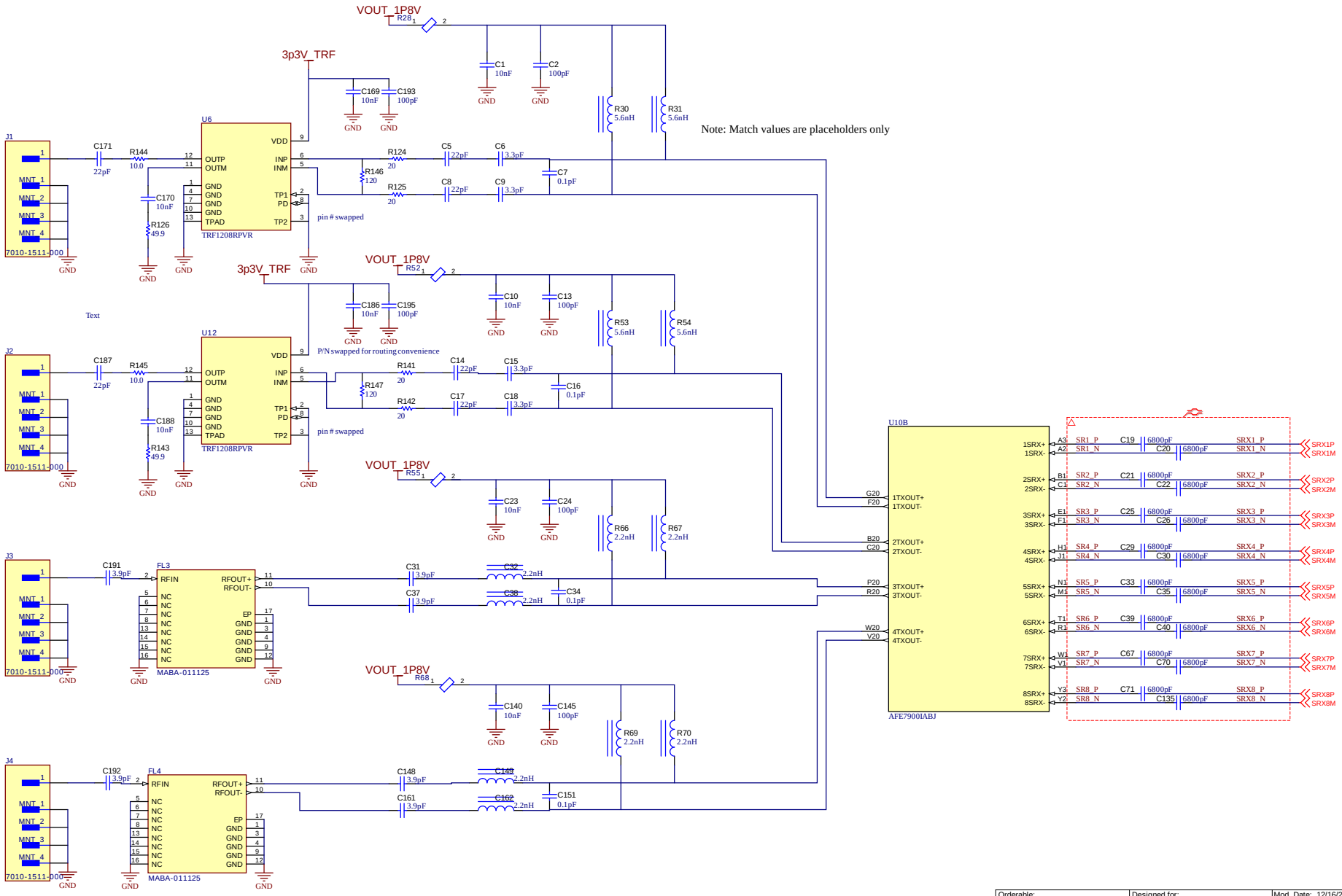

Note: Matching values are placeholders only
Note: Matching values are placeholders only
Swap P/M for better routing
Swap P/M for better routing
Swap P/M for better routing
3p3V_TRF
U8
U5
U7
U9
U11
U10A
AFE7900IABJ
TRF1208RPVR
7010-1511-000
DiffPairRouting
GND



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TID #:		Project Title:	
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SVN Rev: Not in version control		Assembly Variant: Proto	Sheet: 3 of 11
Drawn By:		File: TX_RF_Output.SchDoc	Size: B
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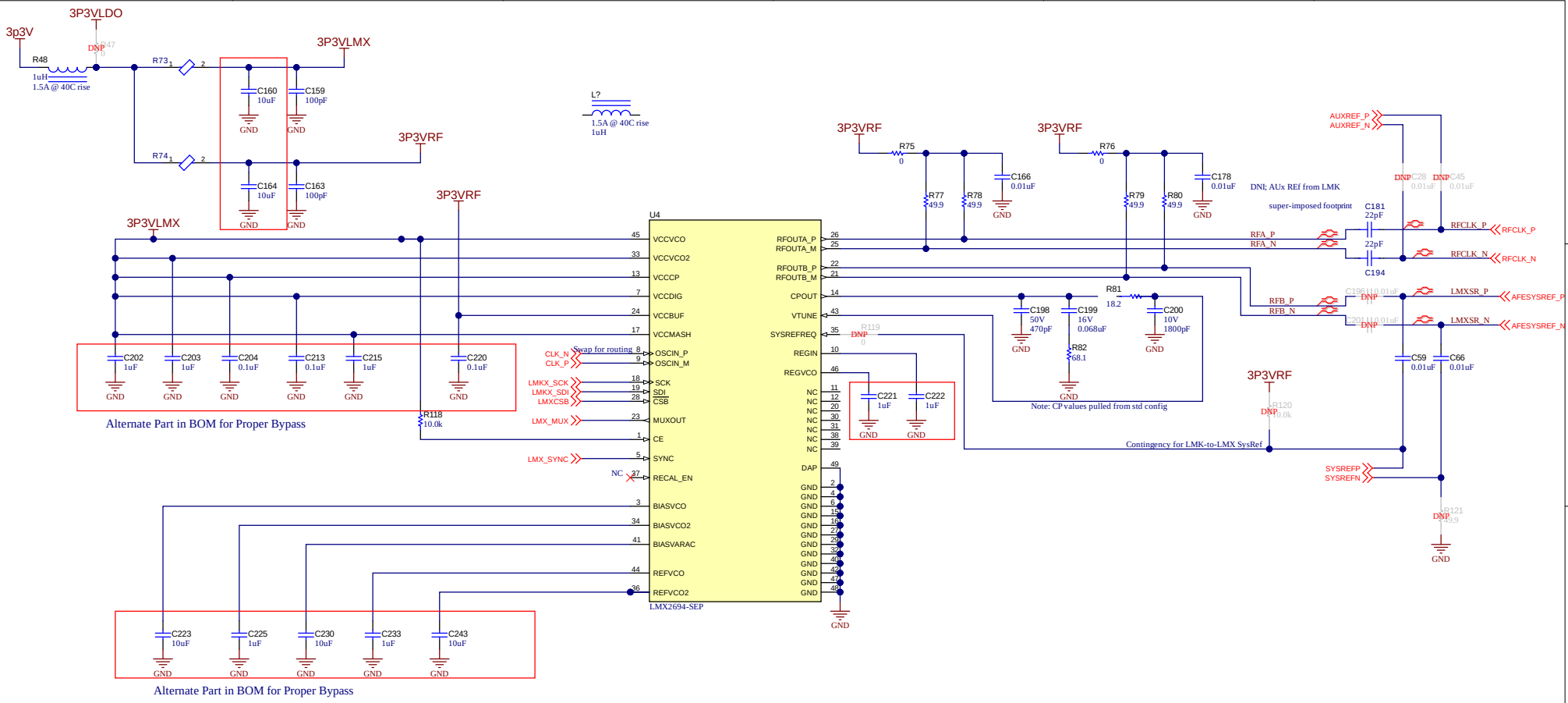

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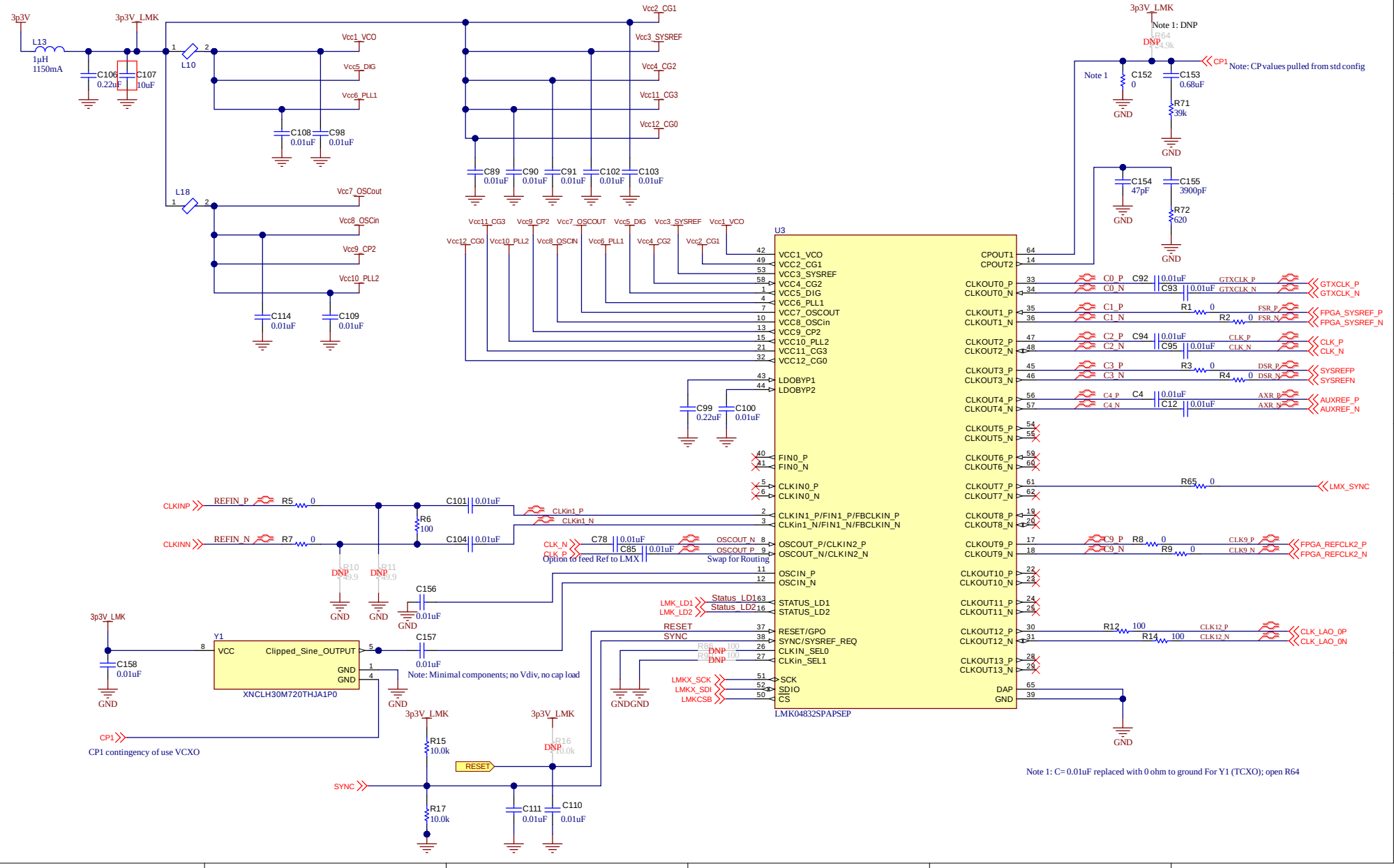
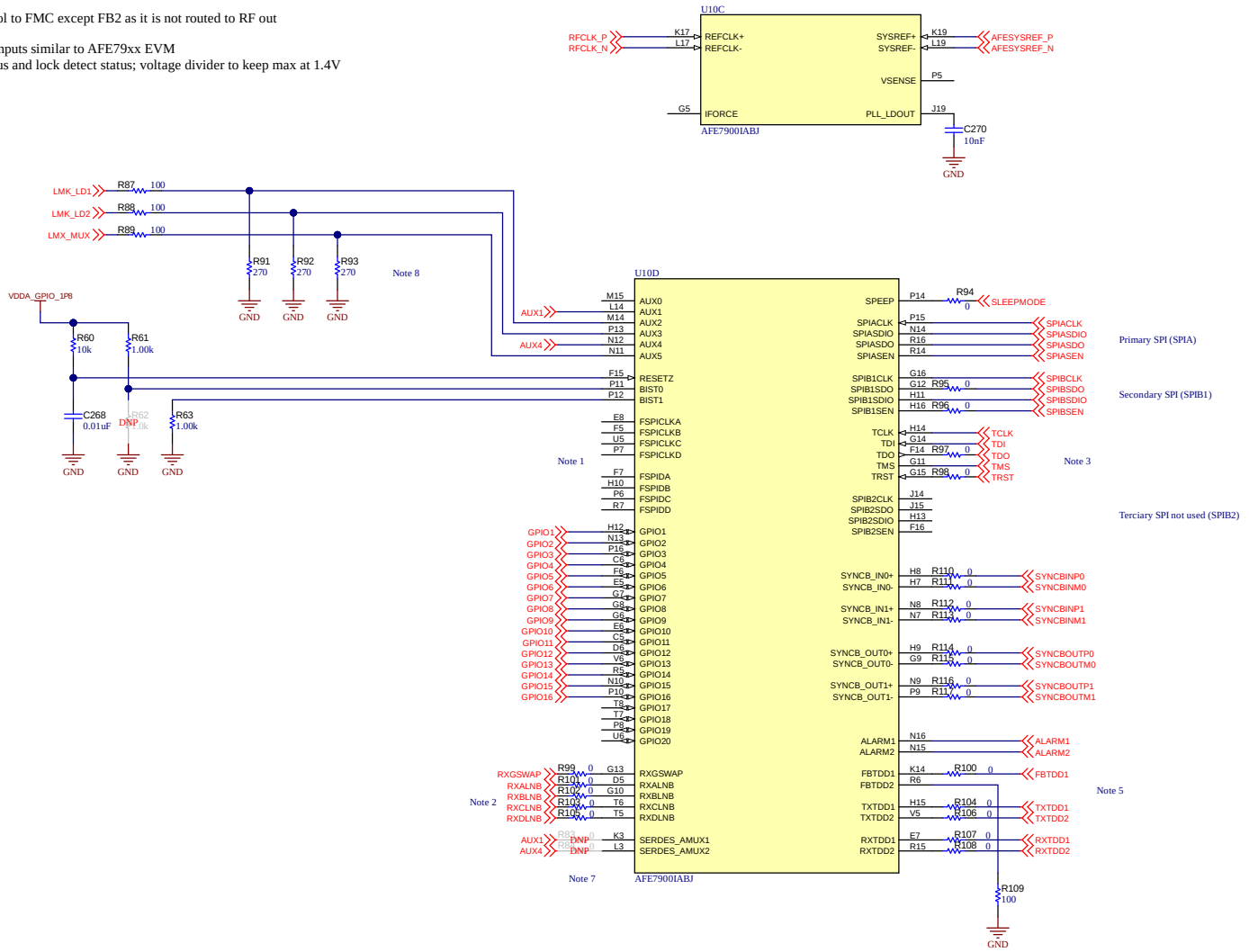
TID #:		Project Title:	
Number:	Rev:	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: Proto	Sheet: 5 of 11
Drawn By:		File: LMX2694.SchDoc	Size: B
Engineer:		Contact:	


3p3V
3p3V_LMK
L13
1µH
1150mA
C106
0.22uF
C107
10uF
L10
Vcc1_VCO
Vcc5_DIG
Vcc6_PLL1
C108
0.01uF
C98
0.01uF
Vcc2_CG1
Vcc3_SYSREF
Vcc4_CG2
Vcc11_CG3
Vcc12_CG0
C89
0.01uF
C90
0.01uF
C91
0.01uF
C102
0.01uF
C103
0.01uF
L18
Vcc7_OSCout
Vcc8_OSCin
Vcc9_CP2
Vcc10_PLL2
C114
0.01uF
C109
0.01uF
U3
VCC1_VCO
VCC2_CG1
VCC3_SYSREF
VCC4_CG2
VCC5_DIG
VCC6_PLL1
VCC7_OSCOUT
VCC8_OSCin
VCC9_CP2
VCC10_PLL2
VCC11_CG3
VCC12_CG0
LDOBYP1
LDOBYP2
C99
0.22uF
C100
0.01uF
FIN0_P
FIN0_N
CLKIN0_P
CLKIN0_N
CLKIN1_P/FIN1_P/FBCLKIN_P
CLKin1_N/FIN1_N/FBCLKIN_N
OSCOUT_P/CLKIN2_P
OSCOUT_N/CLKIN2_N
OSCIN_P
OSCIN_N
STATUS_LD1
STATUS_LD2
RESET/GPO
SYNC/SYSREF_REQ
CLKIN_SEL0
CLKin_SEL1
SCK
SDIO
CS
CPOUT1
CPOUT2
CLKOUT0_P
CLKOUT0_N
CLKOUT1_P
CLKOUT1_N
CLKOUT2_P
CLKOUT2_N
CLKOUT3_P
CLKOUT3_N
CLKOUT4_P
CLKOUT4_N
CLKOUT5_P
CLKOUT5_N
CLKOUT6_P
CLKOUT6_N
CLKOUT7_P
CLKOUT7_N
CLKOUT8_P
CLKOUT8_N
CLKOUT9_P
CLKOUT9_N
CLKOUT10_P
CLKOUT10_N
CLKOUT11_P
CLKOUT11_N
CLKOUT12_P
CLKOUT12_N
CLKOUT13_P
CLKOUT13_N
DAP
GND
LMK04832SPAPSEP
Note 1: DNP
R64
4.9k
DNP
CP1
Note: CP values pulled from std config
Note 1
C152
0
C153
0.68uF
R71
39k
C154
47pF
C155
3900pF
R72
620
C0_P
C0_N
C92
0.01uF
C93
0.01uF
GTXCLK_P
GTXCLK_N
C1_P
C1_N
R1
0
R2
0
FSR_P
FSR_N
FPGA_SYSREF_P
FPGA_SYSREF_N
C2_P
C2_N
C94
0.01uF
C95
0.01uF
CLK_P
CLK_N
C3_P
C3_N
R3
0
R4
0
DSR_P
DSR_N
SYSREFP
SYSREFN
C4_P
C4_N
C4
0.01uF
C12
0.01uF
AXR_P
AXR_N
AUXREF_P
AUXREF_N
R65
0
LMX_SYNC
C9_P
C9_N
R8
0
R9
0
CLK9_P
CLK9_N
FPGA_REFCLK2_P
FPGA_REFCLK2_N
R12
100
R14
100
CLK12_P
CLK12_N
CLK_LAO_0P
CLK_LAO_0N
Note 1: C= 0.01uF replaced with 0 ohm to ground For Y1 (TCXO); open R64
CLKINP
REFIN_P
R5
0
CLKINN
REFIN_N
R7
0
R6
100
C101
0.01uF
C104
0.01uF
CLKin1_P
CLKin1_N
CLK_N
CLK_P
C78
0.01uF
C85
0.01uF
Option to feed Ref to LMX
Swap for Routing
R10
49.9
R11
49.9
C156
0.01uF
LMK_LD1
LMK_LD2
Status_LD1
Status_LD2
RESET
SYNC
R86
100
R87
100
LMKX_SCK
LMKX_SDI
LMKCSB
3p3V_LMK
C158
0.01uF
Y1
VCC
Clipped_Sine_OUTPUT
GND
GND
XNCLH30M720THJA1P0
C157
0.01uF
Note: Minimal components; no Vdiv, no cap load
CP1
CP1 contingency of use VCXO
R15
10.0k
R16
10.0k
DNP
RESET
SYNC
R17
10.0k
C111
0.01uF
C110
0.01uF

1. Fast SPI (FSPICLKA-D and (FSPIDA-D) not used
2. Used to control external LNA if desired
3. JTAG connection; generally not needed
4. Null
5. Provide TDD control to FMC except FB2 as it is not routed to RF out
6. Null
7. Connected to Aux inputs similar to AFE79xx EVM
8: Monitor power status and lock detect status; voltage divider to keep max at 1.4V



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TID #:		Project Title:	
Number:	Rev:	Sheet Title:	
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Drawn By:		File: AFE7950_Clock.SchDoc	Size: B
Engineer:		Contact:	

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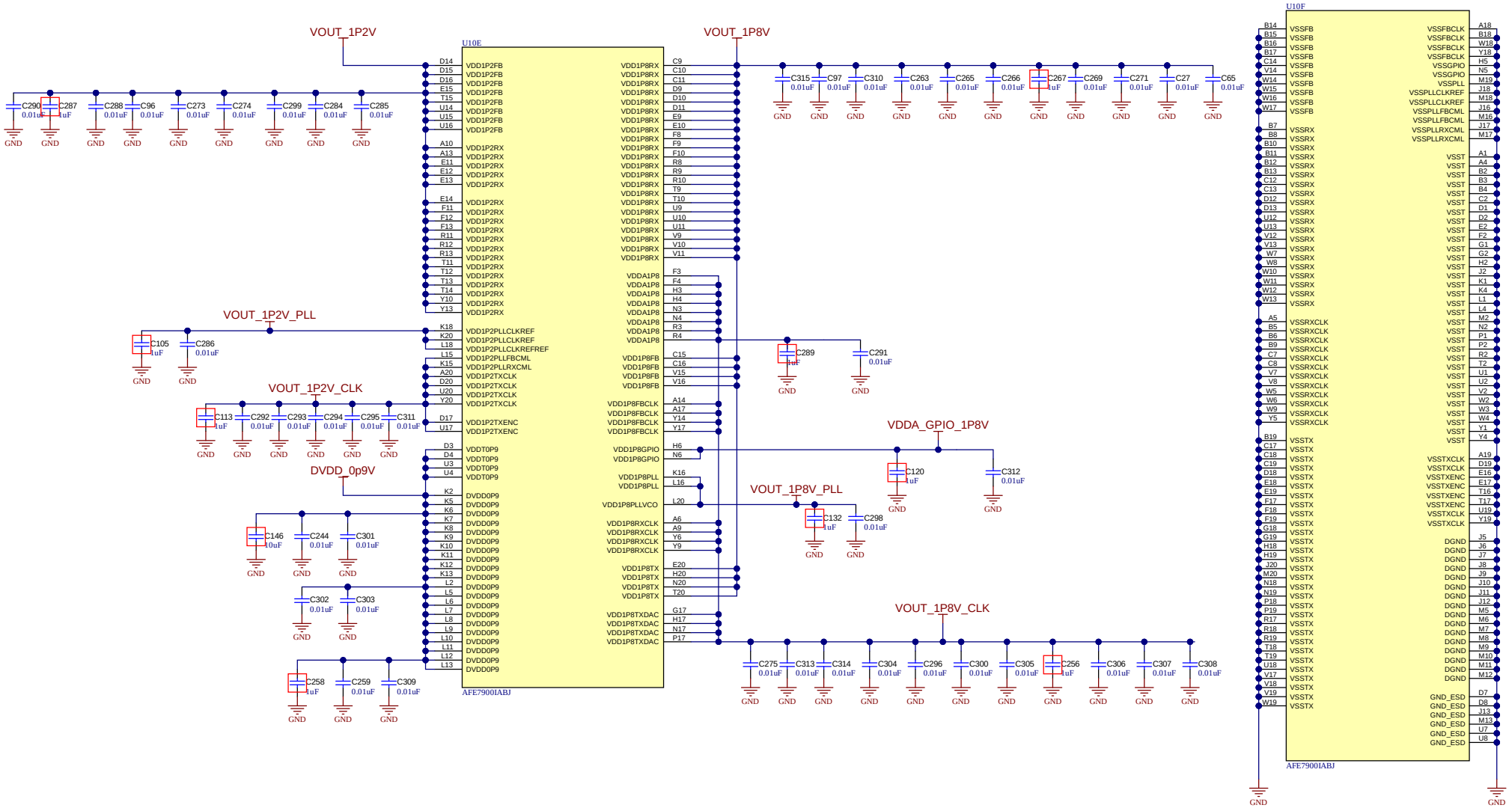

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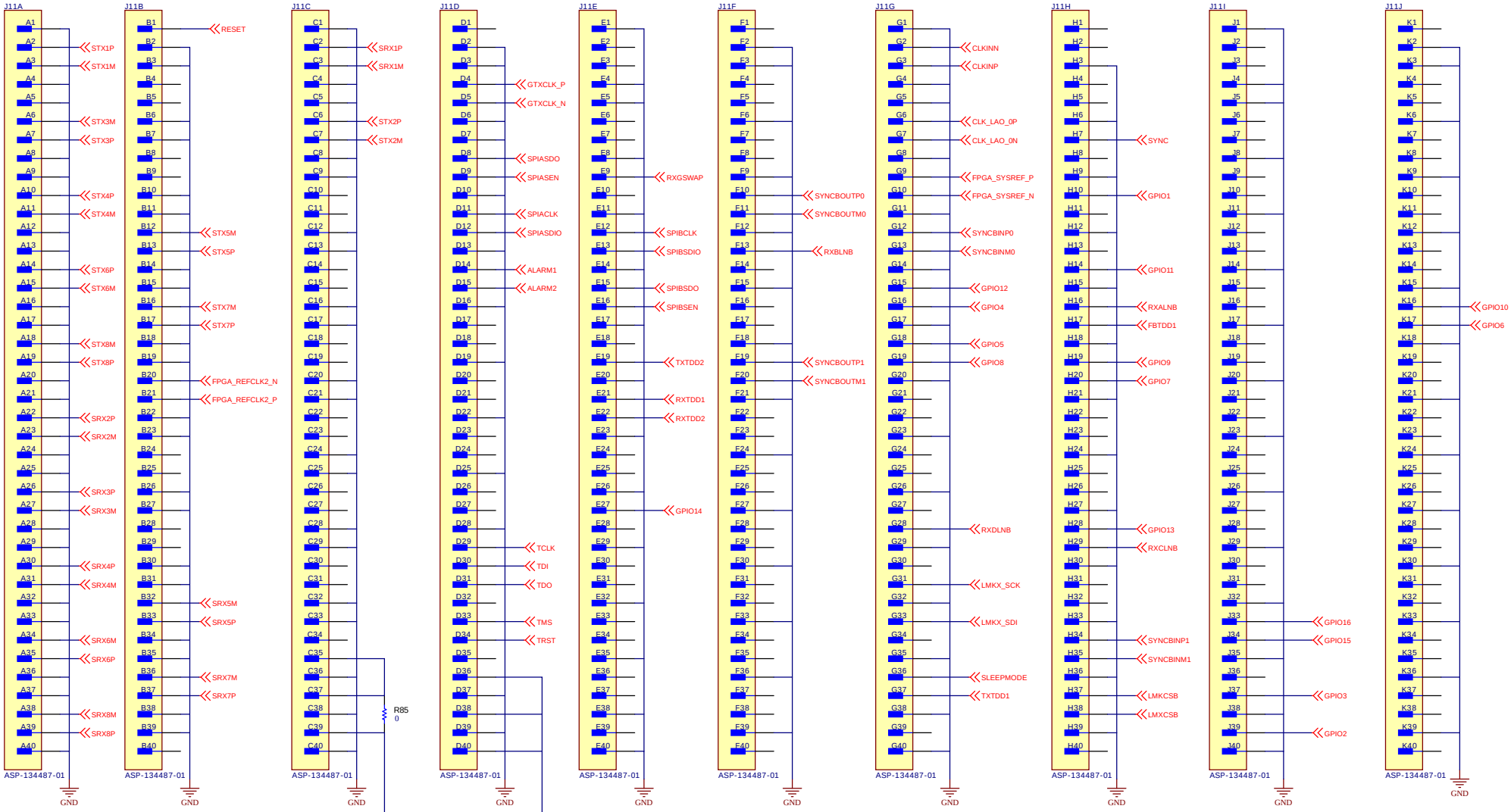

TI TX Std	Config	Flipped
A2 -	STX8	STX1
C6 -	STX7	STX2
A6 -	STX6	STX3 (inv)
A10 -	STX5	STX4
B12 -	STX4	STX5 (inv)
A14 -	STX3	SXT6
B16 -	STX2	STX7 (inv)
A18 -	STX1	STX8 (inv)

TI RX Std	Config	Flipped
C2 -	SRX8	SRX1
A22 -	SRX7	SRX2
A26 -	SRX6	SRX3
A30 -	SRX5	SRX4
B32 -	SRX4	SRX5 (inv)
A34 -	SRX3	SRX6 (inv)
B36 -	SRX2	SRX7 (inv)
A38 -	SRX1	SRX8 (inv)

Note 1: SPIA SEN placed on pin H-37 designated as SPI0_CSB[2] b/c H-34,35 allocated for SysRef
Note 2: Allocate standard 3V3 pins for 5V; option to pull in allocated 12V pins if more pins needed for current distribution.

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Drawn By:		File: FMC_Section.SchDoc	Size: B
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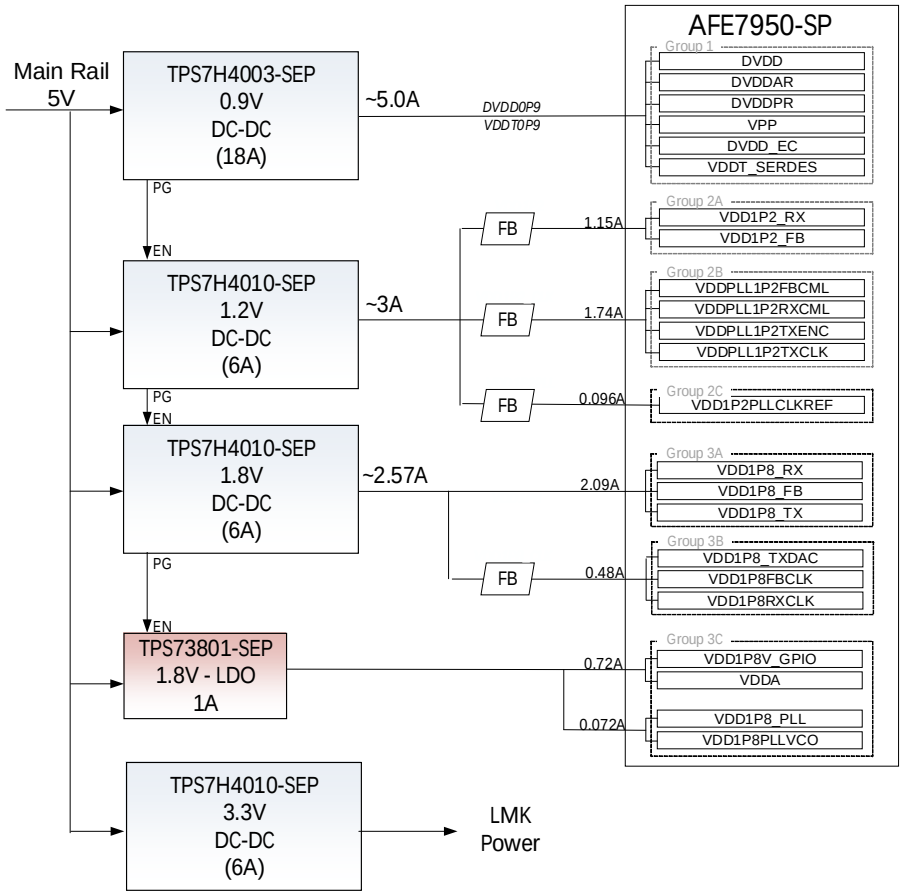

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TID #:		Project Title:	
Number:	Rev:	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: Proto	Sheet: 9 of 11
Drawn By:		File: PowerBlockDiag.SchDoc	Size: B
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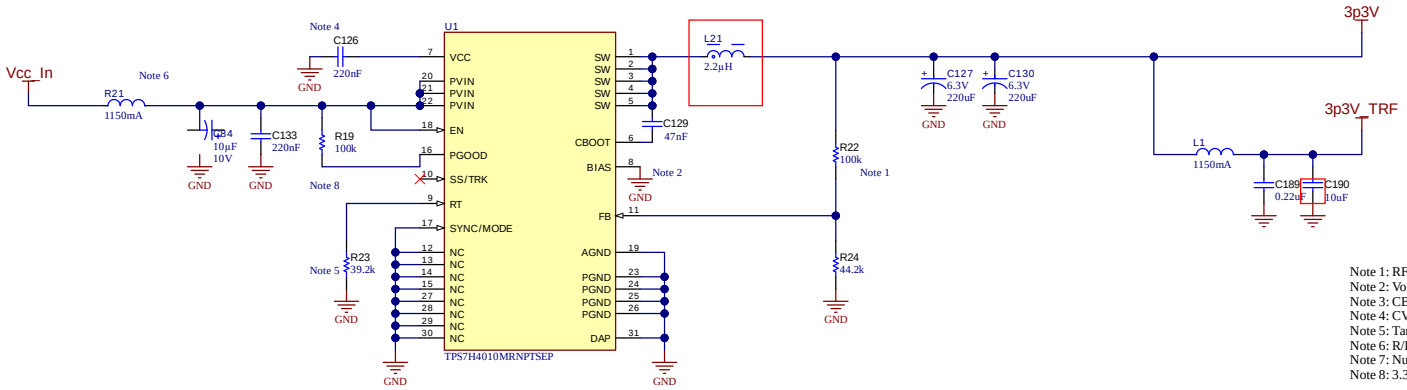
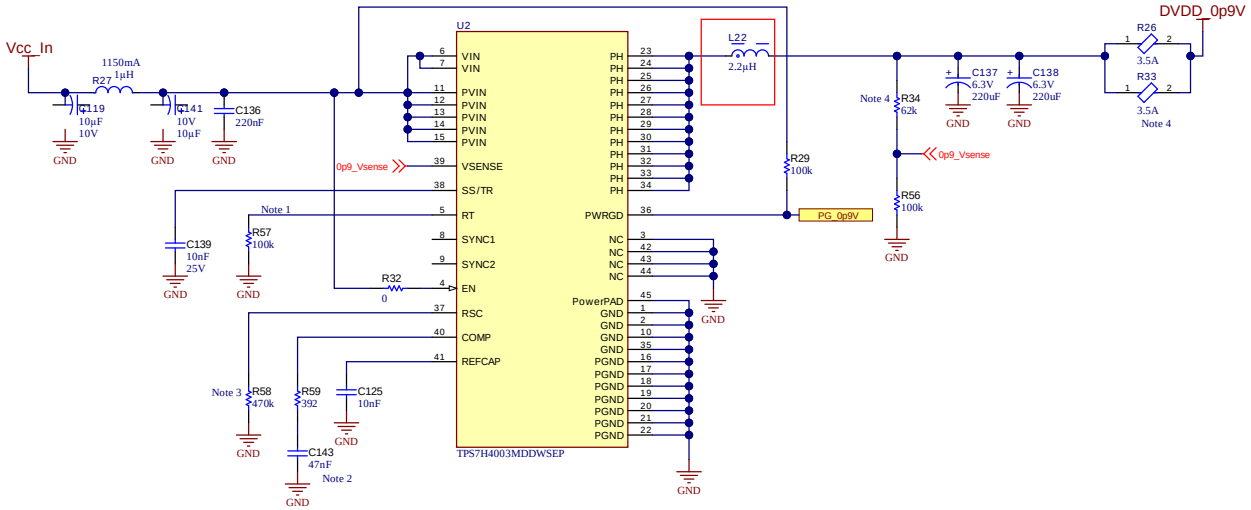


Note 1: RFBT low enough that no CFF needed
Note 2: Vout < 3.3V; Vbias not used; tied to ground
Note 3: CBoot recommended 47 nF
Note 4: CVcc recommended 2.2 uF; use 220 nF based on MIL availability
Note 5: Target Fsw = 1 MHz
Note 6: R/L/FB + C provides RC/LC filtering of any noise/spurs to infecting Vcc supply from DC-DC
Note 7: Null
Note 8: 3.3V PGOOD not used for anything but placeholder applied



Note 1: 100 kohm FSW 765 kHz; max for low Vout
Note 2: Comp Filter ideal given FSW: 370 ohm, 45 nF
Note 3: Rough value for RSC resistor
Note 4: Increase from 51k to 62k corresponding to 0.912V to 0.978V to account for FB voltage drop

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Engineer:		Contact:	

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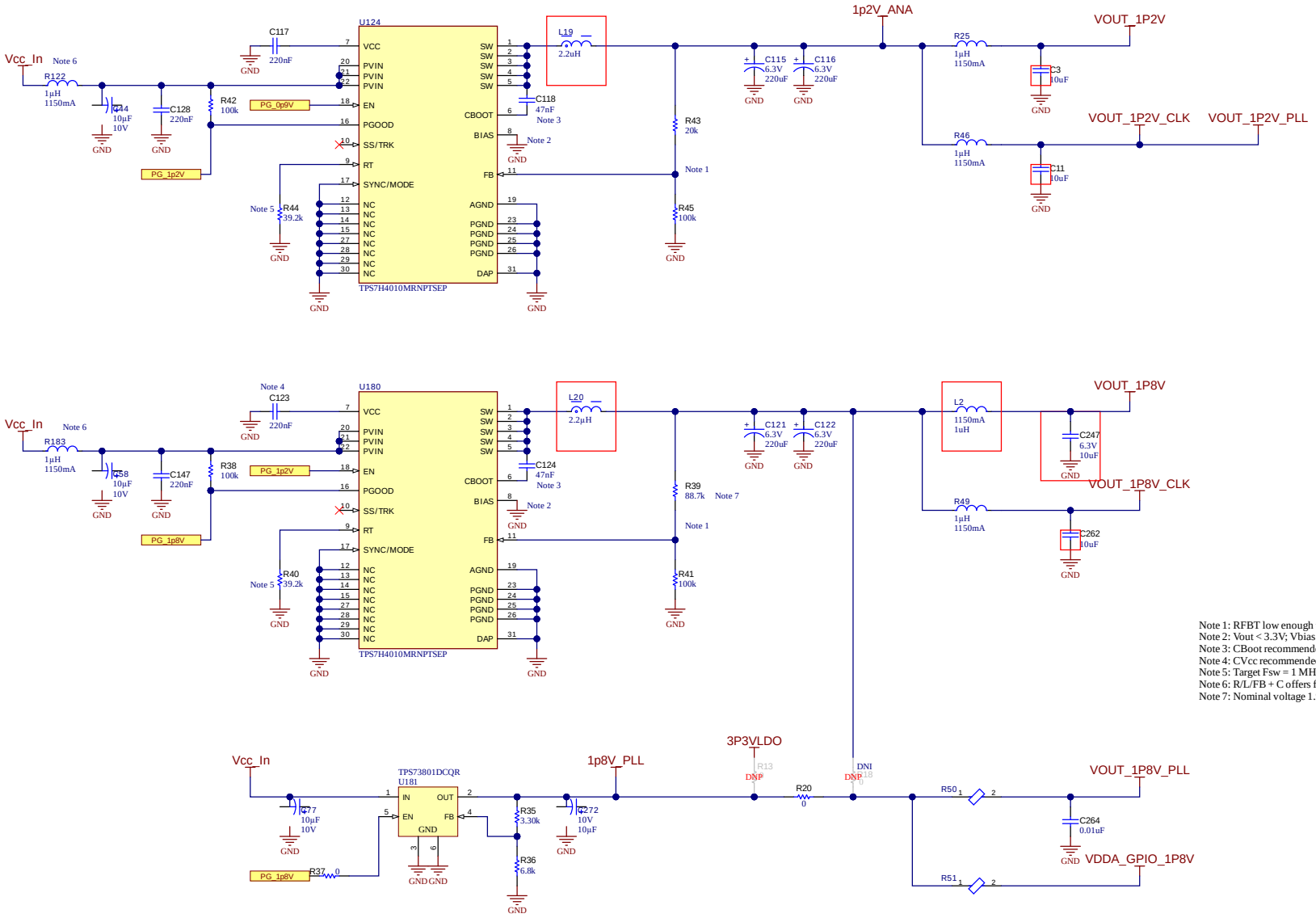

Note 1: RFBT low enough that no CFF needed
Note 2: Vout < 3.3V; Vbias not used; tied to ground
Note 3: CBoot recommended 47 nF; use 18 nF based on MIL availability
Note 4: CVcc recommended 2.2 uF; use 18 nF based on MIL availability
Note 5: Target Fsw = 1 MHz
Note 6: R/L/FB + C offers filtering to Vcc_In
Note 7: Nominal voltage 1.9V to account for Filter Loss

Layout Rework

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TID #:		Project Title:	
Number:	Rev:	Sheet Title:	
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