

User options for analog input:
 1. S/E input, AC-coupled:
 a. Default populate option
 b. Balun is {40MHz, 3GHz}
 2. Differential DC-coupled:
 a. Remove C3, C5.
 b. Populate C1 = C6 = 0 ohm.
 3. Differential AC-coupled:
 a. Remove C3, C5.
 b. Populate C1 = C6 = 100 pF.

Let C1 and C3 share a pad on the common net. Route from VIN_DIFF+ to VIN_P net as 50 ohm S/E.

Let C5 and C6 share a pad on the common net. Route from VIN_DIFF- to VIN_N net as 50 ohm S/E.

Let C32, C30 and C262 share a pad on the common net. Let C33, C36 and C263 share a pad on the common net.

Let R18 and R19 share a pad on the common net. Let R20 and R21 share a pad on the common net.

Priorities for placement:
 1. Decoupling caps close to IC.
 2. J_VA12, J_VA19, J_VD12 close to IC.

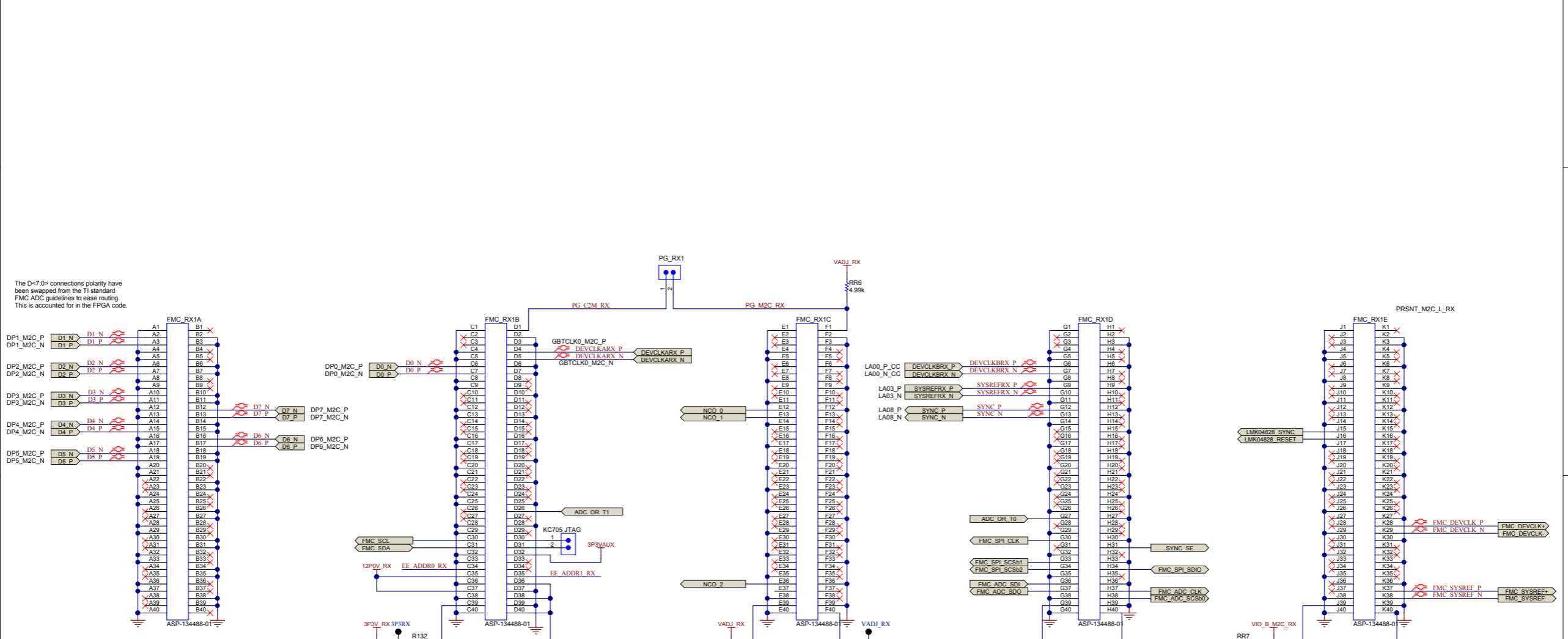
The IC pad is the only ground connection for this IC. Ensure good connection through multiple vias to the PCB ground planes.

Locate close to U2A output pins to minimize stubs

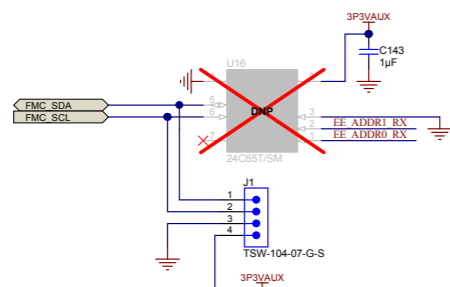
Designed for: Internal Use Only	Mod. Date: 9/10/2014
Project Title: ADC12JXXXXEVM	Number: 600847
Sheet Title:	Rev: A
Assembly Variant: 002_ADC12J4000EVM	Sheet: 1 of 7
File: ADC12JXXXXEVM_A_1_ADC_IO.SchDoc	Size: B
Contact: http://www.ti.com/support	Engineer: Jim Brinkhurst

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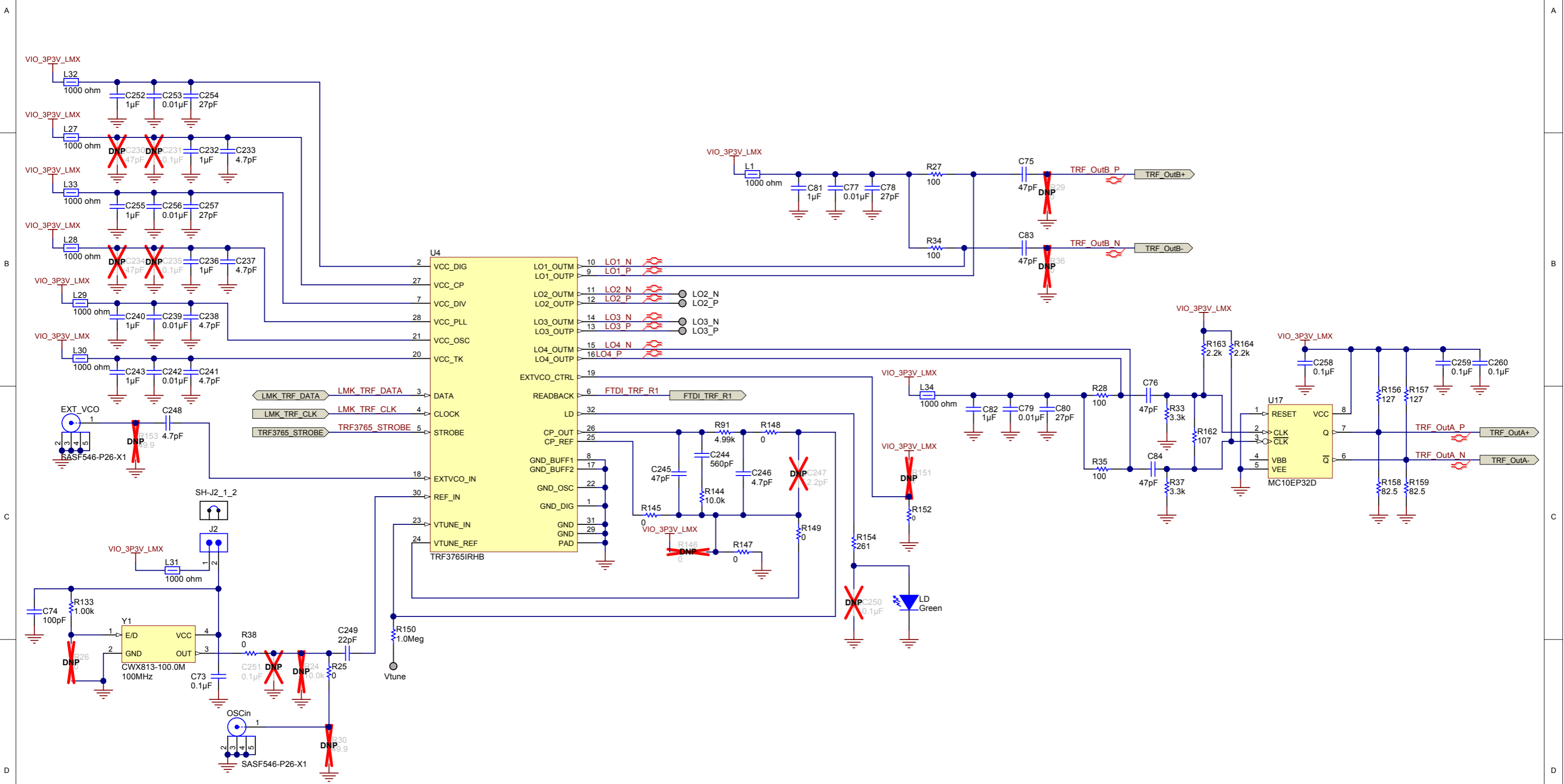




The D<7,0> connections polarity have been swapped from the TI standard FMC ADC guidelines to ease routing. This is accounted for in the FPGA code.



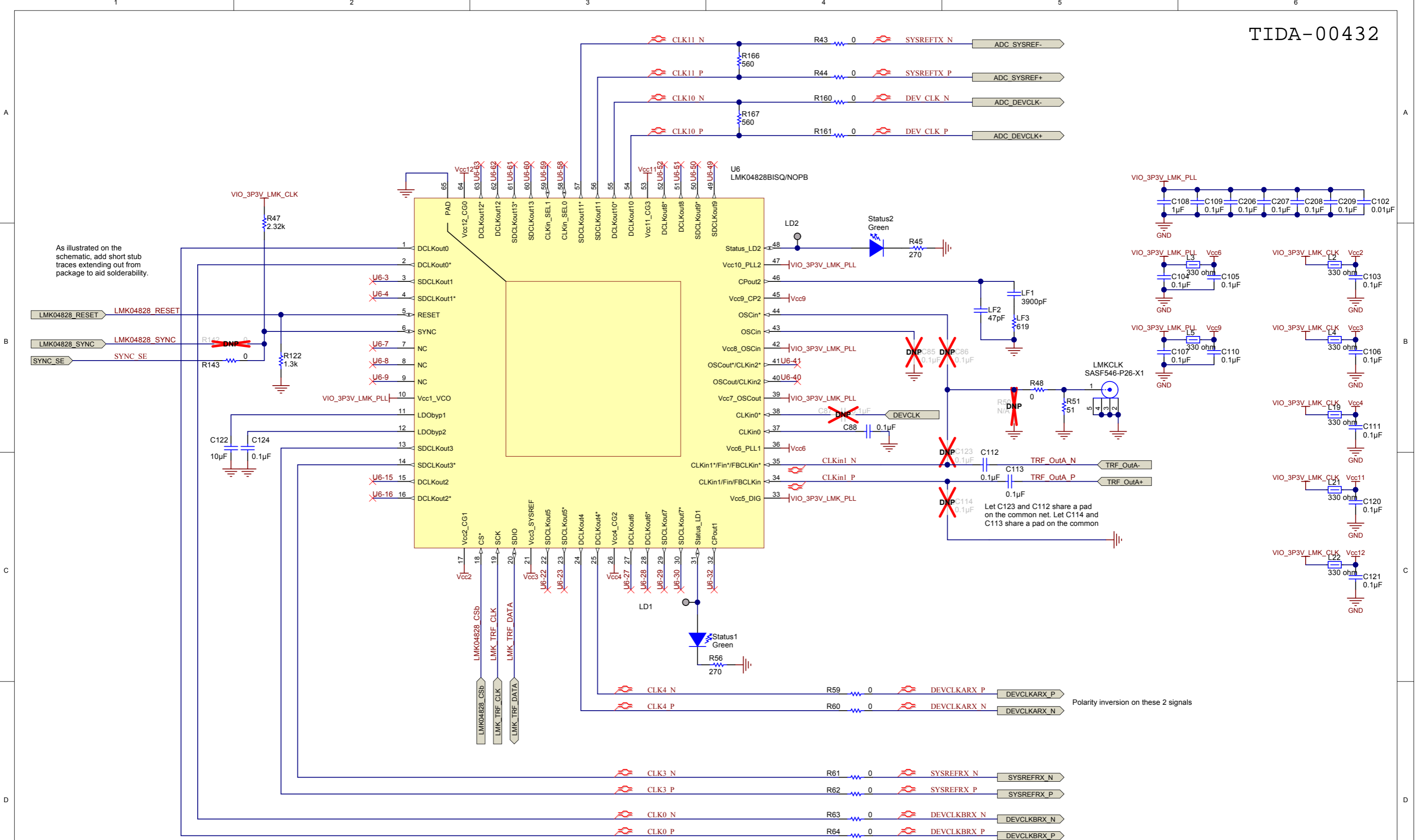
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SVN Rev: Unknown revision	Assembly Variant: 002_ADC12J4000EVM	Project Title: ADC12JXXXXEVM	
Drawn By: Not shown in title block	File: ADC12JXXXXEVM_A_3_TRF3765.SchDoc	Sheet Title: TRF3765	Sheet: 3 of 7
Engineer: Jim Brinkhurst	Contact: http://www.ti.com/support	Size: B	http://www.ti.com





As illustrated on the schematic, add short stub traces extending out from package to aid solderability.

Let C123 and C112 share a pad on the common net. Let C114 and C113 share a pad on the common

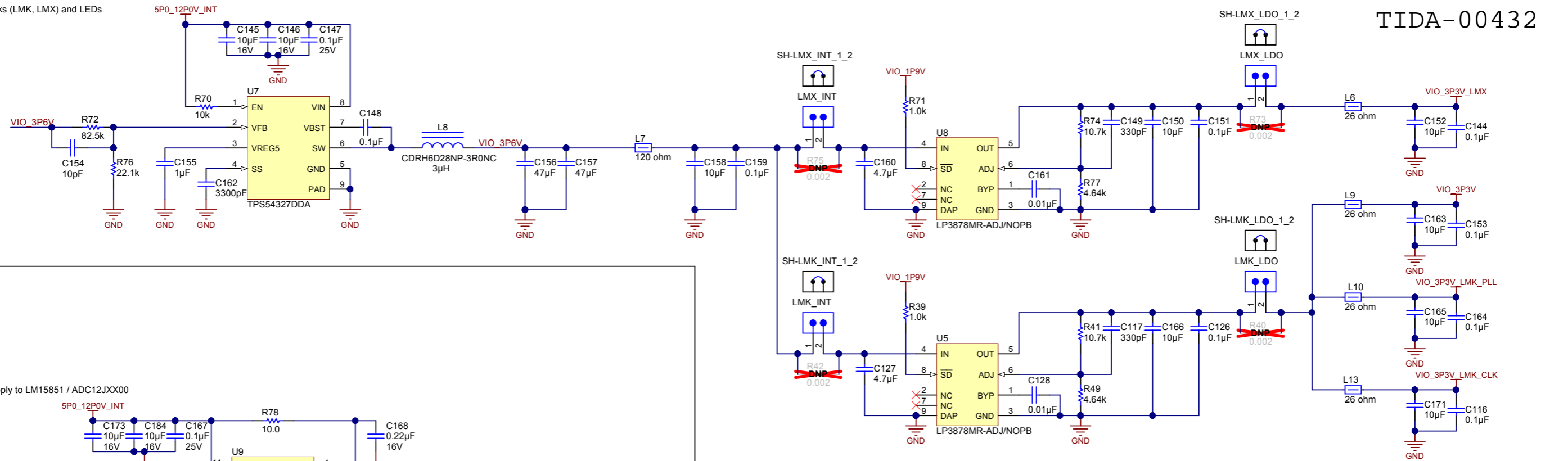
Polarity inversion on these 2 signals

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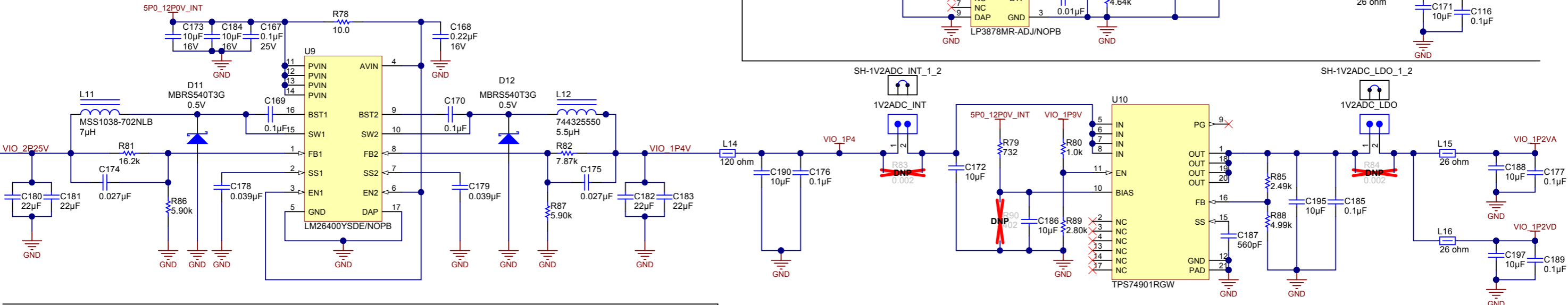
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SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 002_ADC12J4000EVM	Sheet: 4 of 7
		File: ADC12JXXXXEVM_A_4_LMK04828.SchDoc	Size: B
		Contact: http://www.ti.com/support	http://www.ti.com



3.3V supply to clocks (LMK, LMX) and LEDs

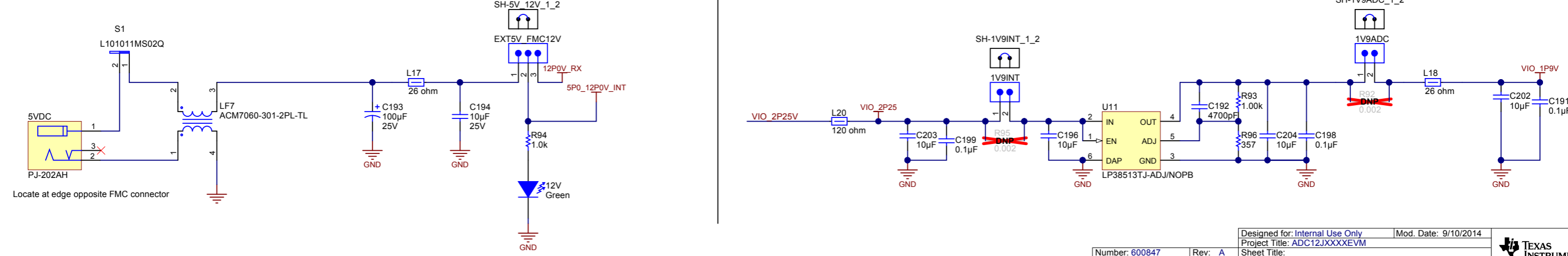


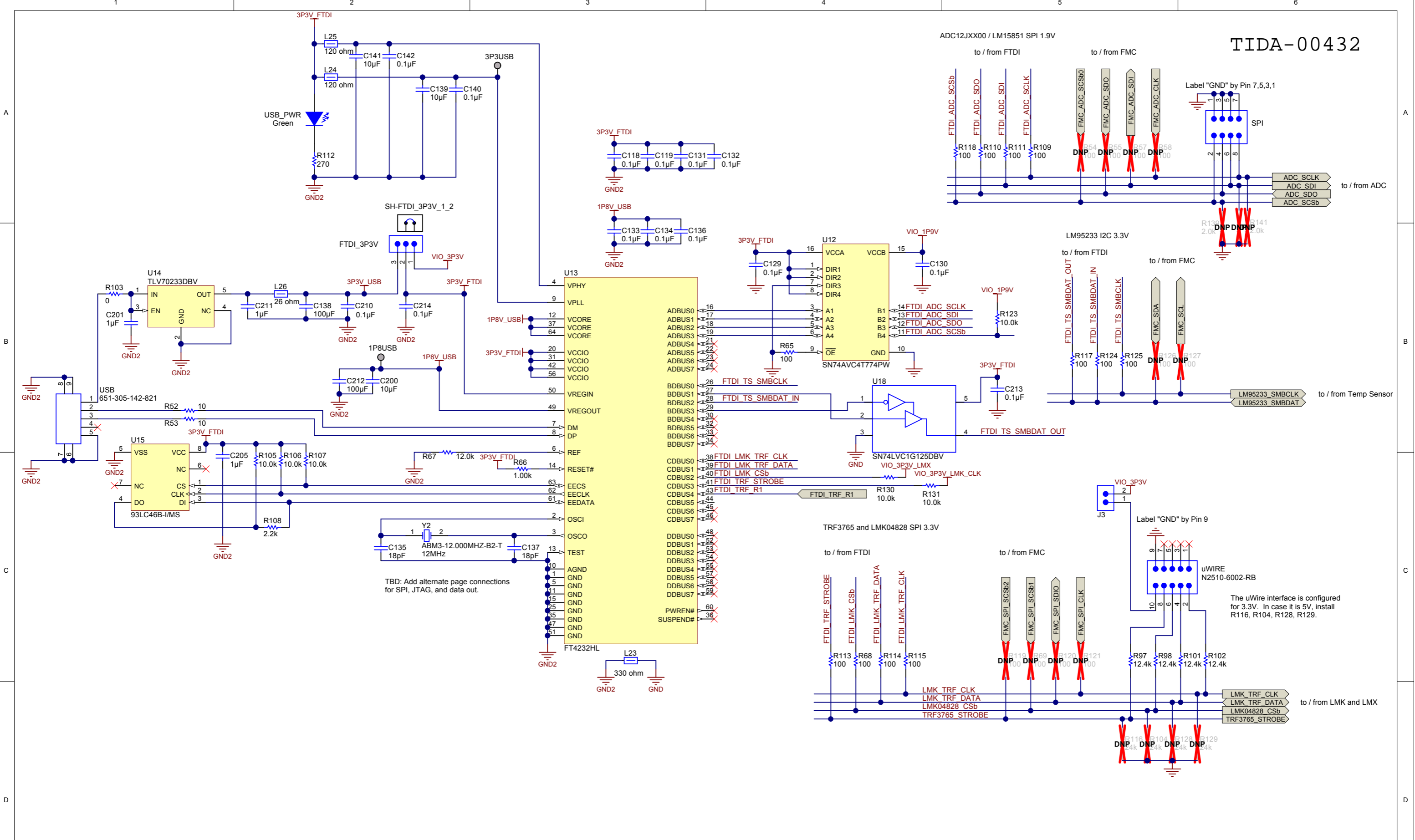
1.9V and 1.2V supply to LM15851 / ADC12JXX00



12V main supply, from jack or via FMC connector to regulators

Add text label: "5V VIA JACK" and "12V VIA FMC, Install R90 for 12V operation"





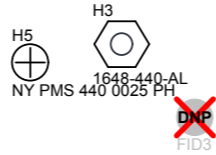
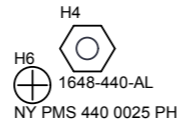
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~~DNP~~
FID1

PCB Number: 600847
PCB Rev: A

PCB
ESD LOGO
ESD Susceptible

PCB
LOGO
Texas Instruments



~~DNP~~
FID2

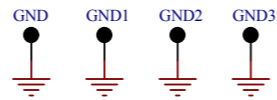
~~DNP~~
FID3

H9
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H10
MECH
FMC - FMC Nut

H11
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H12
MECH
FMC - FMC Nut



Place at least two of the GND test points in the power section.

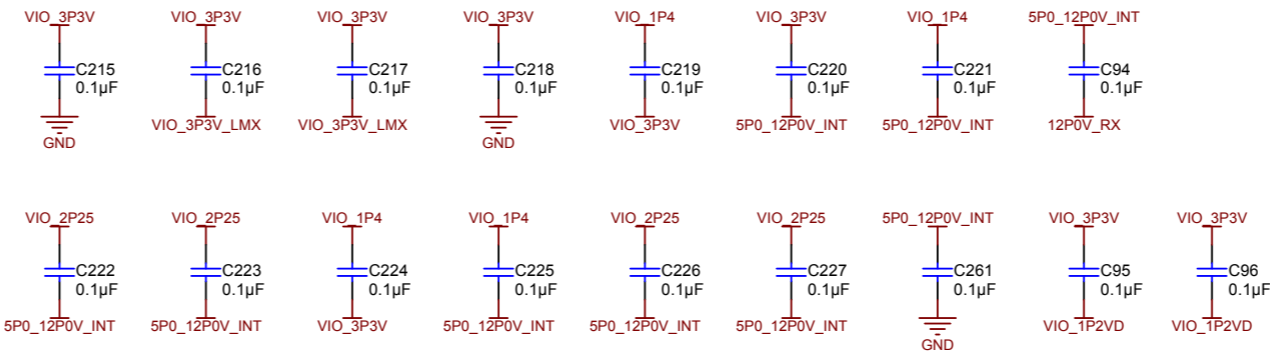
LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2., unless otherwise specified.



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