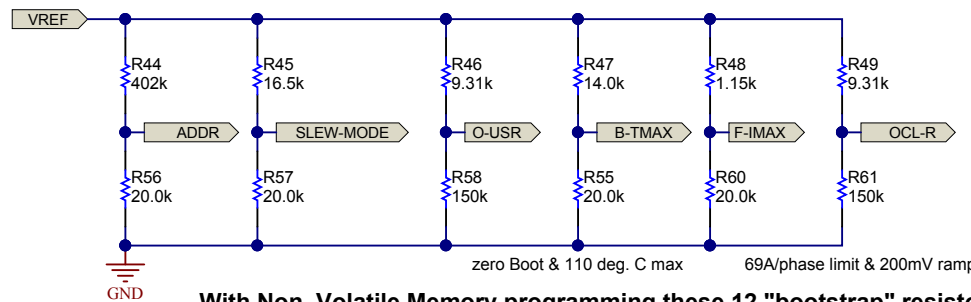


SVID address 0d & PMBus address 97d

OSR & USR both off

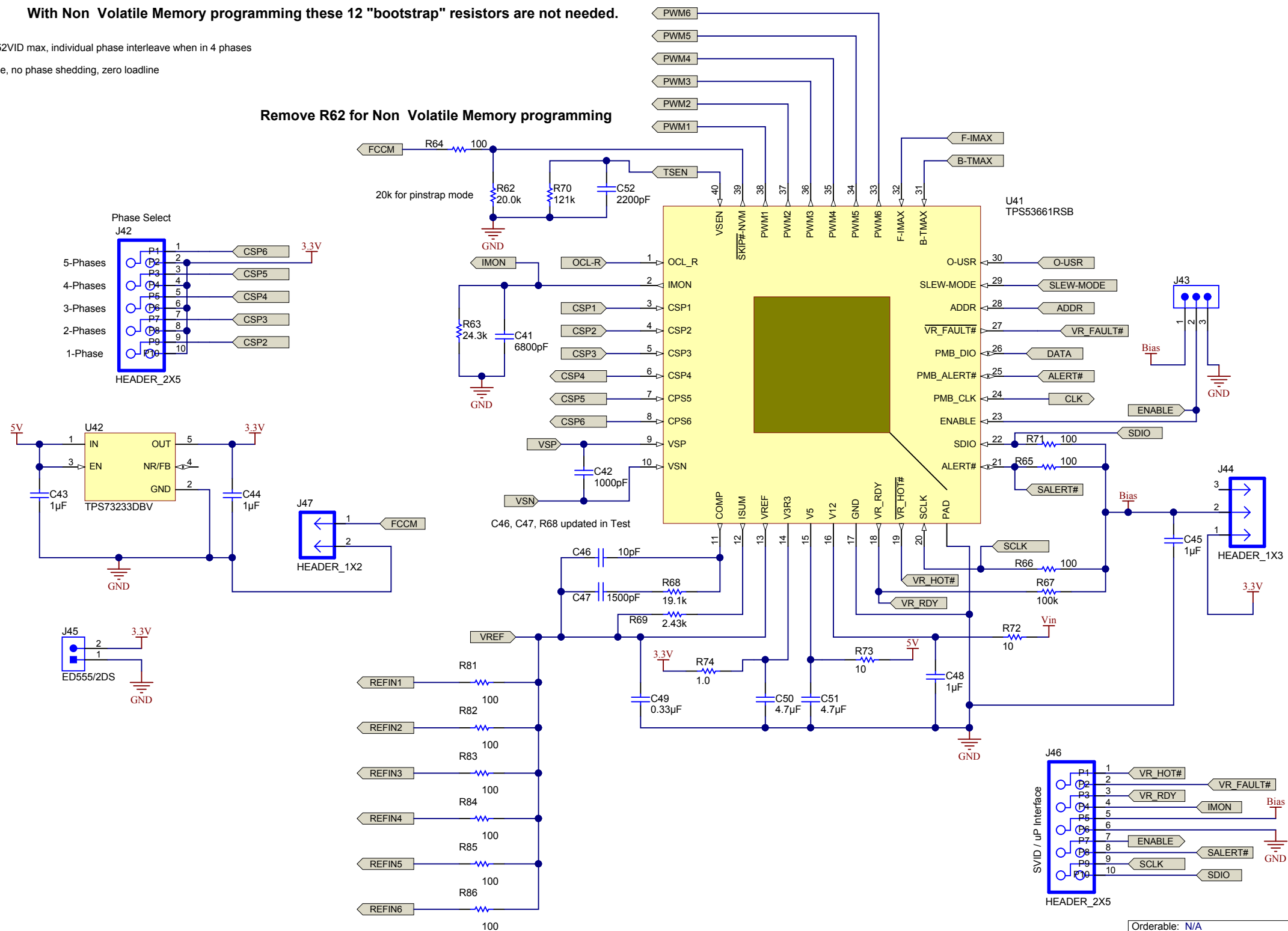
300kHz switching / 240A max



With Non Volatile Memory programming these 12 "bootstrap" resistors are not needed.

slew = 5mV/us, 1.52VID max, individual phase interleave when in 4 phases
no turbo mode, no phase shedding, zero loadline

Remove R62 for Non Volatile Memory programming

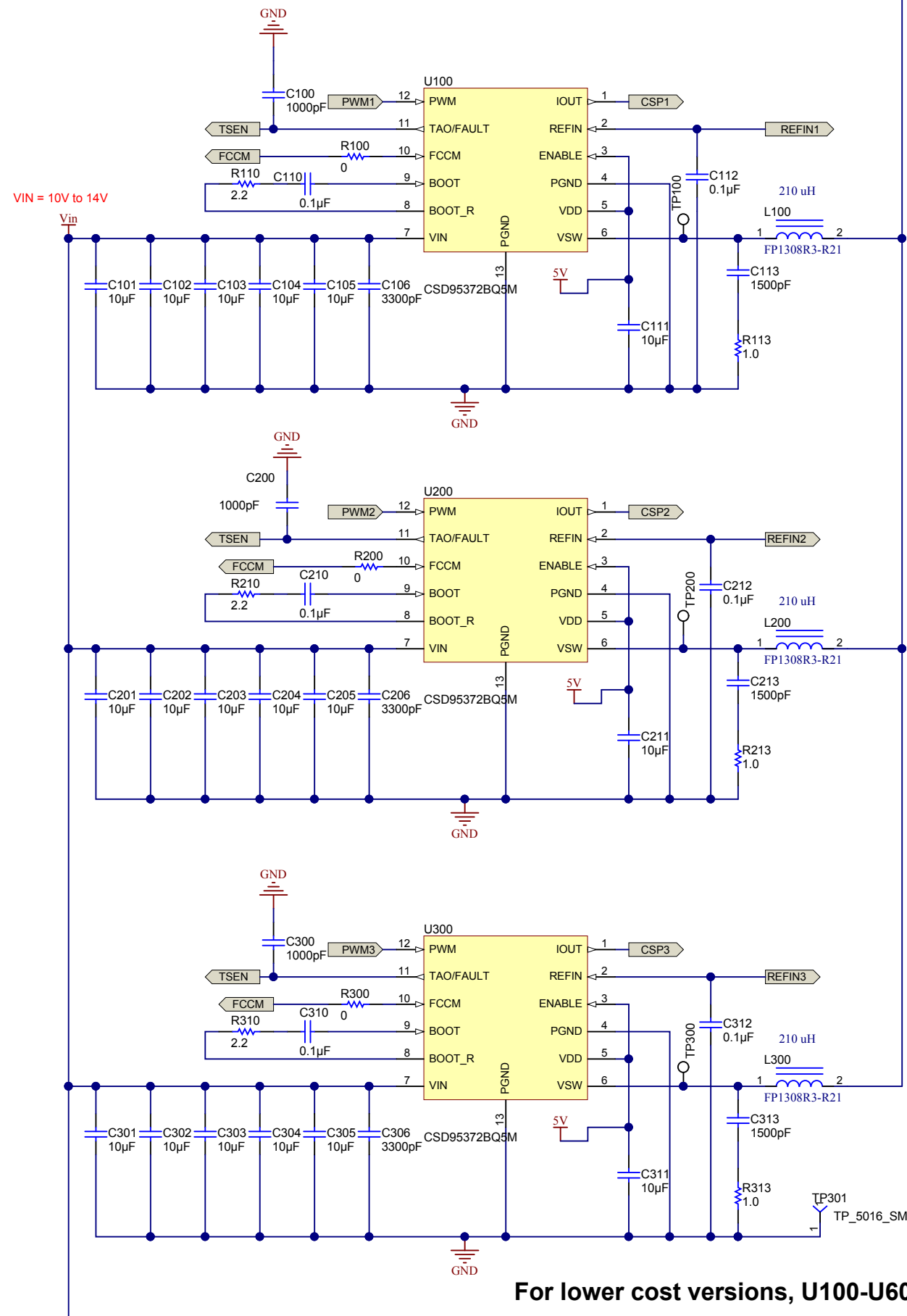


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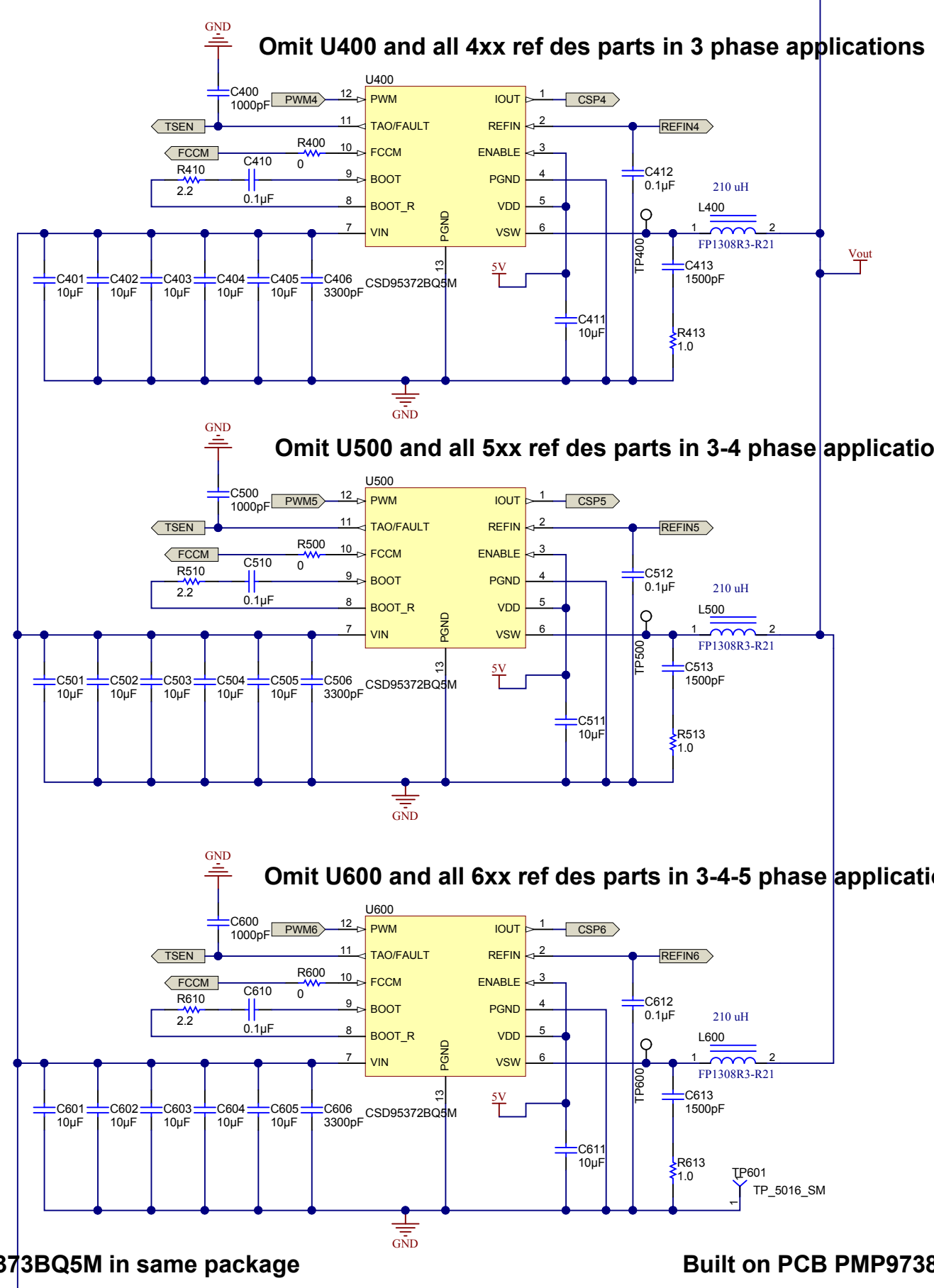
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Orderable: N/A	Designed for: Public Release	Mod. Date: 6/11/2015
TID #: PMP11208	Project Title: 900mV 220A off 11-13Vin 6 Phases	
Number: PMP11208	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 3
Drawn By:	File: PMP11208_TPS53661_Control.SchDoc	Size: B
Engineer: Josh Mandelcom	Contact: http://www.ti.com/support	





For lower cost versions, U100-U600 become CSD95373BQ5M in same package

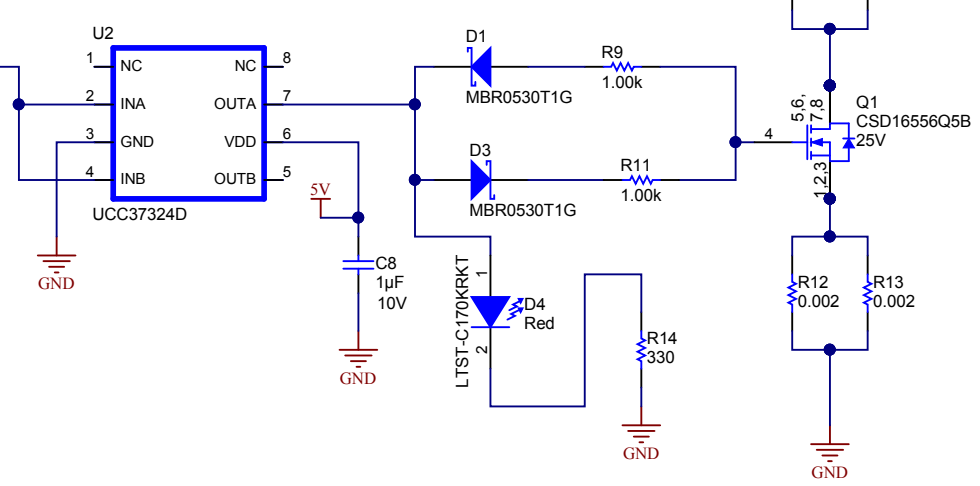
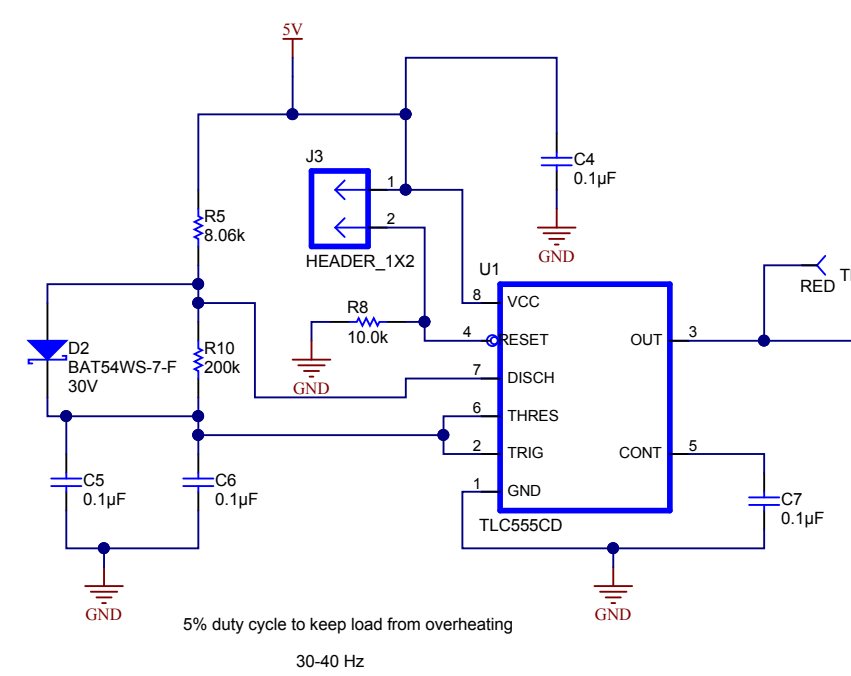
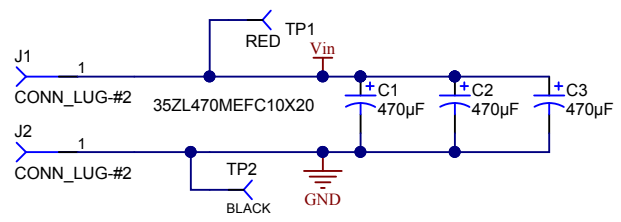


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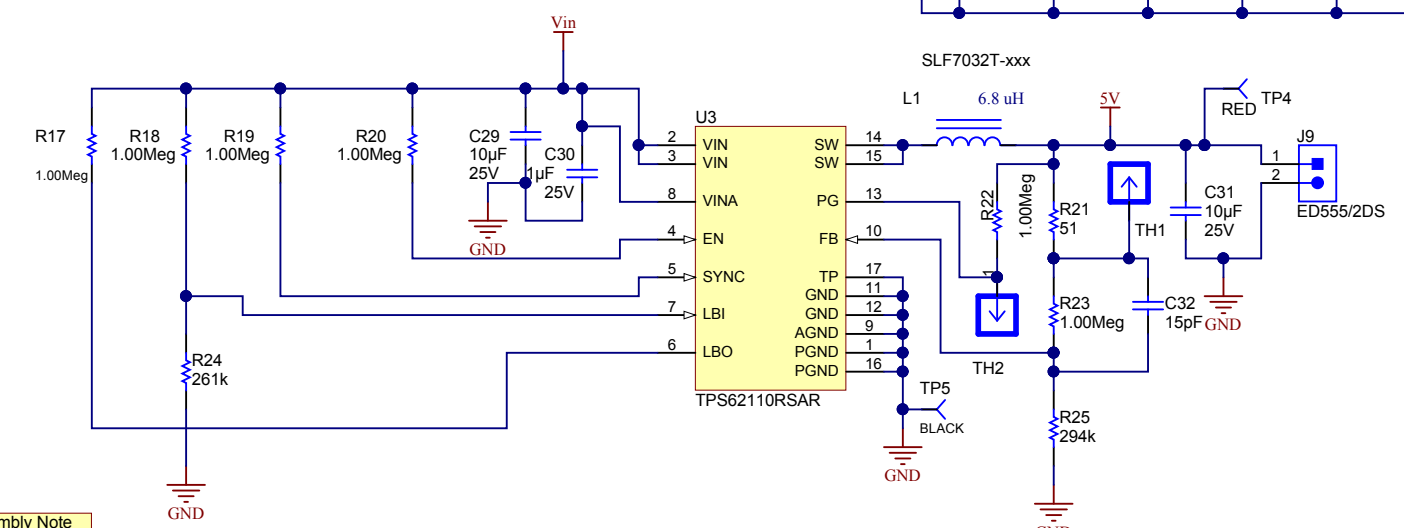
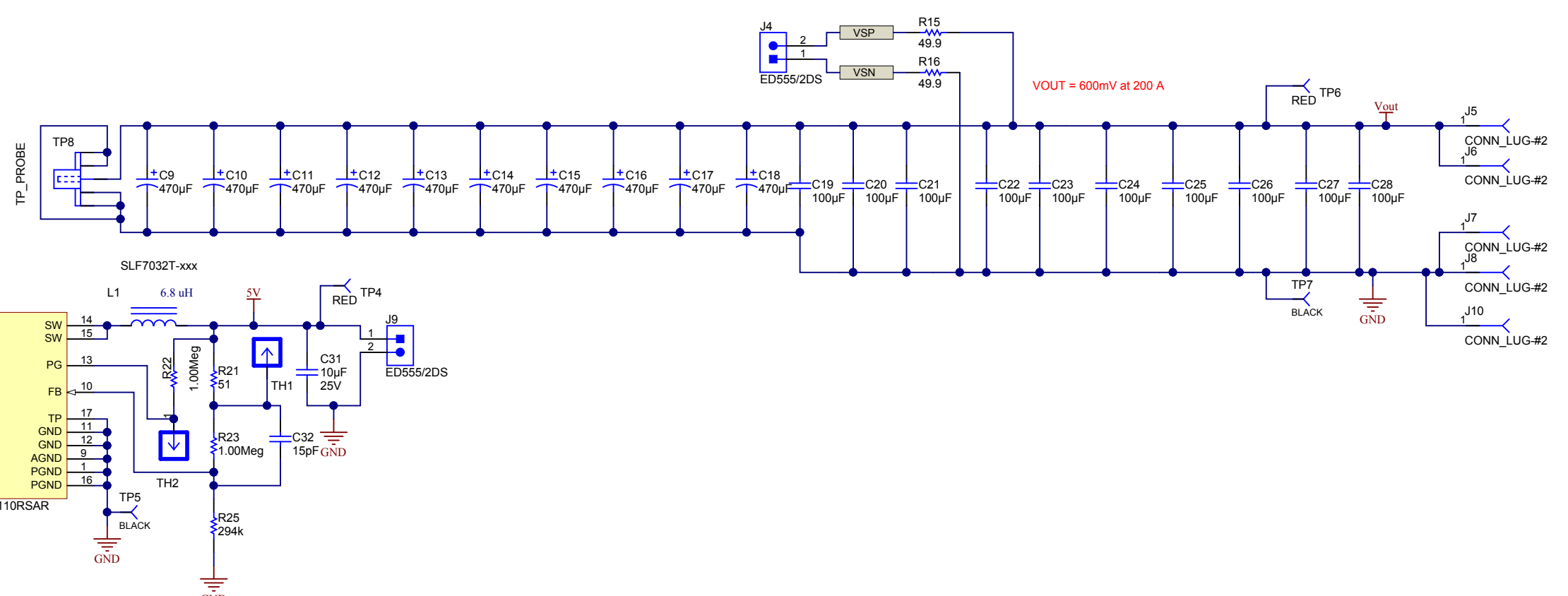
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TID #: PMP11208	Project Title: 900mV 220A off 11-13VIN 6 Phases	
Number: PMP11208	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: PMP11208_PowerTrains_CSD95372Bs.SchDoc	Size: B
Engineer: Josh Mandelcom	Contact: http://www.ti.com/support	





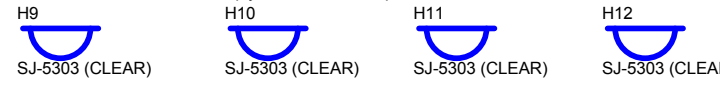
At 600mV output with values shown:
 70A step load in 8 usec
 85A load dump in 8 usec



ZZ2
Assembly Note
 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



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TID #: PMP11208	Project Title: 900mV 220A off 11-13Vin 6 Phases	
Number: PMP11208	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 3
Drawn By:	File: PMP11208_Input_Bias_DynamicLoad.SchDoc	Size: B
Engineer: Josh Mandelcom	Contact: http://www.ti.com/support	



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