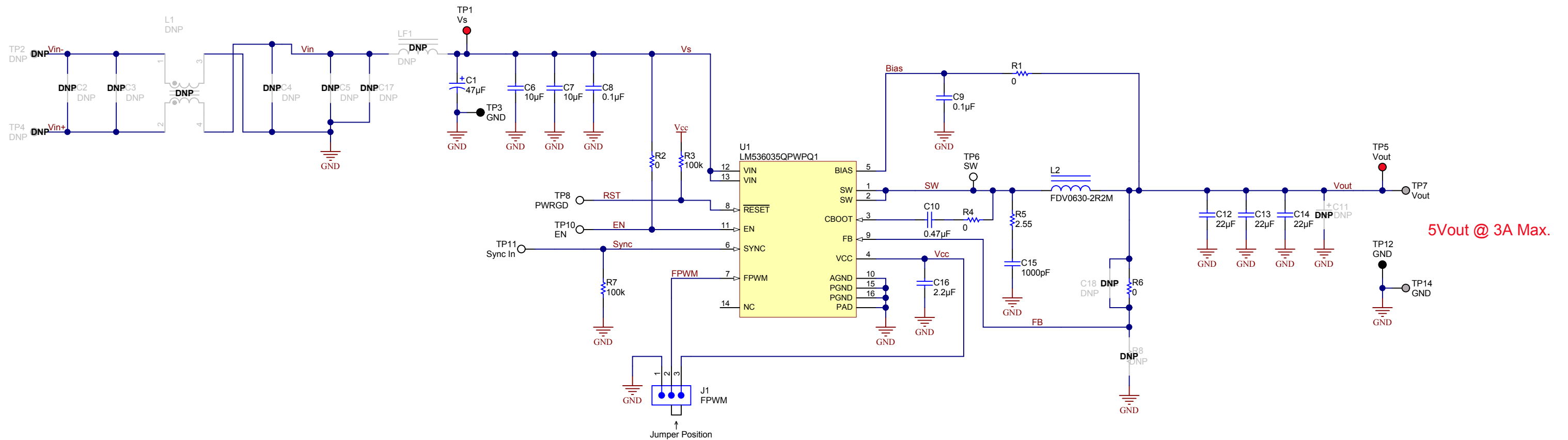


Input Voltage = 7V_{in} to 36V_{in} (40V_{in} Abs. Max.)



NOTES:

1. All components marked with "DNP" which denotes "Do Not Populate" need to be omitted from the circuit.
2. Input supplied at testpoints TP1 and TP3.
3. J1 Connected in FPWM configuration, enabling the part to run in forced PWM mode.
4. Install C11 if improvements are needed for load transient response (i.e. lower under-shoots and over-shoots).
5. The 5V_{out} option of the LM53603 regulator is used for this design (LM536035QPWPQ1), with the displayed resistor divider configuration (i.e. FB is connected directly to V_{out}, with no top or bottom divider resistors).
6. Design is built on the PMP9440 PCB.

Orderable: N/A	Designed for: Public Release	Mod. Date: 4/10/2015
TID #: PMP10534	Project Title: LM53603 Synchronous Buck Regulator	
Number: PMP10534	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 2
Drawn By:	File: PMP10534 Schematics.SchDoc	Size: B
Engineer: Hrag Kasparian	Contact: http://www.ti.com/support	

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H1 NY PMS 440 0025 PH H2 NY PMS 440 0025 PH H3 NY PMS 440 0025 PH H4 NY PMS 440 0025 PH

H5 1902C H6 1902C H7 1902C H8 1902C

FID1 FID2 FID3

PCB Assembly
PMP9440

PCB
LOGO
Texas Instruments




Label Table	
Variant	Label Text
001	

ZZ2
Assembly Note
 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #: PMP10534	Project Title: LM53603 Synchronous Buck Regulator		
Number: PMP10534	Rev: A	Sheet Title: Hardware	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 2	
Drawn By: Hrag Kasparian	File: PMP10534_TID_Hardware.SchDoc	Size: B	
Engineer: Hrag Kasparian	Contact: http://www.ti.com/support		

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