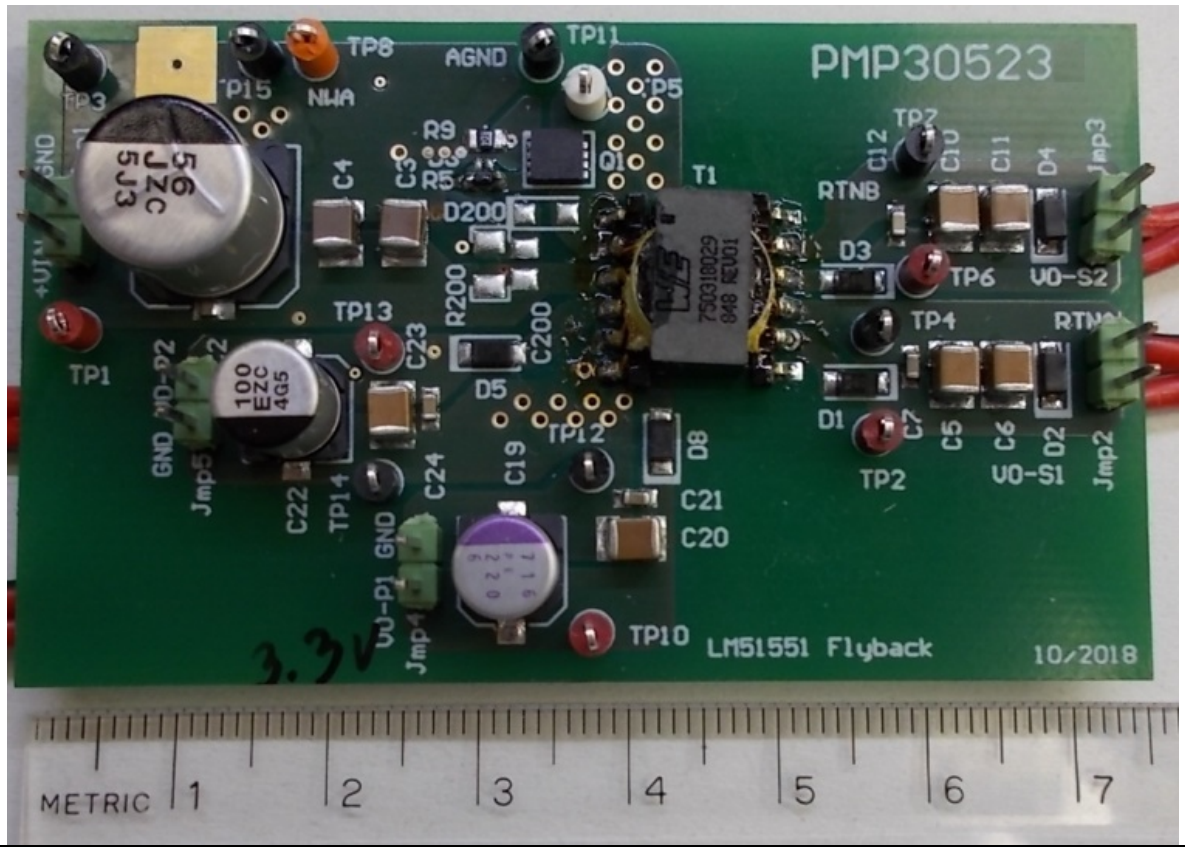
Test Report: PMP30523RevD

Wide Input Range 3 W Power Reference Design with four Outputs

Description

This tiny power supply using LM51551-Q1 generates four output voltages, two of them isolated. On primary side 11 V/100 mA plus 3.3 V/300 mA I/O voltage is available plus another two 11 V/50 mA outputs on secondary side.
By using a cost effective discrete linear regulator the input voltage range is expanded up to 60 V; by diode-ORing the controller itself is supplied out of the primary 11 V, means no losses at the LDO that is just used during startup.
The power stage could be configured either in flyback or SEPIC topology; for less EMI here the SEPIC topology is used by implementing flying capacitor C8. Either flyback or SEPIC is working in DCM to use a small transformer and to achieve best dynamic performance by shifting RHPZ into high frequency range.
The loop is closed on primary side to avoid an opto isolator; by using a multiple feedback path the loop could be closed at 11 V primary or 3.3 V primary – or just using both; by using both paths this could be weighted by the demand of the application. Here the feedback current of 1mA is combined by 500 uA out of 3.3 V, another 500 uA out of 11 V. The primary side regulation needs best coupling in between primary output winding and secondary output winding of the transformer; a coupling >99% is mandatory to achieve reasonable cross regulation and load regulation.
The PCB PMP30523 RevB needs transformer revision r01, that is just suited for prototyping purposes.
For mass production use WE 750 31 80 29 revision r00.



1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage (DC)	6 V to 60 V, startup needs >7.5V
Output Voltage 1 (non-isolated)	3.3 V
Output Current 1 (max)	300 mA
Output Voltage 2 (non-isolated)	11 V
Output Current 2 (max)	100 mA
Output Voltage 3 and 4 **(both isolated)**	11 V
Output Current 3 and 4 (max)	50 mA
Switching frequency	200 kHz

1.2 Considerations

- This circuit switches on at 7.5 V input voltage and switches off at 5.7 V input voltage.
- The regulation is primary side on both non-isolated output voltages (mixed regulation 50% / 50%).
- As load a resistor switchboard was used – 10% / 20% / 50% / 100% load for each output.
- Unless otherwise mentioned the measurements were done with full load at all outputs.
- The converter has been tested at 6V / 24V / 60V input voltage

2 Testing and Results

2.1 Efficiency Graphs

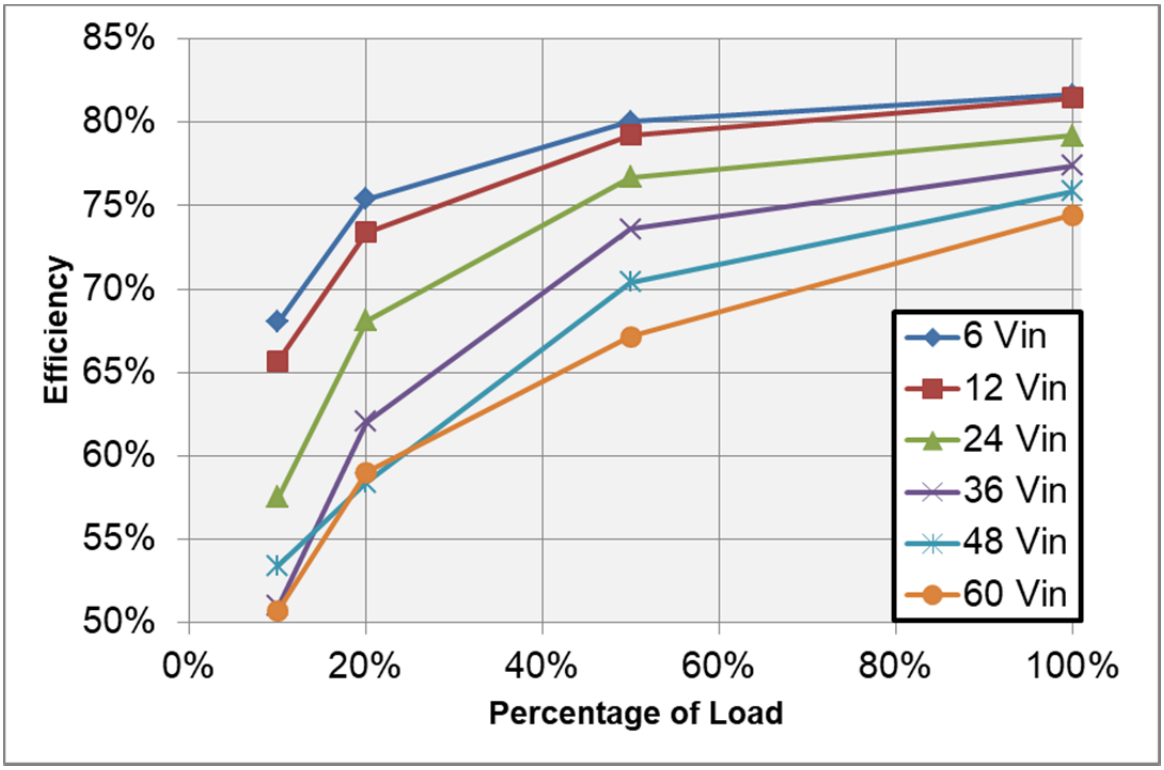


Figure 1. Efficiency vs Load

Due to availability BSZ096N10LS5 was used in the circuit.
With BSZ146N10LS5 the switching losses will be reduces slightly.
A bigger core geometry and rework on the transformer windings will improve efficiency further; this revision has been designed for smallest size.

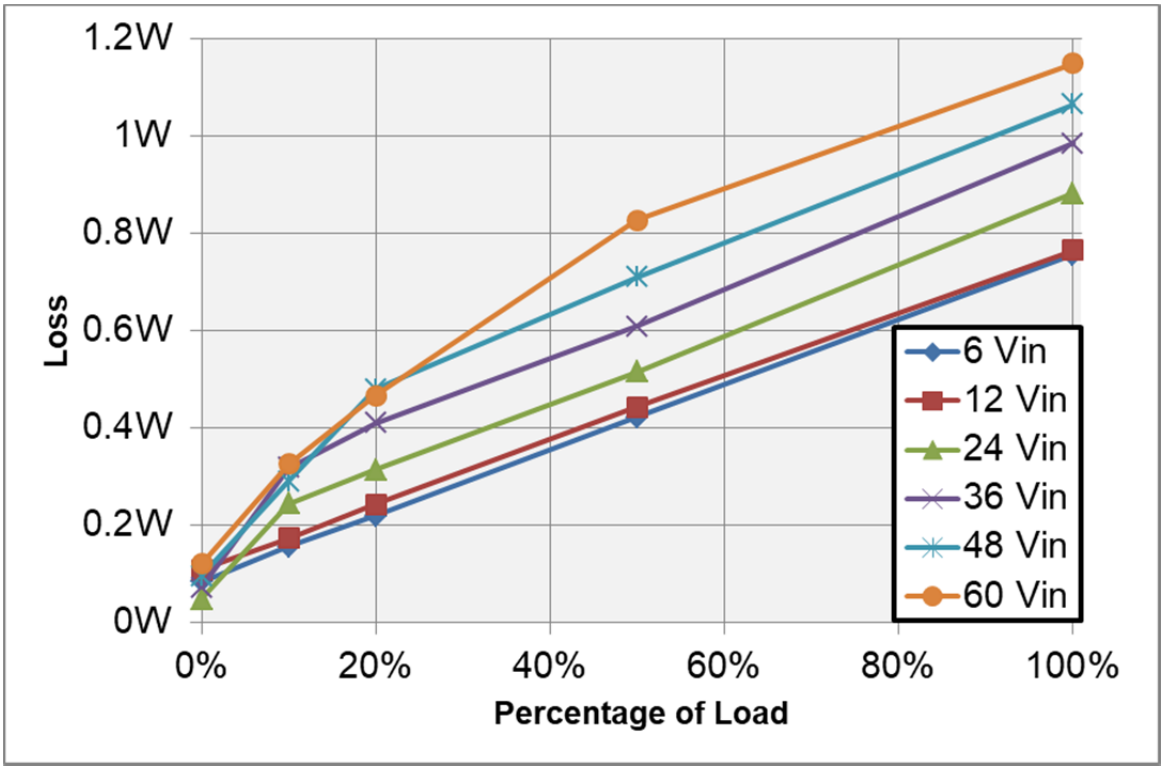


Figure 2. Loss vs Load

2.2 Load Regulation (feedback weighted 50% out of 3.3V pri and 50% out of 11V pri)

2.2.1 6 V Input Voltage

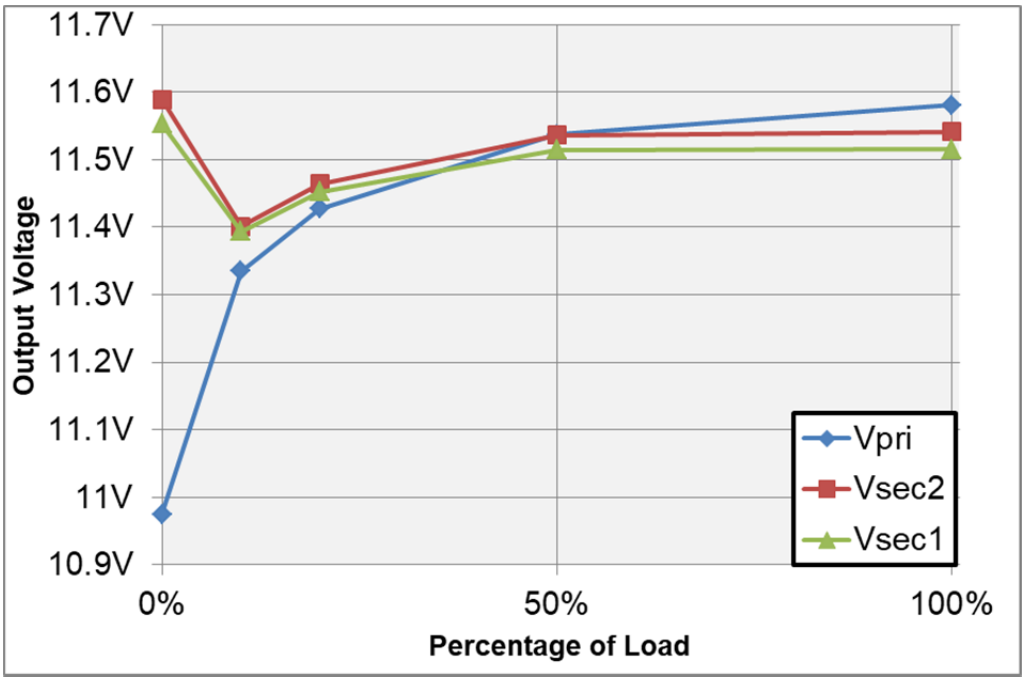


Figure 3. Output Voltage vs Load for the 11 V Outputs

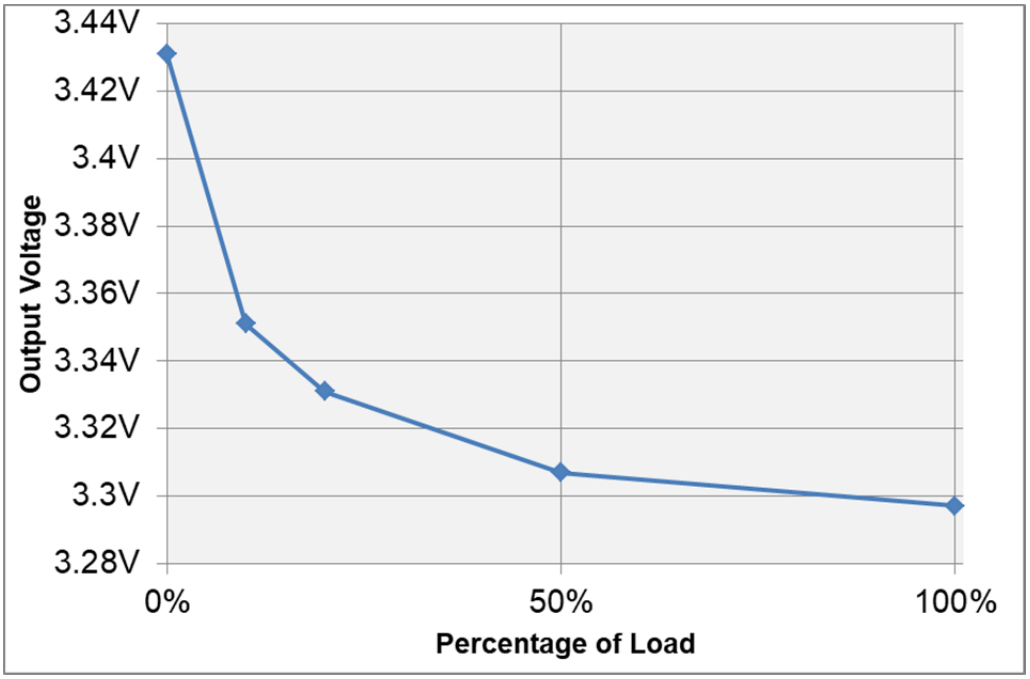


Figure 4. Output Voltage vs Load for the 3.3 V Output

2.2.2 24 V Input Voltage

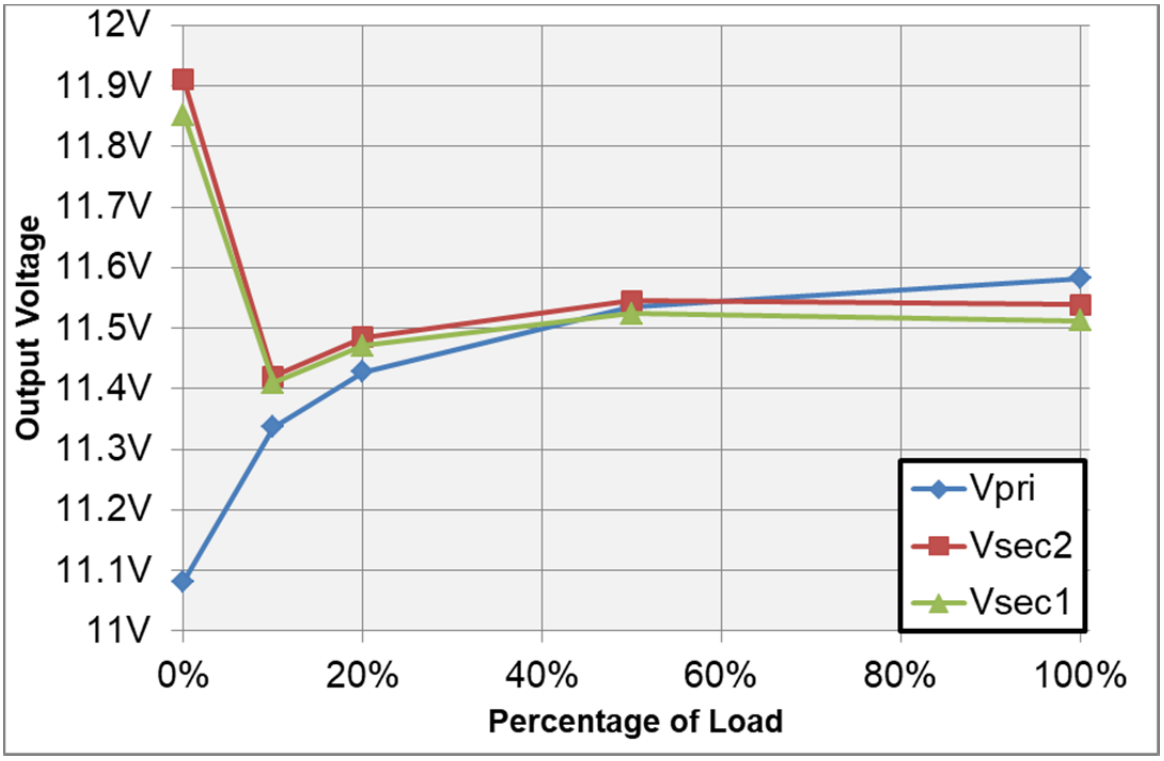


Figure 5. Output Voltage vs Load for the 11 V Outputs

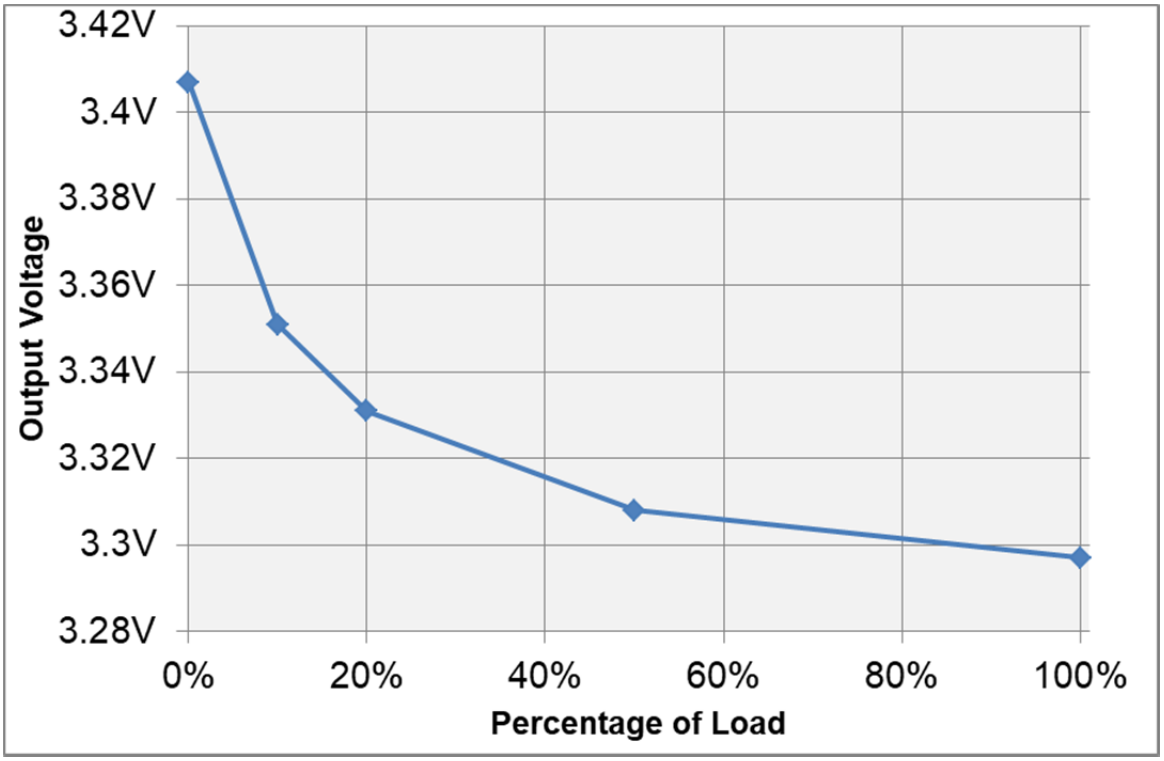


Figure 6. Output Voltage vs Load for the 3.3 V Output

2.2.3 60 V Input Voltage

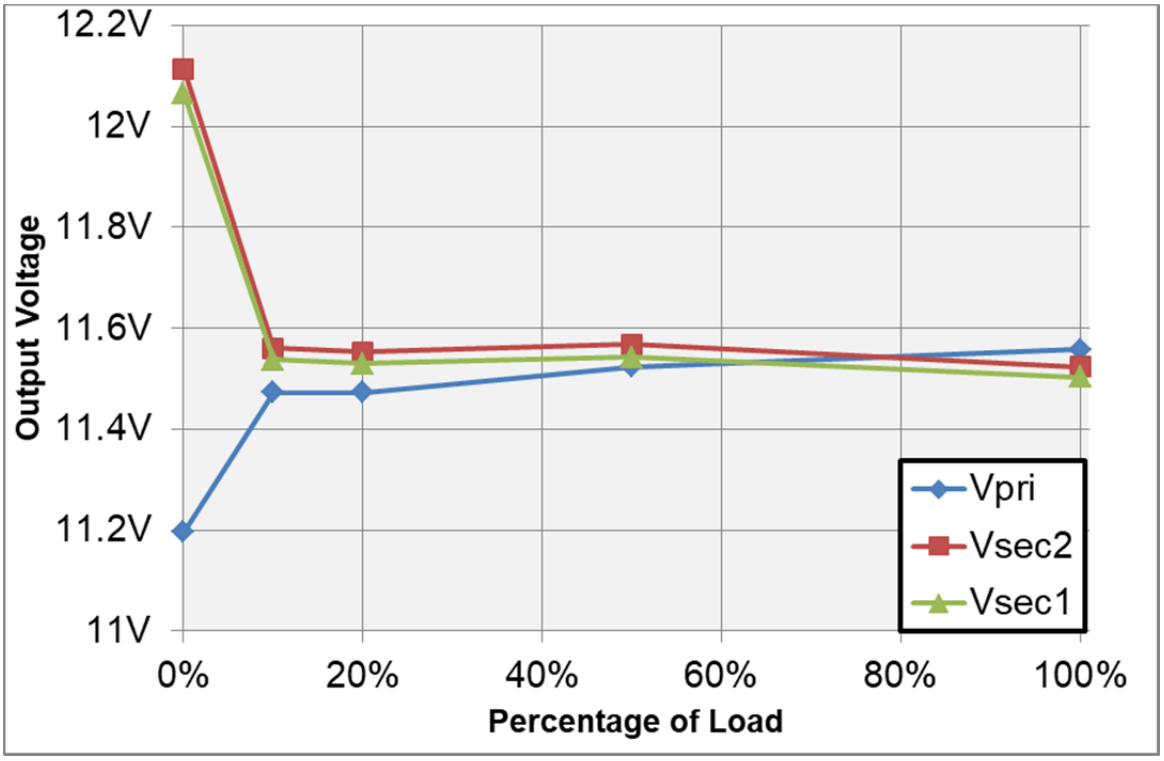


Figure 7. Output Voltage vs Load for the 11 V Outputs

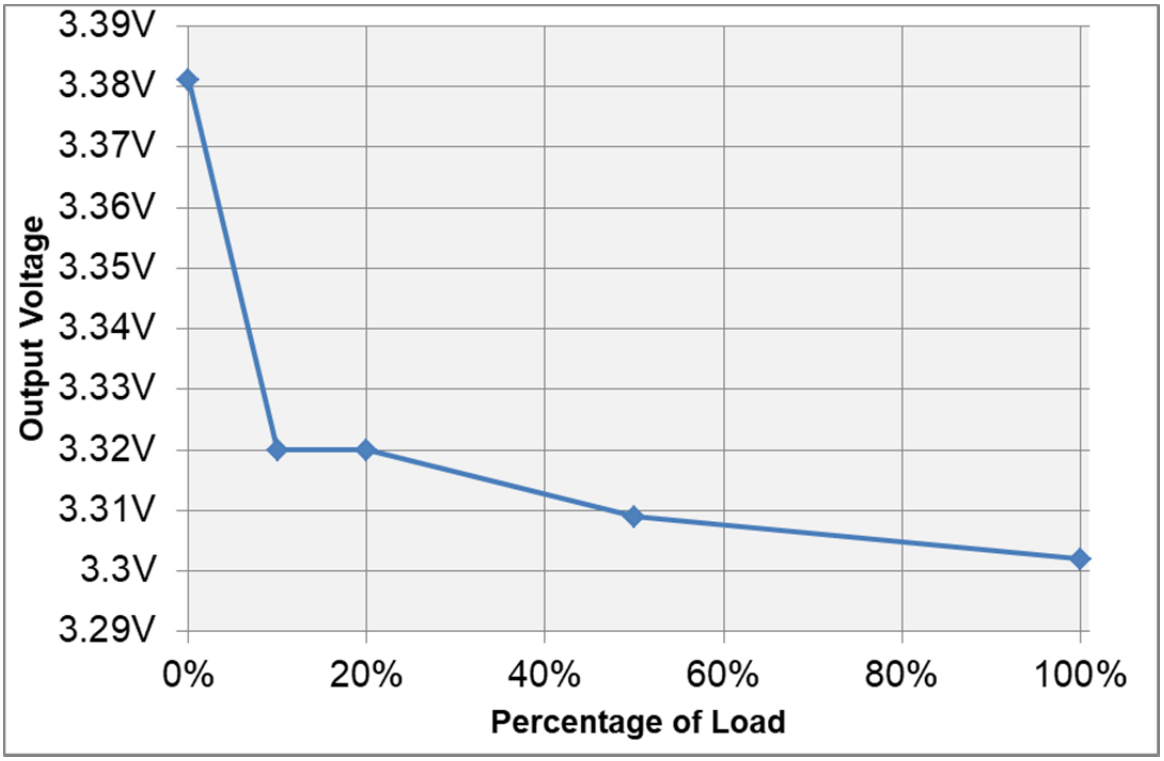


Figure 8. Output Voltage vs Load for the 3.3 V Output

2.3 Cross Regulation 10% load <>100% load

Table 1 shows the cross regulation of all outputs. "0" means 10% of load, "1" stands for 100% of load.

primary				secondary			
11V		3.3V		11V		11V	
0	11.34	0	3.35	0	11.41	0	11.40
0	11.33	0	3.35	0	11.34	1	10.71
0	11.33	0	3.35	1	10.71	0	11.33
0	11.25	0	3.35	1	10.74	1	10.74
0	12.08	1	3.17	0	12.20	0	12.19
0	11.92	1	3.20	0	11.96	1	11.27
0	11.92	1	3.20	1	11.27	0	11.95
0	11.87	1	3.22	1	11.27	1	11.25
1	11.02	0	3.40	0	11.46	0	11.44
1	11.01	0	3.40	0	11.43	1	11.00
1	11.01	0	3.40	1	11.02	0	11.42
1	11.10	0	3.40	1	11.03	1	11.01
1	11.56	1	3.28	0	12.05	0	12.02
1	11.62	1	3.29	0	11.99	1	11.53
1	11.61	1	3.29	1	11.55	0	11.95
1	11.58	1	3.30	1	11.53	1	11.51

Table 1. Cross Regulation

The feedback of the controller is shared between the two non-isolated output voltages by 50% - 50%; this cross regulation has been measured at input voltage 12V;
YELLOW is minimum output voltage, ORANGE is maximum output voltage.

2.4 Line Regulation

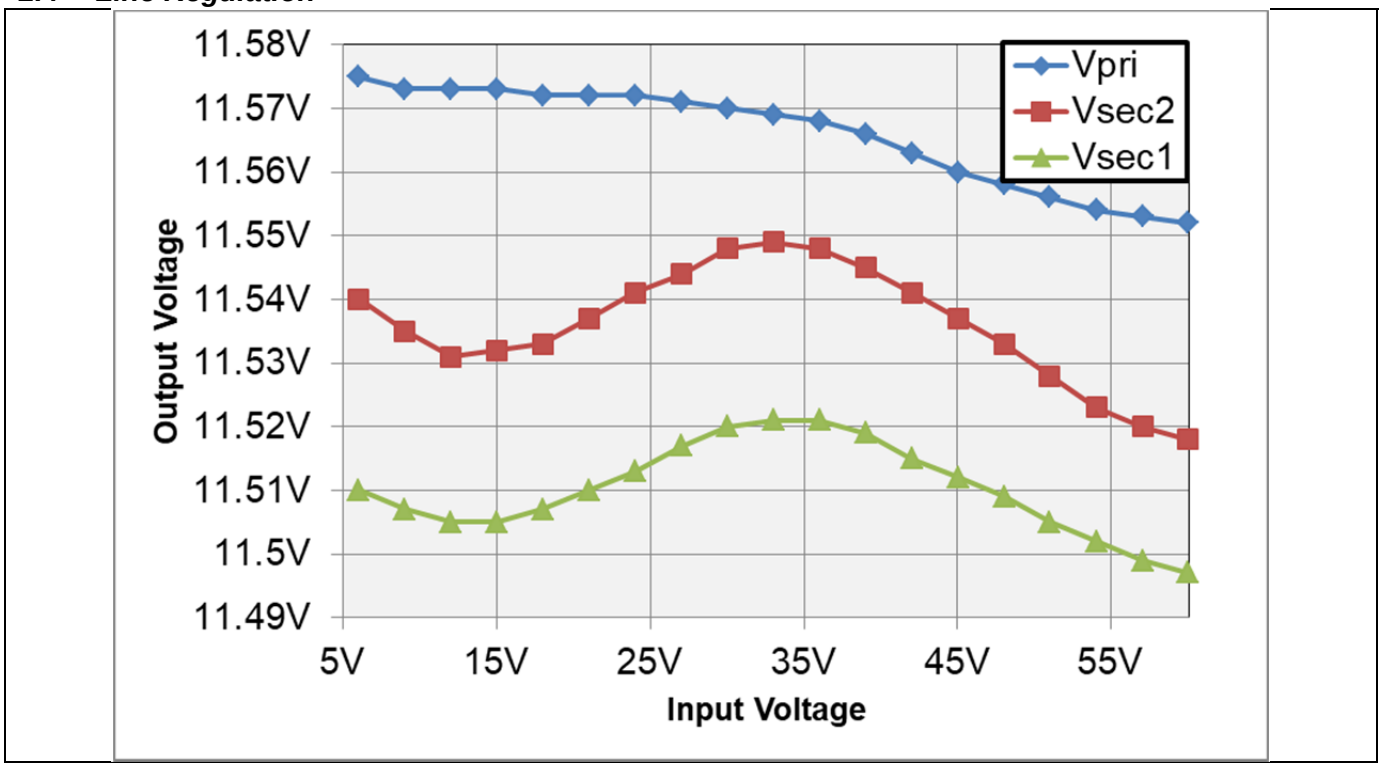


Figure 9. Output Voltage vs Input Voltage for the 11 V Outputs

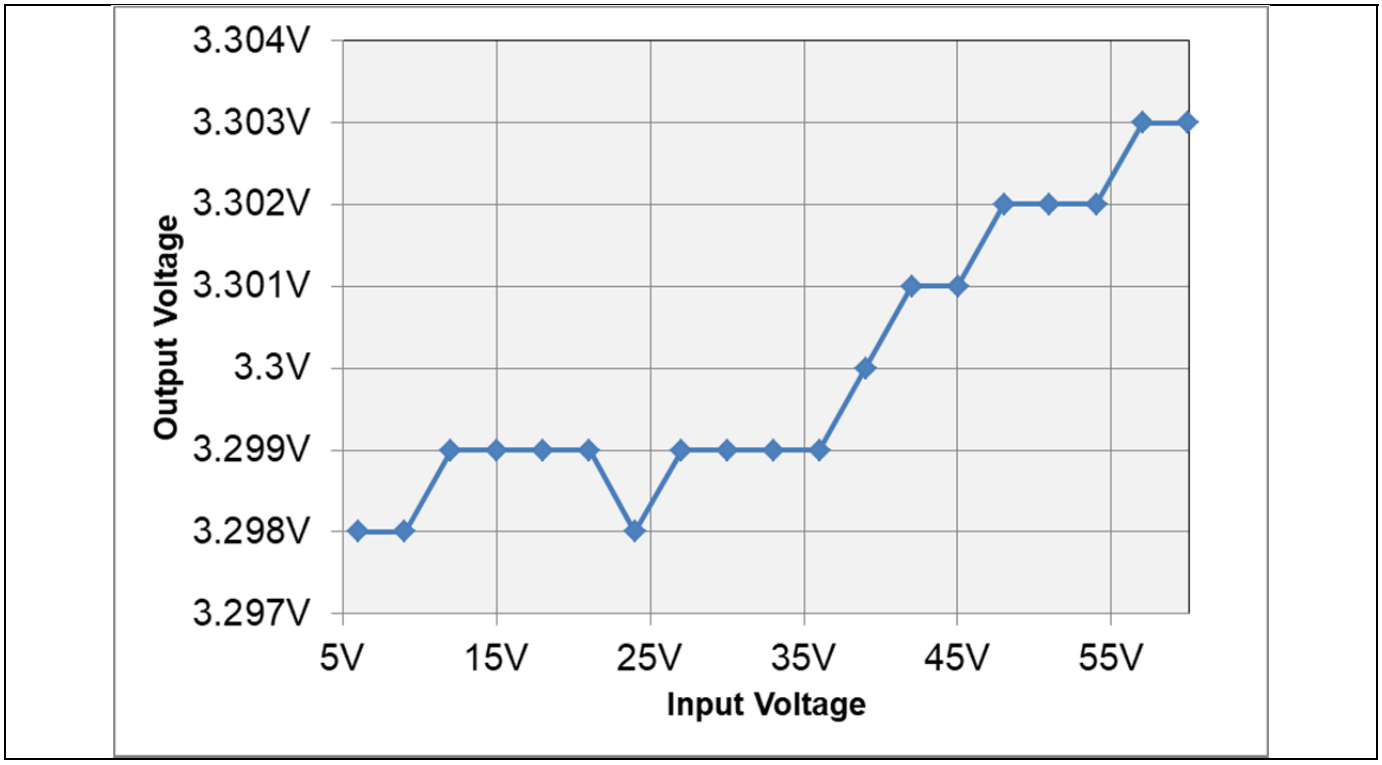


Figure 10. Output Voltage vs Input Voltage for the 3.3 V Output

With the measurement for line regulation efficiency and loss were calculated.

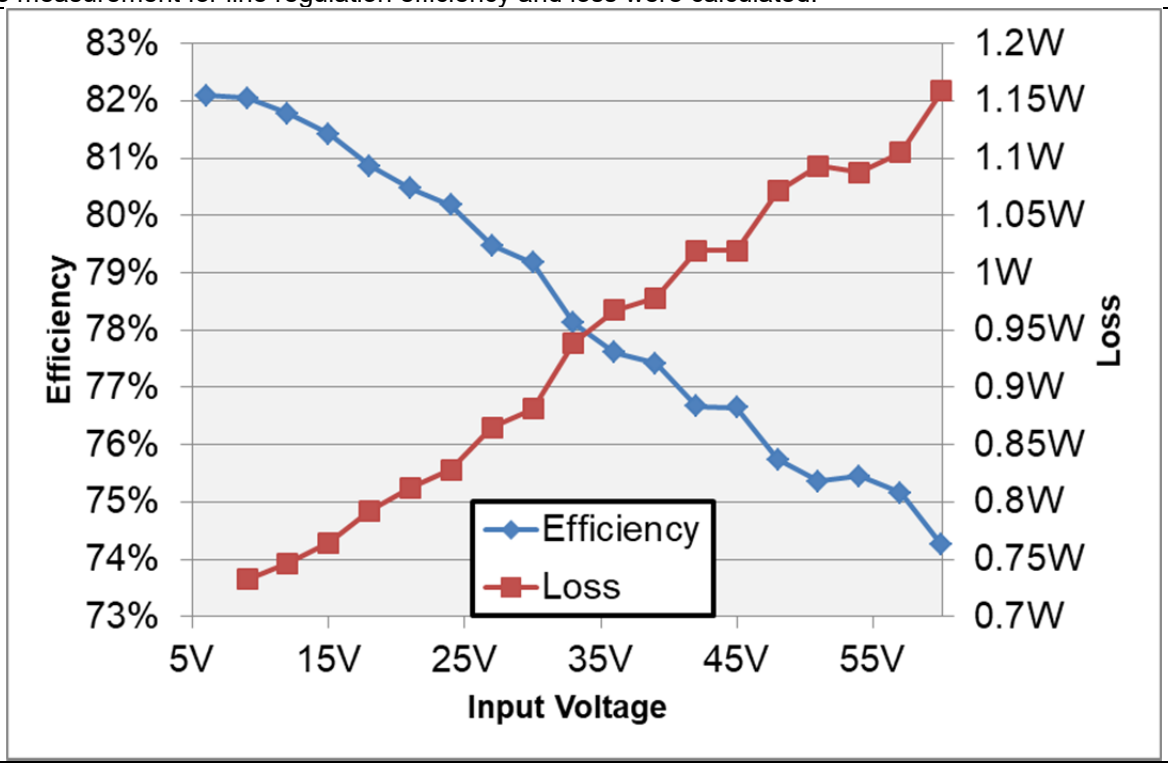


Figure 11 Input Voltage vs Efficiency and Loss

2.5 Thermal Images

Name	6 Vin	24 Vin	Temperature
D1	35.2°C	36.9°C	41.2°C
D3	35.8°C	37.6°C	41.6°C
D5	38.6°C	40.6°C	44.8°C
D8	48.9°C	50.1°C	53.8°C
Q1	37.9°C	49.8°C	49.1°C
T1	44.5°C	40.6°C	59.1°C

Table 2 Summery of Thermal Images

2.5.1 6 V Input Voltage

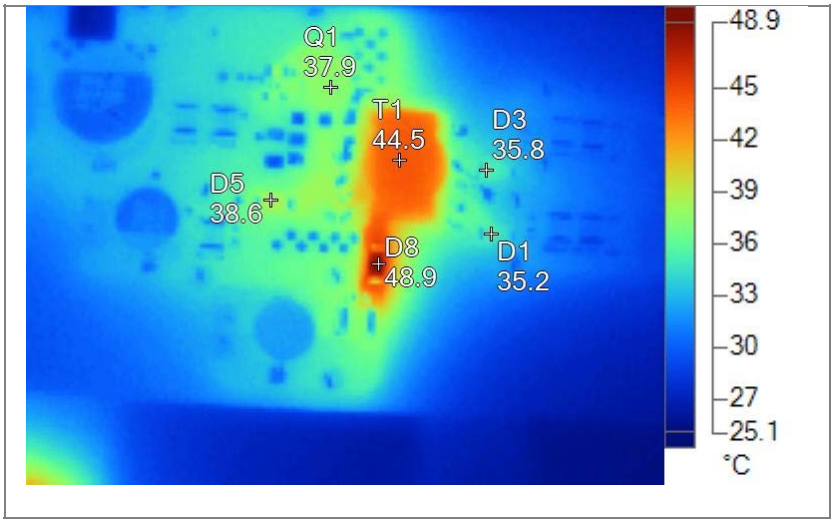


Figure 12. IR-Foto @ 6 Vin

2.5.2 24 V Input Voltage

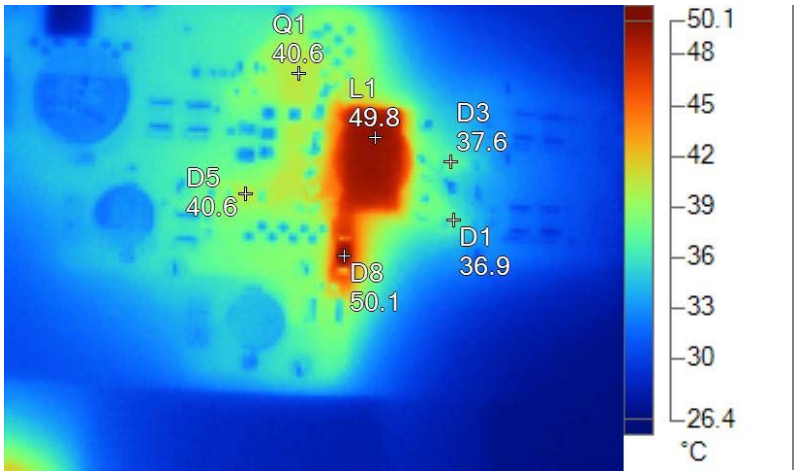


Figure 13. IR Foto @ 24 Vin

2.5.3 60 V Input Voltage

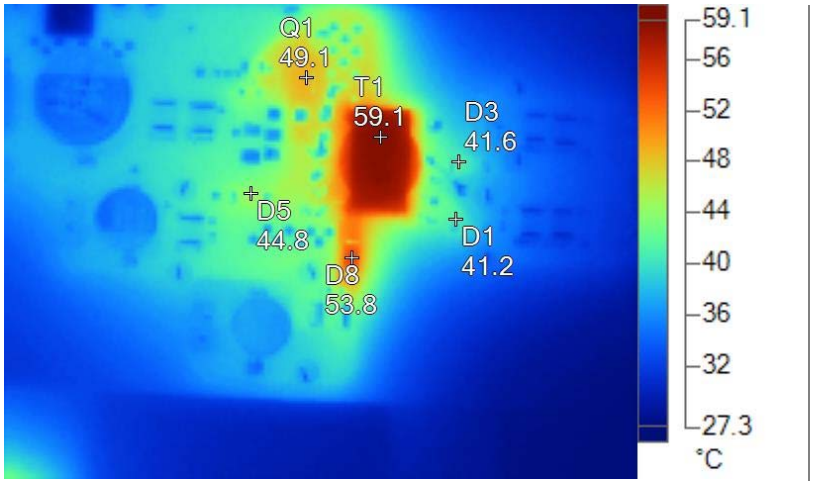


Figure 14. IR Foto @ 24 Vin

3 Waveforms at Full Load in SEPIC Configuration

3.1 Switching

3.1.1 Q1 Drain to GND

3.1.1.1 6 V Input Voltage

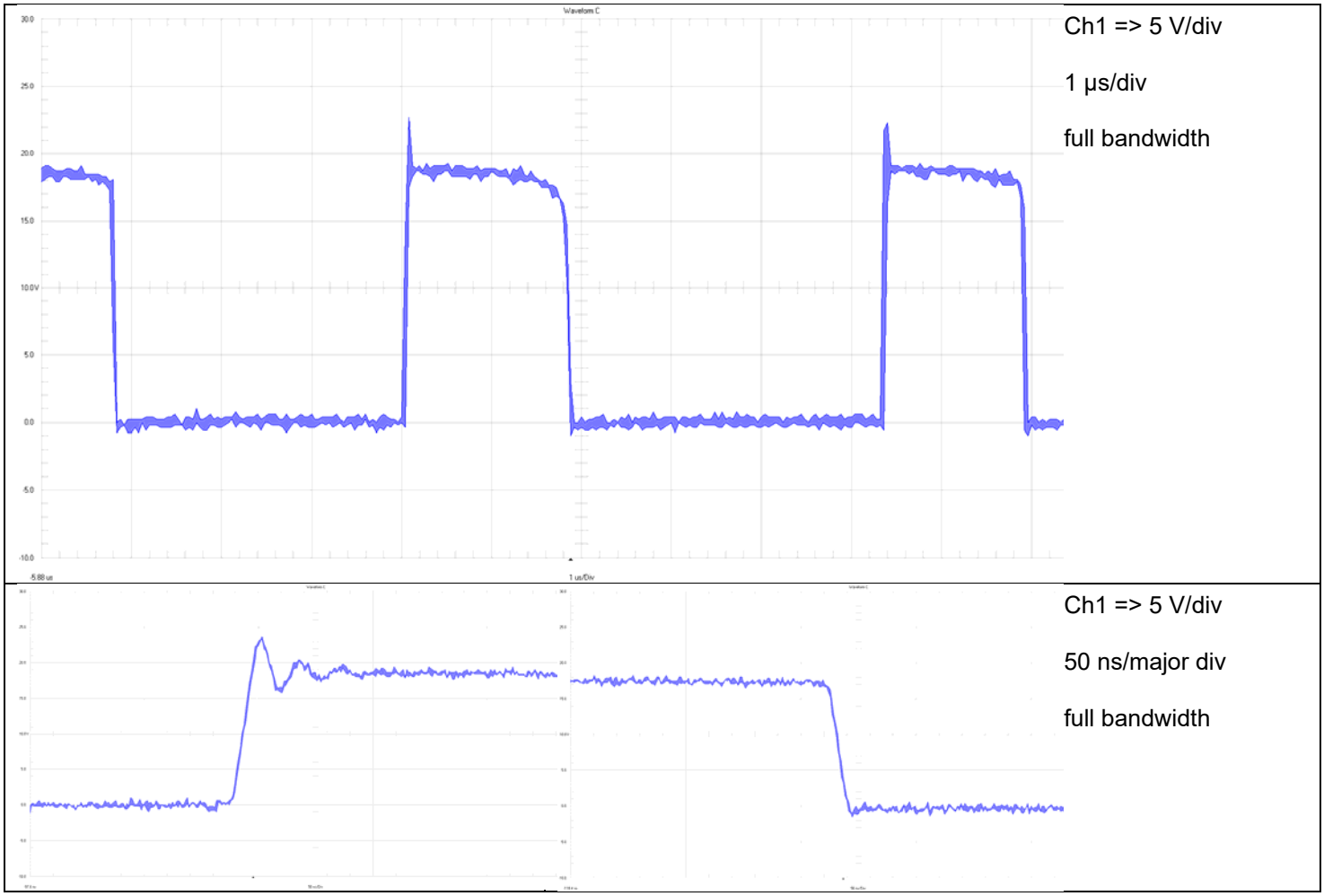


Figure 15 Switchnode to GND @ 6 Vin

3.1.1.2 24 V Input Voltage

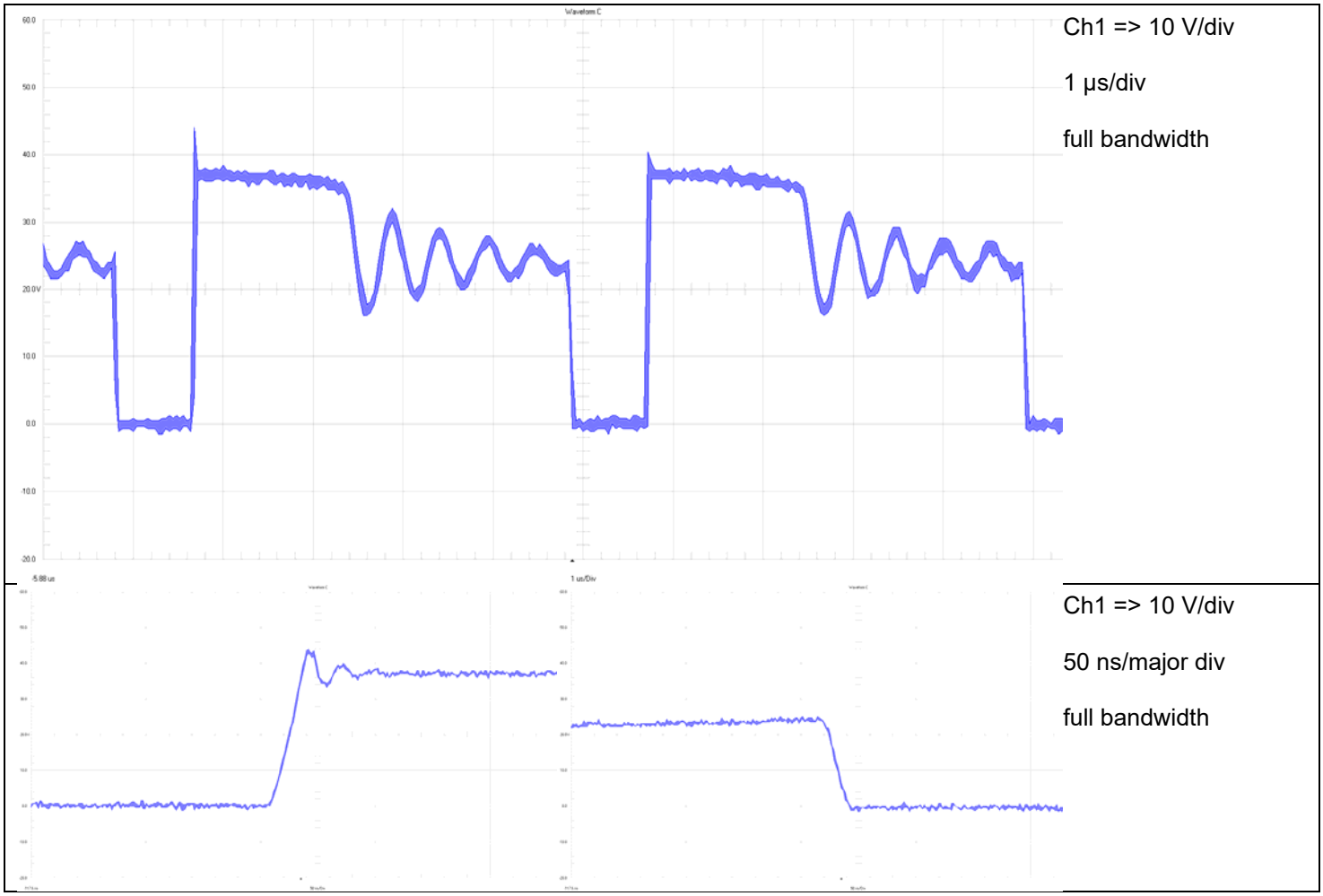


Figure 16. Switchnode to GND @ 24 Vin

3.1.1.3 60 V Input Voltage

3.1.1.3.1 SEPIC Configuration

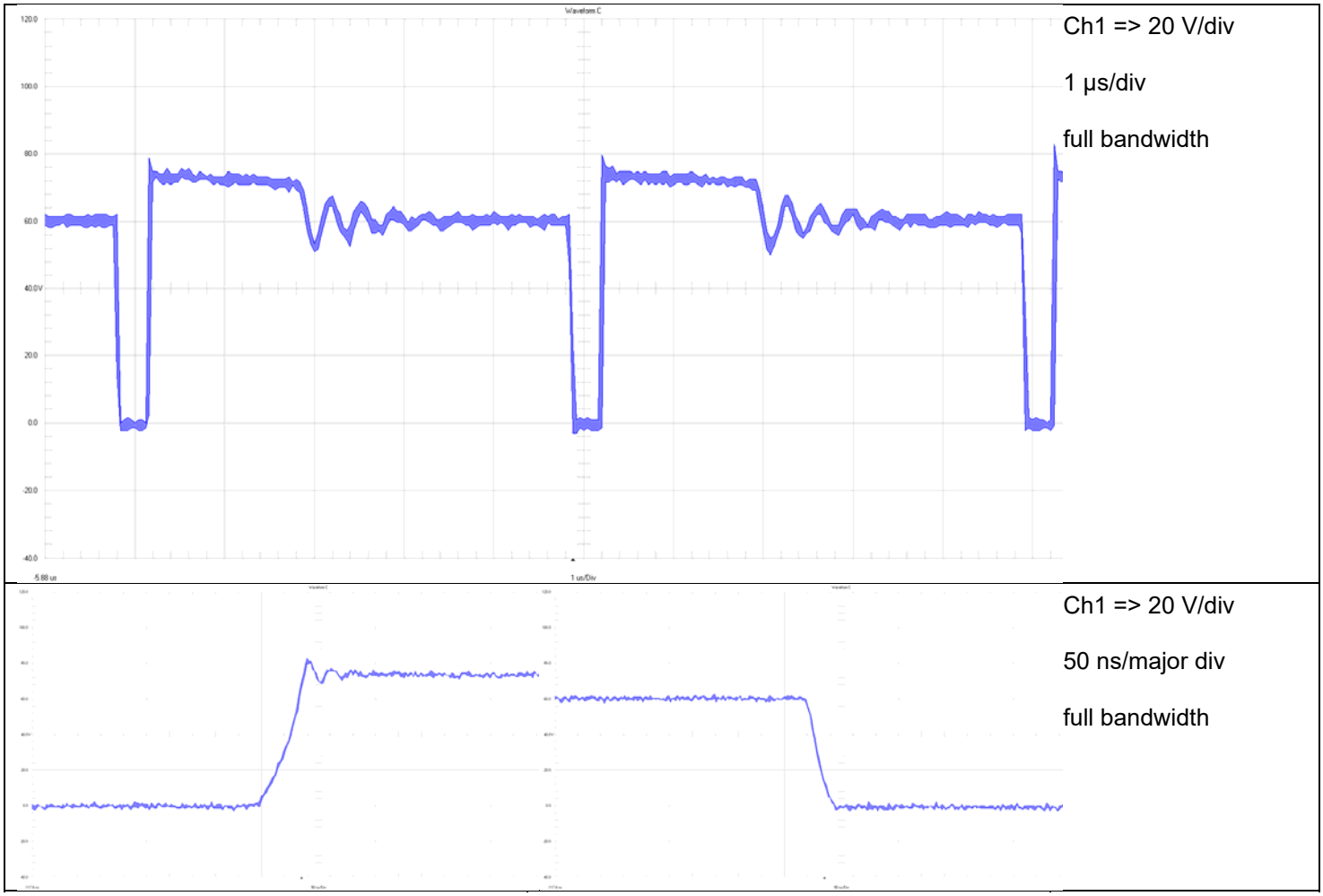


Figure 17 Switchnode to GND @ 60 Vin SEPIC

3.1.1.3.2 Flyback Configuration (to be compared w/ prior SEPIC configuration)

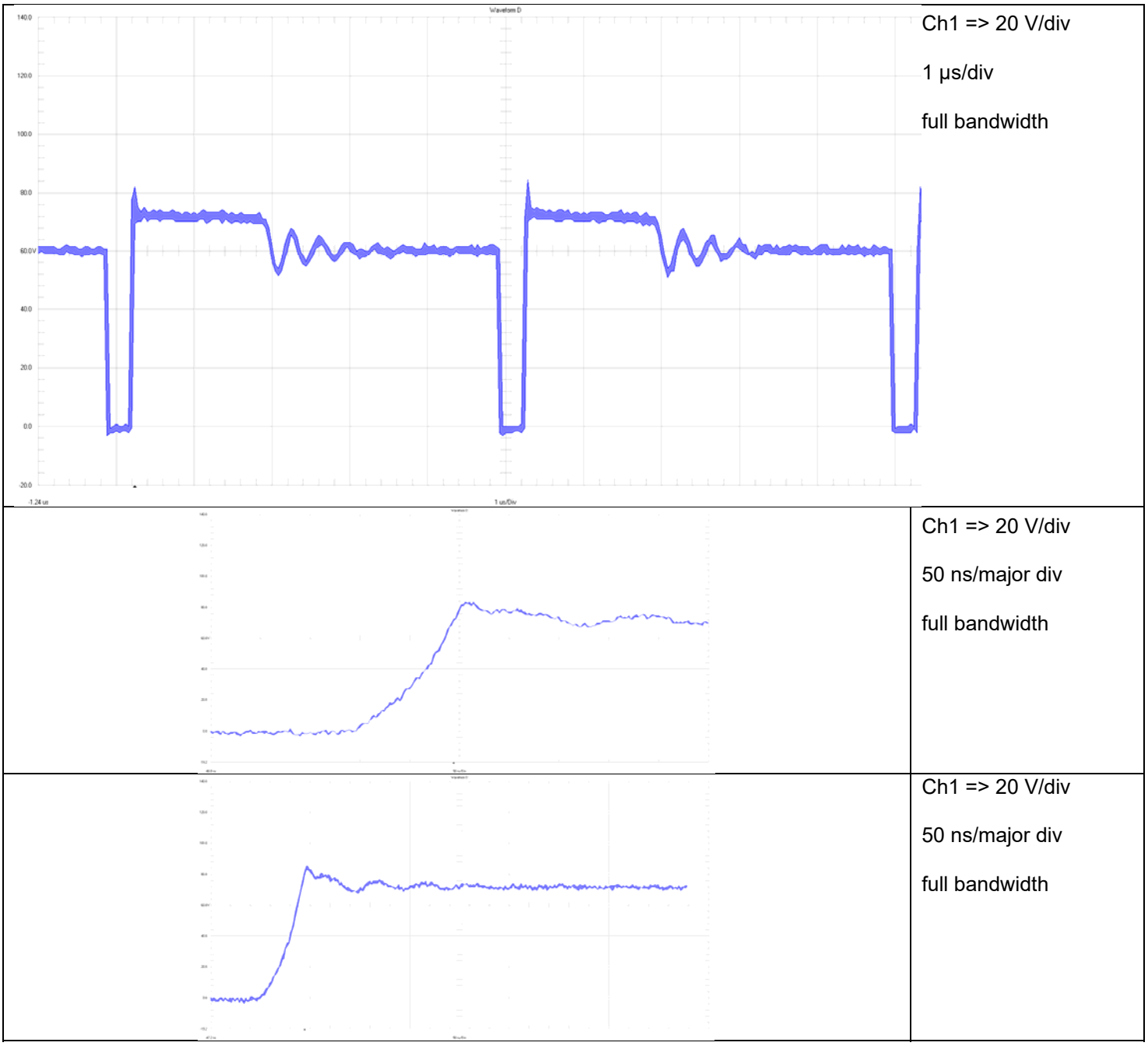


Figure 18 Switchnode to GND @ 60 Vin Flyback with R200 =10 kOhms (= hard clamping of Vds, but lossy)

3.1.2 Q1 Gate to GND

3.1.2.1 6 V Input Voltage

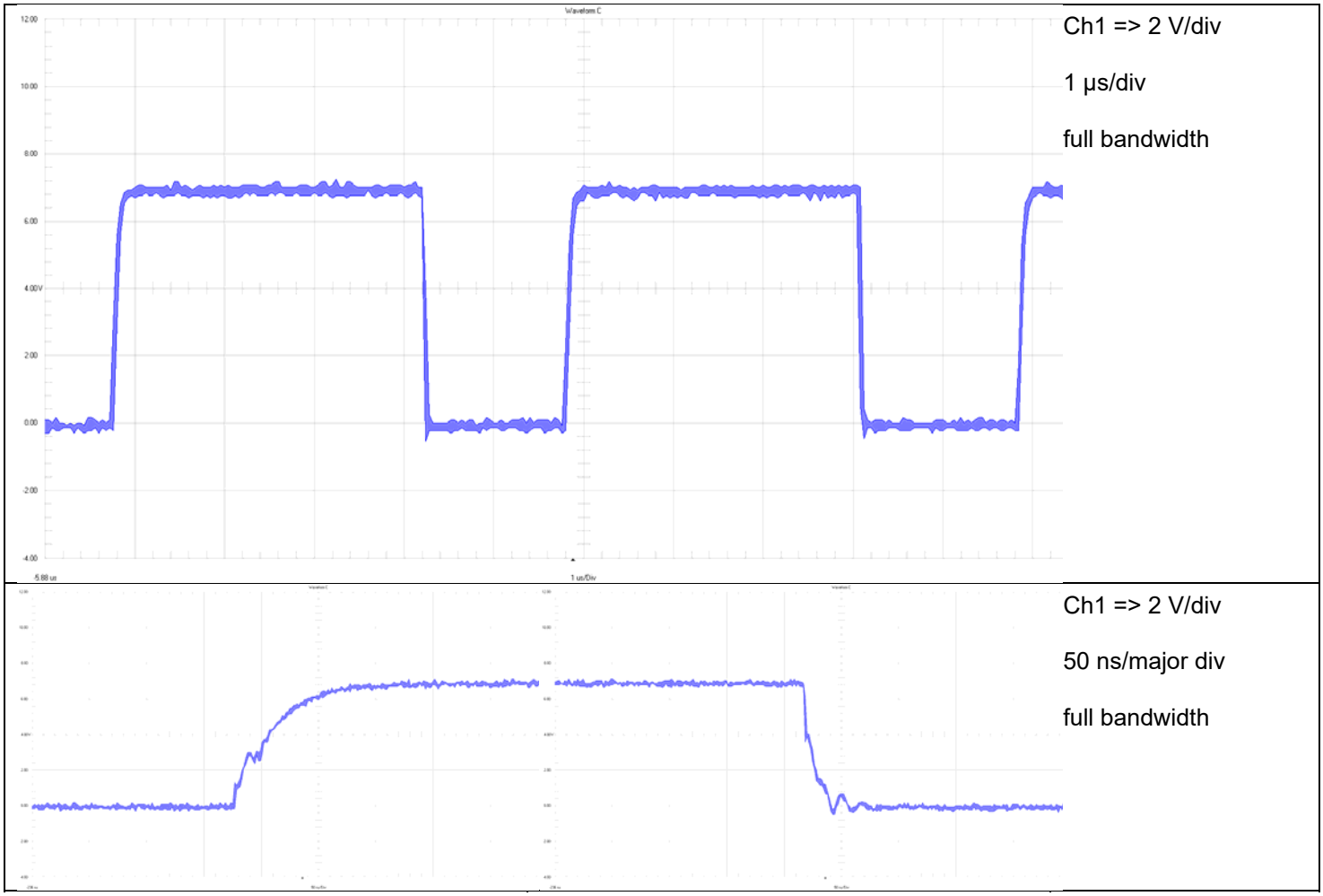


Figure 19 Gate to GND @ 6 Vin

3.1.2.2 24 V Input Voltage

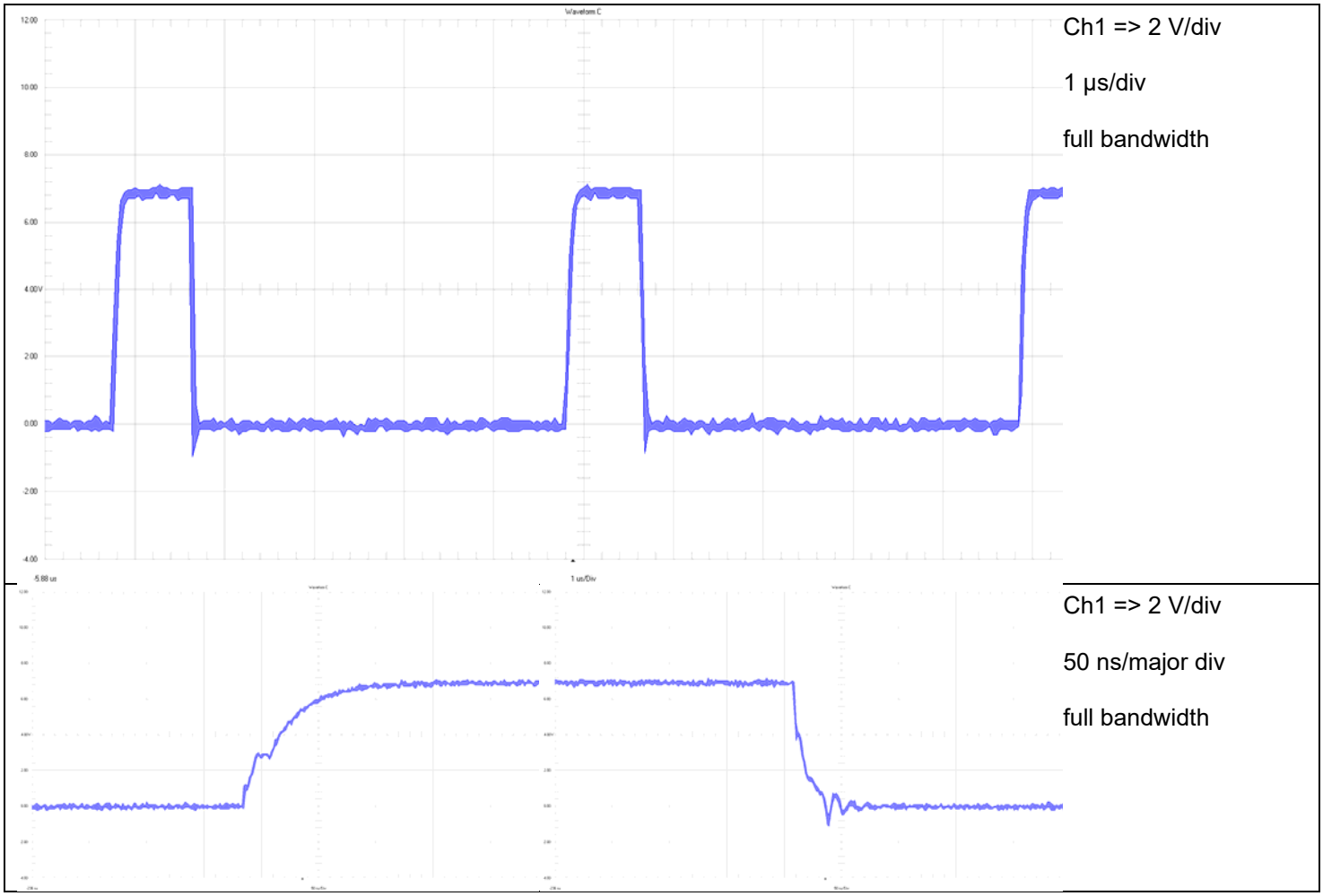


Figure 20. Gate to GND @ 24 Vin

3.1.2.3 60 V Input Voltage

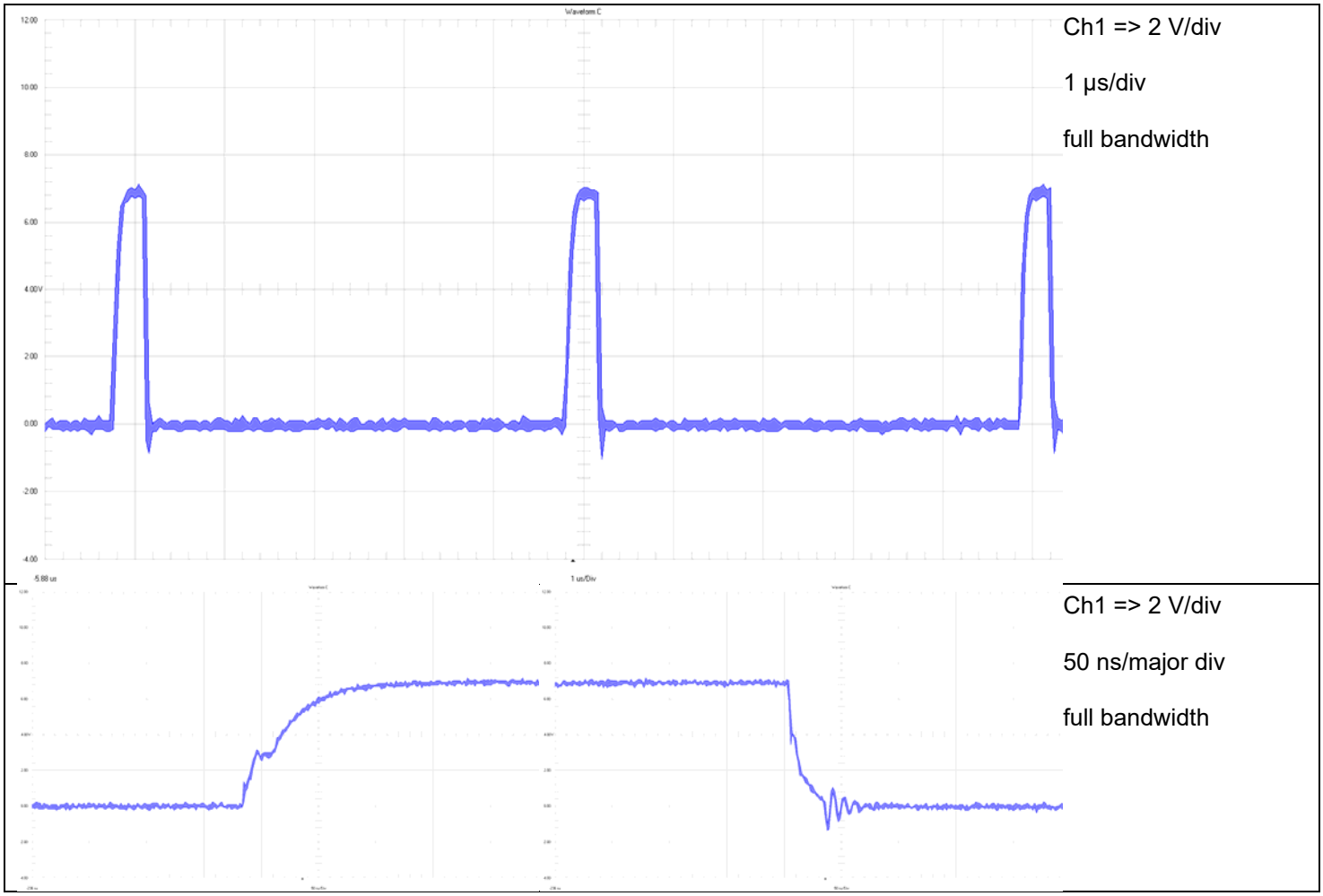


Figure 21. Gate to GND @ 60 Vin

3.2 Output Voltage Ripple

3.2.1 3.3 V Output Voltage (Non-Isolated)

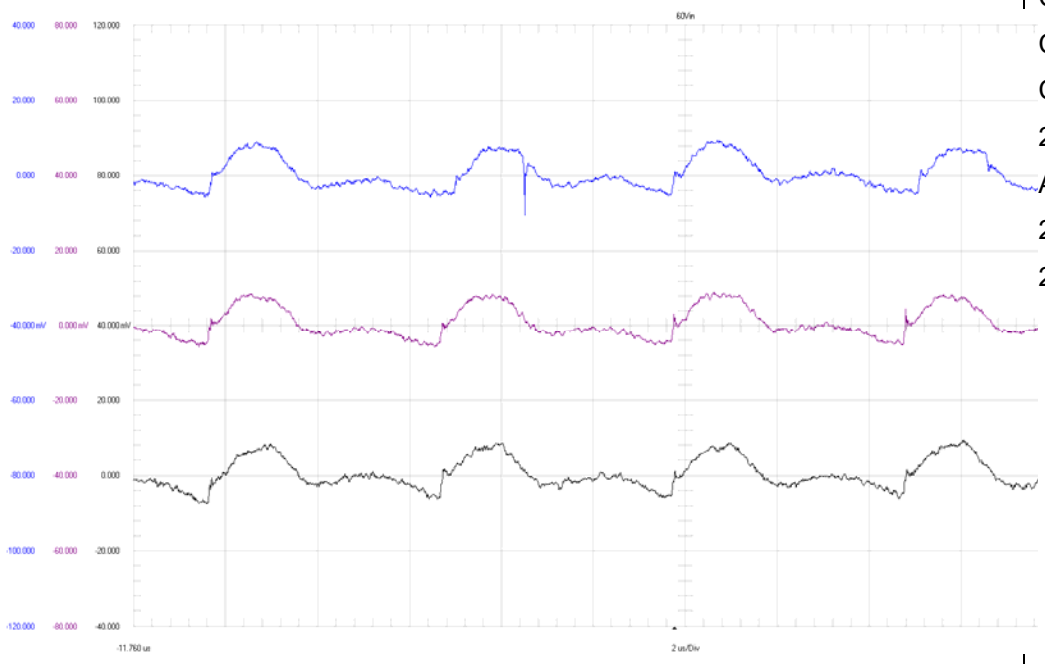


Figure 22. 3.3 V Output Voltage

3.2.2 11 V Output Voltage (Non-Isolated)

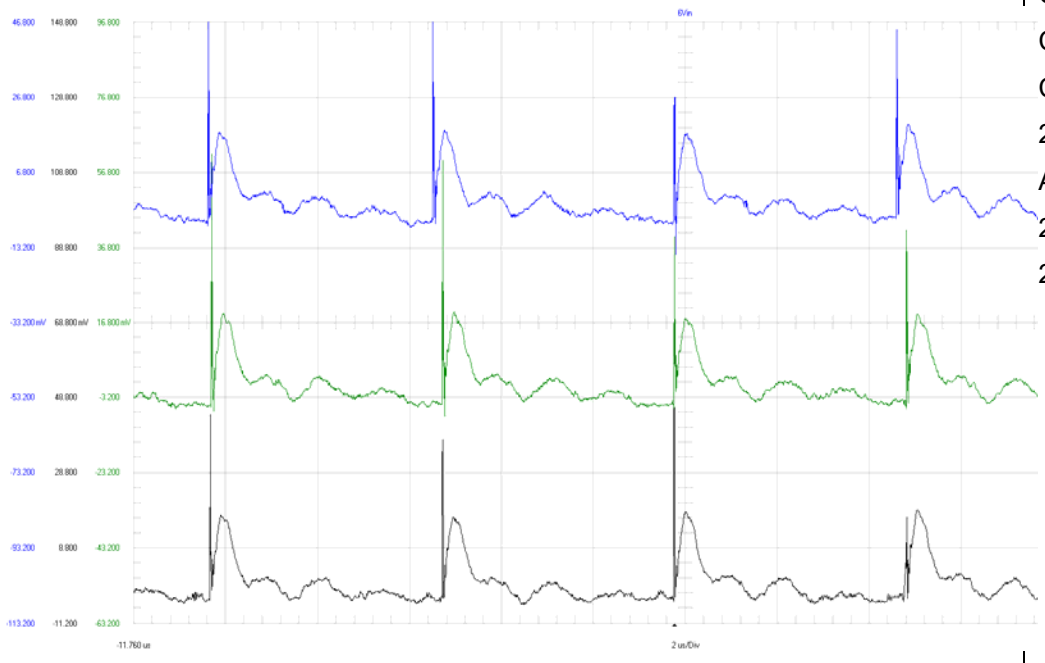


Figure 23. 11 V Output Voltage (Non-isolated)

3.2.3 11 V Output Voltage (Isolated VO1)

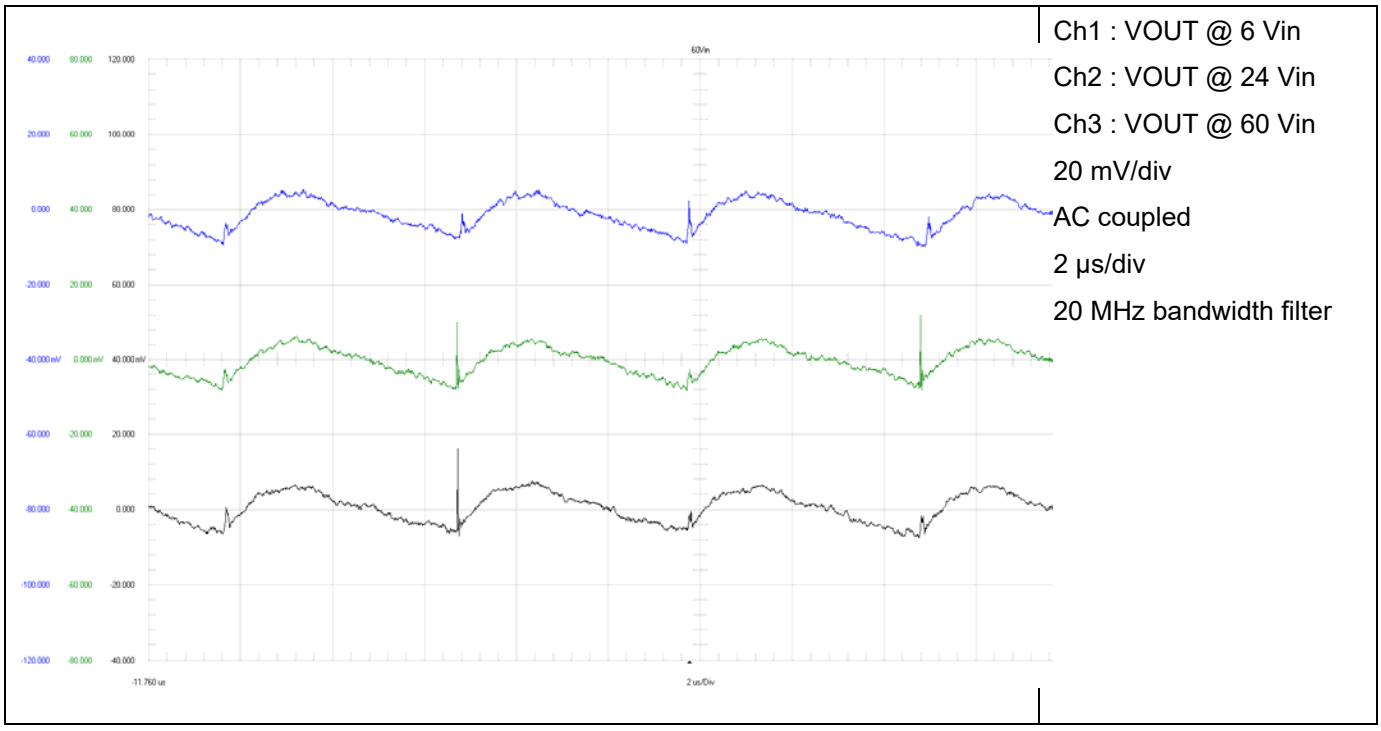


Figure 24. 11 V Output Voltage (Isolated Vo1)

3.2.4 11 V Output Voltage (Isolated VO2)

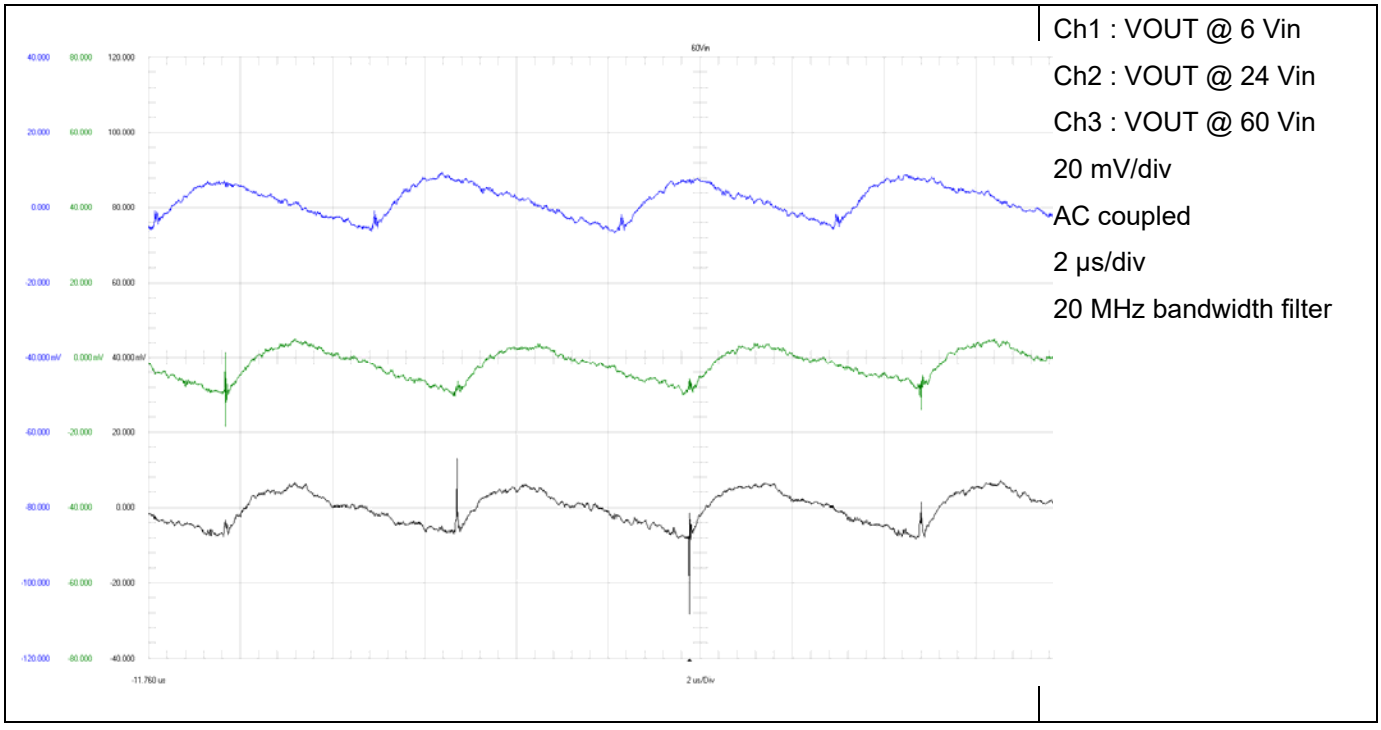
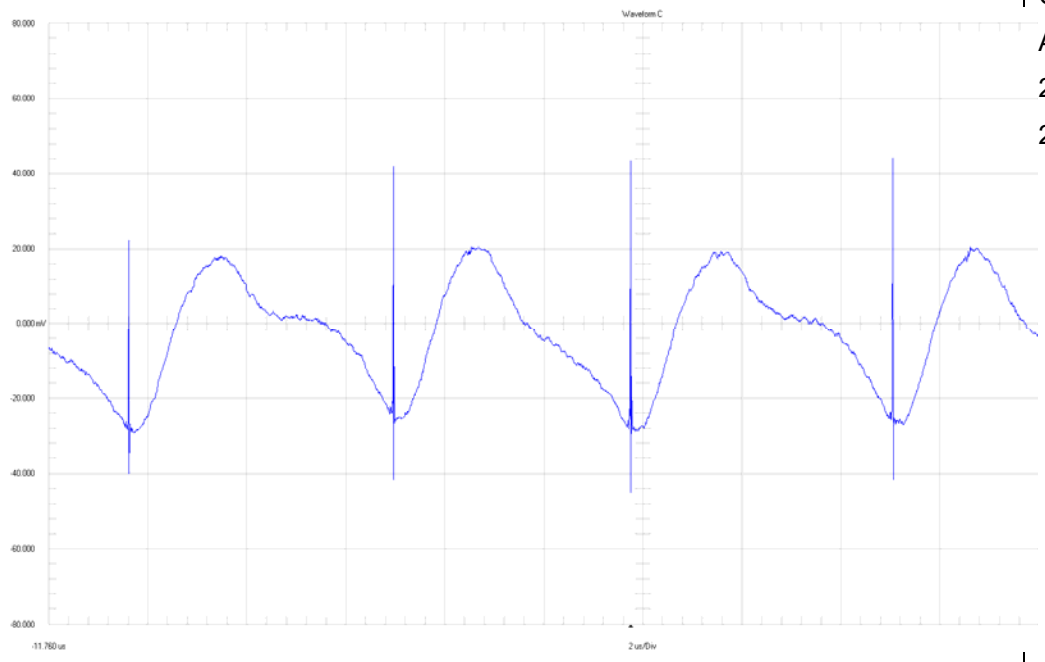


Figure 25. 11 V Output Voltage (Isolated Vo2)

3.3 Input Voltage Ripple

3.3.1 6 V Input Voltage



Ch1 => 20 mV/div

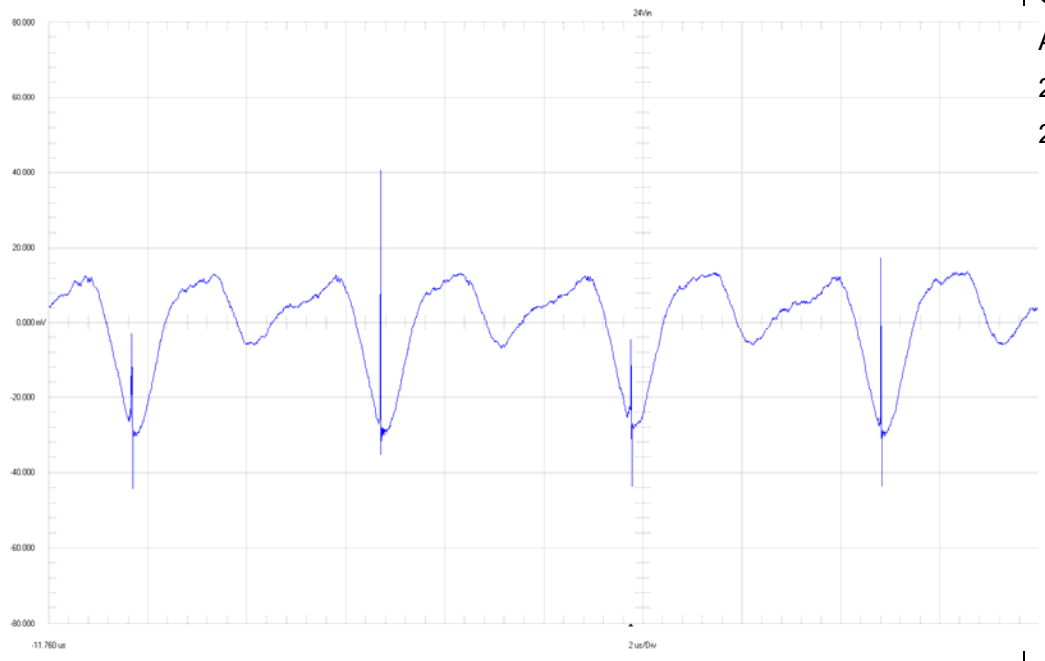
AC coupled

2 µs/div

20 MHz bandwidth filter

Figure 26. Input Voltage Ripple 6 V

3.3.2 24 V Input Voltage



Ch1 => 20 mV/div

AC coupled

2 µs/div

20 MHz bandwidth filter

Figure 27. Input Voltage Ripple 24 V

3.3.3 60 V Input Voltage

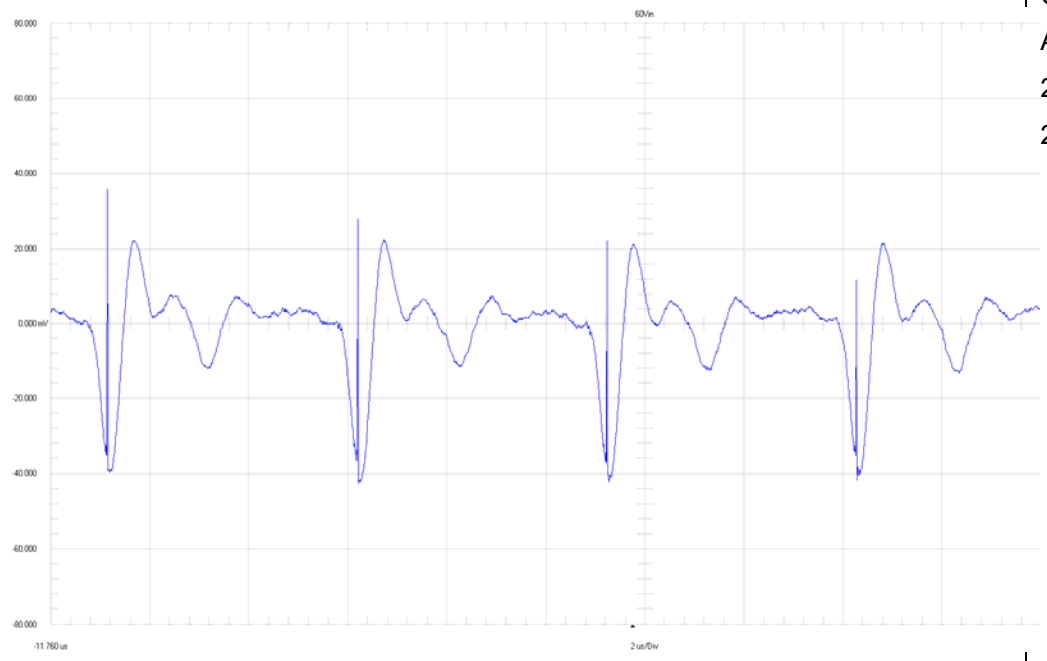


Figure 28. Input Voltage Ripple 60 V

3.4 Bode Plot

3.4.1 Flyback Configuration, 100% feedback 11Vpri

	6 V	24 V	60 V
Bandwidth (kHz)	2.86	2.86	3.18
Phasemargin	80°	79°	80°
slope (20dB/decade)	-1.1	-1.1	-1.1
gain margin (dB)	-24	-34	-36
slope (20dB/decade)	-1.8	0	-0.66
freq (kHz)	78.3	93	101

Table 3. Bodeplots (Flyback)

3.4.1.1 6 V Input Voltage

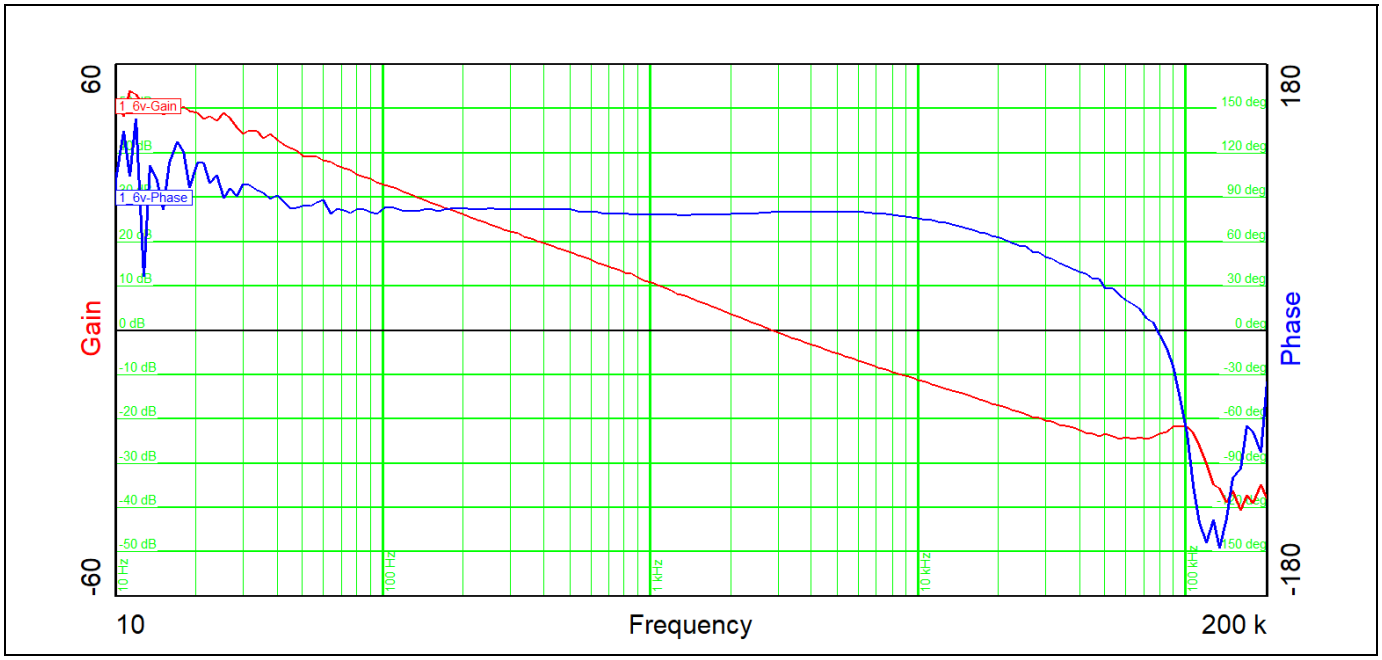


Figure 29. Bode Plot 6 Vin (Flyback 11V FB)

3.4.1.2 24 V Input Voltage

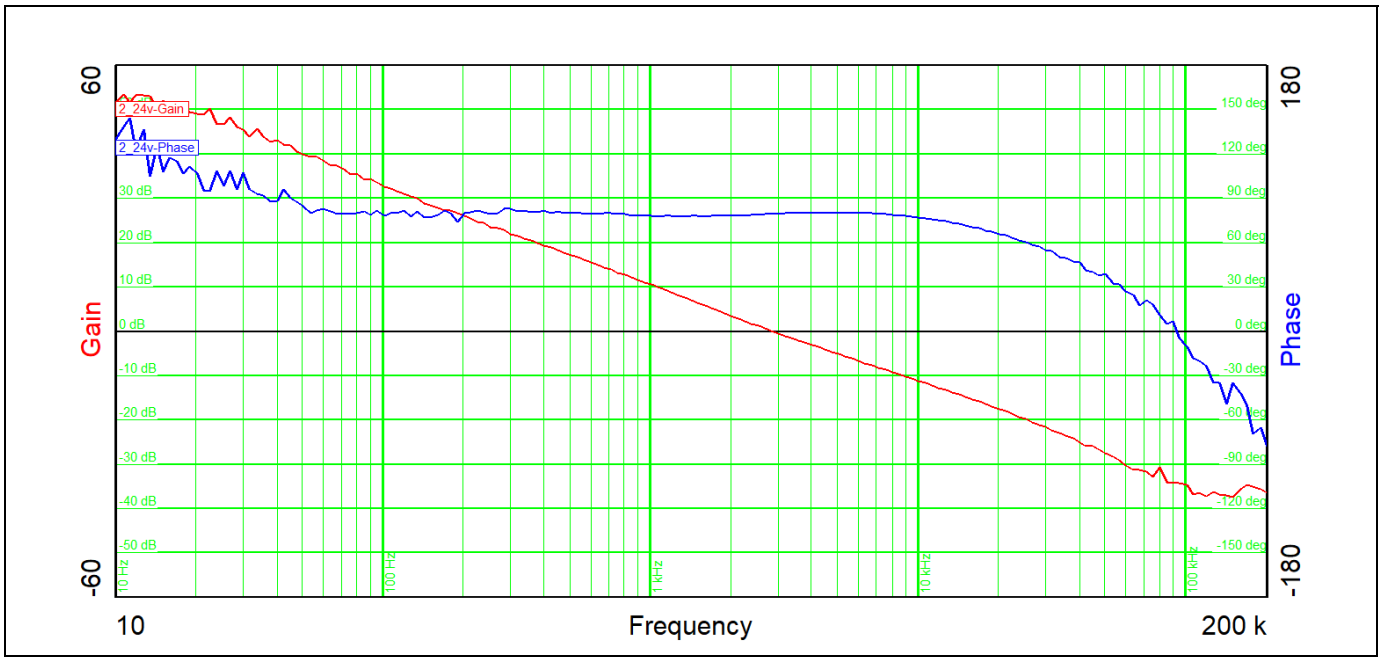


Figure 30. Bode Plot 24 Vin (Flyback 11V FB)

3.4.1.3 60 V Input Voltage

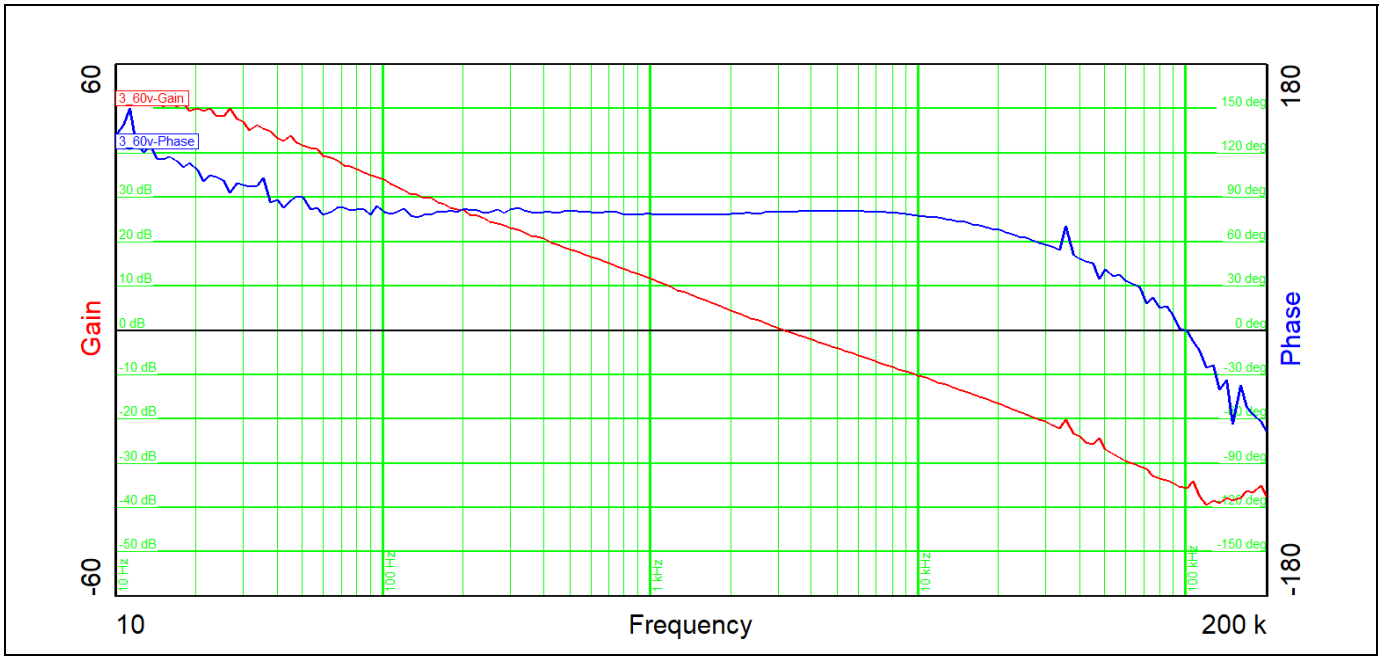


Figure 31. Bode Plot 60 Vin (Flyback 11V FB)

3.4.2 SEPIC Configuration, 100% feedback 11Vpri

	6 V	24 V	60 V
Bandwidth (kHz)	2.67	2.84	3.18
Phasemargin	79°	79°	80°
slope (20dB/decade)	-1.2	-1.1	-1.1
gain margin (dB)	-25	-35	-37
slope (20dB/decade)	-1.1	+1.4	+3
freq (kHz)	77	93	110

Table 4. Bodeplots SEPIC

3.4.2.1 6 V Input Voltage

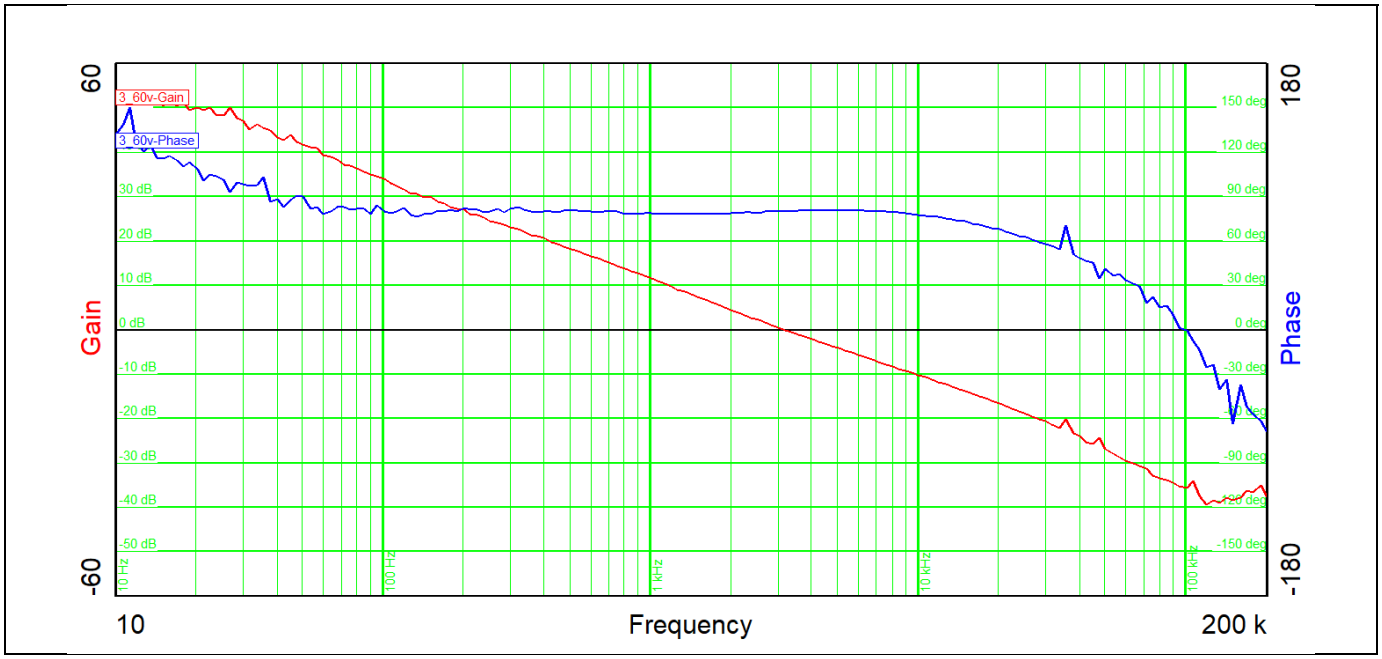


Figure 32. Bode Plot 6 Vin (SEPIC 11V FB)

3.4.2.2 24 V Input Voltage

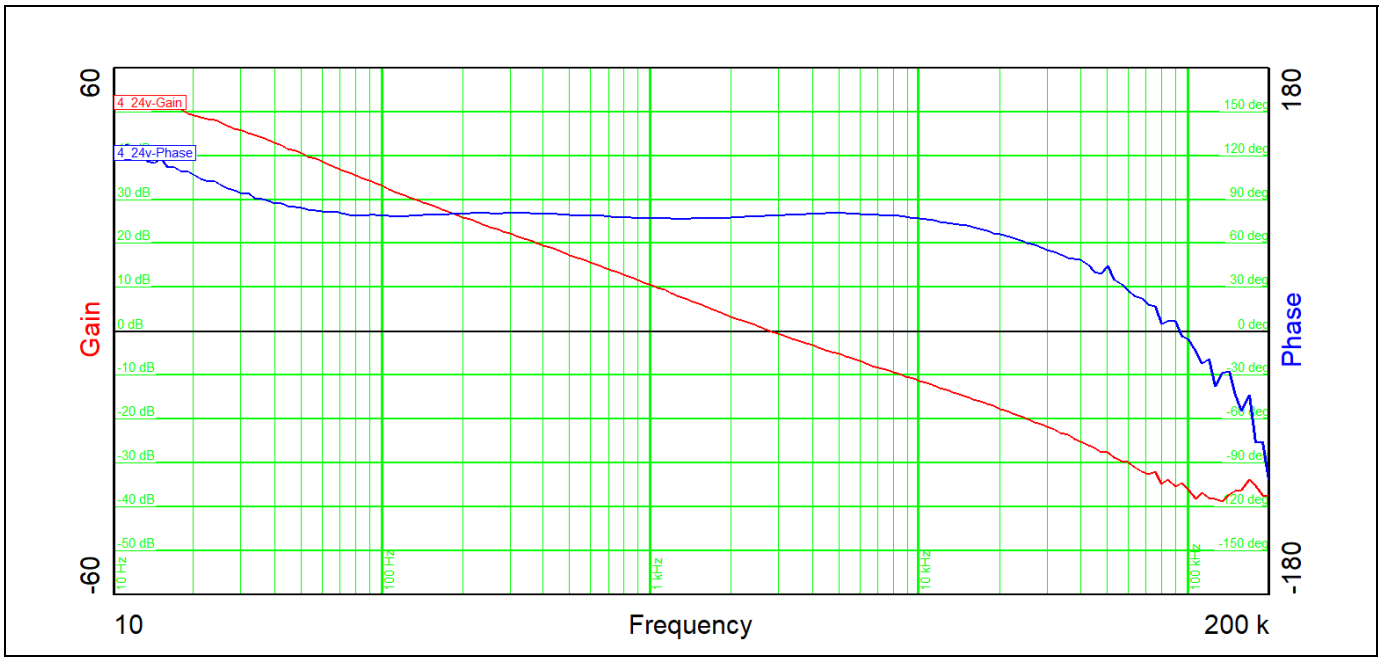


Figure 33. Bode Plot 24 Vin (SEPIC 11V FB)

3.4.2.3 60 V Input Voltage

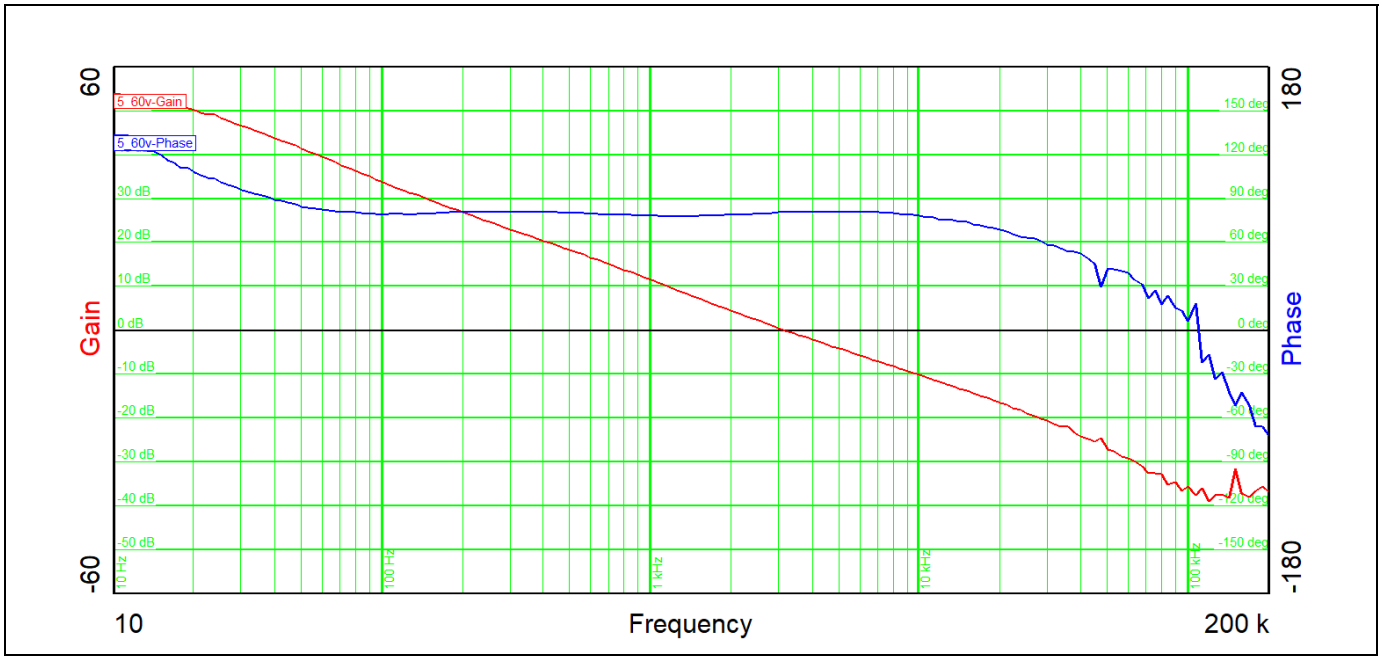


Figure 34. Bode Plot 60 Vin (SEPIC 11V FB)

3.4.3 SEPIC Configuration, 100% feedback 3V3 pri

	12 V	24 V	60 V
Bandwidth (kHz)	6.29	7.06	8.3
Phasemargin	81°	81°	810°
slope (20dB/decade)	-1.1	-1.0	-1.0
gain margin (dB)	-22	-25	-26
slope (20dB/decade)	-1.0	-1.0	-1.3
freq (kHz)	62	77	93

Table 5 Bodeplots SEPIC

3.4.3.1 12 V Input Voltage

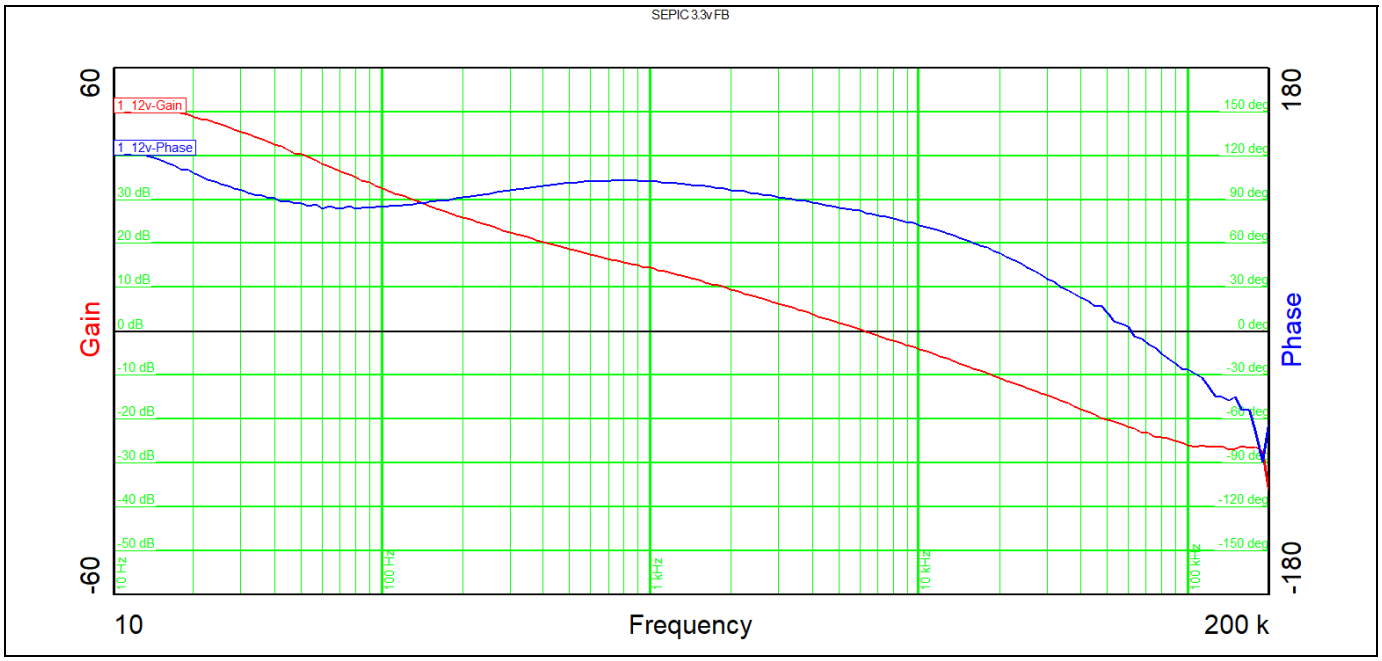


Figure 35. Bode Plot 12 Vin (SEPIC 3.3V FB)

3.4.3.2 24 V Input Voltage

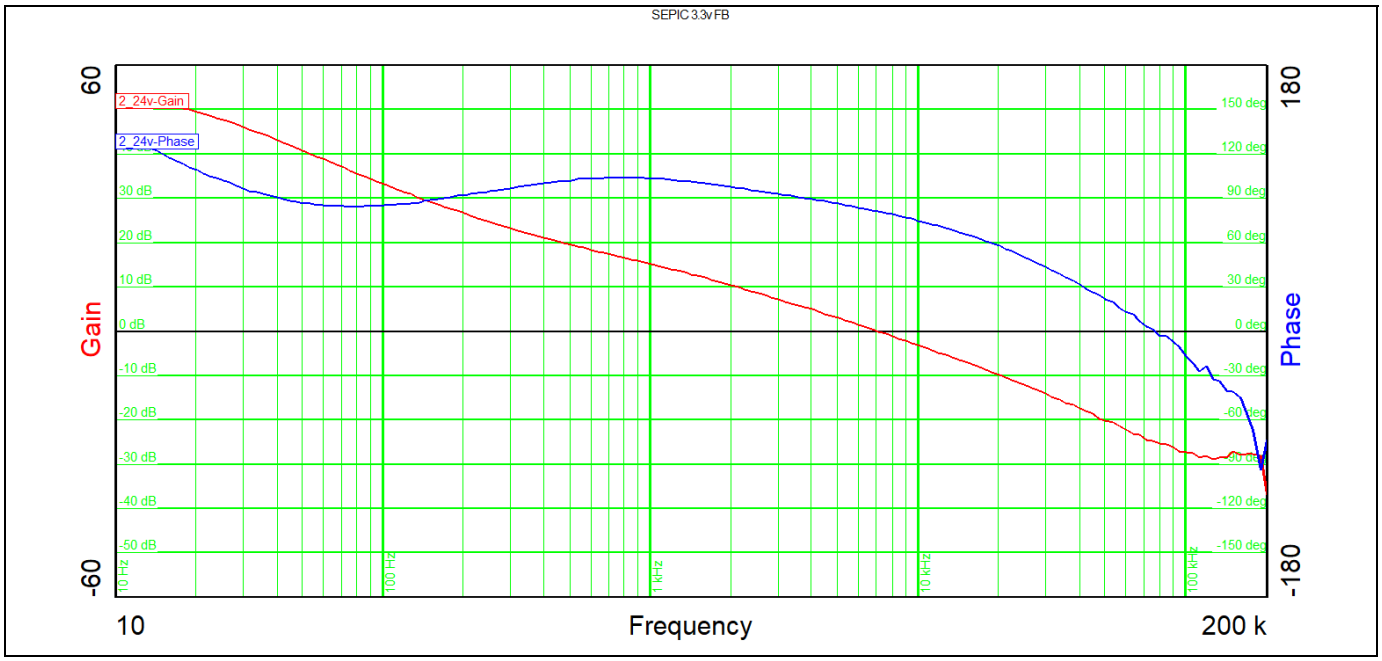


Figure 36. Bode Plot 24 Vin (SEPIC 3.3V FB)

3.4.3.3 60 V Input Voltage

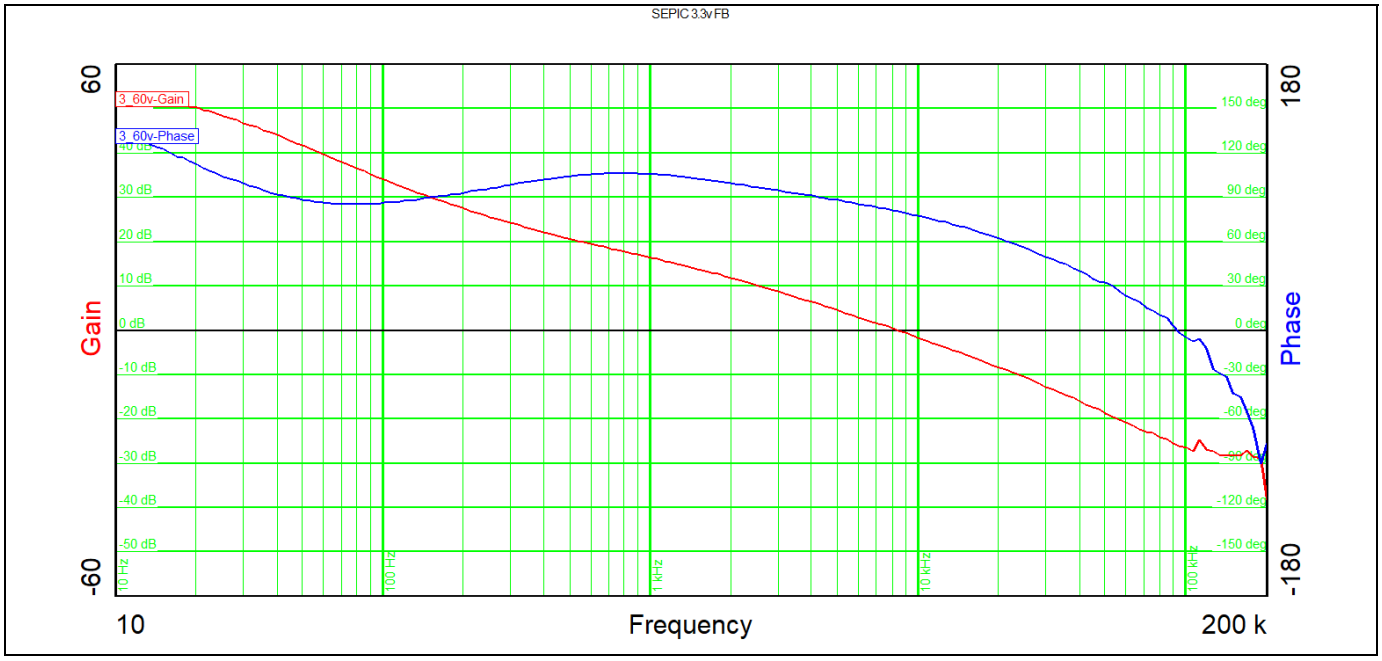


Figure 37. Bode Plot 60 Vin (SEPIC 3.3V FB)

3.5 Start-up Sequence

To get all waveforms in one figure the measurement were done twice with different output connected on one channel (11Vsec).

3.5.1 7.5 V Input Voltage

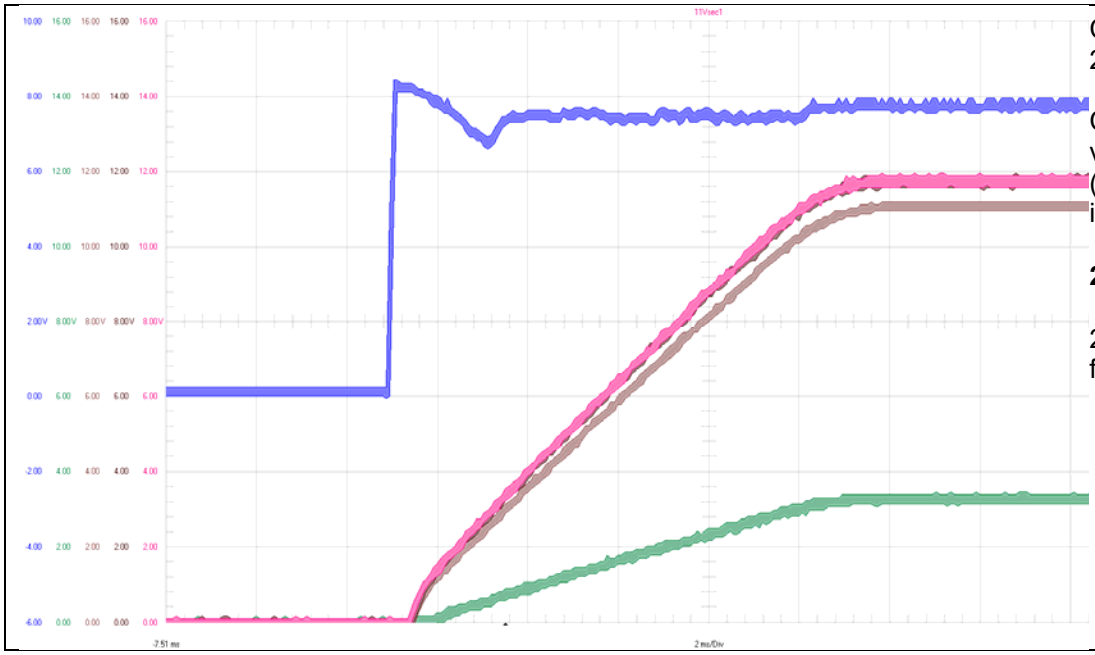


Figure 38. Start-up 7.5 V

3.5.2 24 V Input Voltage

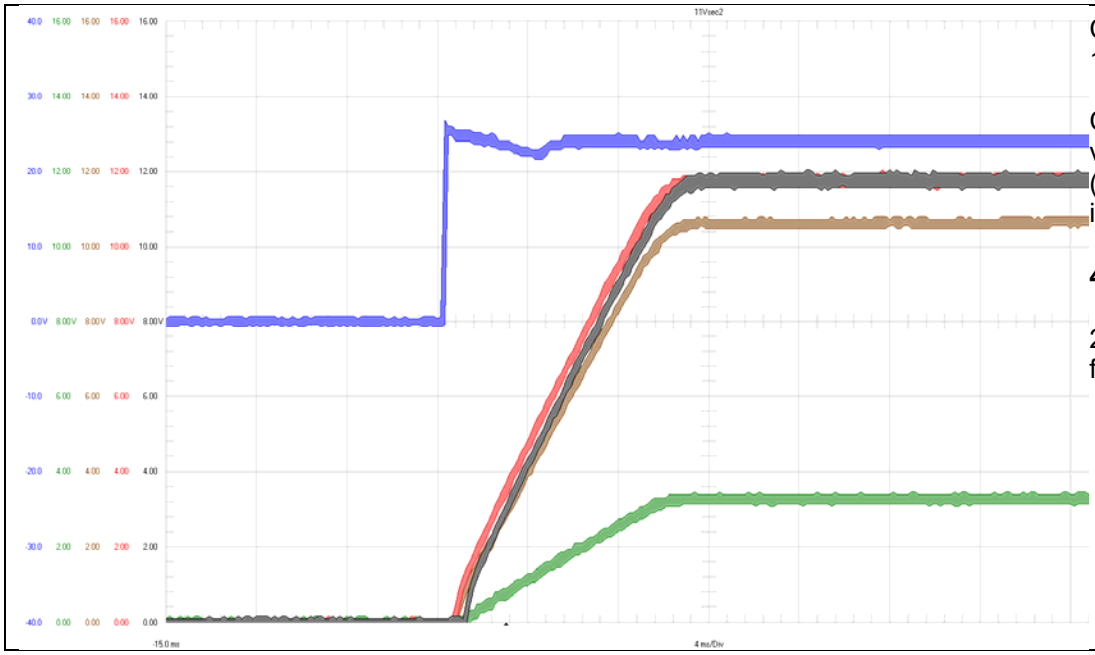


Figure 39. Start-up 24 V

3.5.3 60 V Input Voltage

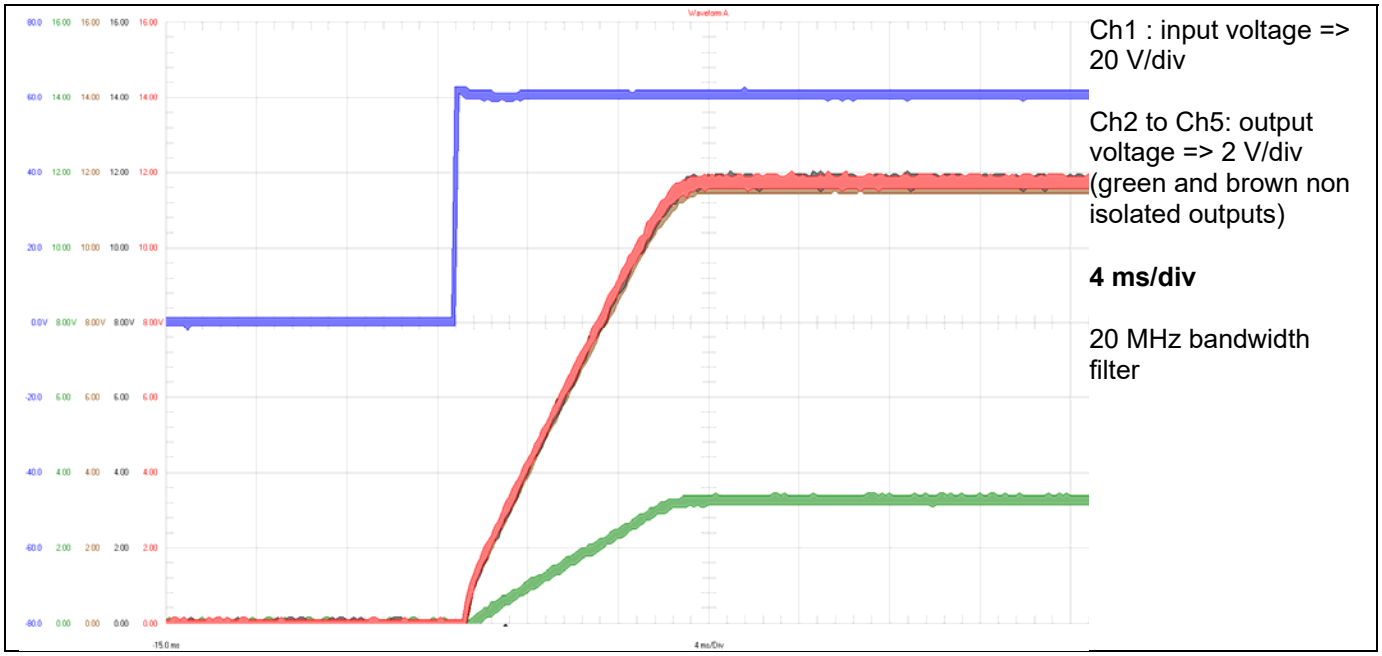
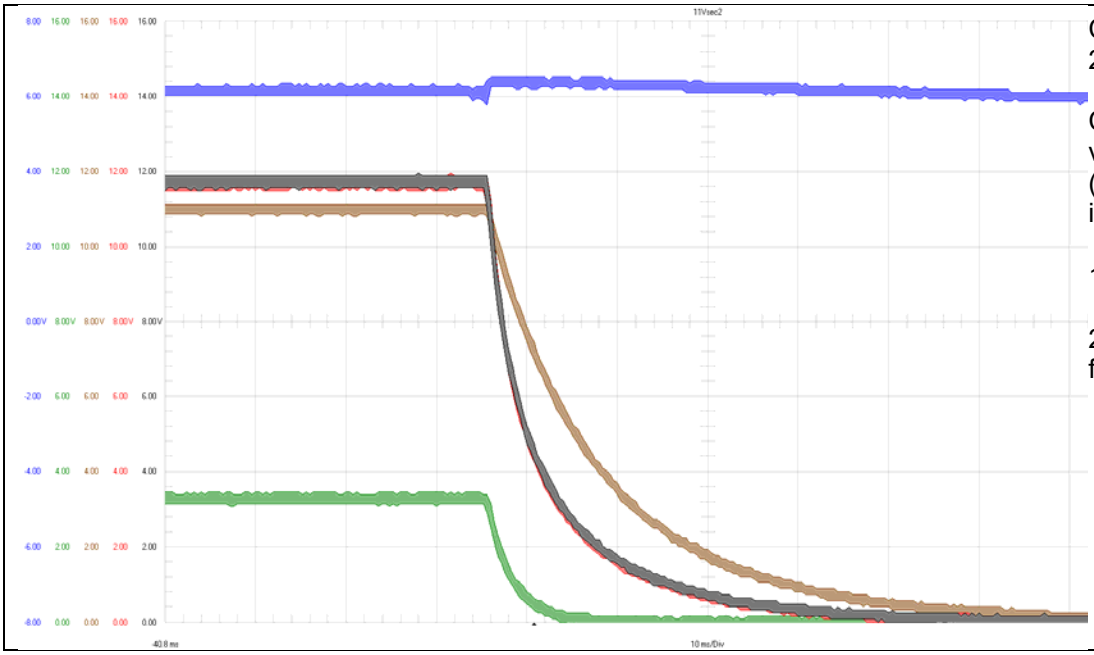


Figure 40. Start-up 60 V

3.6 Shutdown Sequence

To get all waveforms in one figure the measurement were done twice with different output connected on one channel (11 Vsec).

3.6.1 6 V Input Voltage



Ch1 : input voltage => 2 V/div

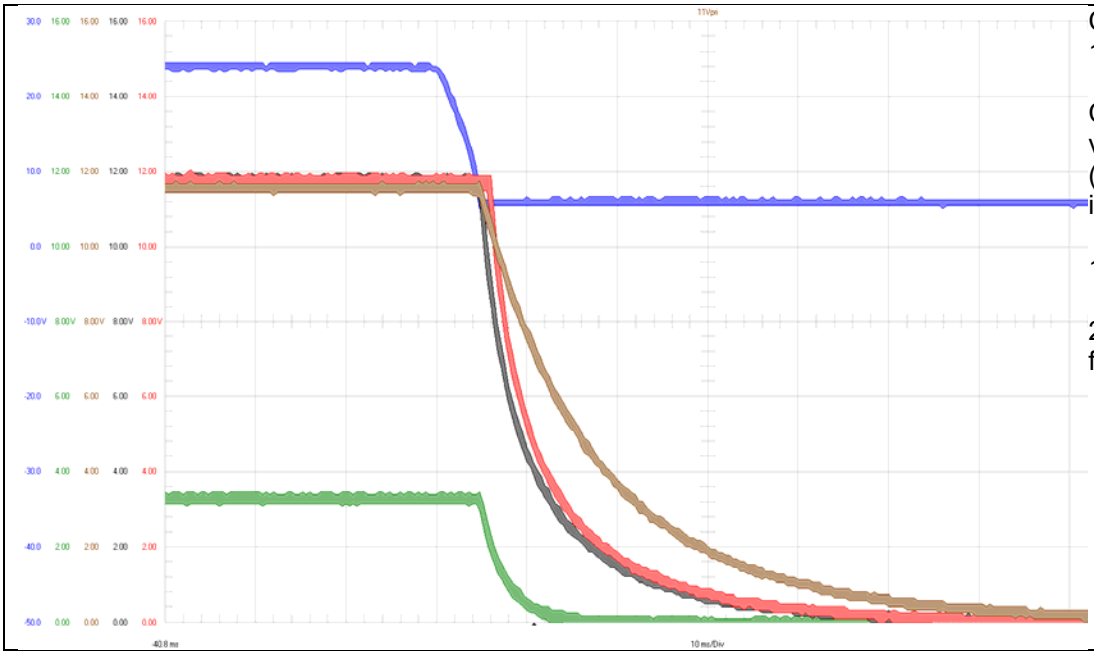
Ch2 to Ch5: output voltage => 2 V/div (green and brown non isolated outputs)

10 ms/div

20 MHz bandwidth filter

Figure 41. Shutdown 6 Vin

3.6.2 24 V Input Voltage



Ch1 : input voltage => 10 V/div

Ch2 to Ch5: output voltage => 2 V/div (green and brown non isolated outputs)

10 ms/div

20 MHz bandwidth filter

Figure 42. Shutdown 24 Vin

3.6.3 60 V Input Voltage

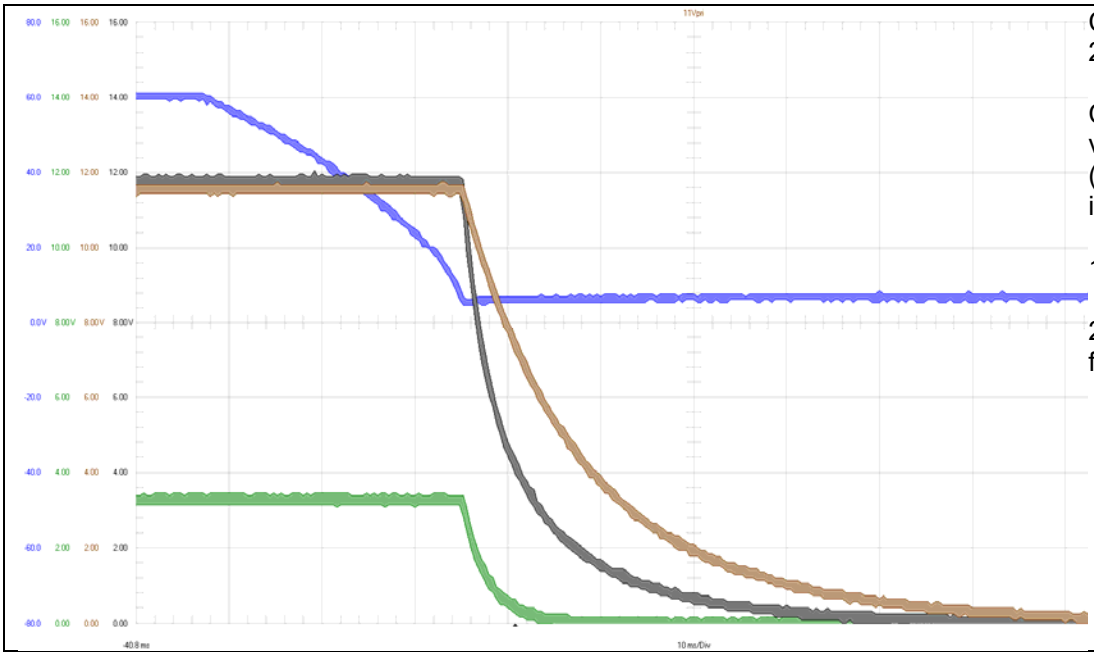


Figure 43. Shutdown 60 Vin

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