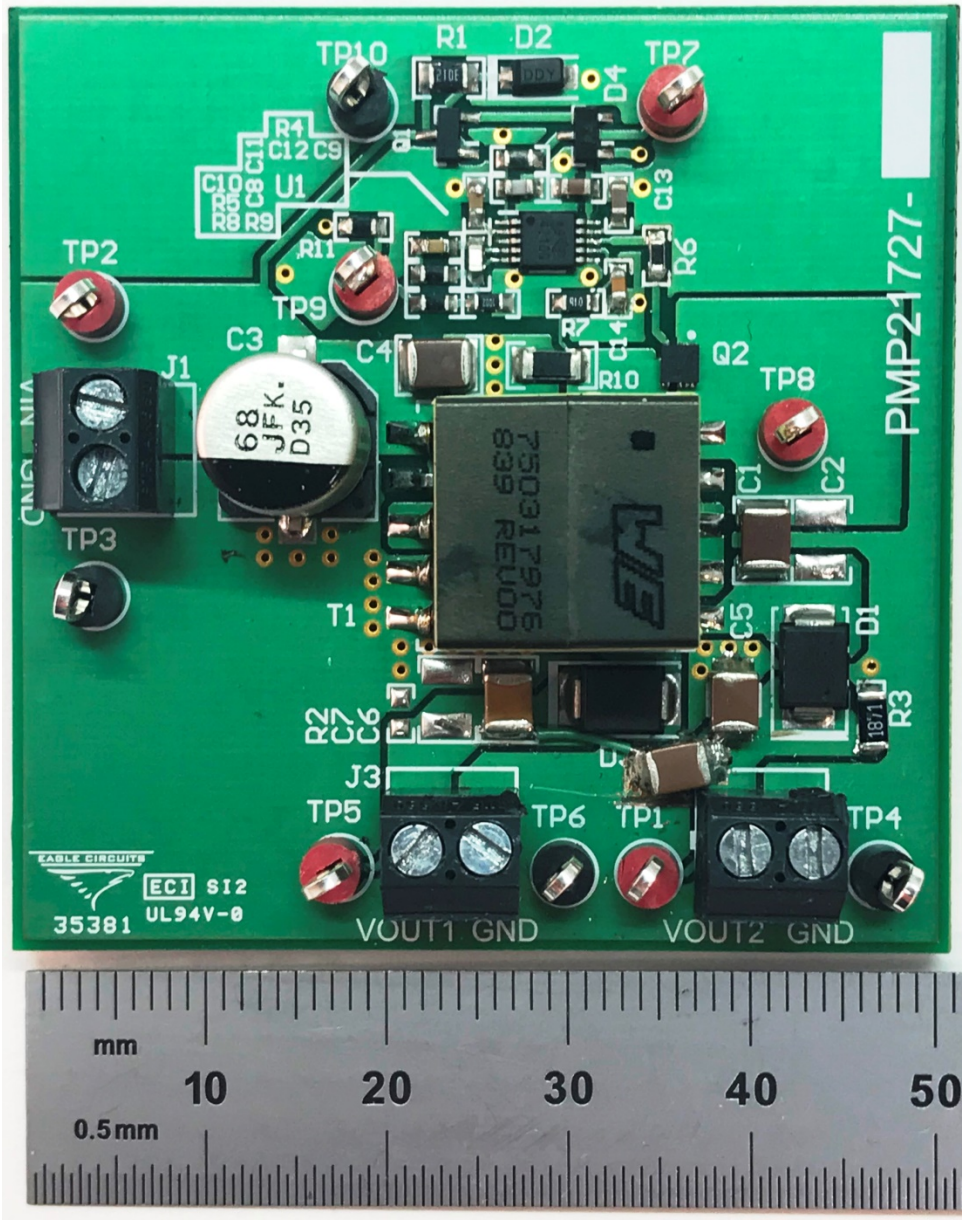
Test Report: PMP21727

Dual output SEPIC converter bias power supply reference design for solar panel applications

Description

This non-isolated design supplies a regulated 3.3 V/0.5 A and an unregulated 10 V/0.1 A for solar applications. It operates over a dual solar panel input voltage range of 7 V - 45 V and offers low cost and a compact form factor. This SEPIC converter features minimal voltage ringing on the FET for lower stress and reduced EMI.



1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

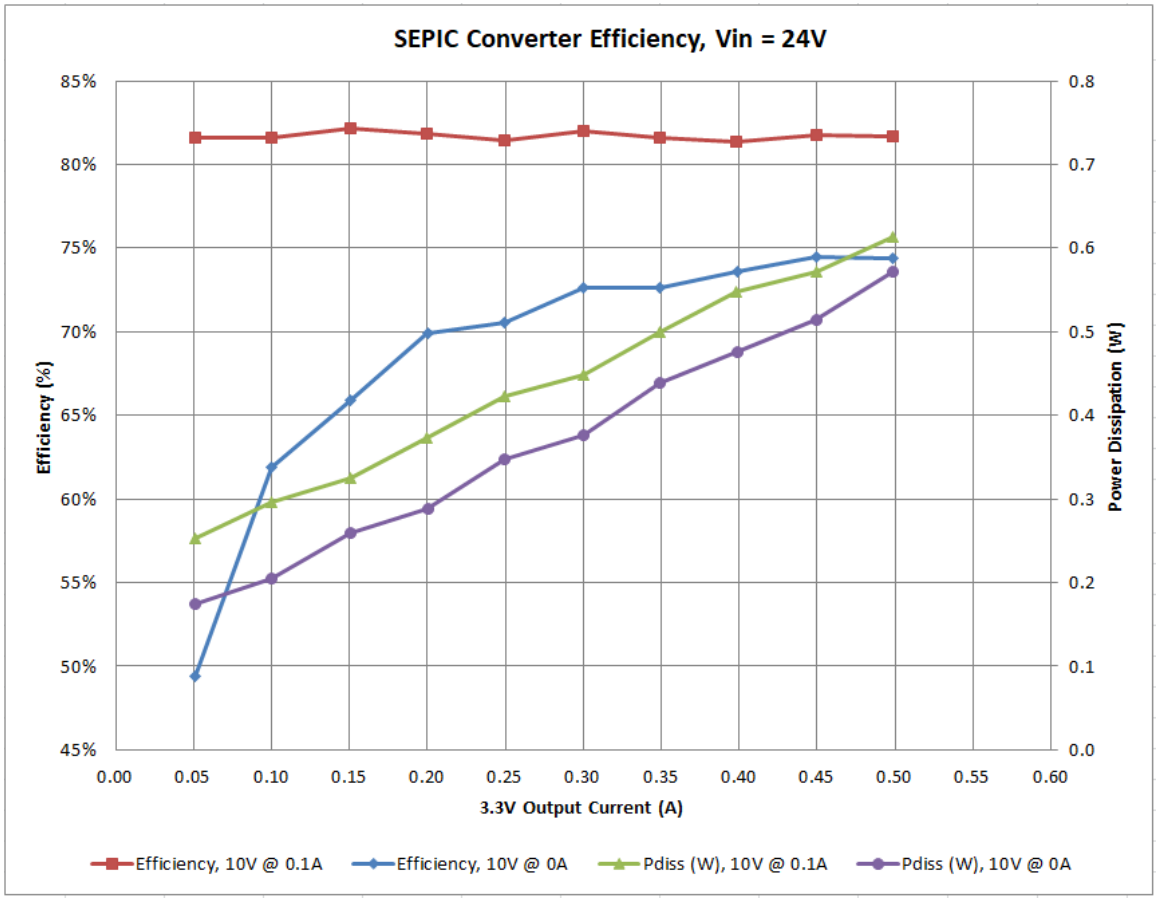
PARAMETER	SPECIFICATIONS
Input voltage range	7 - 45V
Output voltage and current	3.3V @ 0.5A and 10V @ 0.1A
Switching frequency	150kHz
Isolation	No

1.2 Required Equipment

- Dual electronic loads (2W min each) or power resistors (resistor decade box)
- Power supply capable of handling 50V and 1A
- Oscilloscope and probes
- Digital Multimeters
- Stability measurement device (Venable or Bode)

2 Testing and Results

2.1 Efficiency and Power Dissipation Graphs



This graph displays the efficiency and power dissipation of the converter with the 10V at full load and zero loads.

2.2 Efficiency and Power Dissipation Data

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency, 10V @ 0.1A	Pdiss (W), 10V @ 0.1A
24.0445	0.0572	3.3353	0.0507	9.726	0.09795	1.122	1.375	81.6%	0.254
24.0415	0.0668	3.3351	0.0999	9.850	0.09919	1.310	1.606	81.6%	0.296
24.0430	0.0759	3.3353	0.1508	9.948	0.10018	1.500	1.825	82.2%	0.325
24.0406	0.0854	3.3352	0.1999	10.029	0.10100	1.680	2.053	81.8%	0.373
24.0404	0.0949	3.3351	0.2492	10.100	0.10171	1.858	2.281	81.5%	0.423
24.0409	0.1035	3.3353	0.3000	10.162	0.10234	2.041	2.488	82.0%	0.448
24.0332	0.1130	3.3353	0.3493	10.213	0.10285	2.215	2.716	81.6%	0.500
24.0324	0.1221	3.3349	0.3983	10.255	0.10327	2.387	2.934	81.4%	0.547
24.0250	0.1306	3.3354	0.4494	10.292	0.10365	2.566	3.138	81.8%	0.572
24.0020	0.1395	3.3354	0.4984	10.323	0.10396	2.736	3.348	81.7%	0.613

This table shows the efficiency data for the converter with the 10V @ 0.1A.

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency, 10V @ 0A	Pdiss (W), 10V @ 0A
24.0511	0.0143	3.3355	0.0509	10.134	0	0.170	0.344	49.4%	0.174
24.0479	0.0224	3.3354	0.1000	10.354	0	0.334	0.539	61.9%	0.205
24.0475	0.0317	3.3353	0.1507	10.528	0	0.503	0.762	65.9%	0.260
24.0462	0.0397	3.3354	0.2000	10.676	0	0.667	0.955	69.9%	0.288
24.0448	0.0490	3.3352	0.2492	10.815	0	0.831	1.178	70.5%	0.347
24.0433	0.0573	3.3353	0.3000	10.952	0	1.001	1.378	72.6%	0.377
24.0416	0.0667	3.3353	0.3493	11.080	0	1.165	1.604	72.7%	0.439
24.0400	0.0751	3.3353	0.3985	11.205	0	1.329	1.805	73.6%	0.476
24.0389	0.0837	3.3353	0.4492	11.329	0	1.498	2.012	74.5%	0.514
24.0336	0.0930	3.3352	0.4986	11.447	0	1.663	2.235	74.4%	0.572

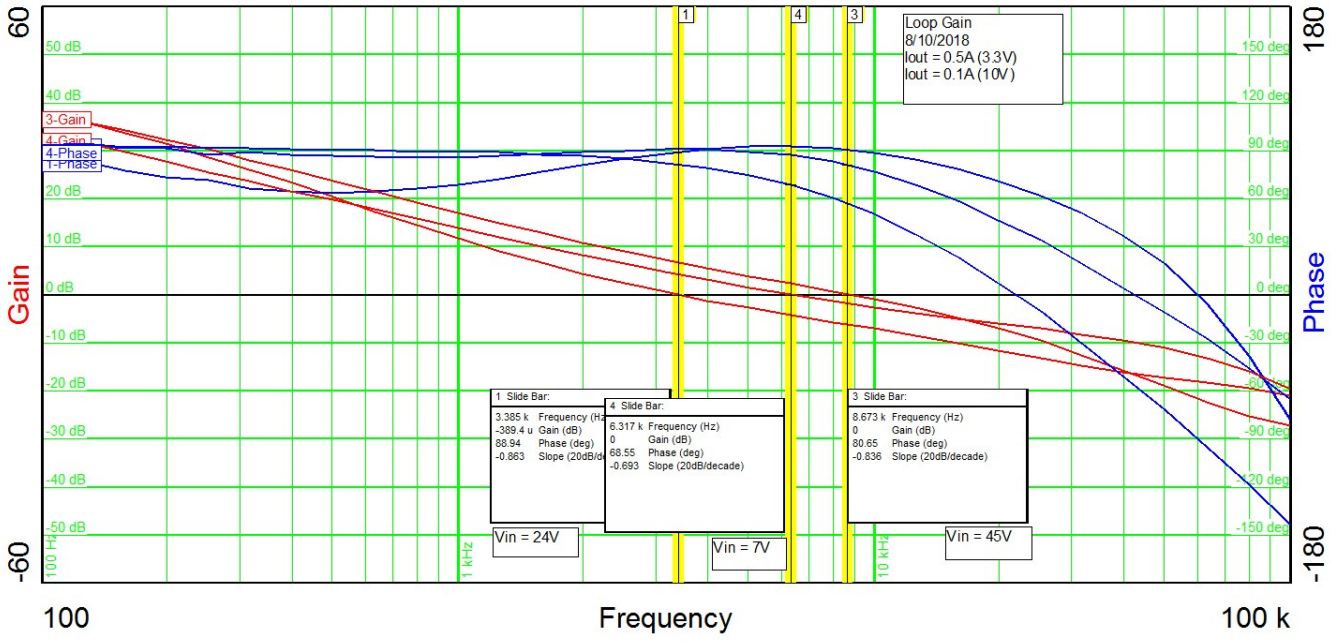
This table shows the efficiency data for the converter with the 10V @ 0A.

2.2.1 Cross Regulation

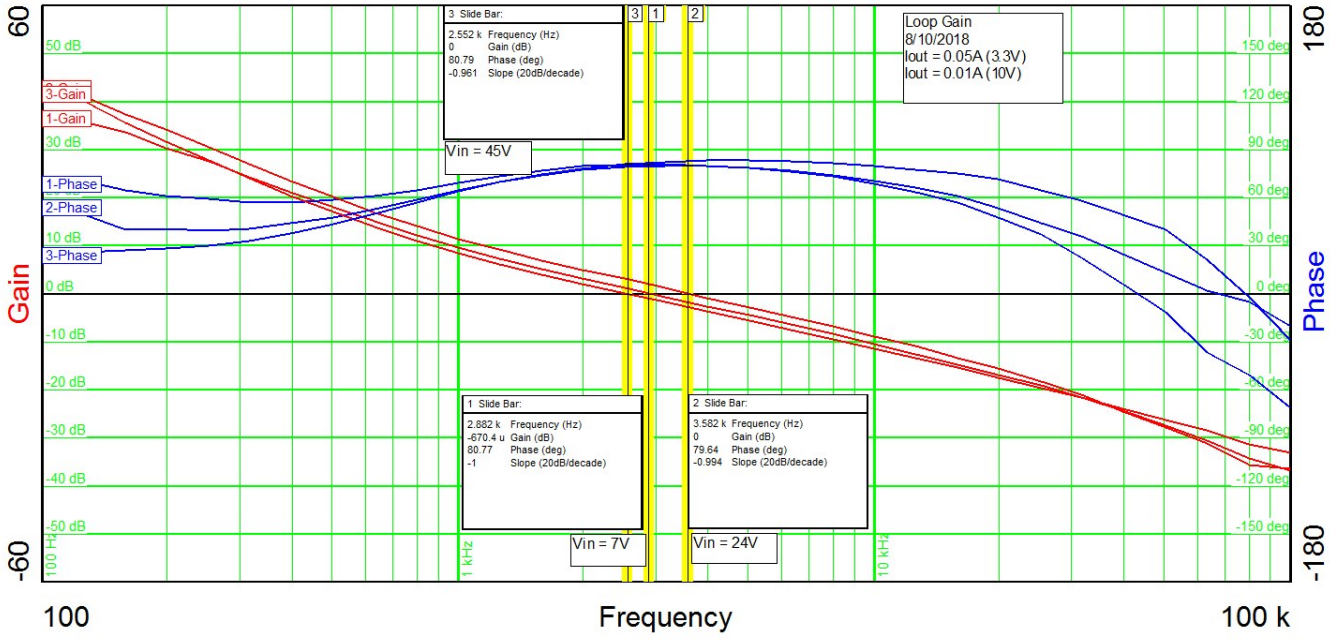
Voltage Regulation Data				
VIN (V)	VOUT 3.3V (V)	IOUT 3.3V (A)	VOUT 10V (V)	IOUT 10V (A)
No Load Conditions				
7	3.334	0	9.371	0
24	3.334	0	9.395	0
45	3.334	0	9.395	0
Full Load Conditions				
7	3.334	0.5	10.476	0.1
24	3.335	0.5	10.327	0.1
45	3.337	0.5	10.286	0.1
Cross Loading				
7	3.334	0	8.939	0.1
7	3.334	0.5	11.296	0
24	3.335	0	8.618	0.1
24	3.335	0.5	11.447	0
45	3.337	0	8.558	0.1
45	3.337	0.5	11.423	0
			10.193	High/Low Avg (V)
			-12.30	Percent Low (%)
			12.30	Percent High (%)

This table shows the voltage regulation on the unregulated 10V output under various cross load conditions. The high and low levels are highlighted in yellow.

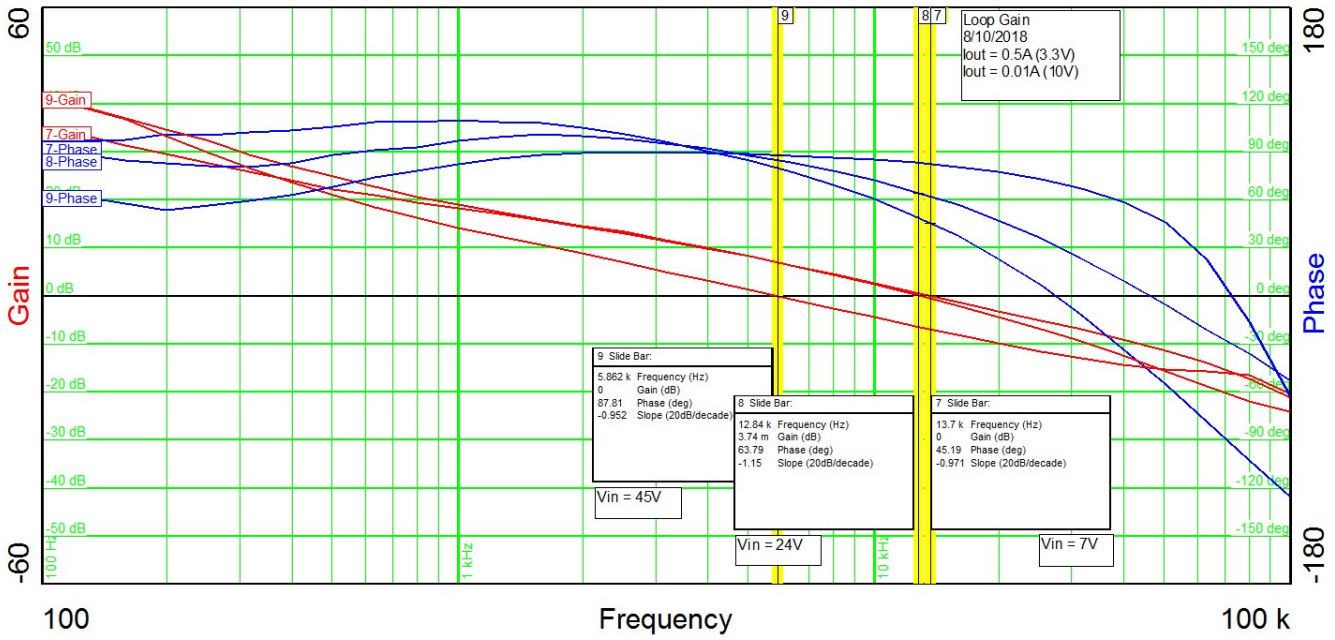
2.3 Loop Gain



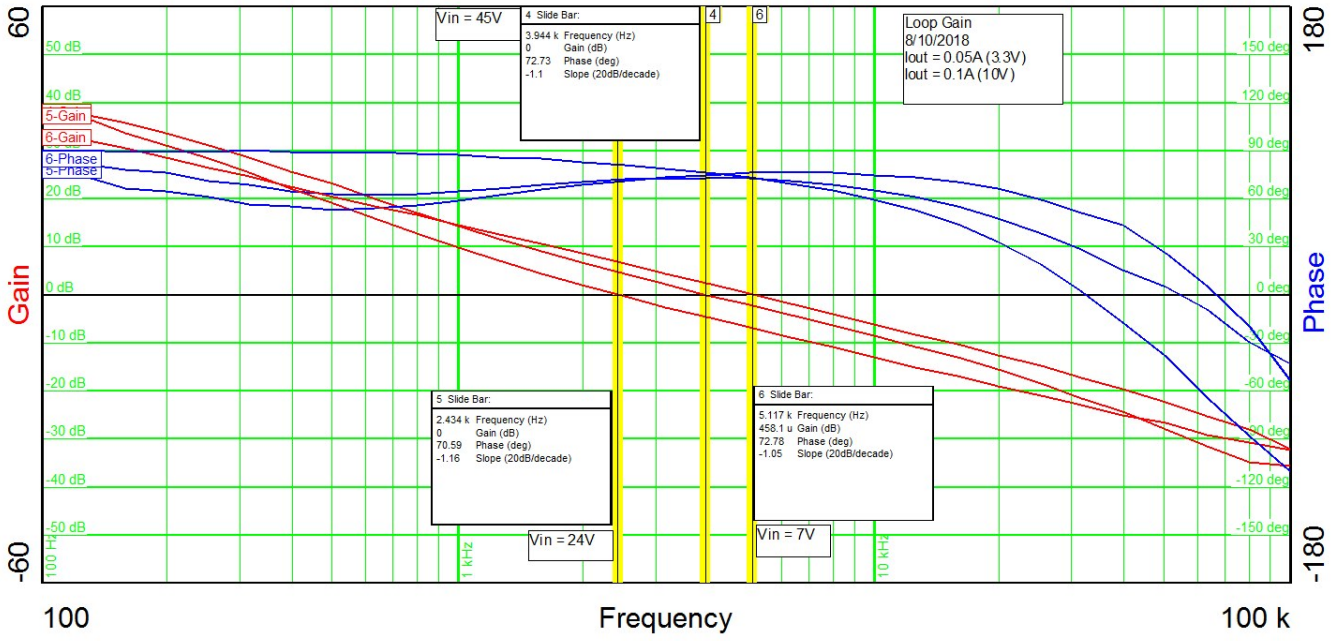
3V@0.5A, 10V@0.1A	Vin = 7V	Bandwidth = 6.32 kHz	Phase Margin = 69 degrees
3V@0.5A, 10V@0.1A	Vin = 24V	Bandwidth = 3.39 kHz	Phase Margin = 89 degrees
3V@0.5A, 10V@0.1A	Vin = 45V	Bandwidth = 8.67 kHz	Phase Margin = 81 degrees



3V@0.05A, 10V@0.01A	Vin = 7V	Bandwidth = 2.88 kHz	Phase Margin = 81 degrees
3V@0.05A, 10V@0.01A	Vin = 24V	Bandwidth = 3.58 kHz	Phase Margin = 80 degrees
3V@0.05A, 10V@0.01A	Vin = 45V	Bandwidth = 2.55 kHz	Phase Margin = 81 degrees

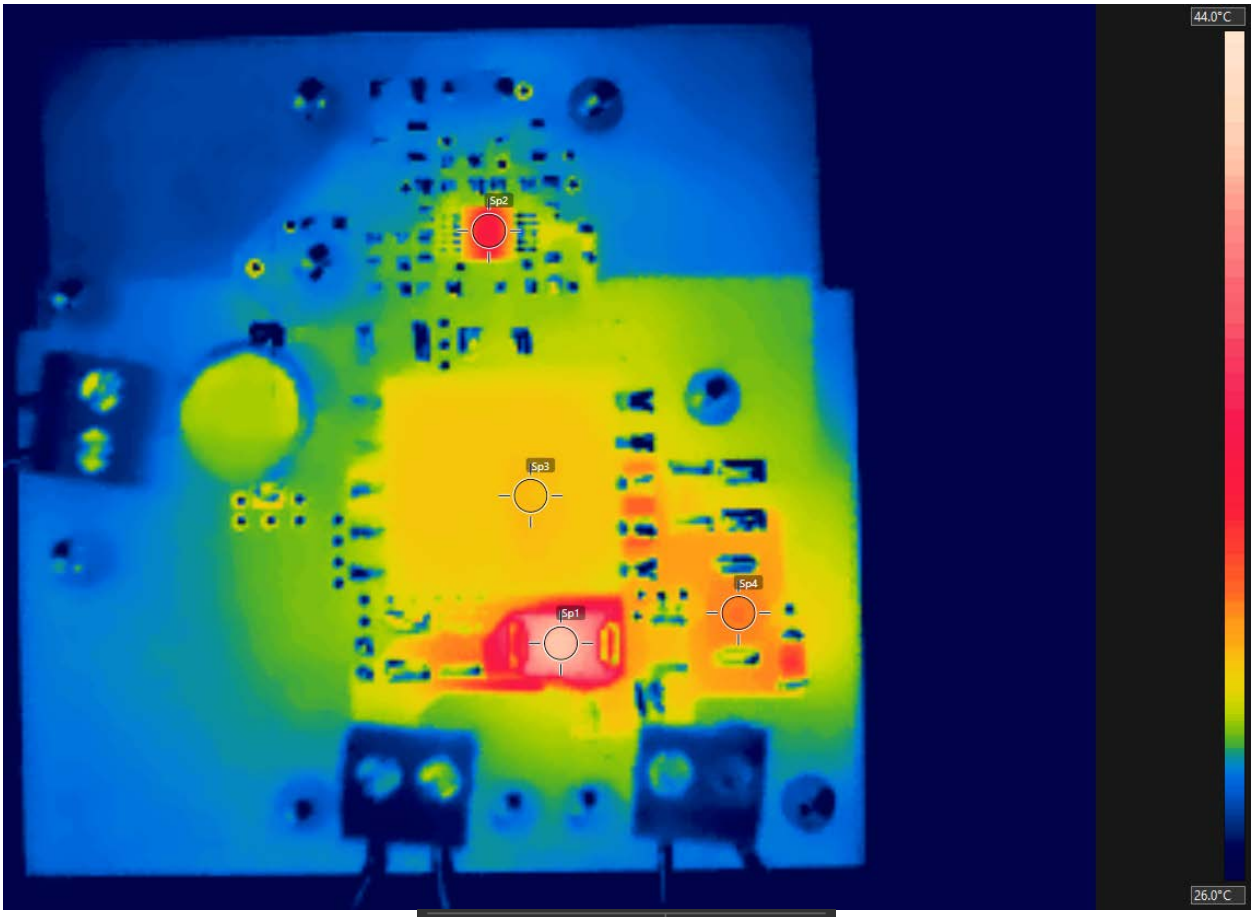


3V@0.5A, 10V@0.01A	Vin = 7V	Bandwidth = 13.7 kHz	Phase Margin = 45 degrees
3V@0.5A, 10V@0.01A	Vin = 24V	Bandwidth = 12.8 kHz	Phase Margin = 64 degrees
3V@0.5A, 10V@0.01A	Vin = 45V	Bandwidth = 5.86 kHz	Phase Margin = 88 degrees



3V@0.05A, 10V@0.1A	Vin = 7V	Bandwidth = 5.12 kHz	Phase Margin = 73 degrees
3V@0.05A, 10V@0.1A	Vin = 24V	Bandwidth = 2.43 kHz	Phase Margin = 71 degrees
3V@0.05A, 10V@0.1A	Vin = 45V	Bandwidth = 3.94 kHz	Phase Margin = 73 degrees

2.4 Thermal Images

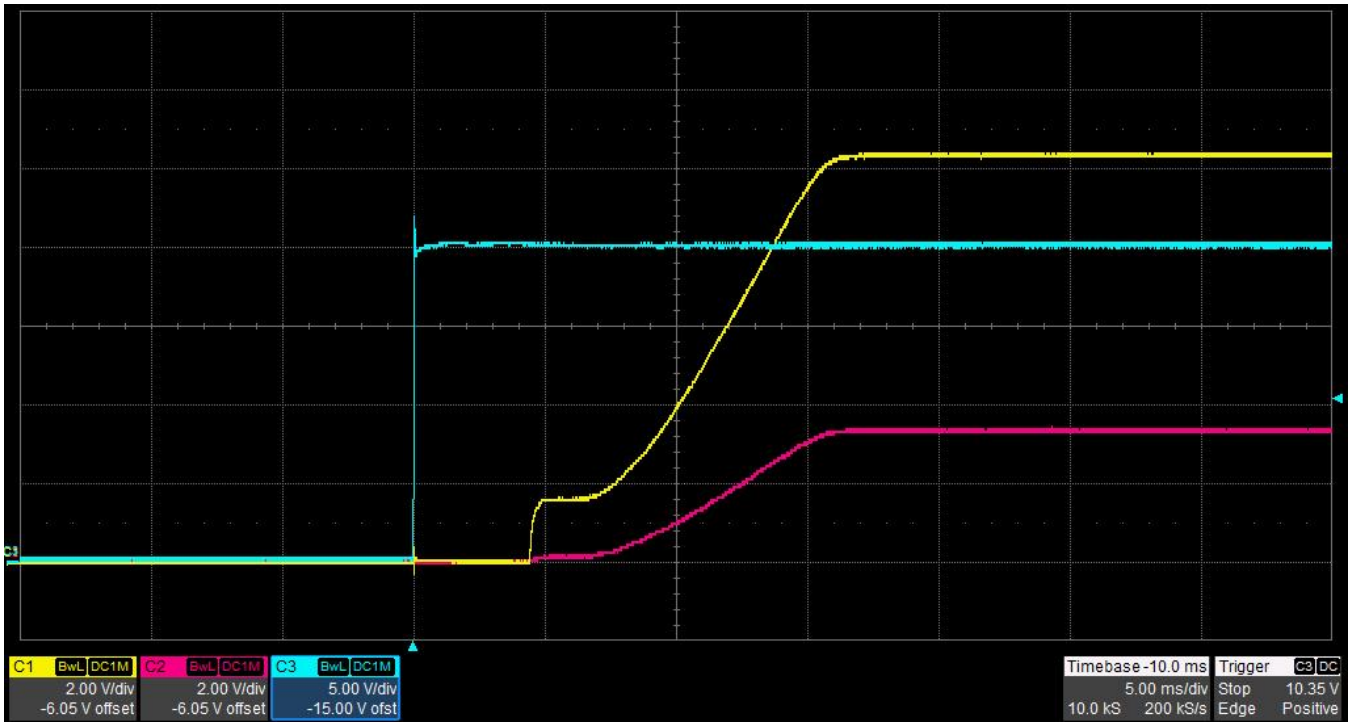


Sp1	41.5 °C
Sp2	35.1 °C
Sp3	31.0 °C
Sp4	32.3 °C

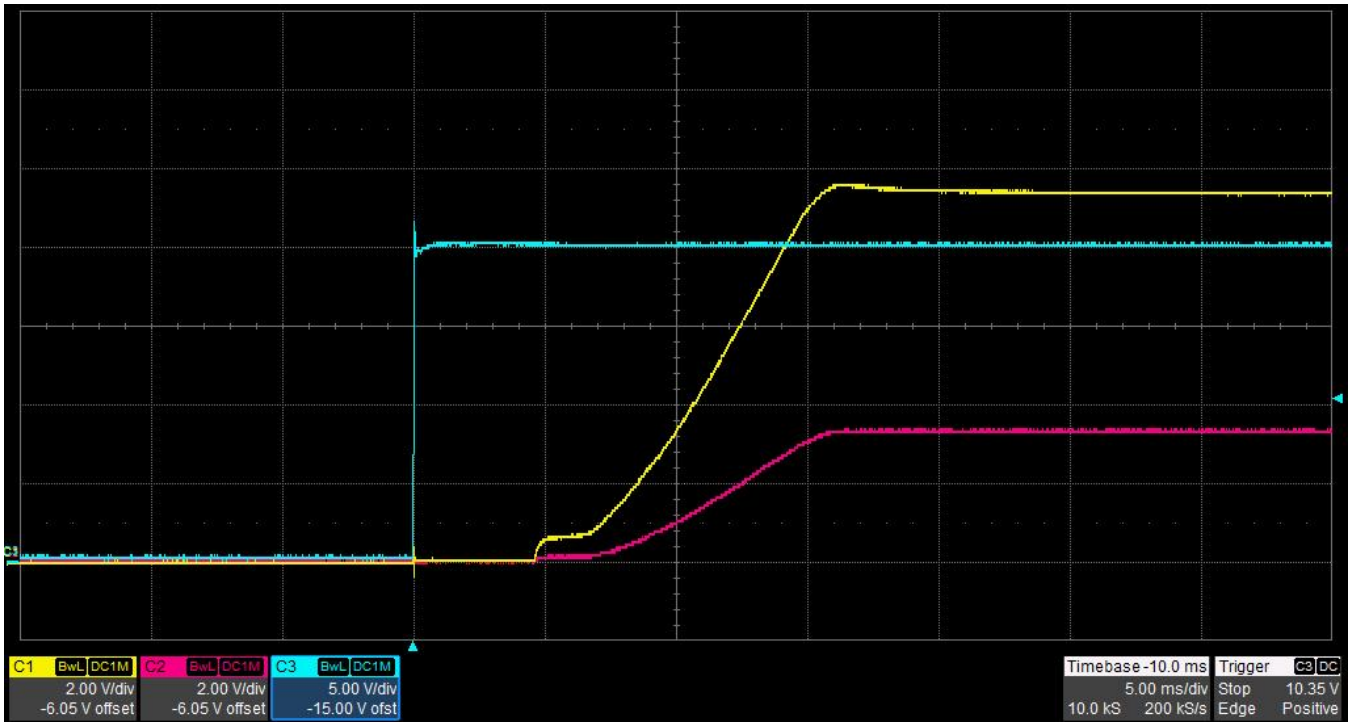
This thermal image shows the operating temperature of the board with 24V input and max loads at room temperature.

3 Waveforms

3.1 Startup Sequence

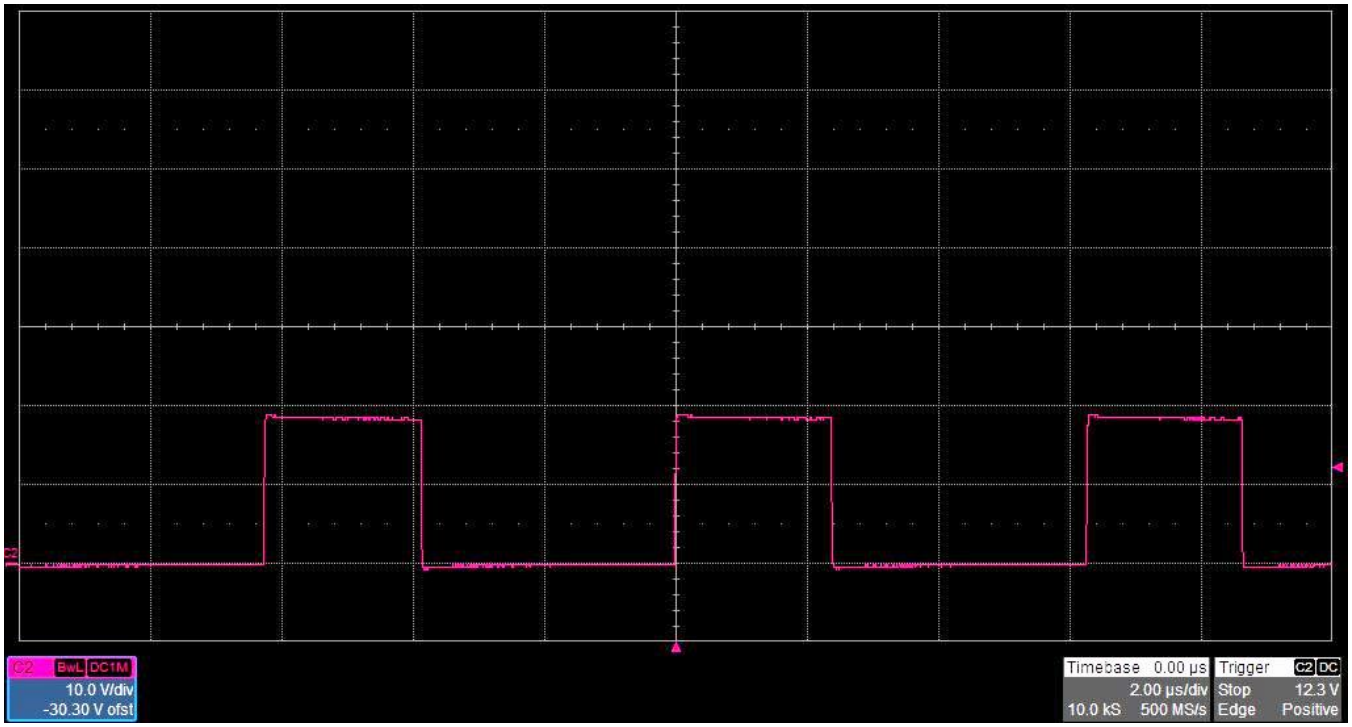


Start-up sequence for Vin = 20V (blue) and max loads; 3.3V@0.5A (red), 10V@0.1A (yellow)



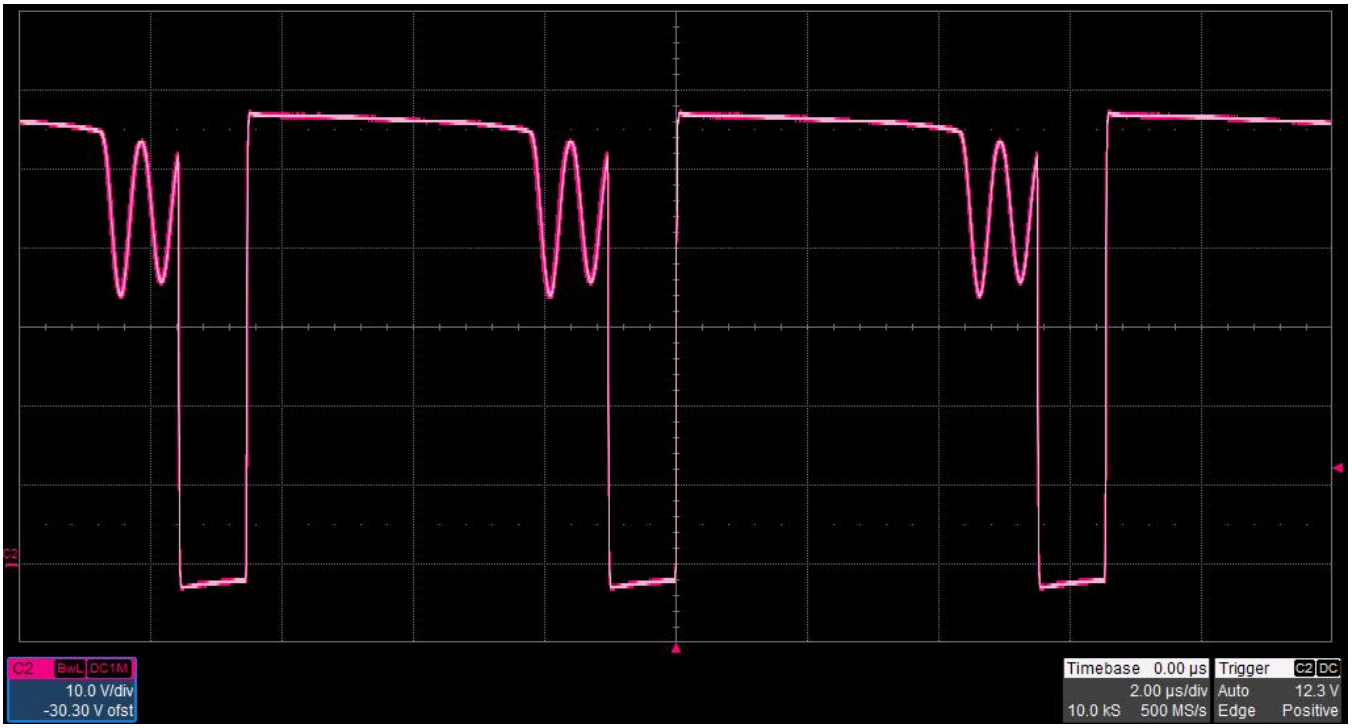
Start-up sequence for Vin = 20V (blue) and no loads; 3.3V@0A (red), 10V@0A (yellow)

3.2 Switch Node

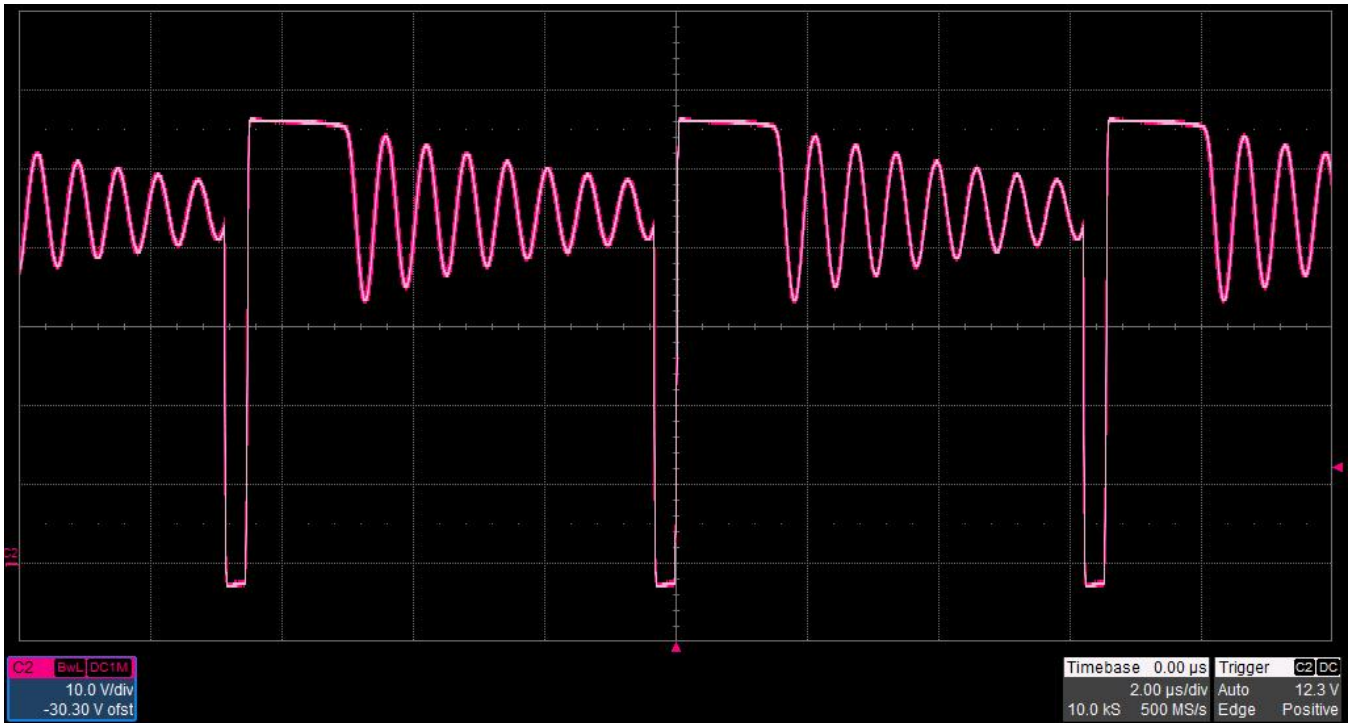


Switch node of FET Q2 with Vin = 7V and 3.3V @ 0.5A and 10V @ 0.1A

Switch node of FET Q2 with Vin = 7V and 3.3V @ 0.05A and 10V @ 0.01A

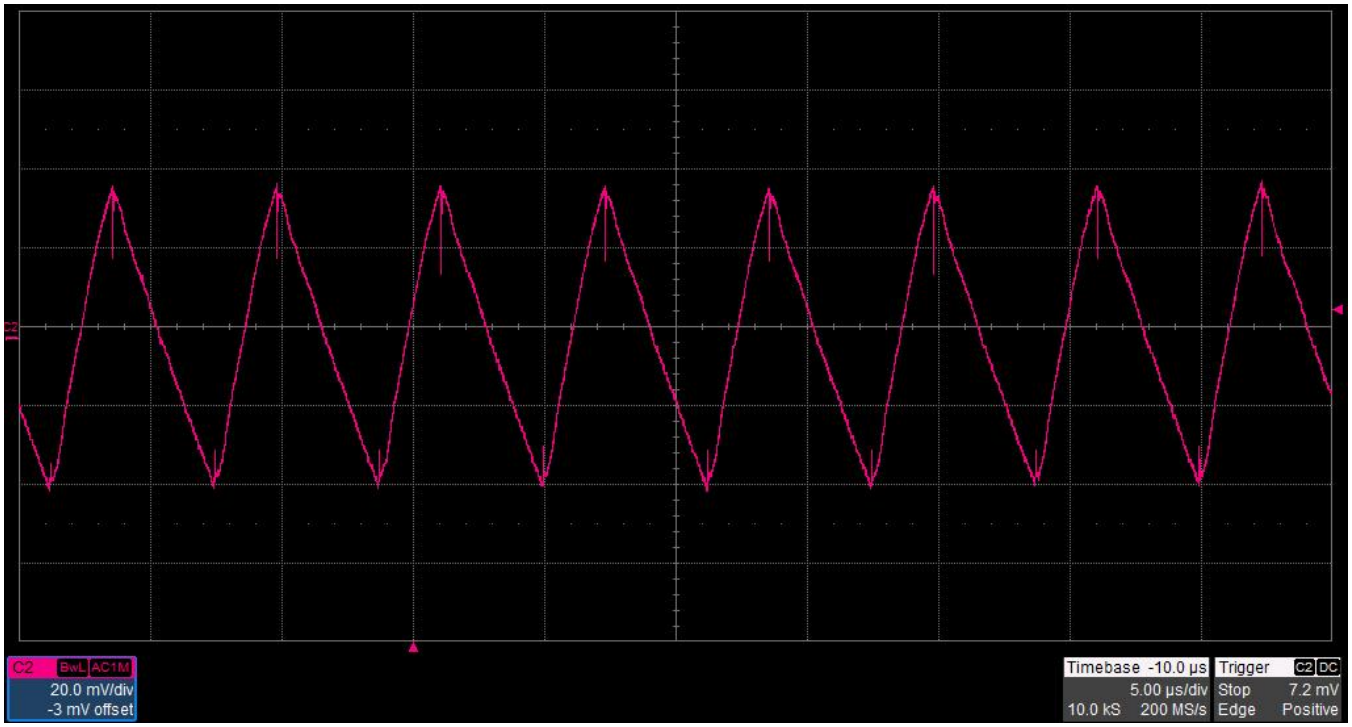


Switch node of FET Q2 with Vin = 45V and 3.3V @ 0.5A and 10V @ 0.1A

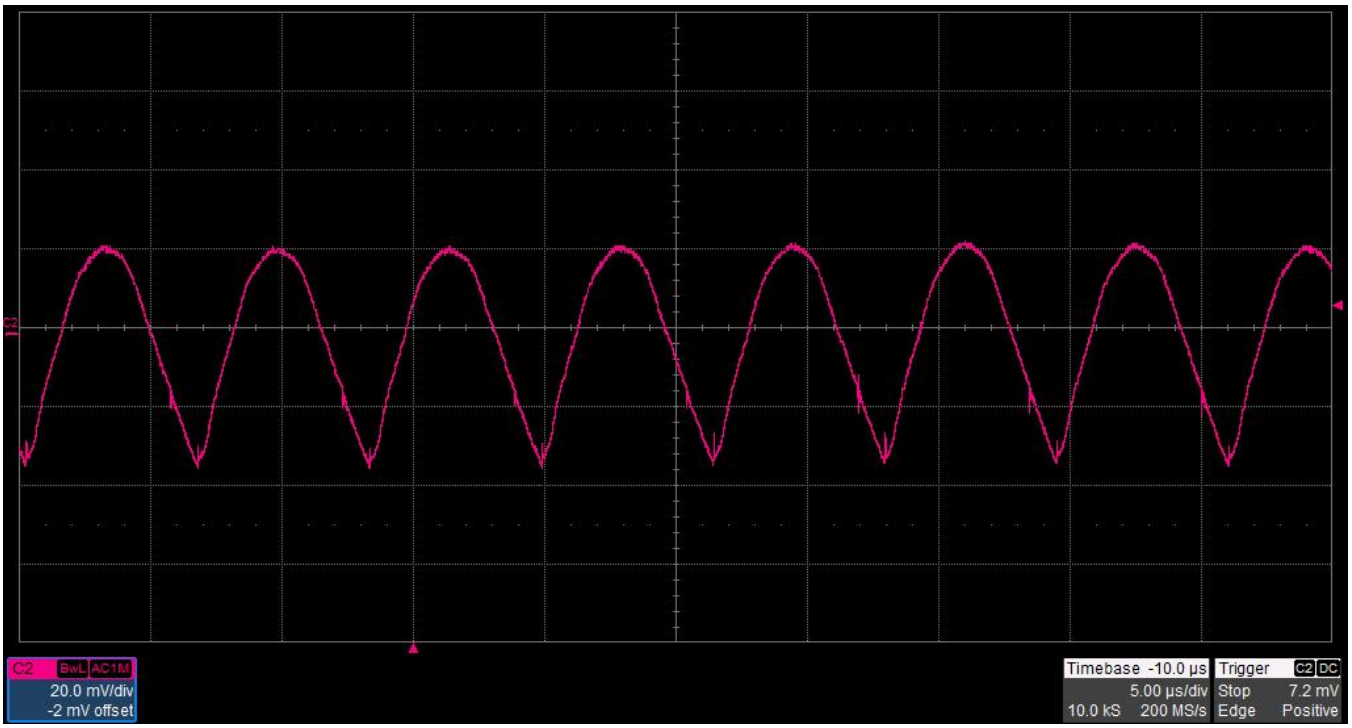


Switch node of FET Q2 with Vin = 45V and 3.3V @ 0.05A and 10V @ 0.01A

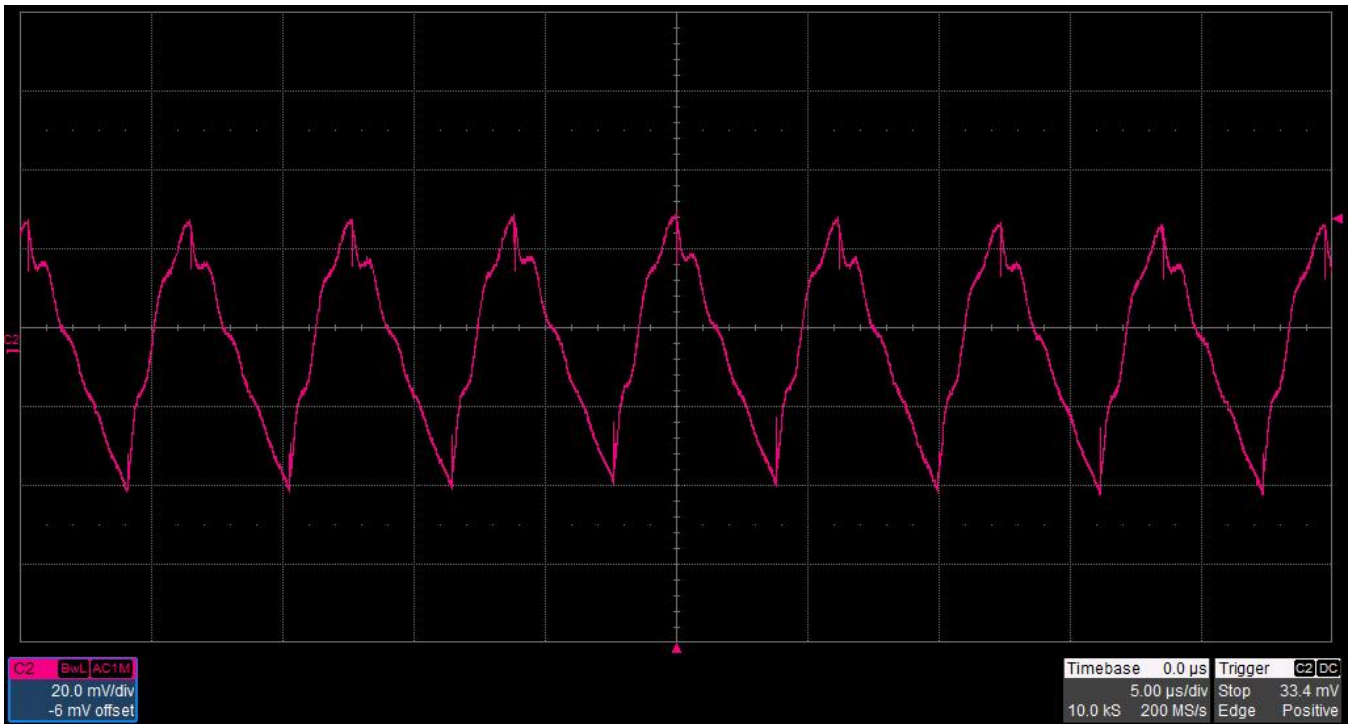
3.3 Output Voltage Ripple



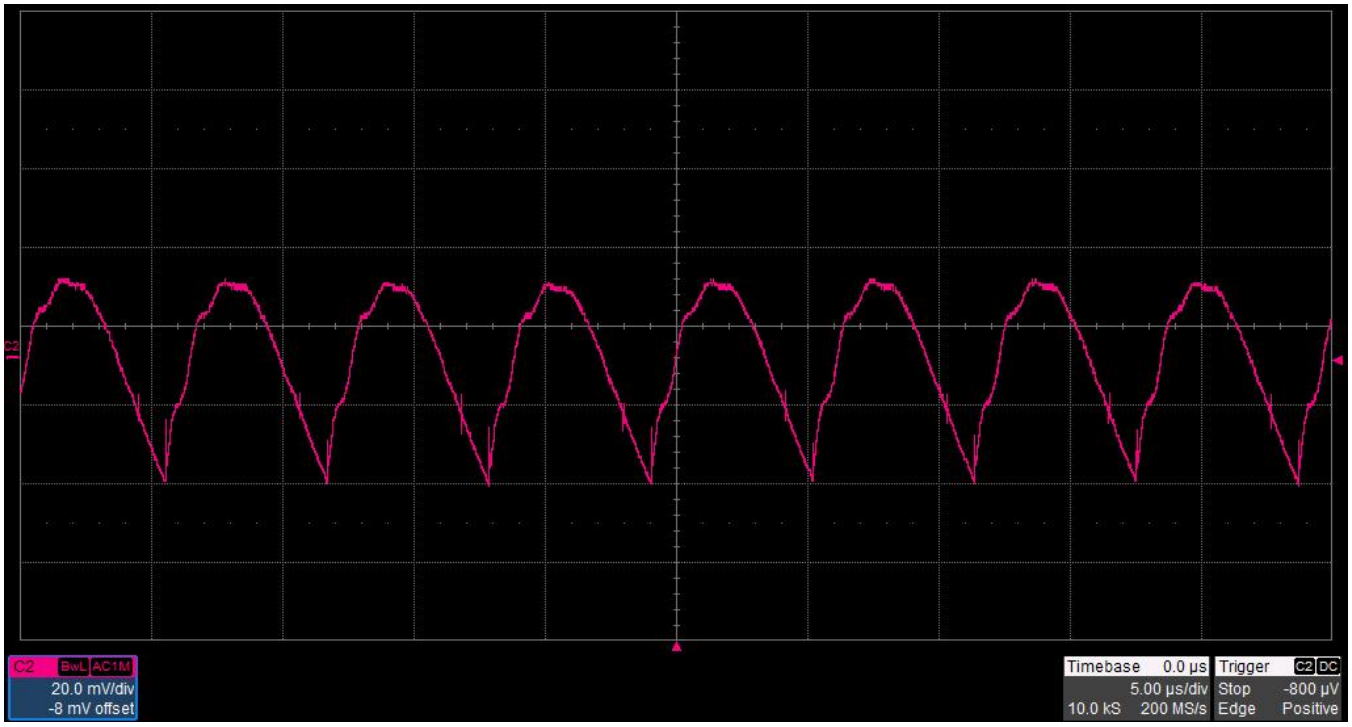
3.3V ripple voltage with Vin = 7V and 3.3V @ 0.5A and 10V @ 0.1A



3.3V ripple voltage with Vin = 45V and 3.3V @ 0.5A and 10V @ 0.1A

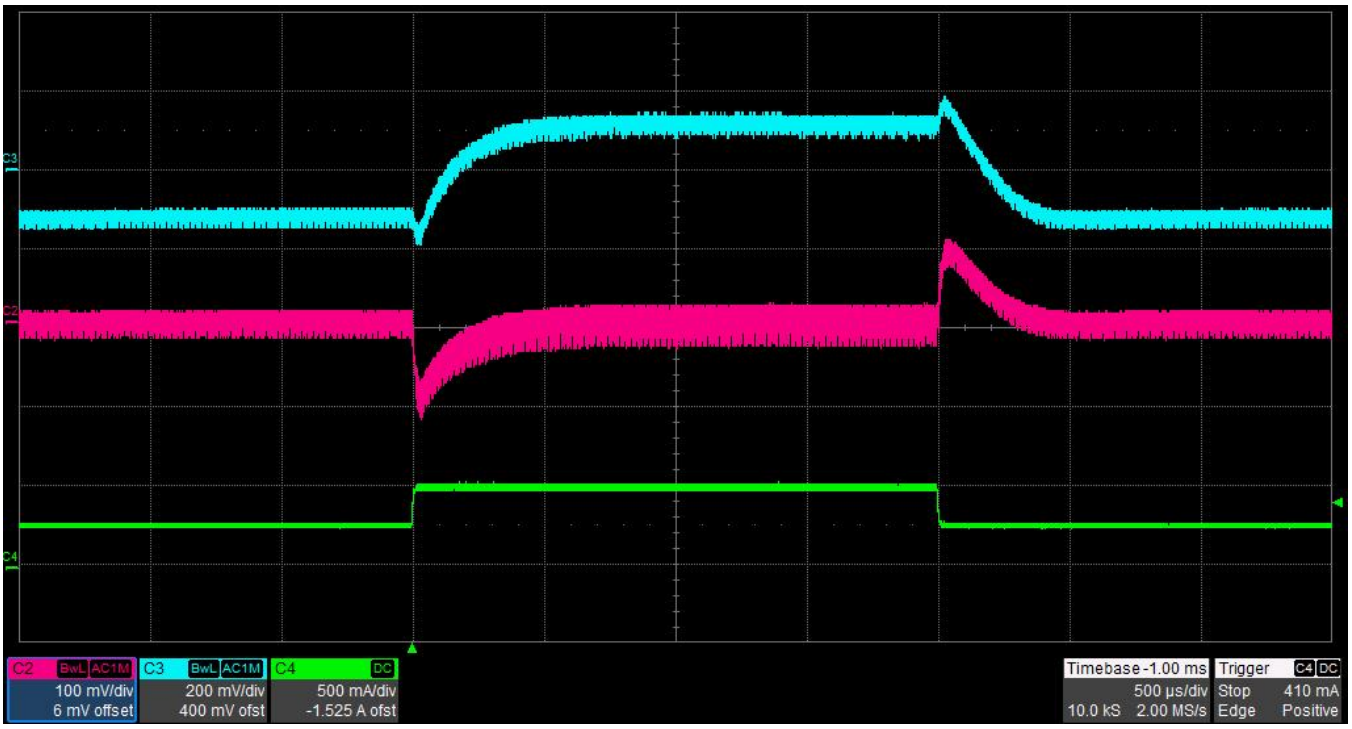


10V ripple voltage with Vin = 7V and 3.3V @ 0.5A and 10V @ 0.1A

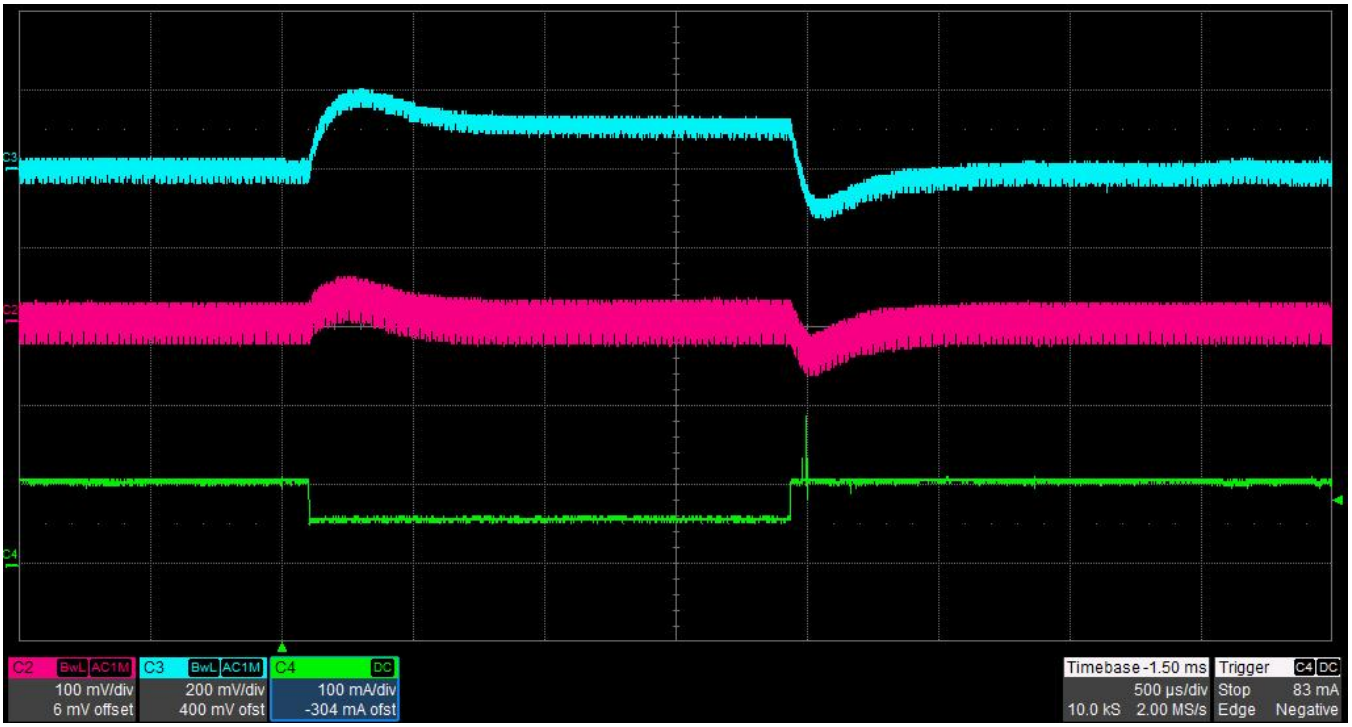


10V ripple voltage with Vin = 45V and 3.3V @ 0.5A and 10V @ 0.1A

3.4 Load Transients



50% to 100% load transient on the 3.3V output with Vin = 20V. 10V output (blue) and 3.3V (red)



50% to 100% load transient on the 10V output with Vin = 20V. 10V output (blue) and 3.3V (red)

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