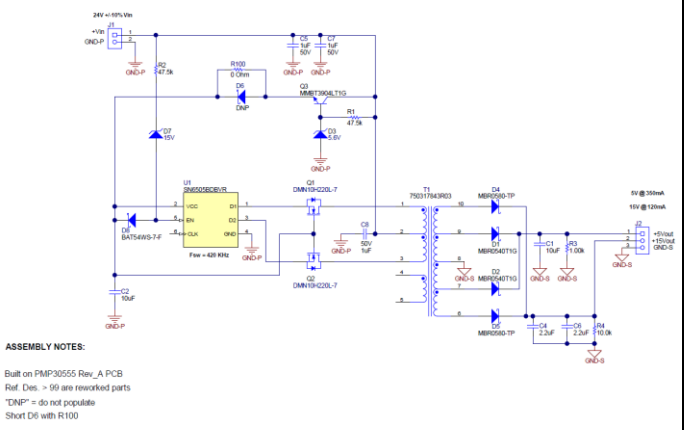
Test Report: PMP30555

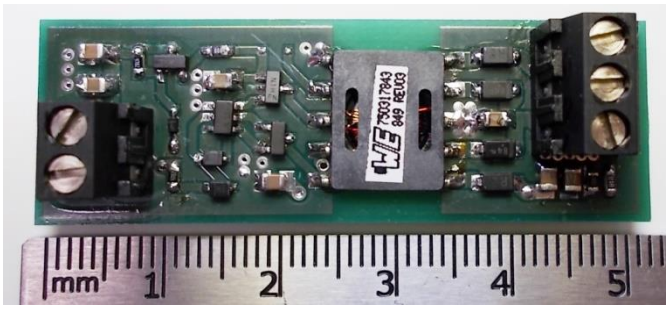
3.5-W Isolated Push-Pull Reference Design for Auxiliary Power Supply

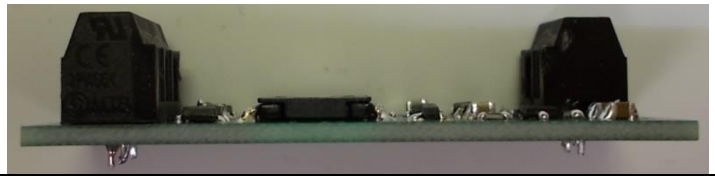
Description

This reference design is an isolated open-loop push-pull with “cascode” FETs that finds its typical application in isolated gate drive supply. The cascode connection extends the input voltage range of SN6505B from 5 V to 24 V, and two outputs supply 15 V at 120 mA and 5 V at 350 mA. Its 2-mm transformer makes the solution ultra-thin.

The PMP30555 Rev_B Reference Design has been built on PMP30555 Rev_A PCB.







1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	24 V ± 10% (DC)
Output #1, Voltage	15 V ± 10% (DC) at 24 Vin
Output #1, Current	120 mA
Output #2, Voltage	5 V ± 10% (DC) at 24 Vin
Output #2, Current	350 mA

1.2 Required Equipment

- 0…30 V, (min. 300 mA), constant voltage source (VS1)
- 0…20 V, (0…150 mA), constant current electronic load
- 0…10 V, (0…500 mA), constant current electronic load
- Oscilloscope (min. 100 MHz bandwidth)

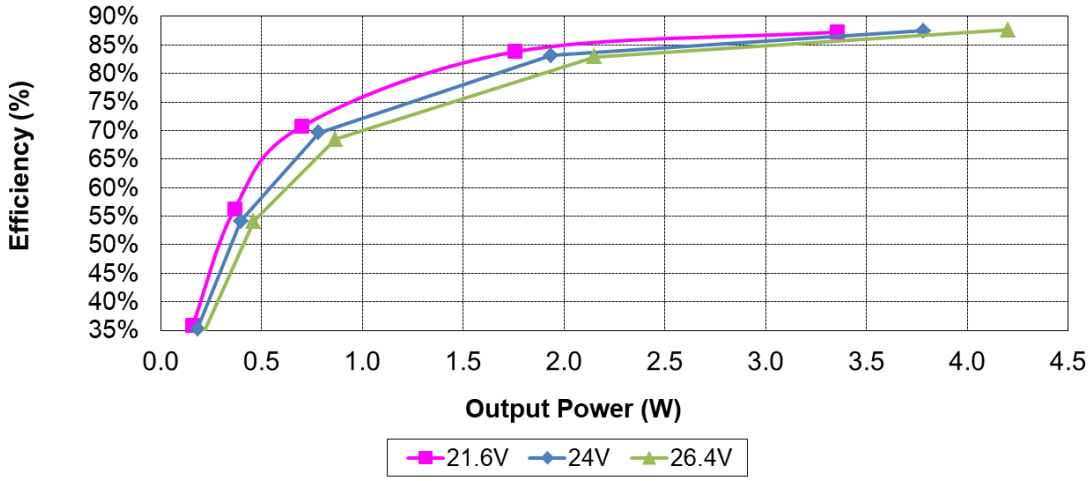
1.3 Considerations

a) Connect the source VS1 to pin 1 & 2 of J1.
b) Connect the loads to J2 (pin 1 & 2) with common ground to pin 3, set to CC mode.
c) Connect oscilloscope probes to Q2-Drain and Q2-Source versus primary ground.
d) Connect oscilloscope probes to C1, C4 and anode terminal of D4.

2 Testing and Results

2.1 *Efficiency Graphs:*

The efficiency graphs, versus output currents, are shown below. The voltage of power source has been set to 21.6 V, 24 V and 26.4 V (24 V ± 10 %).



2.2 *Efficiency Data:*

The efficiency graph reports the data from the tables shown below:

Vin(V)	Iin(mA)	Pin (W)	V15 (V)	I15 (mA)	V5 (V)	I5 (mA)	Pout (W)	Efficiency (%)
21.63	13.2	0.286	14.87	0	4.985	0	0	0%
21.64	20.4	0.441	14.81	6.2	4.950	13.5	0.159	35.94%
21.62	30.1	0.651	14.76	12.3	4.907	37.6	0.366	56.25%
21.61	45.9	0.992	14.70	23.8	4.872	72.3	0.702	70.78%
21.59	97.1	2.096	14.55	63.5	4.794	173.8	1.757	83.82%
21.62	177.8	3.844	14.35	119.4	4.683	350.5	3.355	87.27%

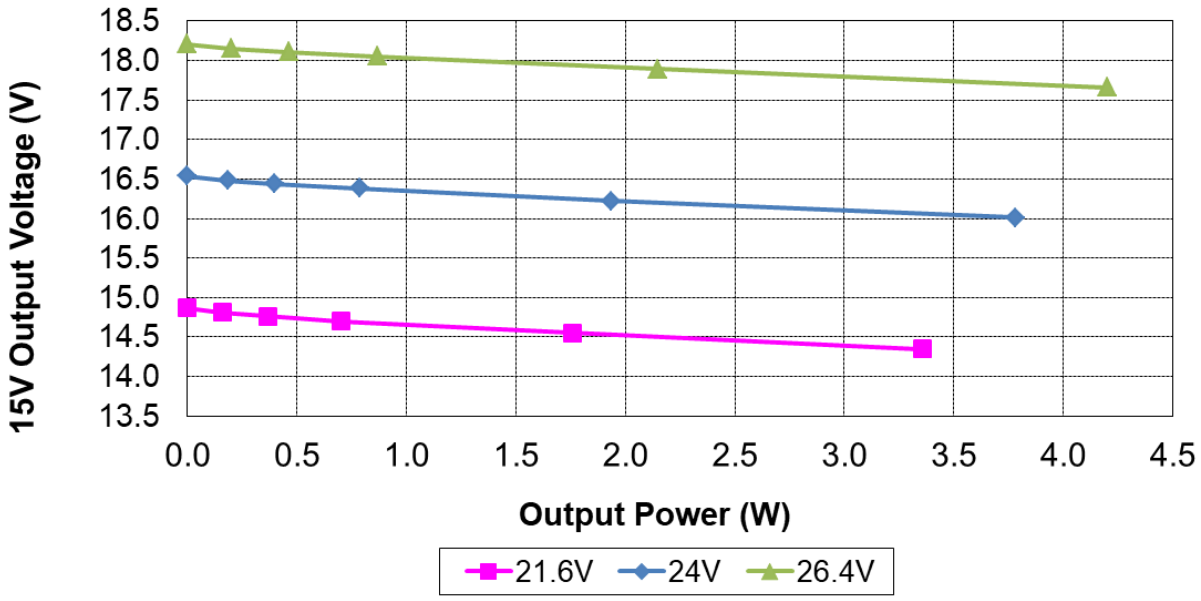
Vin(V)	Iin(mA)	Pin (W)	V15 (V)	I15 (mA)	V5 (V)	I5 (mA)	Pout (W)	Efficiency (%)
24.02	14.1	0.339	16.54	0	5.566	0	0	0%
24.04	21.6	0.519	16.48	6.6	5.527	13.5	0.183	35.32%
24.03	30.6	0.735	16.44	11.6	5.493	37.7	0.398	54.10%
24.03	46.9	1.127	16.38	23.8	5.458	72.3	0.784	69.61%
24.01	97.0	2.329	16.22	61.8	5.374	173.9	1.937	83.17%
24.02	180.1	4.326	16.01	121.1	5.261	350.5	3.783	87.44%

Vin(V)	Iin(mA)	Pin (W)	V15 (V)	I15 (mA)	V5 (V)	I5 (mA)	Pout (W)	Efficiency (%)
26.42	14.9	0.394	18.21	0	6.153	0	0	0%
26.43	22.6	0.597	18.15	6.6	6.111	13.5	0.202	33.87%
26.43	32.2	0.851	18.11	12.8	6.076	37.7	0.461	54.15%
26.42	47.9	1.266	18.05	23.8	6.040	72.3	0.866	68.45%
26.40	98.2	2.592	17.89	62.3	5.955	173.9	2.150	82.94%
26.40	181.7	4.797	17.66	122.1	5.838	350.5	4.203	87.61%

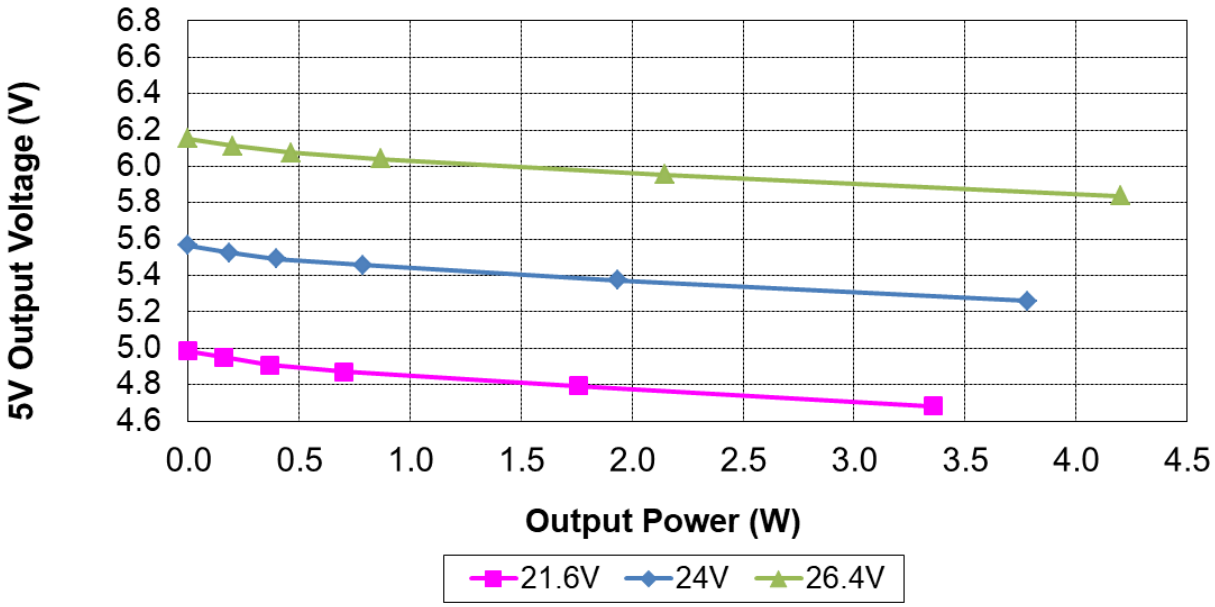
2.3 Output Voltage Regulation

The output voltage regulation graphs, for each output, are shown below.
Both outputs have been loaded with the same percent, at the same time, of their nominal currents.

15 V output voltage:

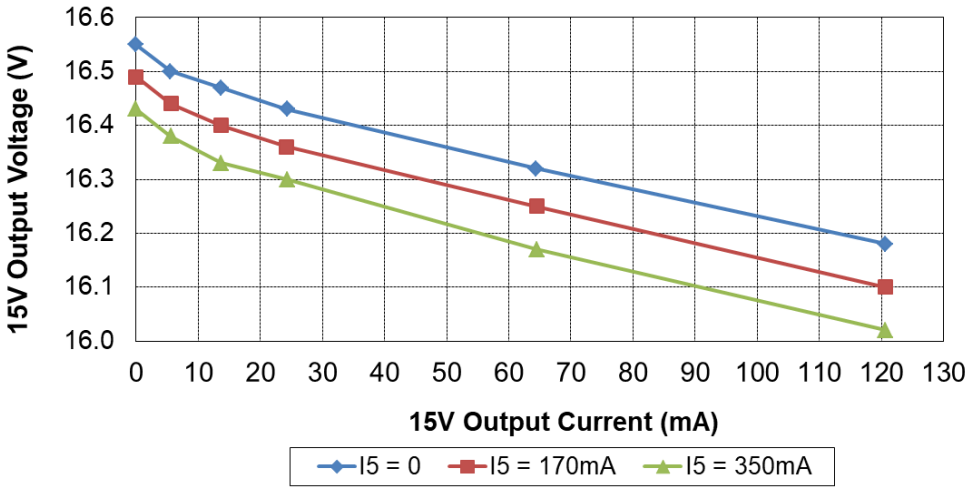


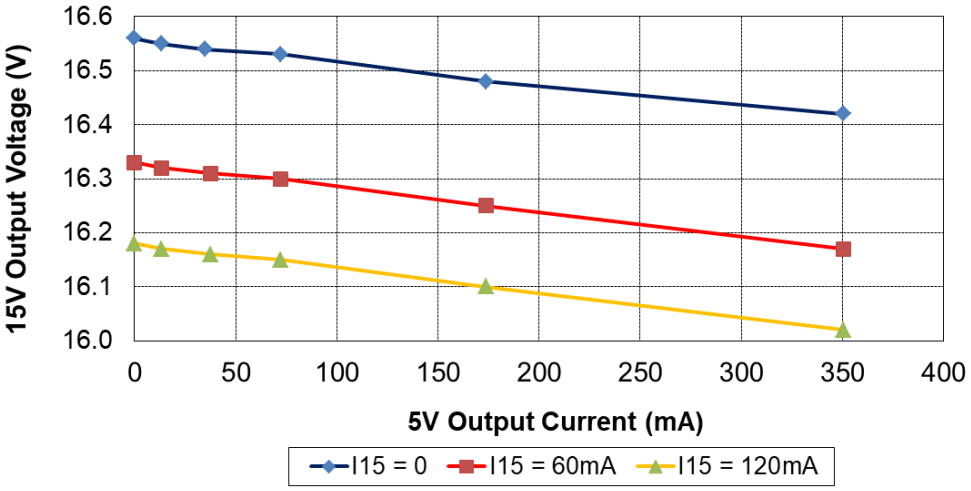
5 V output voltage:

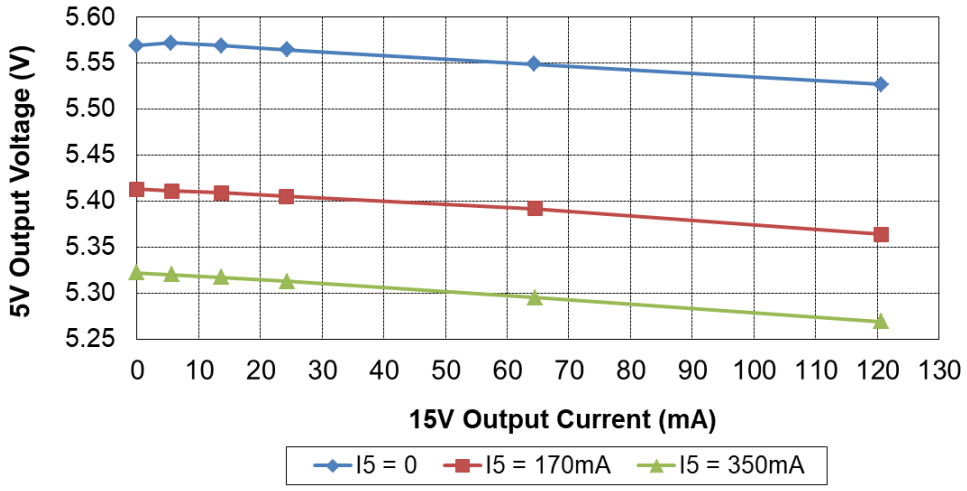


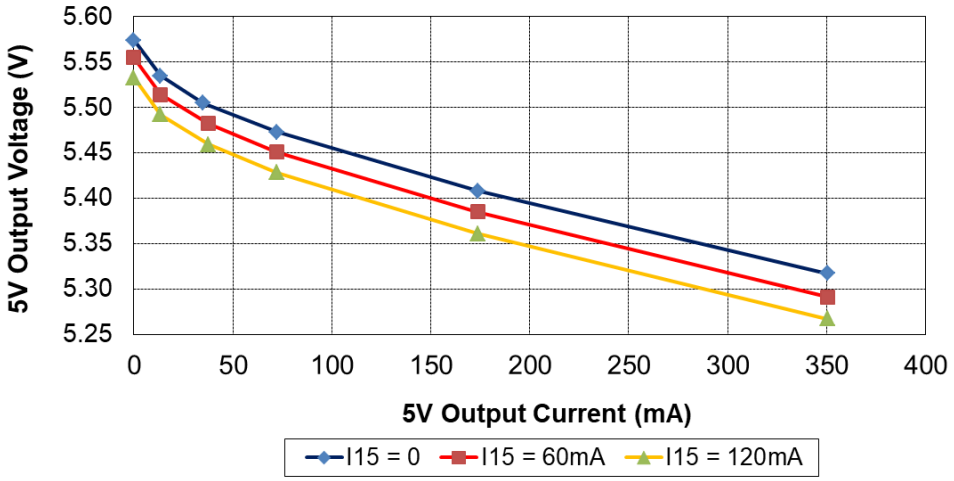
2.4 Cross Regulation

While one output of the converter was loaded at constant fixed current (0, 50 % and 100 % of nominal load), in the other one the load current has been varied from 0 to 100 % and the cross-regulation performance has been measured. The input voltage of the converter was 24 V.









2.5 Dimensions

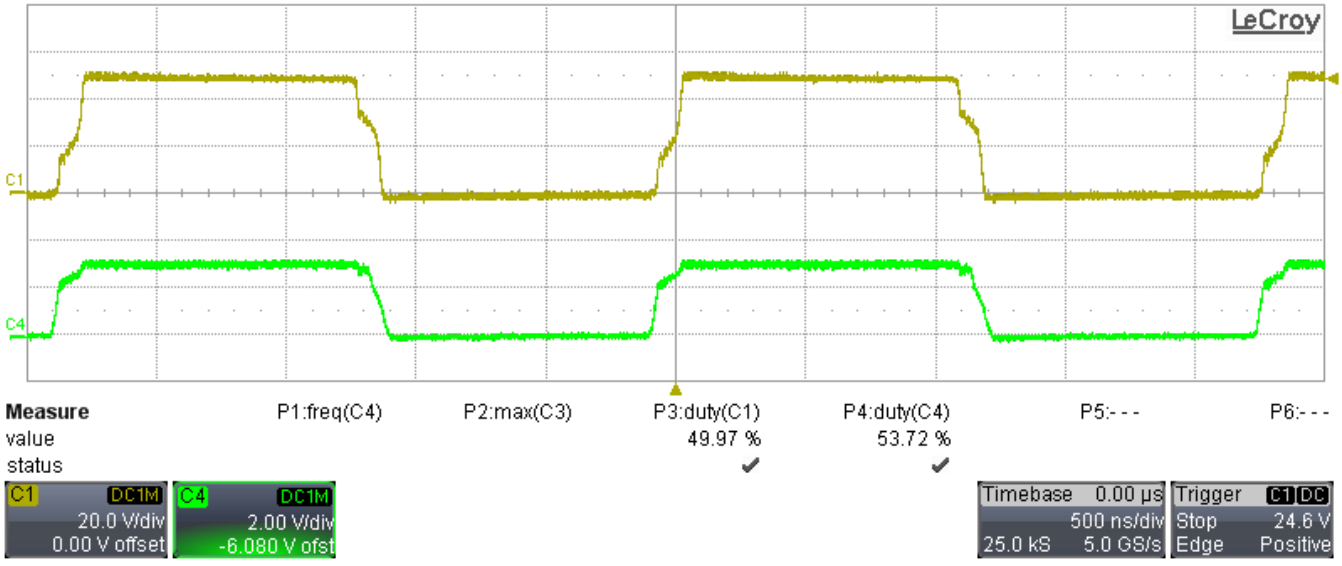
The board dimensions are 51.56 mm x 17.27 mm, height = 2 mm (without terminal blocks).

3 Waveforms

3.1 Switching

The switching waveforms have been measured by supplying the converter at 24 V in full load condition (120 mA and 350 mA), with waveforms referred to primary ground.

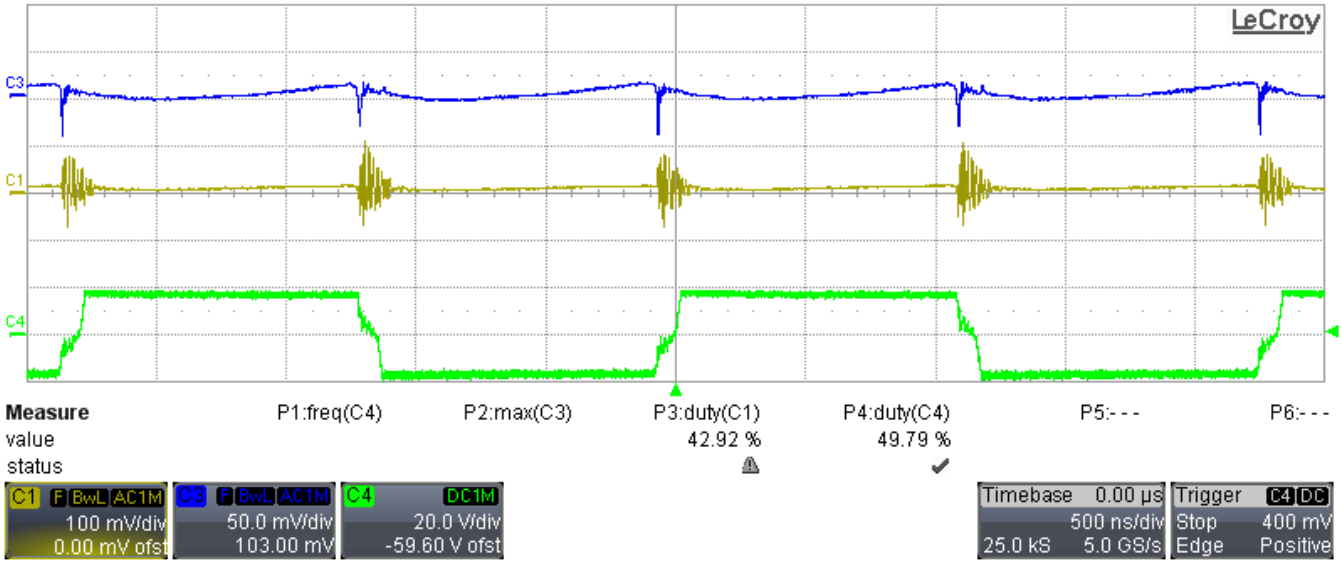
C1: Drain voltage of Q2 (20 V/div, 500 nsec/div, no BWL)
C4: Source voltage of Q2 (2 V/div, no BWL)



3.2 Output Voltage Ripples and D4 Anode Voltage

The output voltage ripples, and the switch-node of output diode D4 have been measured by supplying the converter at 24 V, in full-load condition.

C1: 15V output voltage (100 mV/div, 500 nsec/div, AC coupling, 20 MHz BWL)
C3: 5V output voltage (50 mV/div, AC coupling, 20 MHz BWL)
C4: D4-Anode voltage (20 V/div, 200 MHz BWL)

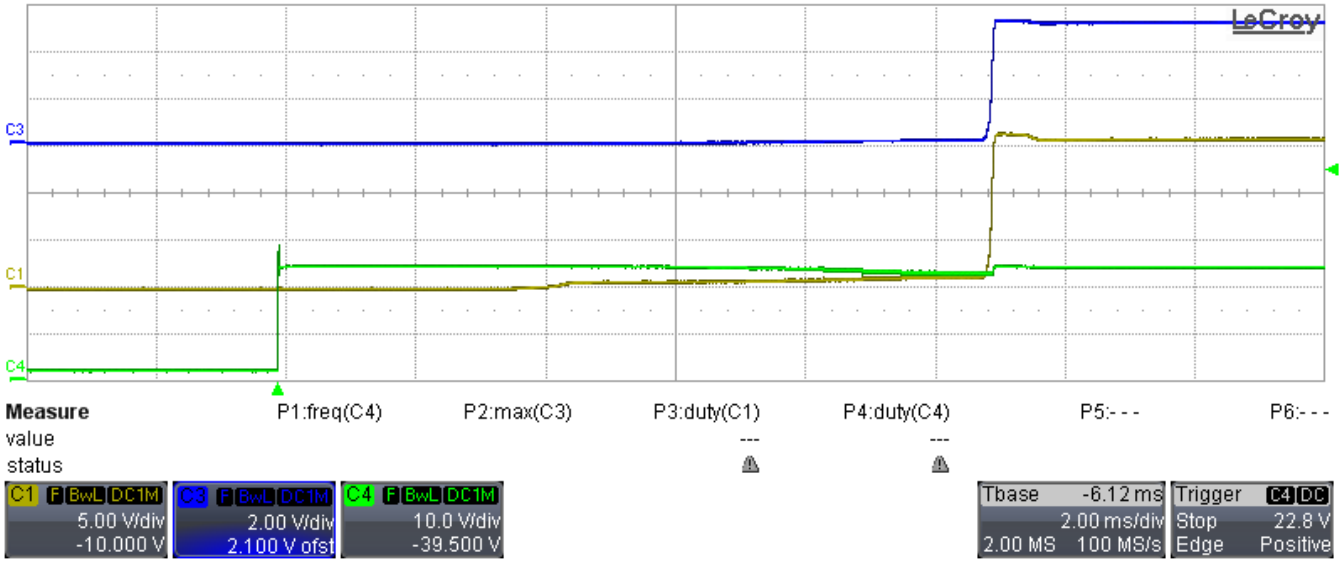


3.3 Startup

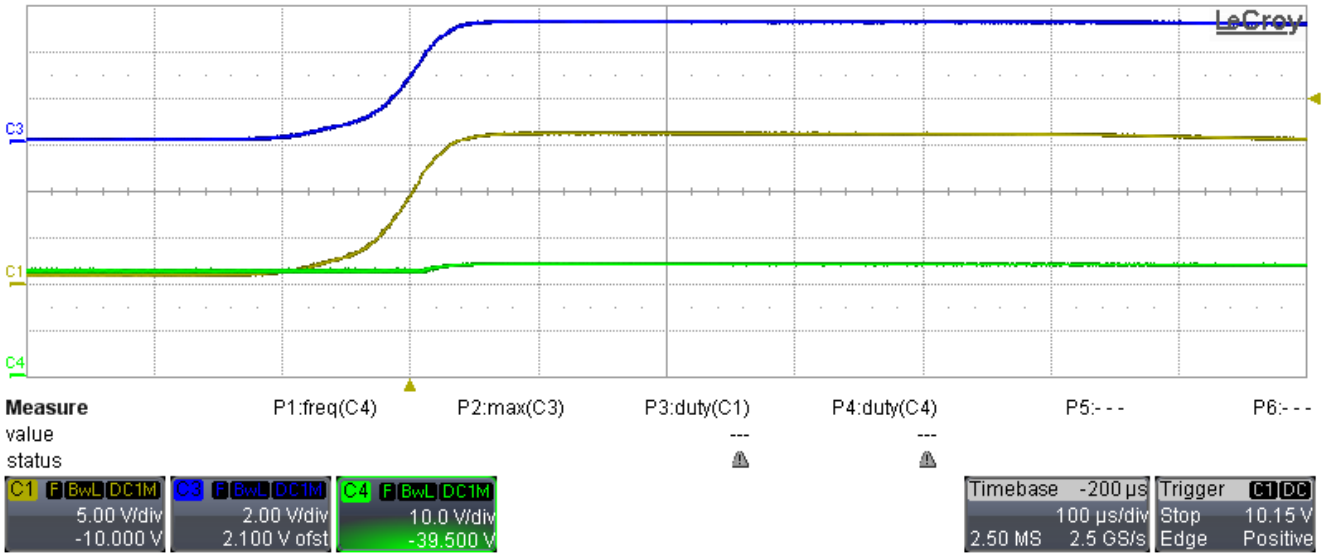
The behavior of the converter, showing Vin and output voltages, is shown below.
In these graphs, Vin has been applied by connecting the source to the power supply, when it was already on.

Conditions: Vin = 24 V, both outputs fully loaded.

C1: 15V output voltage (5 V/div, 2msec/div, 20 MHz BWL)
C3: 5V output voltage (2 V/div, 20 MHz BWL)
C4: Input voltage (10 V/div, 20 MHz BWL)

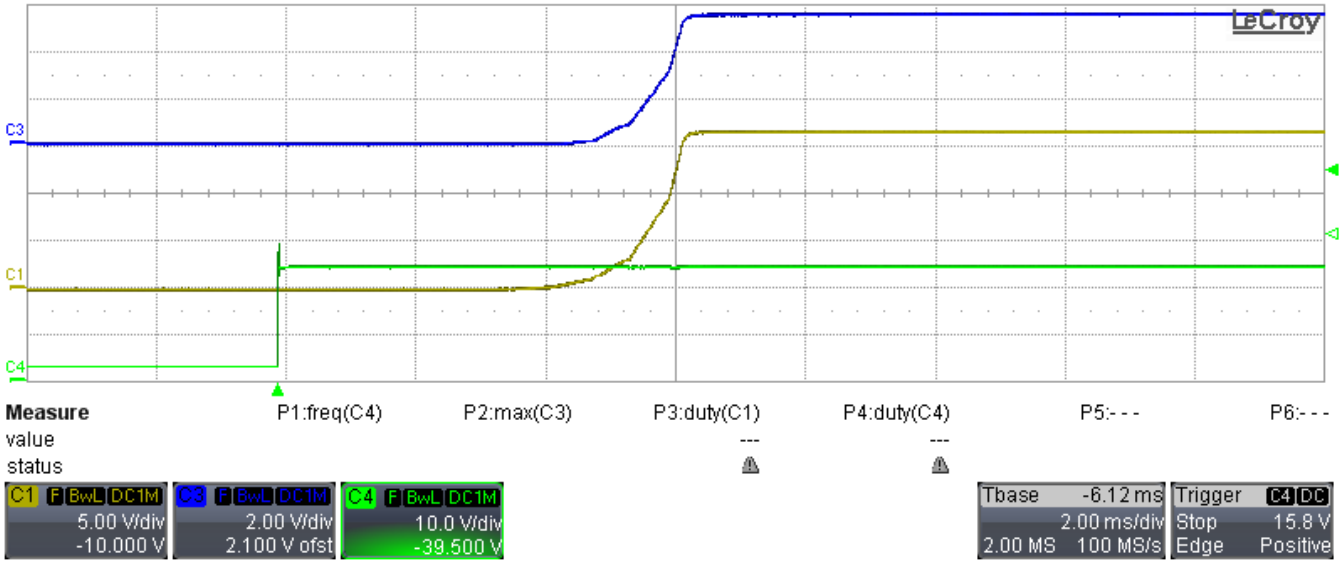


Same conditions like previous graph, but with smaller time scale (100 usec/div).



Conditions: Vin = 24 V, both outputs at zero load.

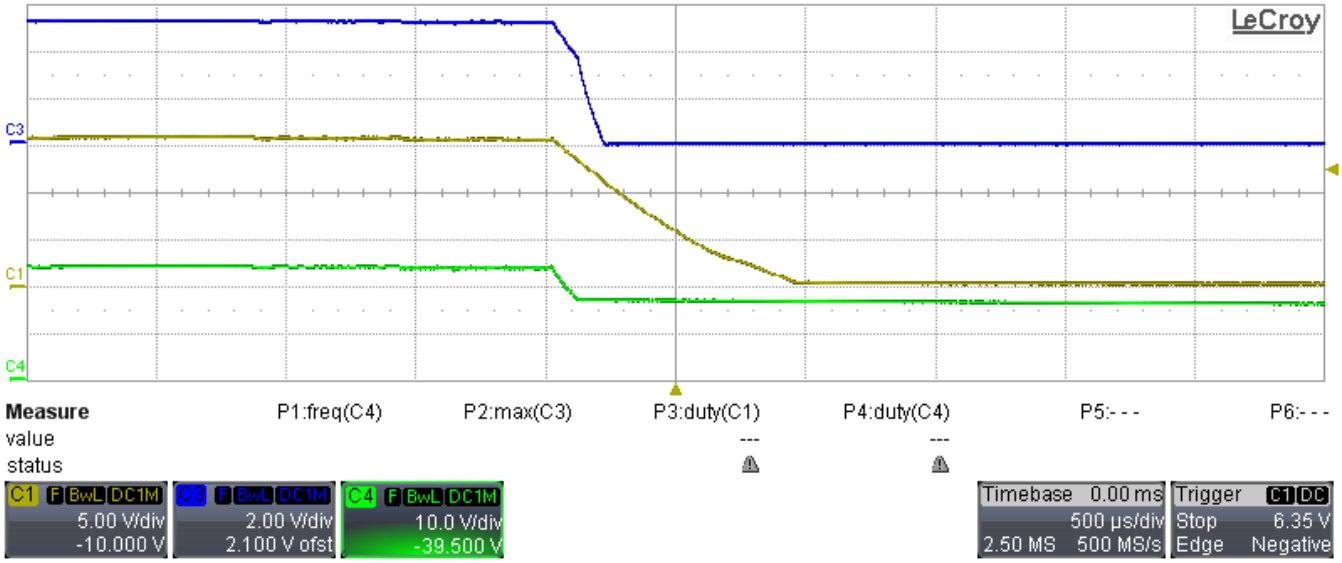
C1: 15V output voltage (5 V/div, 2msec/div, 20 MHz BWL)
C3: 5V output voltage (2 V/div, 20 MHz BWL)
C4: Input voltage (10 V/div, 20 MHz BWL)



3.4 Shut Down

The behavior of the converter, during shut down, has been measured and shown below.

Conditions: Vin = 24 V, both outputs fully loaded.
C1: 15V output voltage (5 V/div, 500 usec/div, 20 MHz BWL)
C3: 5V output voltage (2 V/div, 20 MHz BWL)
C4: Input voltage (10 V/div, 20 MHz BWL)



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