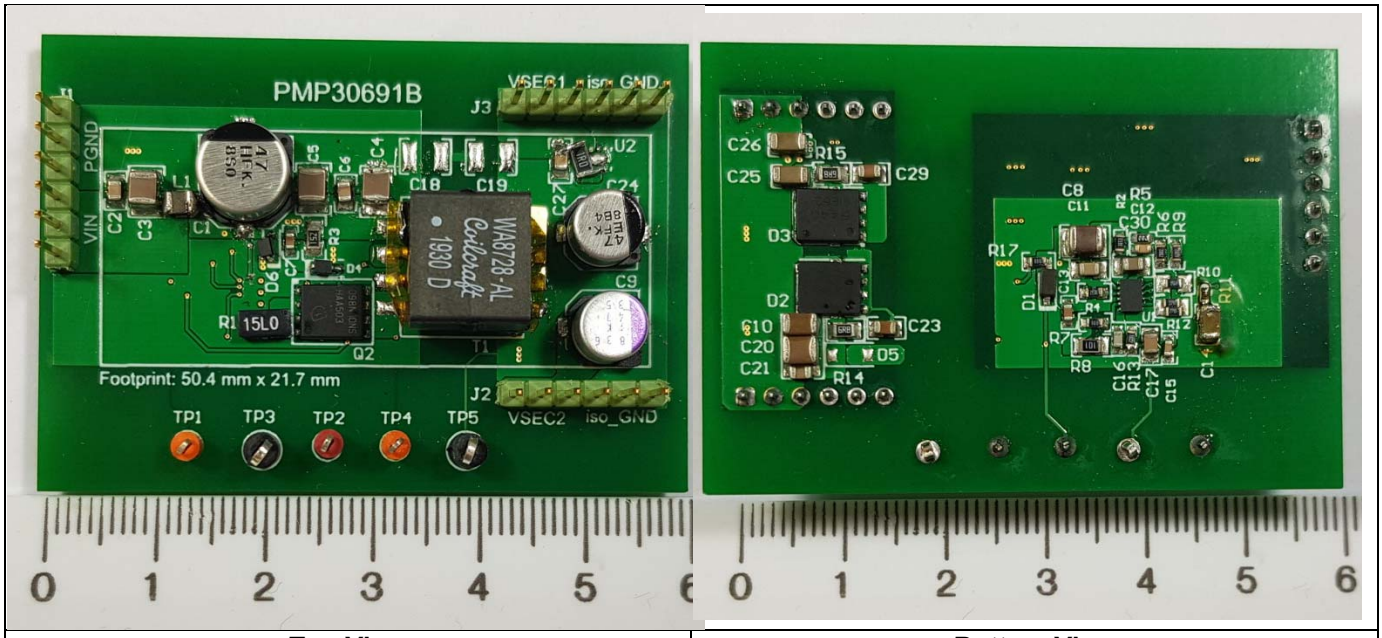
Test Report: PMP30691

Automotive 8-W Primary Side Regulated Flyback With Multioutput Rails Reference Design

Description

This reference design depicts the performance of an isolated primary side regulated Flyback using the LM5155-Q1 with a transformer from Coilcraft (WA8728-AL). The measurements were performed at room temperature.



Top View	Bottom View

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	Vin = 7 V…16 V, Vin(typ) = 12 V
Auxiliary Voltage and Current	Vaux = 8.5 V @ 20 mA
Output Voltage and Current	Vsec2 = 15 V @ 200 mA
Output Voltage and Current	Vsec1 = 8.5 V @ 500 mA
Switching Frequency	Fsw = 350 kHz
Isolation	Isolated
Transformer (Coilcraft – WA8728-AL))	Primary Inductance: Lmag = 2.7 uH Leakage Inductance: Lleak = 25 nH Winding Ratio: PRI : AUX : SEC1 : SEC2 = 1 : 2 : 1 : 2

1.2 Required Equipment*

- Power Supply: EA-PS-3032-10B
- Ohmic Load
- Frequency Response Analyzer: Venable Model 3120
- Digital Amperemeter

1.3 Considerations*

Switching Node Overshoot damped with RCD- Snubber (R3, C7, D4):

- *R3 = 1 kΩ, C7 = 4.7 nF → Vx = 60 % x Vsec*
- *Use shottky diode for D4 to mitigate reverse recovery ringing*

Chapter 2.3 shows the load regulation of the design – in general it is recommended to balance out the loading of both secondary winding on this topology.

Additionally it is recommended to have a minimum bias loading on both rails of 20 mA to prevent an overshoot as depicted in Chapter 2.3.

2 Testing and Results

The following graphs show the efficiency at nominal input voltage of 12 V.

2.1 Thermal Performance

The following graphs show the thermal performance of the reference design under full load conditions.

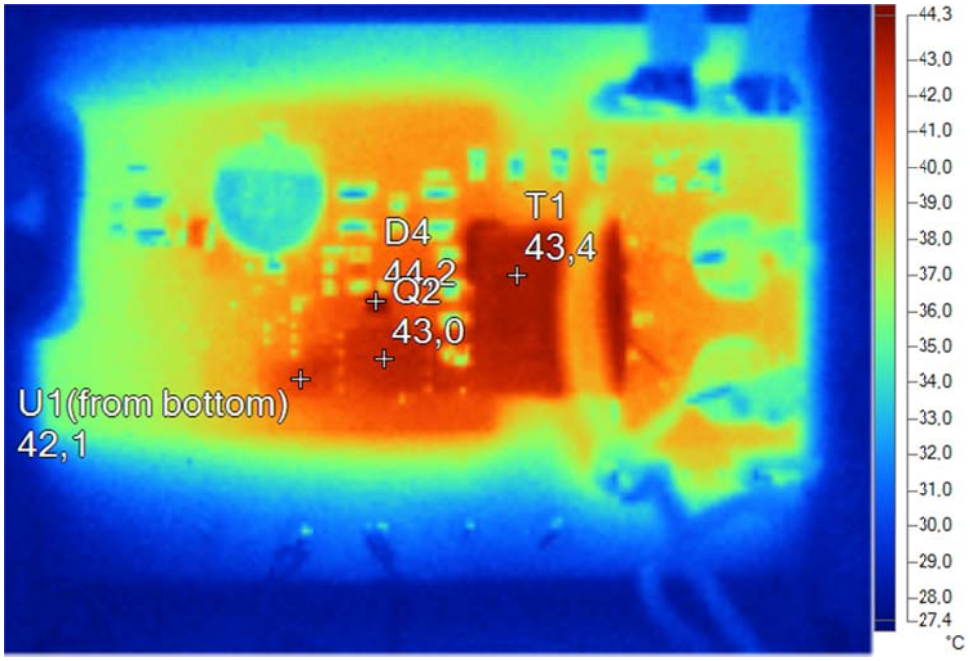


Figure 1: Thermal Image – Top Side

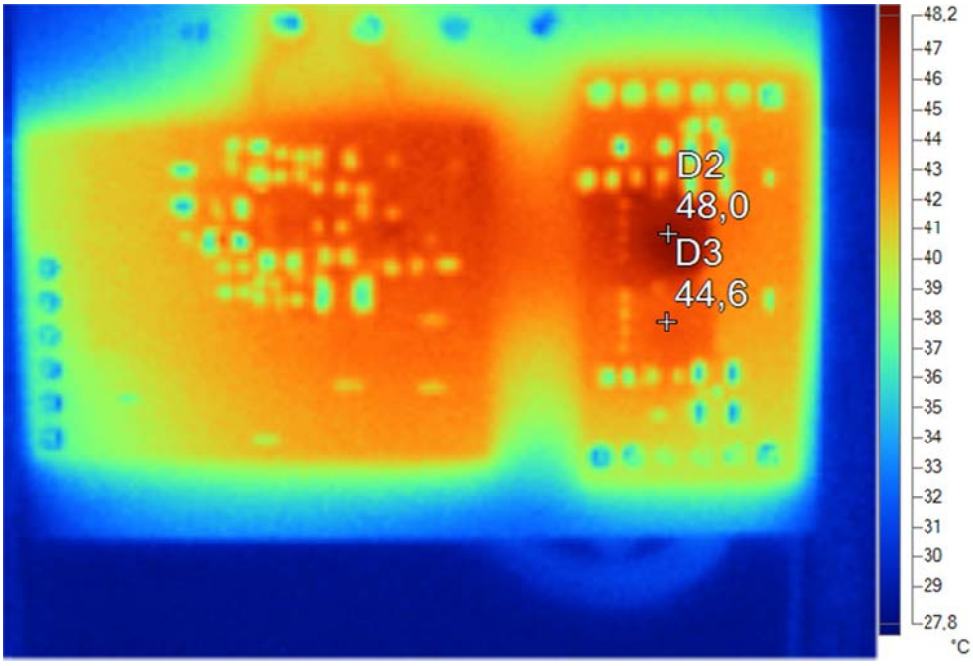


Figure 2: Thermal Image – Bottom Side

2.2 Efficiency Graphs

The following graphs show the efficiency at different input voltages.
For the purpose to show the impact of each secondary winding the below graphs are showing the efficiency at either constant loading on VSEC1 (8.5V) or constant loading of VSEC2 (15V)

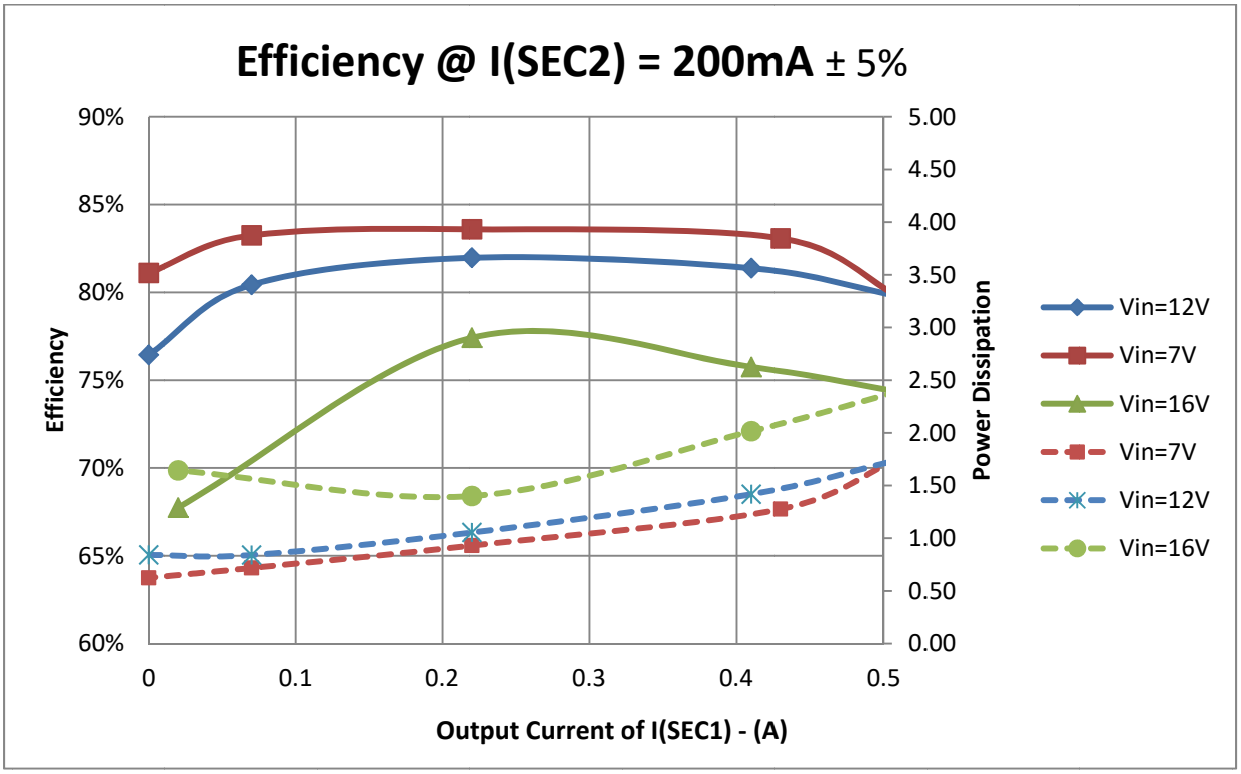


Figure 3: Efficiency Graph, constant loading on VSEC2 (8.5V)

Efficiency Data

Vin (V)	Iin (A)	Vaux (V)	Iaux (A)	Vsec1 (V)	Isec1 (A)	Vsec2 (V)	Isec2 (A)	Eff (1)	Pd (W)
7.00	1.24	8.60	0.02	12.81	0.22	7.70	0.51	0.80	1.76
7.00	1.08	8.60	0.02	12.89	0.21	7.90	0.43	0.83	1.28
7.05	0.80	8.60	0.02	13.03	0.21	8.26	0.22	0.84	0.93
7.09	0.60	8.60	0.02	13.12	0.21	8.55	0.07	0.83	0.72
7.10	0.47	8.60	0.02	13.12	0.19	8.78	0.00	0.81	0.62
12.06	0.30	8.60	0.02	13.18	0.19	8.80	0.00	0.76	0.84
12.00	0.36	8.59	0.02	13.15	0.20	8.59	0.07	0.80	0.84
11.98	0.49	8.59	0.02	13.10	0.21	8.32	0.22	0.82	1.05
11.95	0.64	8.59	0.02	13.00	0.21	8.00	0.41	0.81	1.42
11.94	0.72	8.60	0.02	12.94	0.21	7.82	0.51	0.80	1.74
16.02	0.58	8.61	0.02	13.01	0.21	7.87	0.51	0.74	2.39
16.04	0.52	8.61	0.02	13.06	0.22	8.05	0.41	0.76	2.01
16.06	0.39	8.60	0.02	13.11	0.21	8.34	0.22	0.77	1.40
16.07	0.32	8.60	0.02	13.92	0.22	8.78	0.02	0.68	1.64

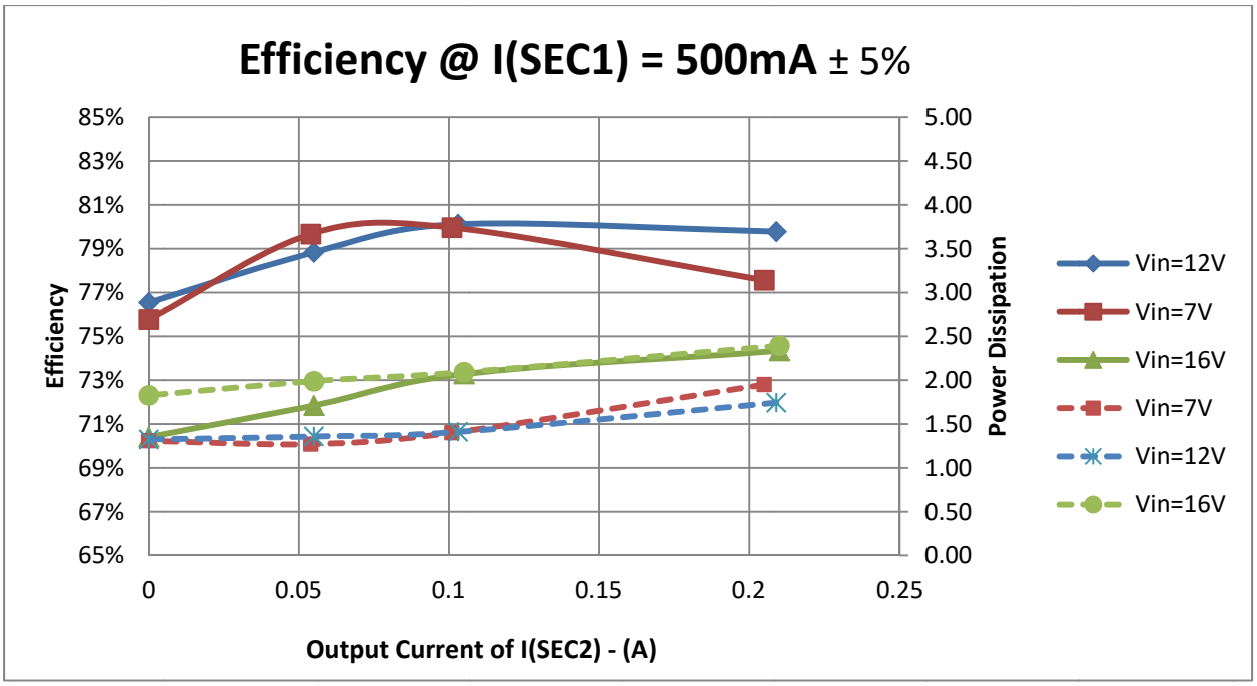


Figure 4: Efficiency graph, constant loading on VSEC1 (15-V)

Efficiency Data

Vin	Iin	Vaux	Iaux	Vsec1	Isec1	Vsec2	Isec2	Eff	Pd
7.00	1.24	8.60	0.02	12.81	0.21	7.70	0.51	0.78	1.95
7.00	1.00	8.59	0.02	12.92	0.10	7.73	0.53	0.80	1.40
7.02	0.89	8.59	0.02	12.99	0.05	7.72	0.53	0.80	1.27
7.04	0.77	8.60	0.02	23.89	0.00	7.66	0.51	0.76	1.31
11.94	0.72	8.60	0.02	12.94	0.21	7.82	0.51	0.80	1.74
12.00	0.59	8.59	0.02	13.03	0.10	7.84	0.53	0.80	1.41
12.01	0.53	8.59	0.02	13.12	0.06	7.83	0.53	0.79	1.36
12.03	0.47	8.59	0.02	16.57	0.00	7.80	0.53	0.77	1.32
16.02	0.58	8.61	0.02	13.01	0.21	7.87	0.51	0.74	2.39
16.04	0.49	8.59	0.02	13.10	0.11	7.88	0.53	0.73	2.09
16.05	0.44	8.59	0.02	13.15	0.06	7.86	0.53	0.72	1.99
16.03	0.39	8.59	0.02	14.27	0.00	7.85	0.53	0.70	1.83

2.3 Load Regulation

Load regulation measures the output voltage droop under varying load conditions.

Table 1: Load Regulation

VIN (V)	VAUX (V)	VSEC1 7.5V(V)	DEVIATION (%)	ISEC1 (MA)	VSEC2 15V(V)	DEVIATION (%)	ISEC2 (MA)
No Load Condition							
7.05	8.60	10.46	-23*	0	14.12	5.8	0
12.1	8.59	10.48	-23*	0	14.02	6.5	0
16.01	8.60	10.78	-26.8*	0	13.95	7.0	0
Cross Loading							
VSEC2 loaded at 200 mA							
7	8.60	7.7	9.4	510	12.81	14.6	205
7	8.60	7.9	7.1	430	12.89	14.1	208
7.05	8.60	8.26	2.8	220	13.03	13.1	210
7.09	8.59	8.55	-0.6	70	13.12	12.5	212
7.1	8.60	8.78	-3.3	0	13.19	12.1	193
12.06	8.59	8.8	-11.5	0	13.18	12.1	193
12	8.60	8.59	-3.5	70	13.15	12.1	213
11.98	8.59	8.32	-1.1	220	13.1	12.3	212
11.95	8.60	8	2.1	410	13	12.7	210
11.94	8.60	7.82	5.9	510	12.94	13.3	209
16.02	8.60	7.87	7.4	510	13.01	13.3	210
16.04	8.60	8.05	5.3	410	13.06	12.9	211
16.06	8.60	8.34	1.9	220	13.11	12.6	212
16.07	8.60	8.58	-0.9	70	13.12	12.5	212
VSEC1 loaded at 500 mA							
7.02	8.59	7.72	9.2	530	12.99	13.4	101
7	8.60	7.73	9.1	530	12.92	13.9	54
7.04	8.59	7.66	9.9	510	23.89	-59.3*	0
12.01	8.60	7.83	7.9	510	13.03	12.5	105
12	8.60	7.84	7.8	510	13.12	13.1	54
12.03	8.60	7.8	8.2	510	16.57	-10.5*	0
16.05	8.60	7.86	7.5	530	13.15	12.3	105
16.04	8.60	7.88	7.3	530	13.1	12.7	54
16.03	8.60	7.85	7.6	510	14.27	4.9	0
Full Load Condition							
7.05	8.59	8.16	4.2	510	12.58	16.1	400
12.1	8.60	8.2	3.6	510	12.64	15.7	400
16.01	8.60	8.34	1.9	510	12.83	14.4	400

* Consider to use TVS- Diode

3 Waveforms

3.1 Switching

Following graphs show the switching node on the primary side of the power supply at an input voltage of 7 V, 12 V and 16 V and full load on both rails.

Whereas,

CH1: Switching Node on Primary Side (5 V/DIV)
Timescale: 2 us/DIV

The maximum overshoot at Vin = 7 V and both secondary windings loaded at maximum results in a total value of 17.7 V.

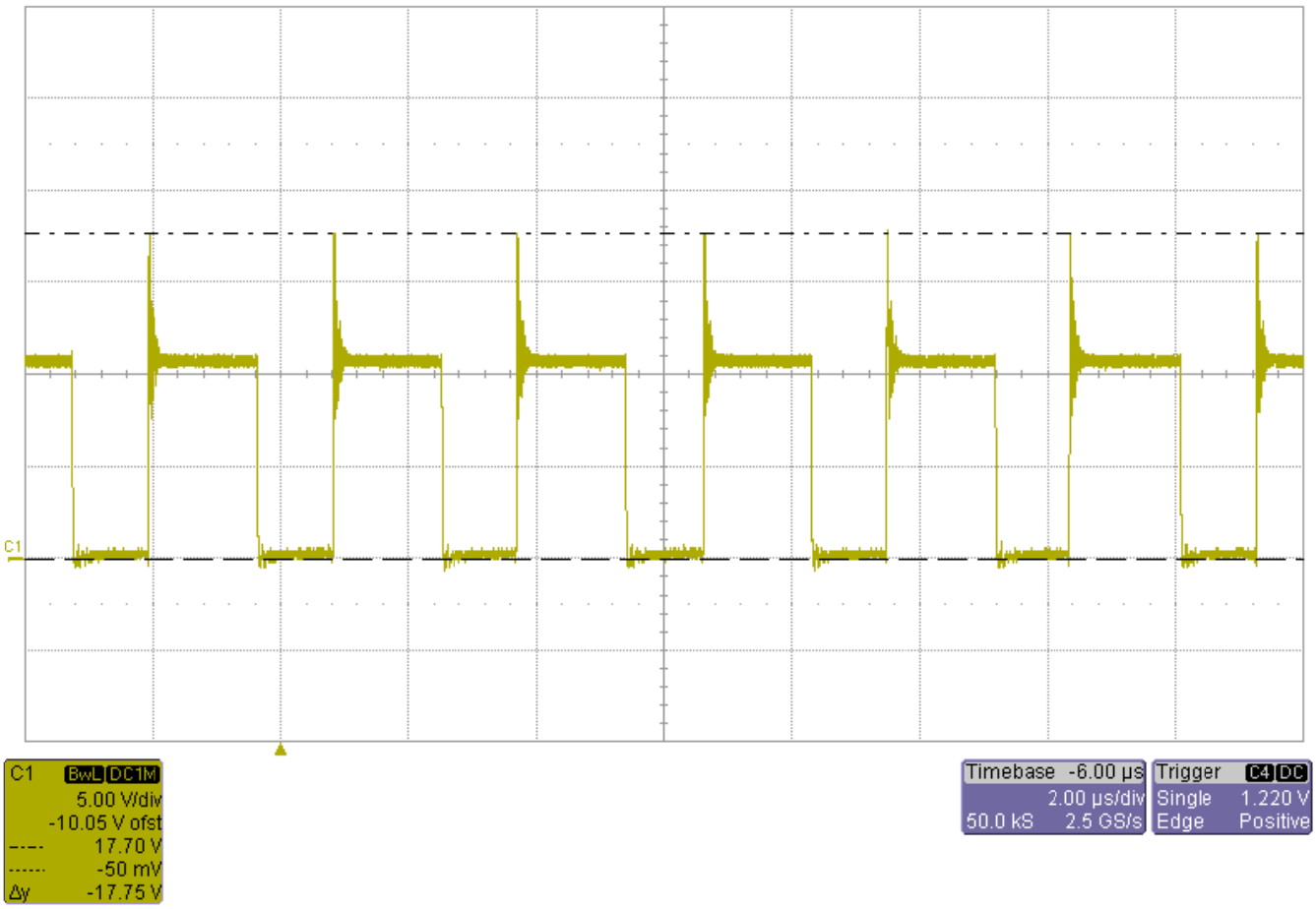


Figure 5: Switching Node on Primary Side, Vin = 7 V, both secondary windings fully loaded

The maximum overshoot at Vin = 12 V and both secondary windings loaded at maximum results in a total value of 20 V.

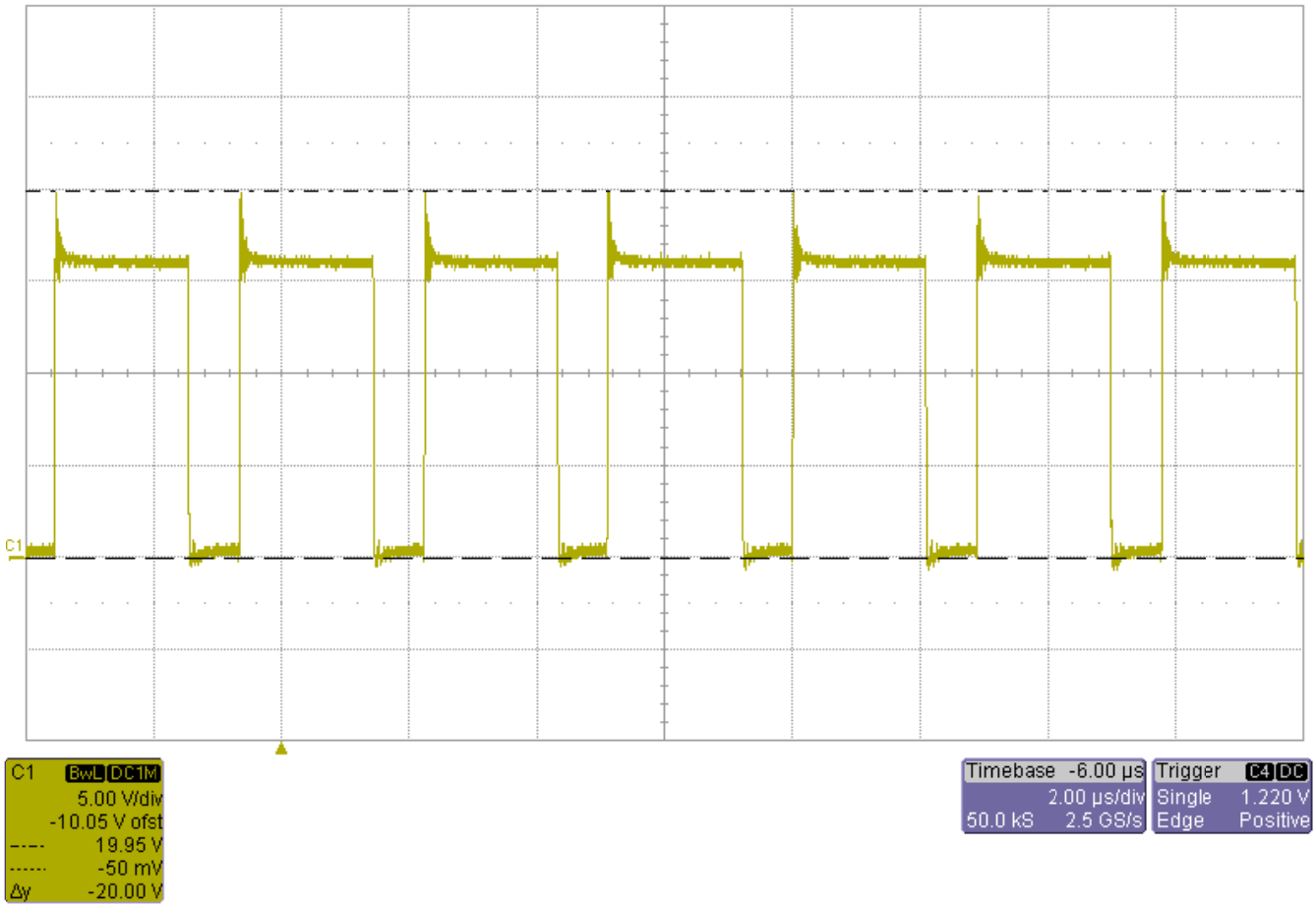


Figure 6: Switching Node on Primary Side, Vin = 12 V, both secondary windings fully loaded

3.2 Output Voltage Ripple

The following graphs show the output voltage ripple at an input voltage of 12 V and maximum loading on both rails.

Whereas,

CH1: Output Voltage Ripple of VSEC2 (AC coupled, 200 mV/DIV)
CH3: Output Voltage Ripple of VSEC1 (AC coupled, 200 mV/DIV)

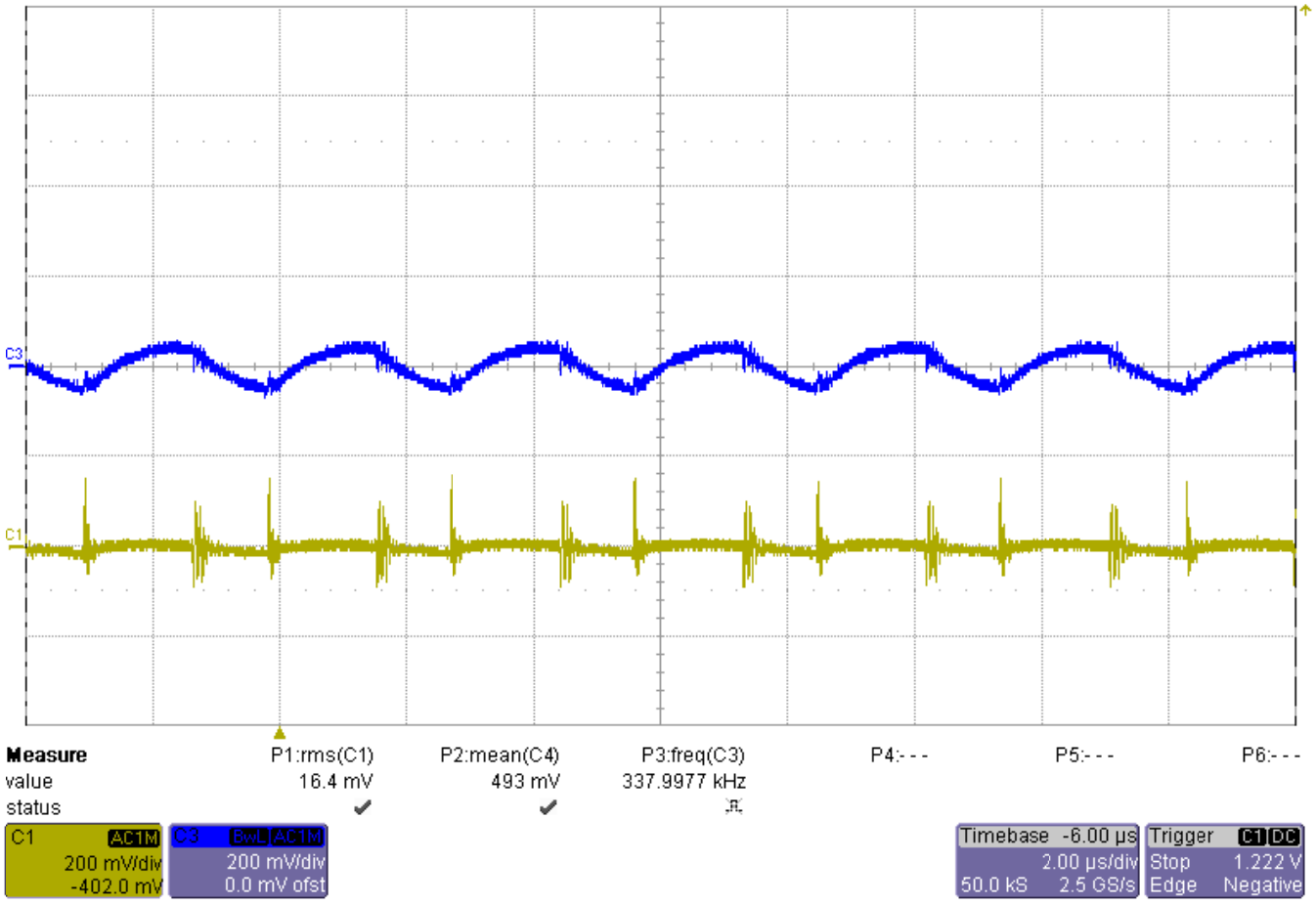


Figure 7: Output Voltage Ripple, Vin = 7 V

The maximum voltage ripple of VSEC2 is at Vpp = 120 mV which corresponds to 0.8 % (typical).

The maximum voltage ripple of VSEC1 is at Vpp = 50 mV which corresponds to 1 % (typical).

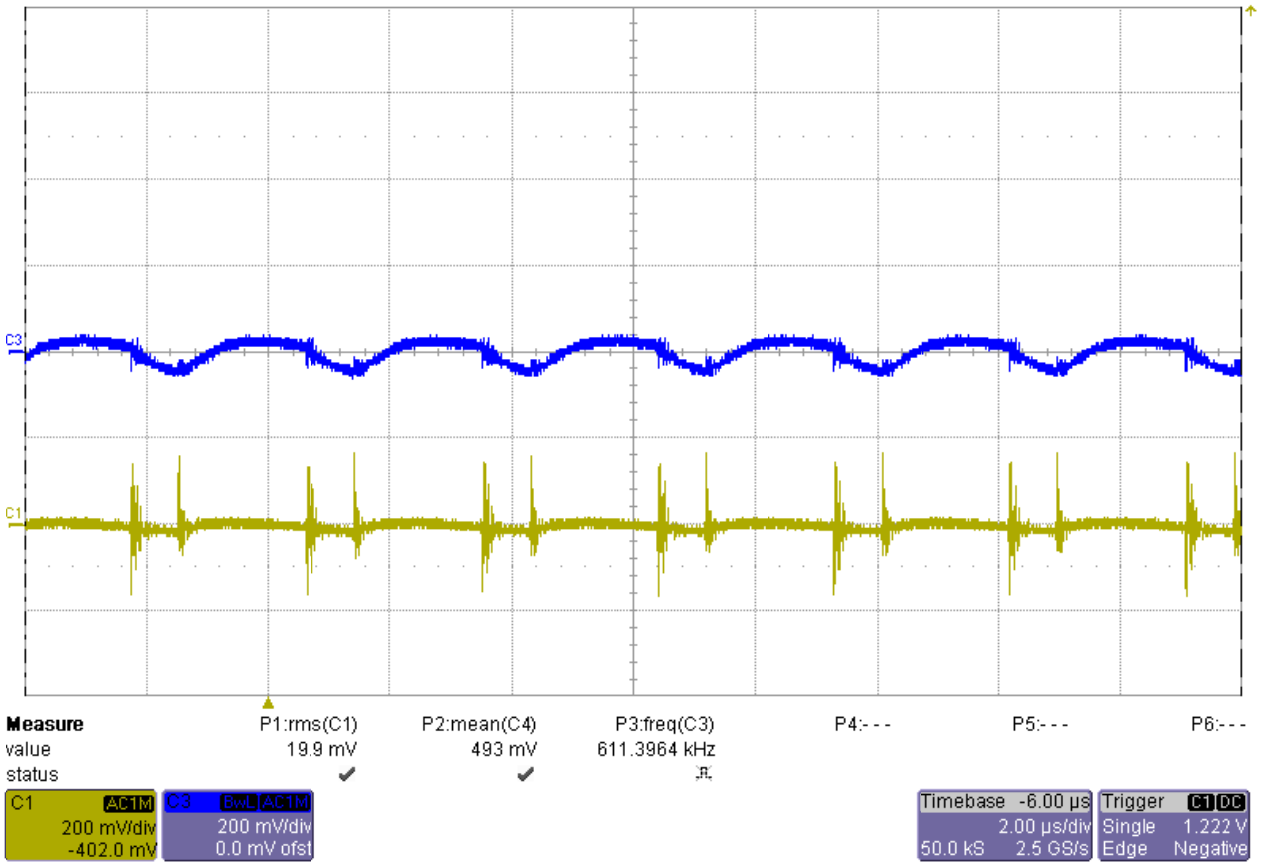


Figure 8: Output Voltage Ripple, Vin = 12 V

The maximum voltage ripple of VSEC2 is at Vpp = 80 mV which corresponds to 0.54 % (typical).

The maximum voltage ripple of VSEC1 is at Vpp = 20 mV which corresponds to 0.4 % (typical).

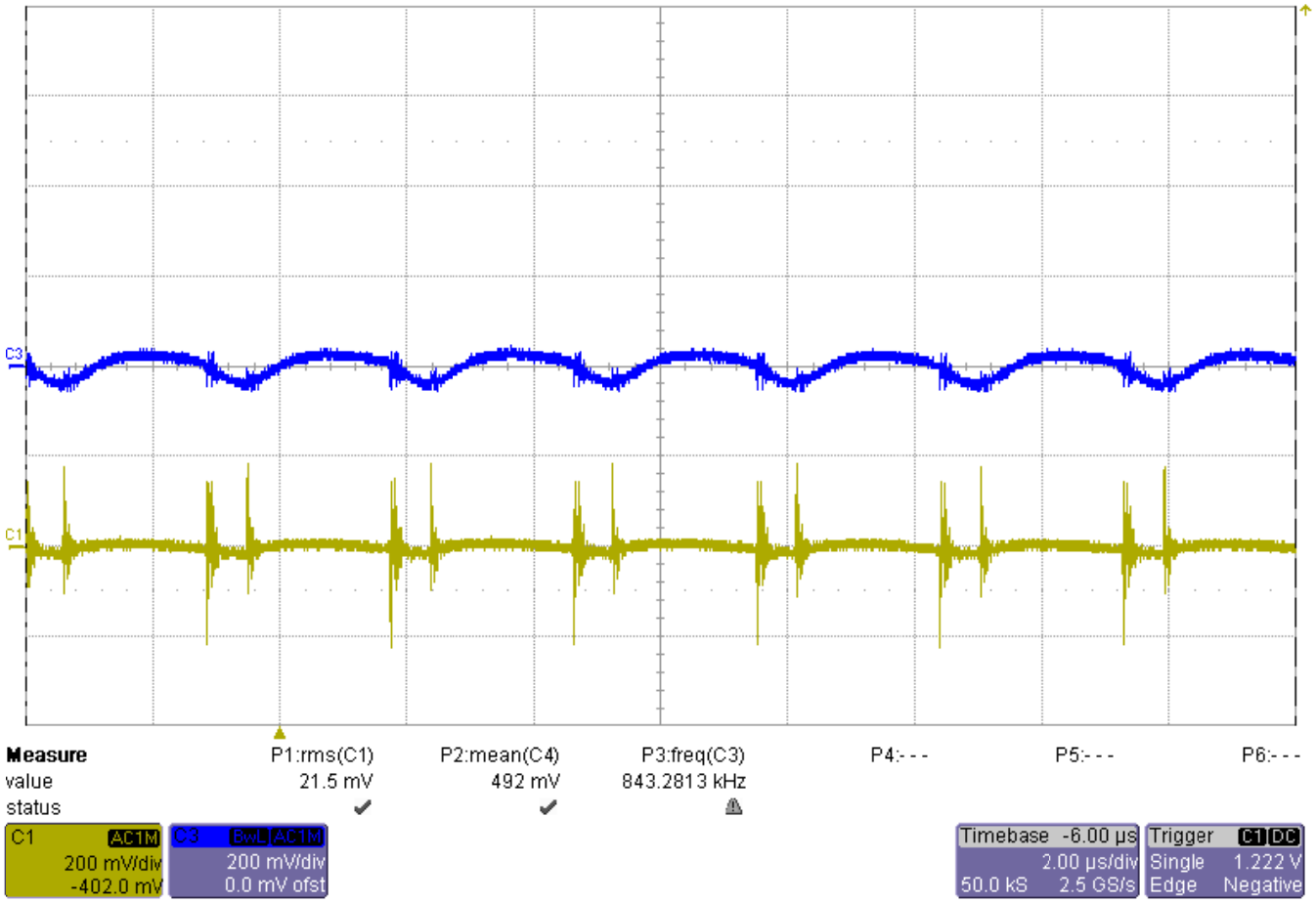


Figure 9: Output Voltage Ripple, Vin = 16 V

The maximum voltage ripple of VSEC2 is at Vpp = 80 mV which corresponds to 0.54 % (typical).

The maximum voltage ripple of VSEC1 is at Vpp = 20 mV which corresponds to 0.4 % (typical).

3.3 Bode Plot

Following graph show the small signal response of the auxiliary winding at an input voltage of 12 V.

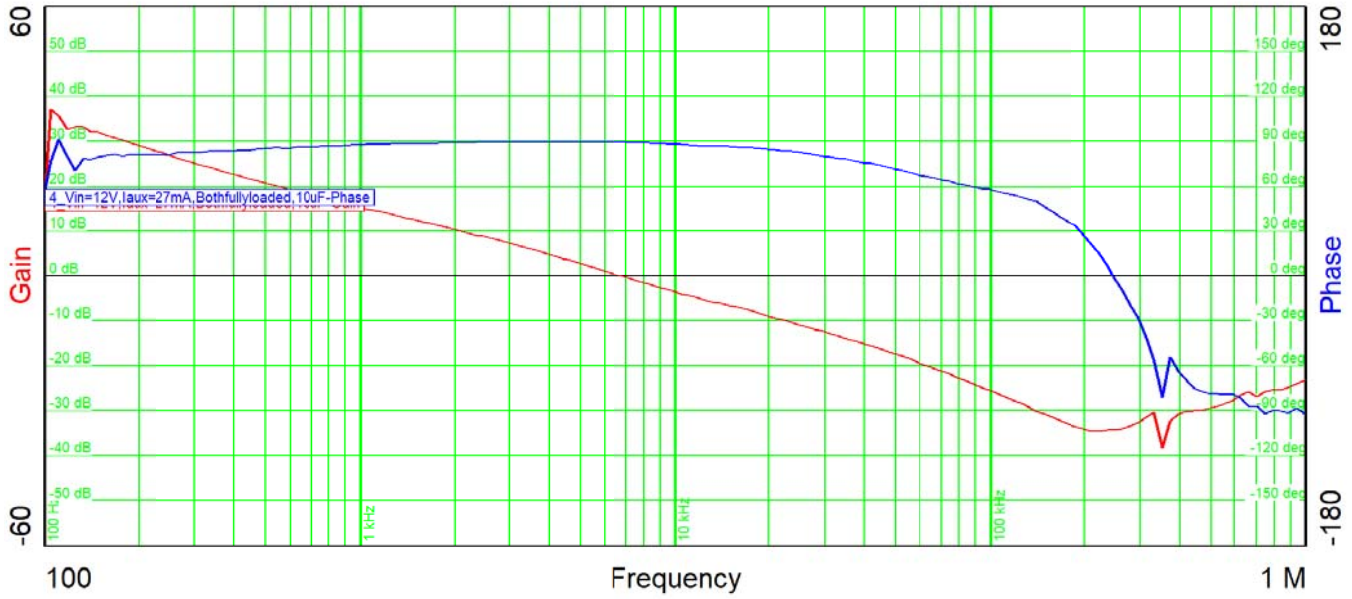


Figure 10: Bode Plot of Vaux at nominal input voltage of 12 V

Input Voltage	Crossover Frequency	Phase Margin	Slope 20dB/decade	Crossover Frequency	Gain Margin	Slope 20dB/decade
12 V	**6.7 kHz**	**89.3 deg**	**-1.1**	**246.7 kHz**	**-34.4 dB**	**-0.14**

3.4 Load Transients

3.4.1 Load Transient – VSEC1 (8.5V), VSEC2 (15V) at constant load

The following graphs show the load step response of the 15-V rail. The load step response was performed at

- Falling Slope: 500 mA → 250 mA at a slew rate of 25 mA/us
- Rising Slope: 250 mA → 500 mA at a slew rate of 25 mA/us

Whereas:
CH3: Output Voltage (AC, coupled, 200 mV/DIV)
CH4: Output Current (200 mA/DIV)
Time Scale: 20 ms/DIV

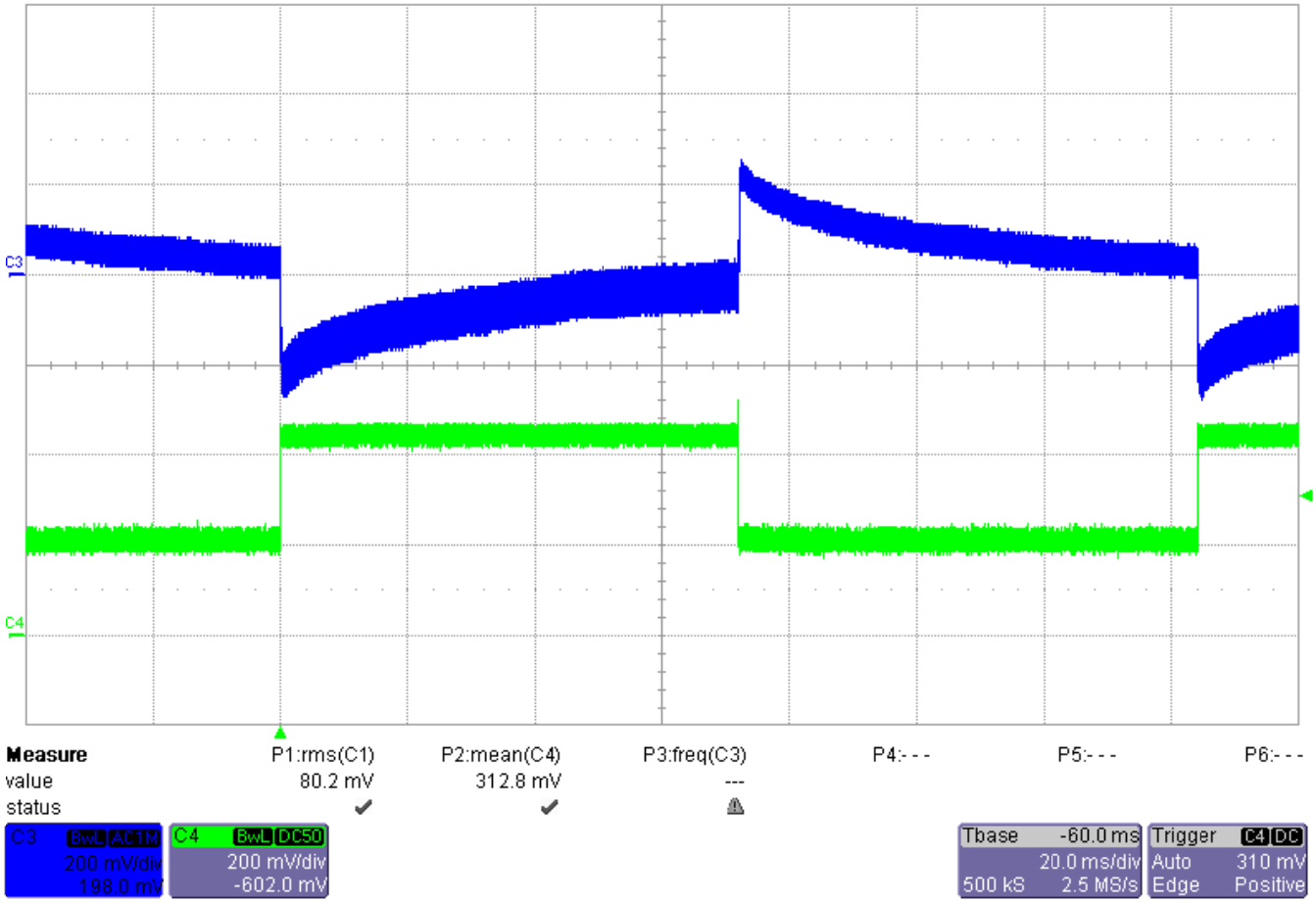


Figure 11: Load Step Response VSEC1 – Vin = 7 V, VSEC2 (15-V) loaded at 200 mA

At a positive load step of 250 mA → 500 mA the maximum output voltage deviation is at 240 mV which corresponds to 4.8% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 500 mA → 250 mA the maximum output voltage deviation is at 250 mV which corresponds to 5 % (typical). This is the case when VSEC2 is loaded at 200 mA.

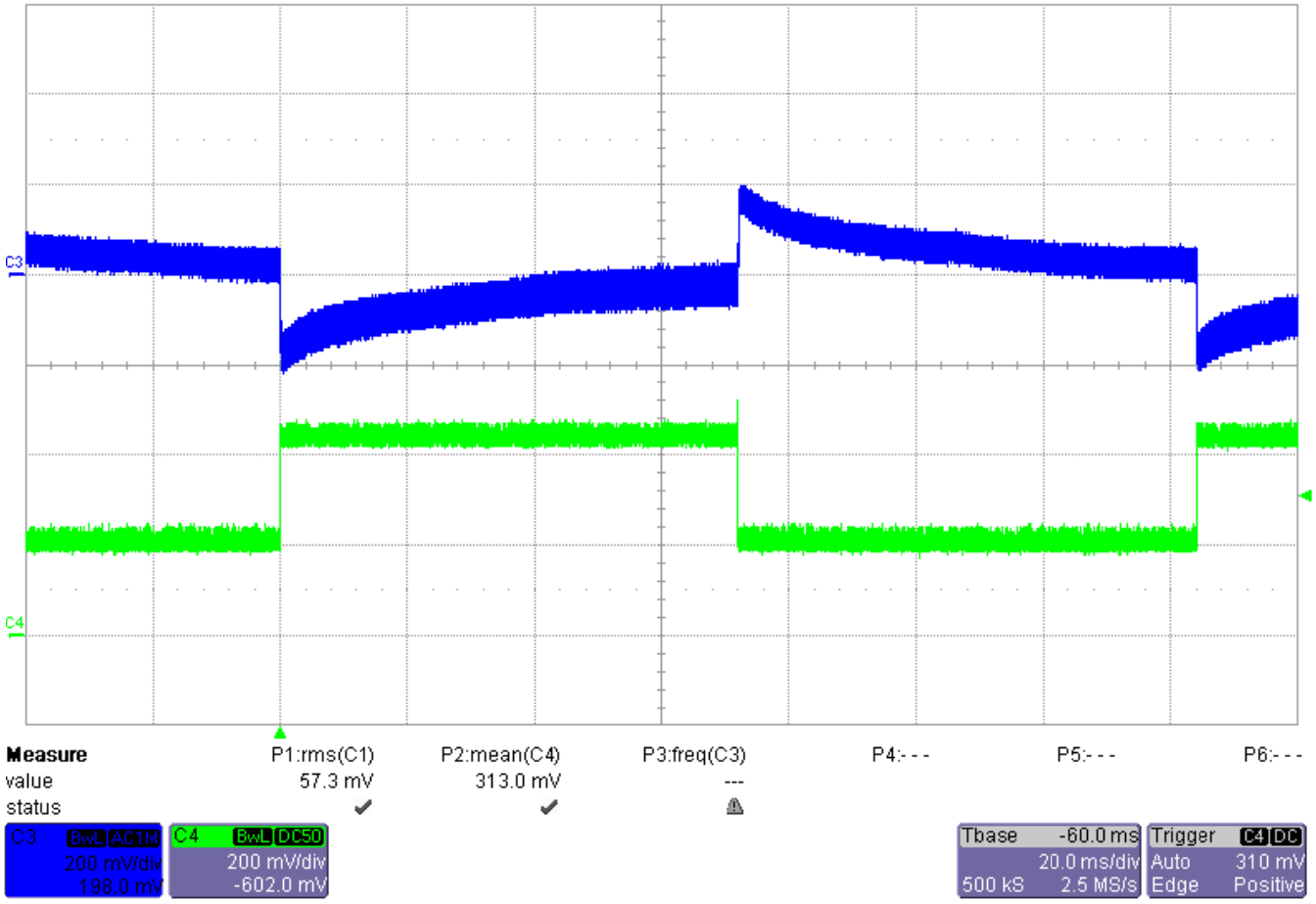


Figure 12: Load Step Response VSEC1 – Vin = 12 V, VSEC2 (15-V) loaded at 200 mA

At a positive load step of 250 mA → 500 mA the maximum output voltage deviation is at 210 mV which corresponds to 4.2% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 500 mA → 250 mA the maximum output voltage deviation is at 200 mV which corresponds to 4 % (typical). This is the case when VSEC2 is loaded at 200 mA.

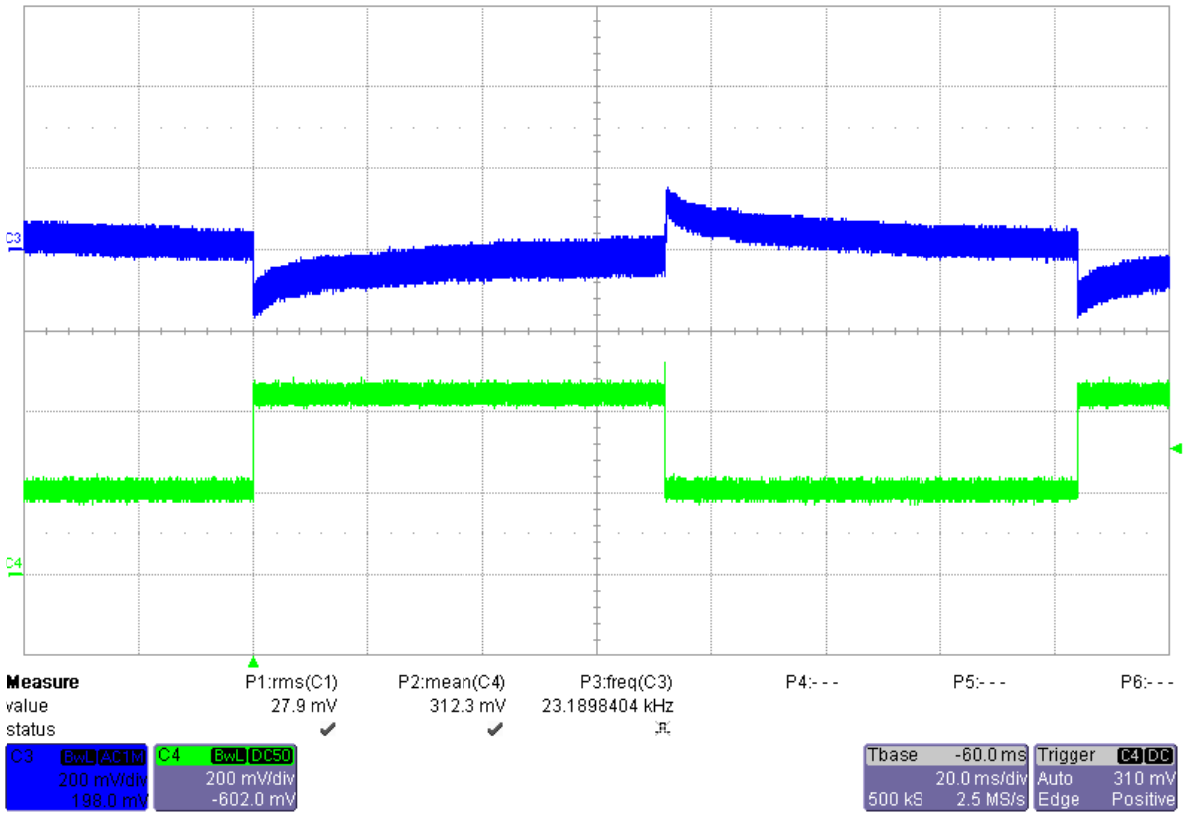


Figure 13: Load Step Response VSEC1 – Vin = 16 V, VSEC2 (15-V) loaded at 200 mA

At a positive load step of 250 mA → 500 mA the maximum output voltage deviation is at 180 mV which corresponds to 3.6% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 500 mA → 250 mA the maximum output voltage deviation is at 180 mV which corresponds to 3.6 % (typical). This is the case when VSEC2 is loaded at 200 mA.

3.4.2 Load Transient – VSEC2 (15V), VSEC1 (8.5V) at constant load

The following graphs show the load step response of the 5-V rail. The load step response was performed at

- Falling Slope: 500 mA → 250 mA at a slew rate of 25 mA/us
- Rising Slope: 250 mA → 500 mA at a slew rate of 25 mA/us

Whereas:
CH3: Output Voltage (AC, coupled, 200 mV/DIV)
CH4: Output Current (200 mA/DIV)
Time Scale: 20 ms/DIV

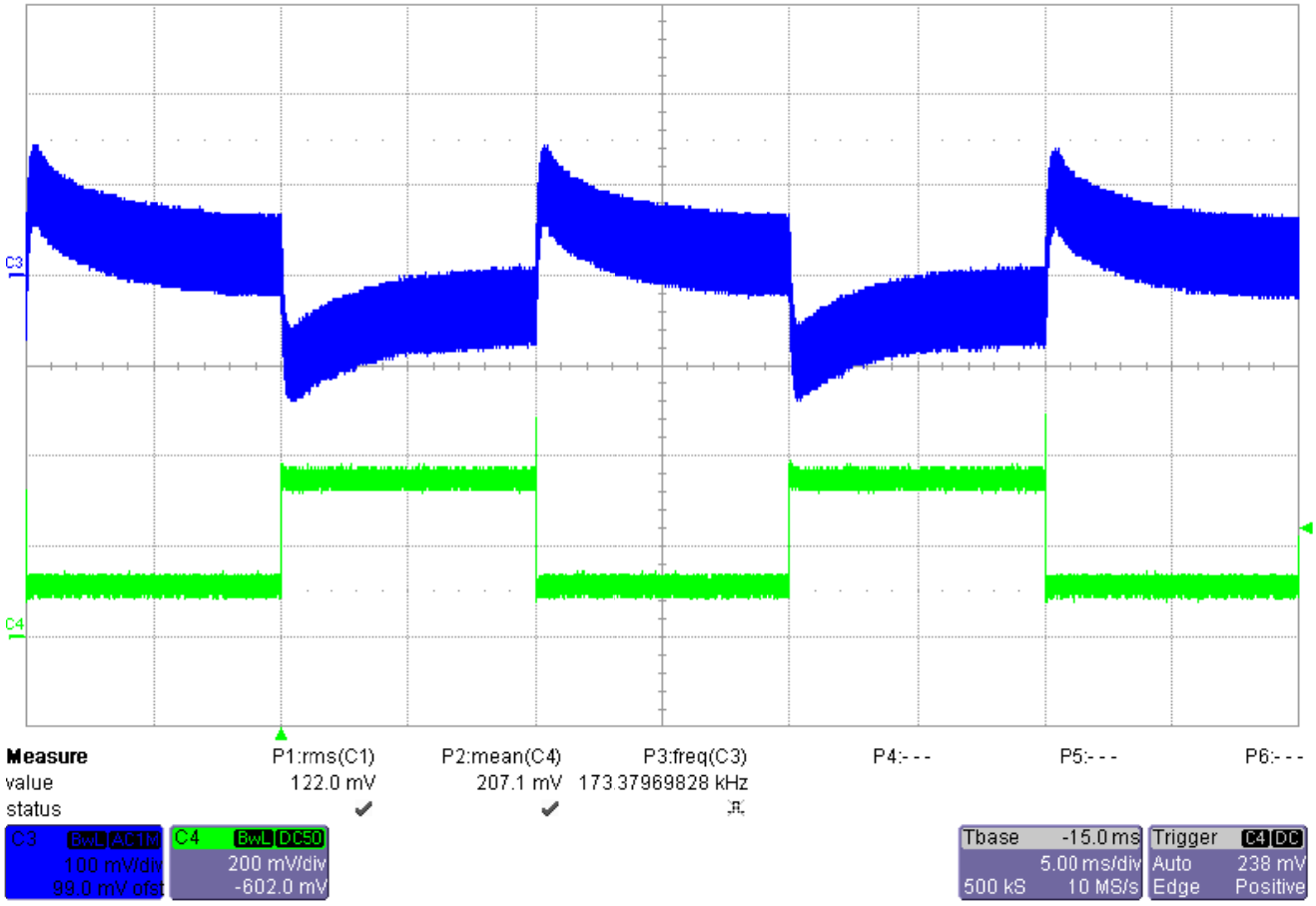


Figure 14: Load Step Response VSEC2 – Vin = 7 V, VSEC1 (8.5-V) loaded at 500 mA

At a positive load step of 100 mA → 300 mA the maximum output voltage deviation is at 150 mV which corresponds to 1% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 100 mA → 300 mA the maximum output voltage deviation is at 140 mV which corresponds to 0.9 % (typical). This is the case when VSEC2 is loaded at 200 mA.

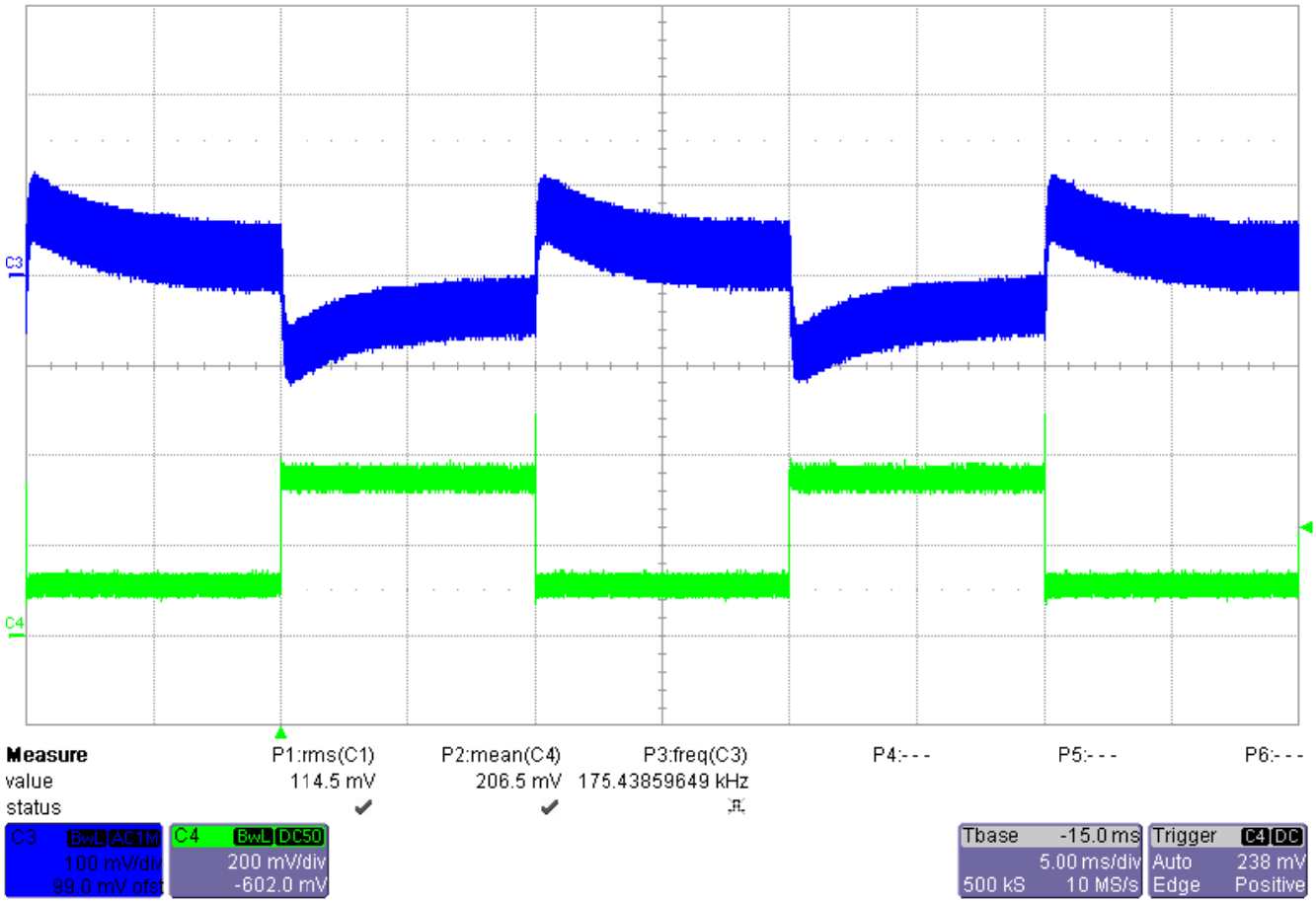


Figure 15: Load Step Response VSEC2 – Vin = 12 V, VSEC1 (8.5-V) loaded at 500 mA

At a positive load step of 100 mA → 300 mA the maximum output voltage deviation is at 110 mV which corresponds to 0.7% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 100 mA → 300 mA the maximum output voltage deviation is at 100 mV which corresponds to 0.67 % (typical). This is the case when VSEC2 is loaded at 200 mA.

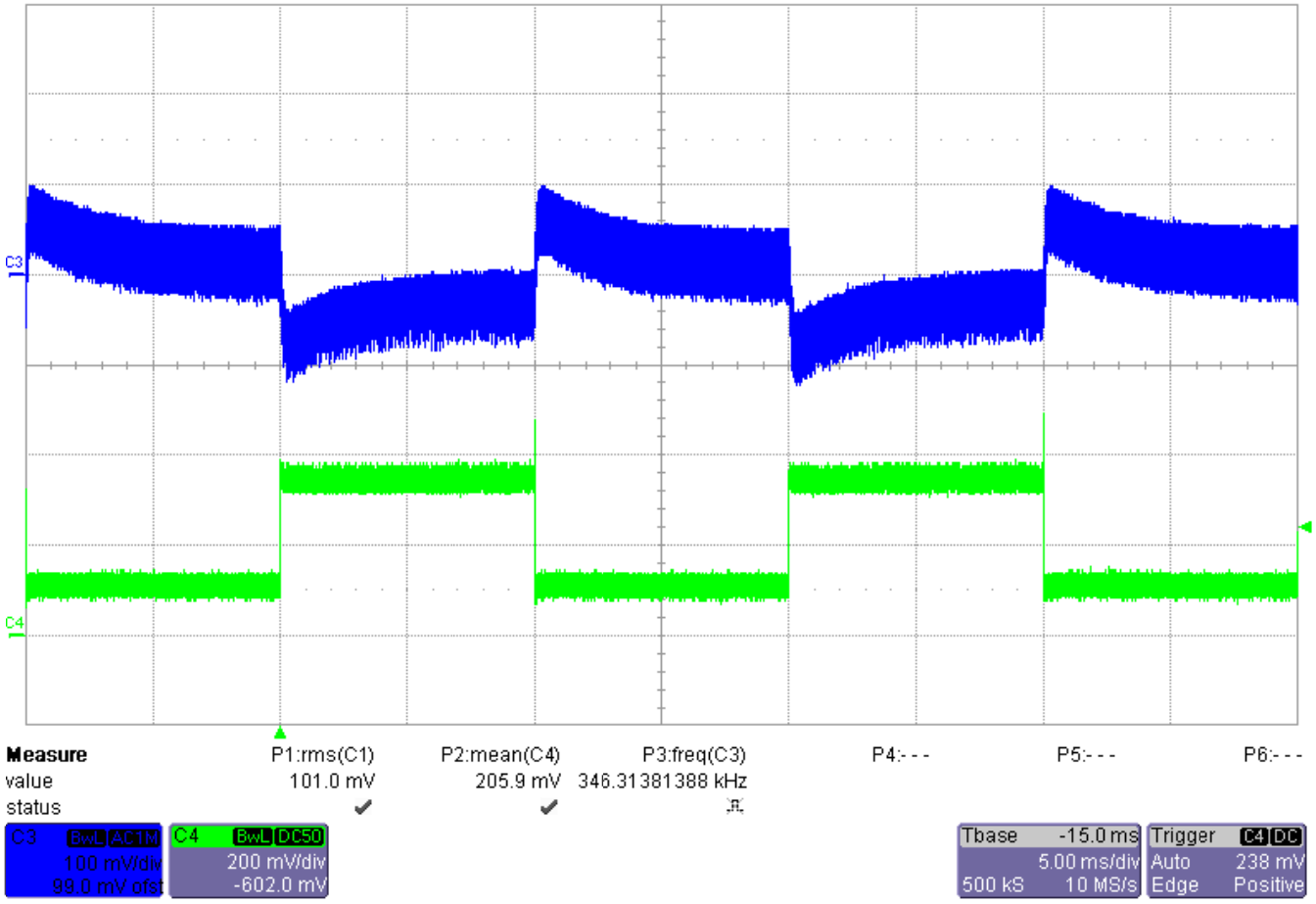


Figure 16: Load Step Response VSEC2 – Vin = 16 V, VSEC1 (8.5-V) loaded at 500 mA

At a positive load step of 100 mA → 300 mA the maximum output voltage deviation is at 100 mV which corresponds to 0.67% (typical). This is the case when VSEC2 is loaded at 200 mA.

At a negative load step of 100 mA → 300 mA the maximum output voltage deviation is at 100 mV which corresponds to 0.67 % (typical). This is the case when VSEC2 is loaded at 200 mA.

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