Test Report: PMP22288

15-W Flyback Reference Design for Automotive Inverter Power

Description:

This reference design uses the UCC28730-Q1 flyback controller to produce an isolated 15-V output. The design is capable of 0.33-A from a 40-V to 250-Vdc input and 1-A from a 250-V to 550-Vdc input. This power system is designed for an inverter bias supply application and is an automotive-qualified solution.

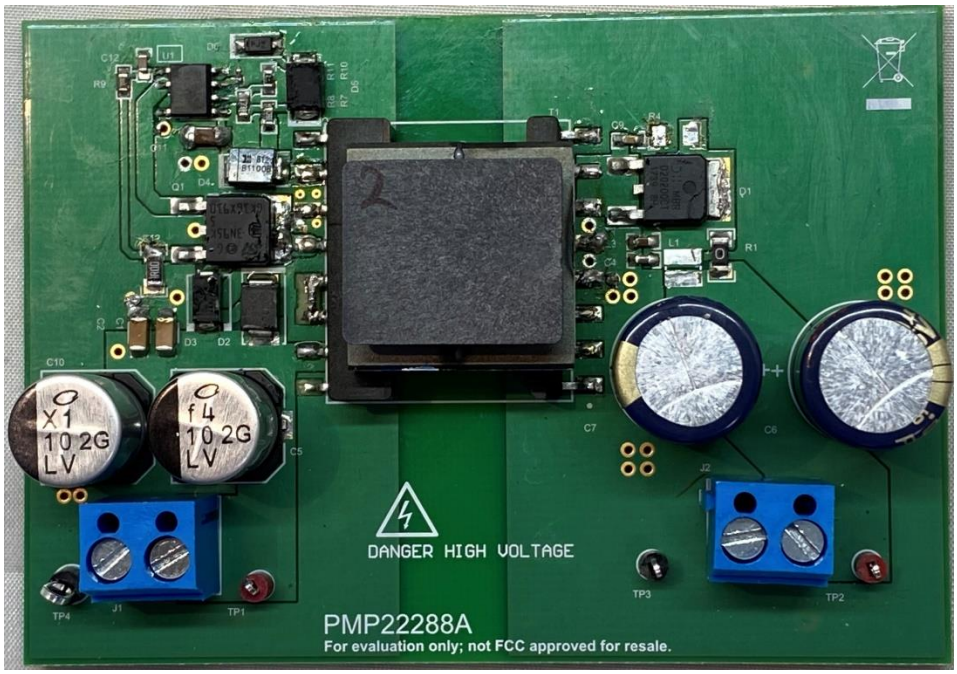

Figure 1. Board Top

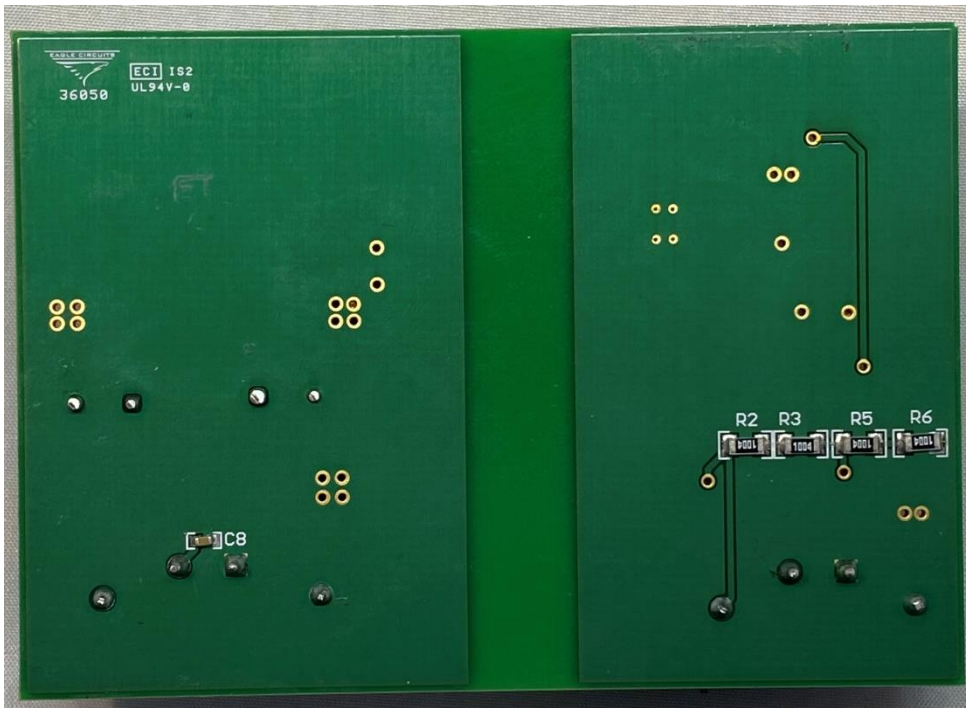

Figure 2. Board Bottom

1 Flyback Stage

1.1 Test Prerequisites

1.1.1 Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	40 Vdc – 550 Vdc
Output Voltage	15 V
Output Current	0.33A max for Vin = 40-250V 1A max for Vin = 250-550V
Switching Frequency	70 kHz

1.1.2 Considerations

1) For all tests an electronic load was used.
2) The circuit needs a pre-load of 0.04 A to start up.

1.2 Testing and Results

1.2.1 Efficiency Graphs

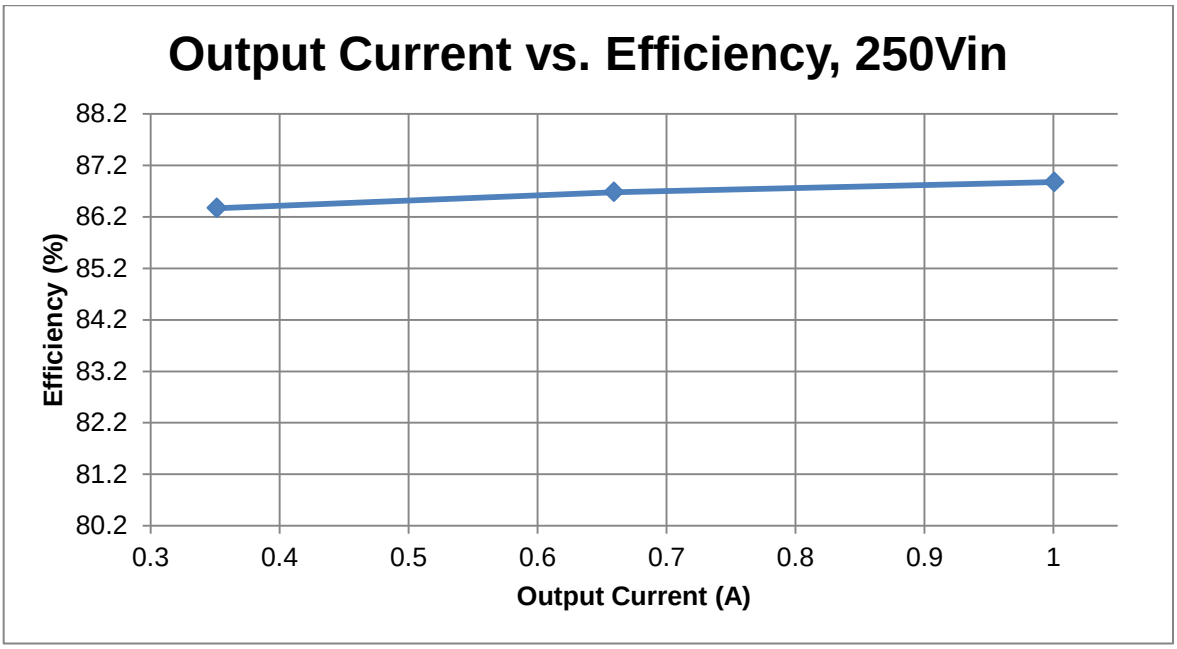

Figure 3. Efficiency for 250 Vdc input

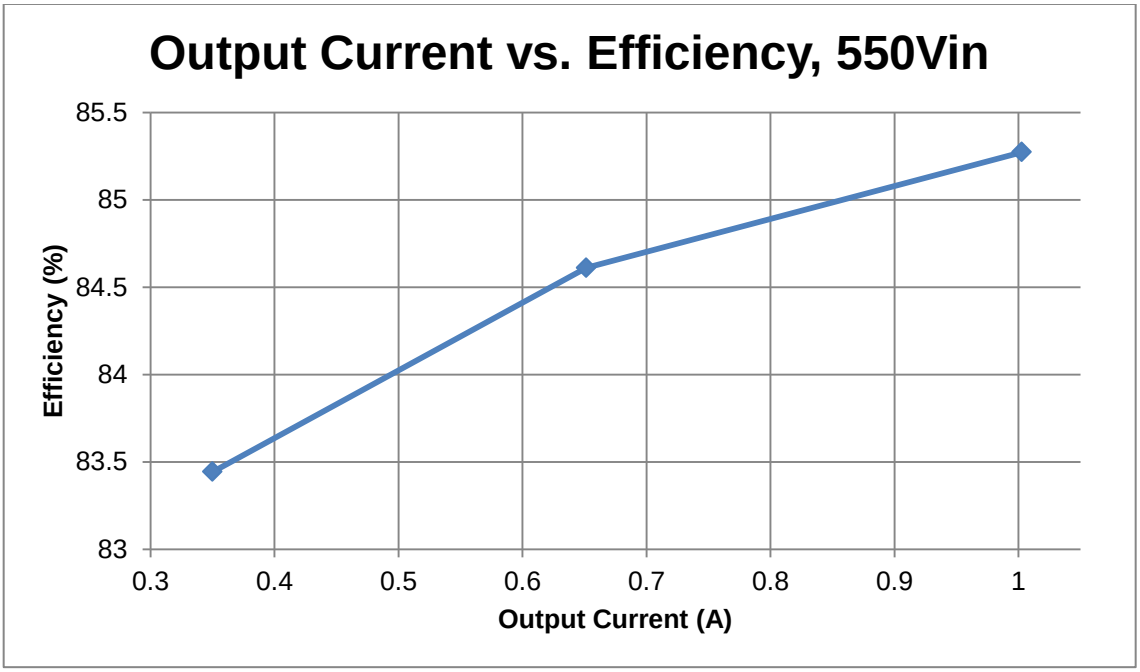

Figure 4. Efficiency for 550 Vdc input

1.2.2 Efficiency Data

Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Power Loss (W)	Efficiency (%)
39.985	0.158	6.317	15.348	0.327	5.026	1.291	79.562
80.085	0.074	5.950	15.372	0.327	5.026	0.923	84.476
150.07	0.038	5.837	15.369	0.328	5.044	0.793	86.405
249.70	0.025	6.262	15.392	0.351	5.408	0.853	86.367
250.01	0.047	11.750	15.446	0.659	10.185	1.565	86.678
249.96	0.071	17.872	15.511	1.001	15.526	2.345	86.875
550.12	0.01173	6.452	15.380	0.350	5.384	1.068	83.443
550.15	0.0216	11.883	15.433	0.651	10.054	1.828	84.611
550.14	0.033	15.494	15.494	1.002	15.537	2.683	85.273

Figure 5. Efficiency data from light load and full load at varying input voltage

1.2.3 Thermal Images

Thermal images (with no airflow) were taken for 40Vin, 250Vin, and 550Vin at varying loads. The board had a soak time of 10 minutes.

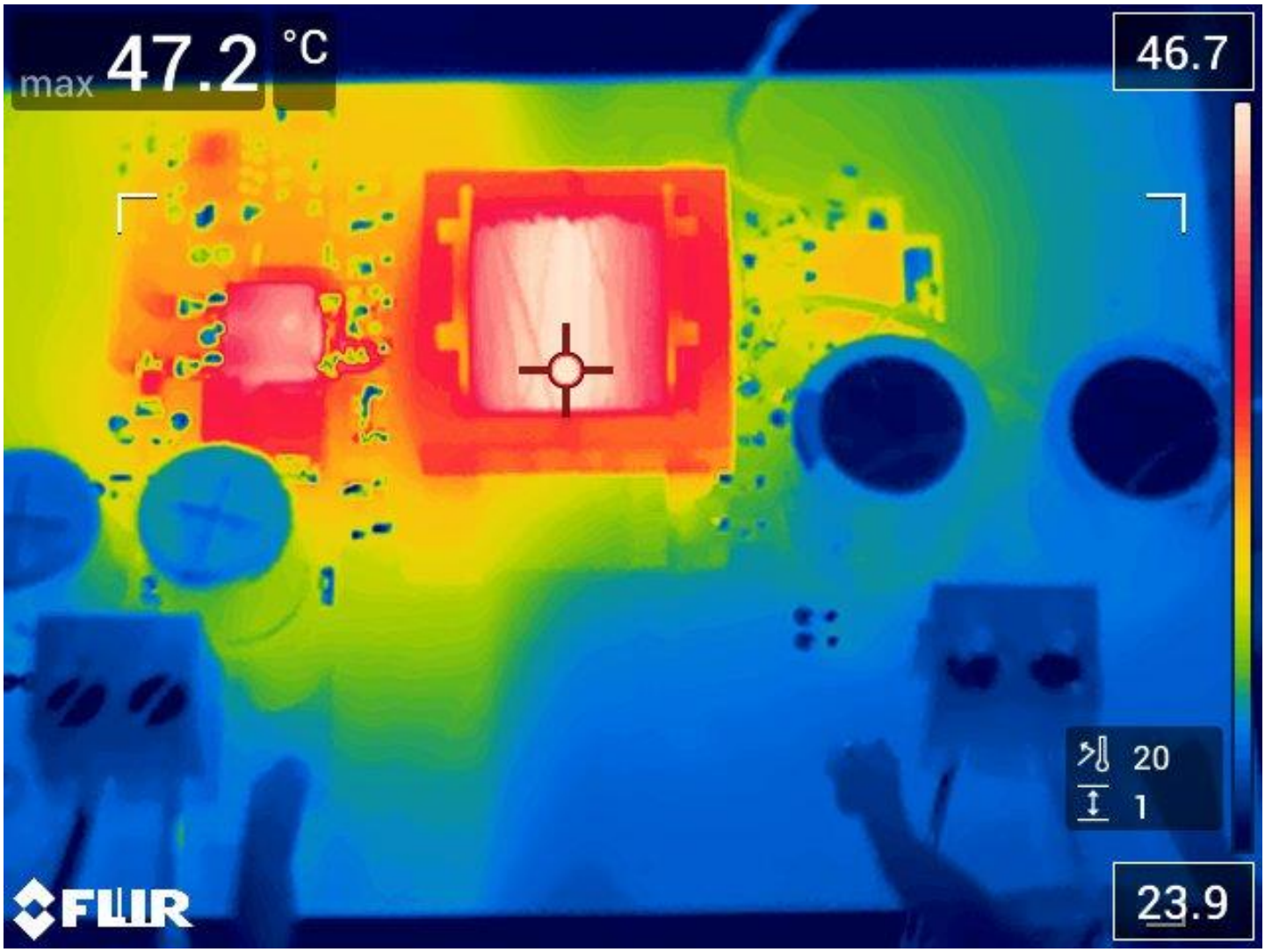

Figure 6. Board top thermal image, 40Vin, 0.33 A out

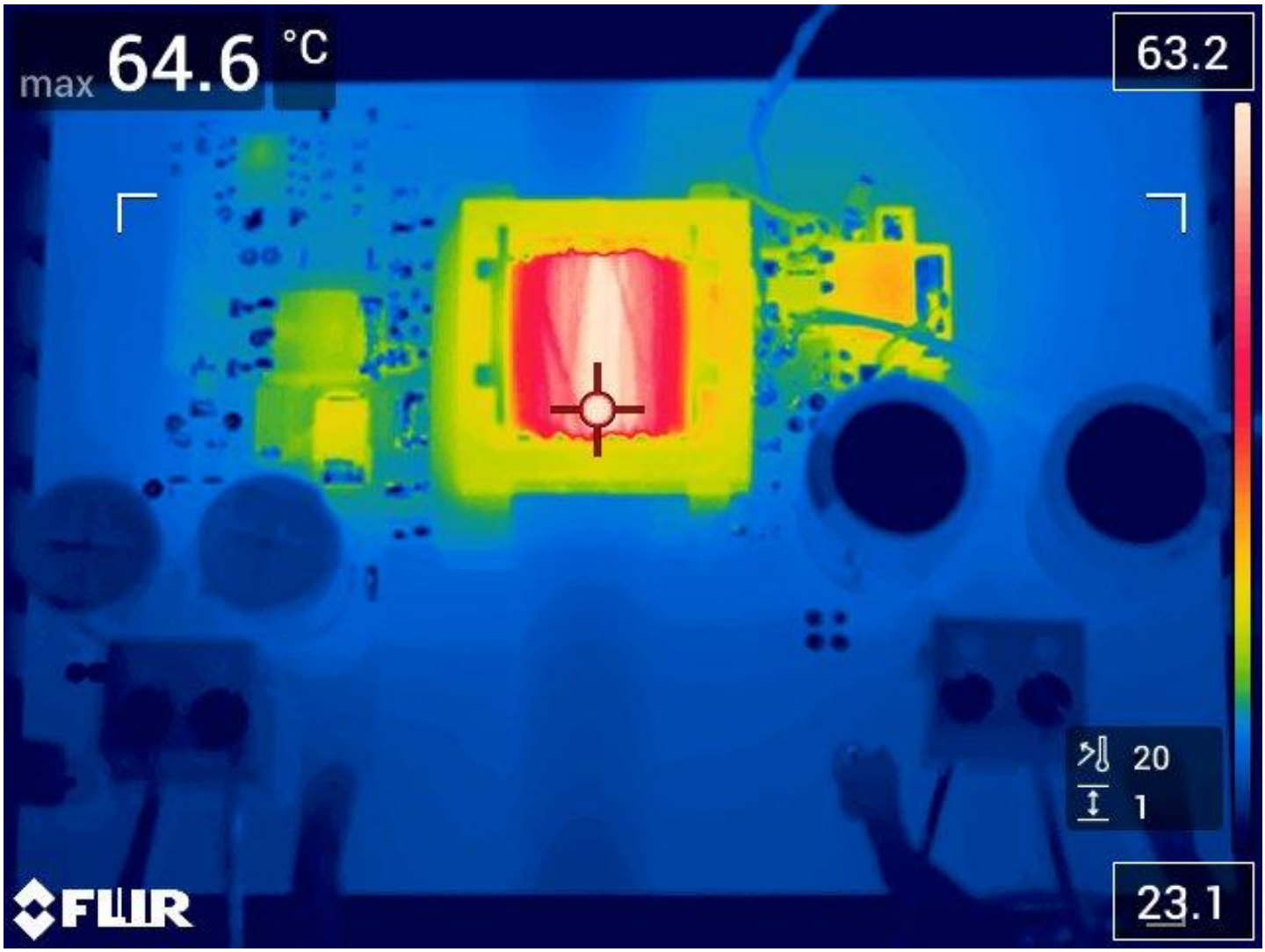

Figure 7. Board top thermal image, 250Vin, 1 A out

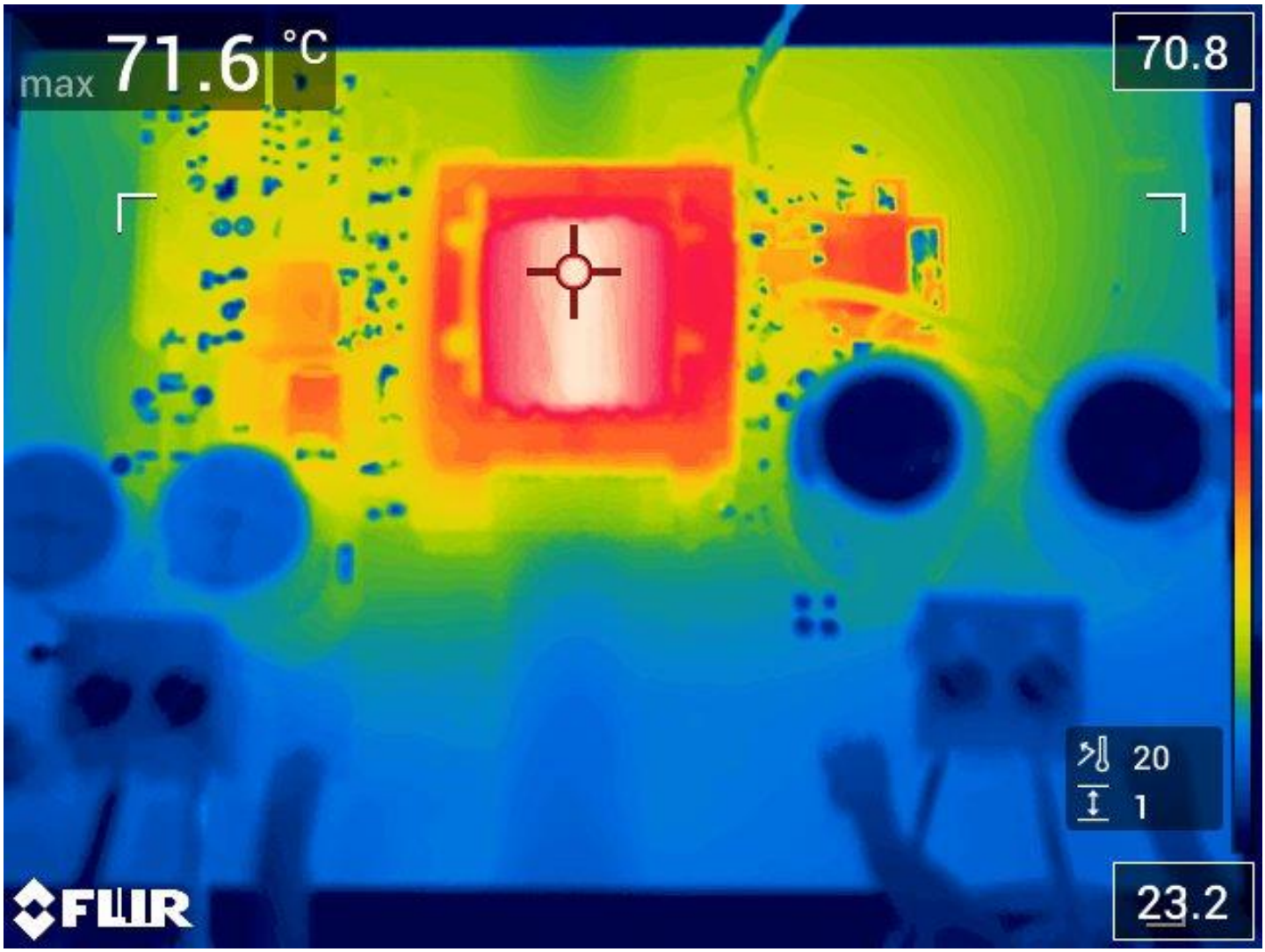

Figure 8. Board top thermal image, 550Vin, 1 A out

1.3 Waveforms

1.3.1 Switching

The switch node was measured at both the primary and secondary side at various loading conditions.

The primary side was measured from the drain (Pin 4) of 950V FET (Q1) to GND.

The secondary side was measured using two probes at each side of the diode (D1) and the math function. Channel 1 was measured from Pin 2 of D1 to GND, Channel 3 was measured from Pin 1 of D1 to GND, and the Math function shows C1-C3.

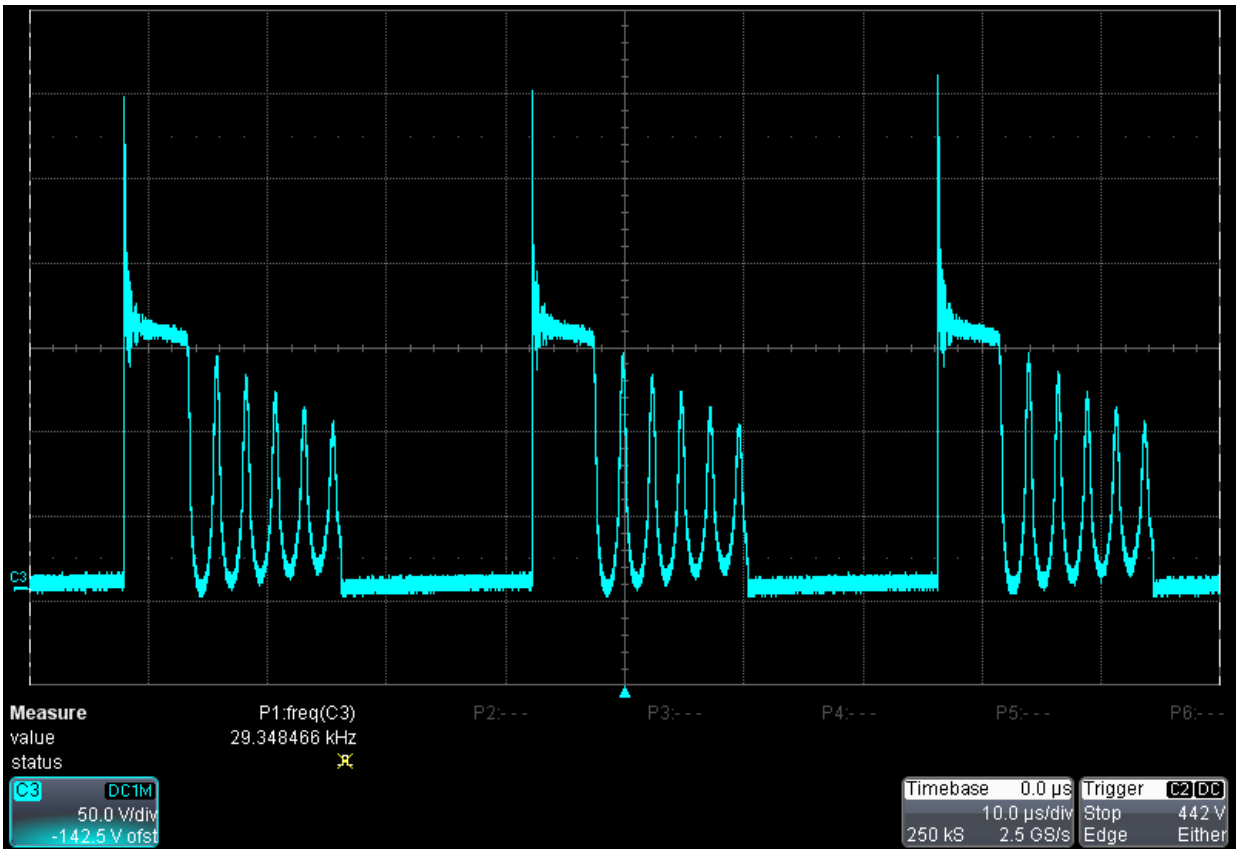

Figure 9. Primary Switch Node at 40 Vdc Input, 0.33 A out

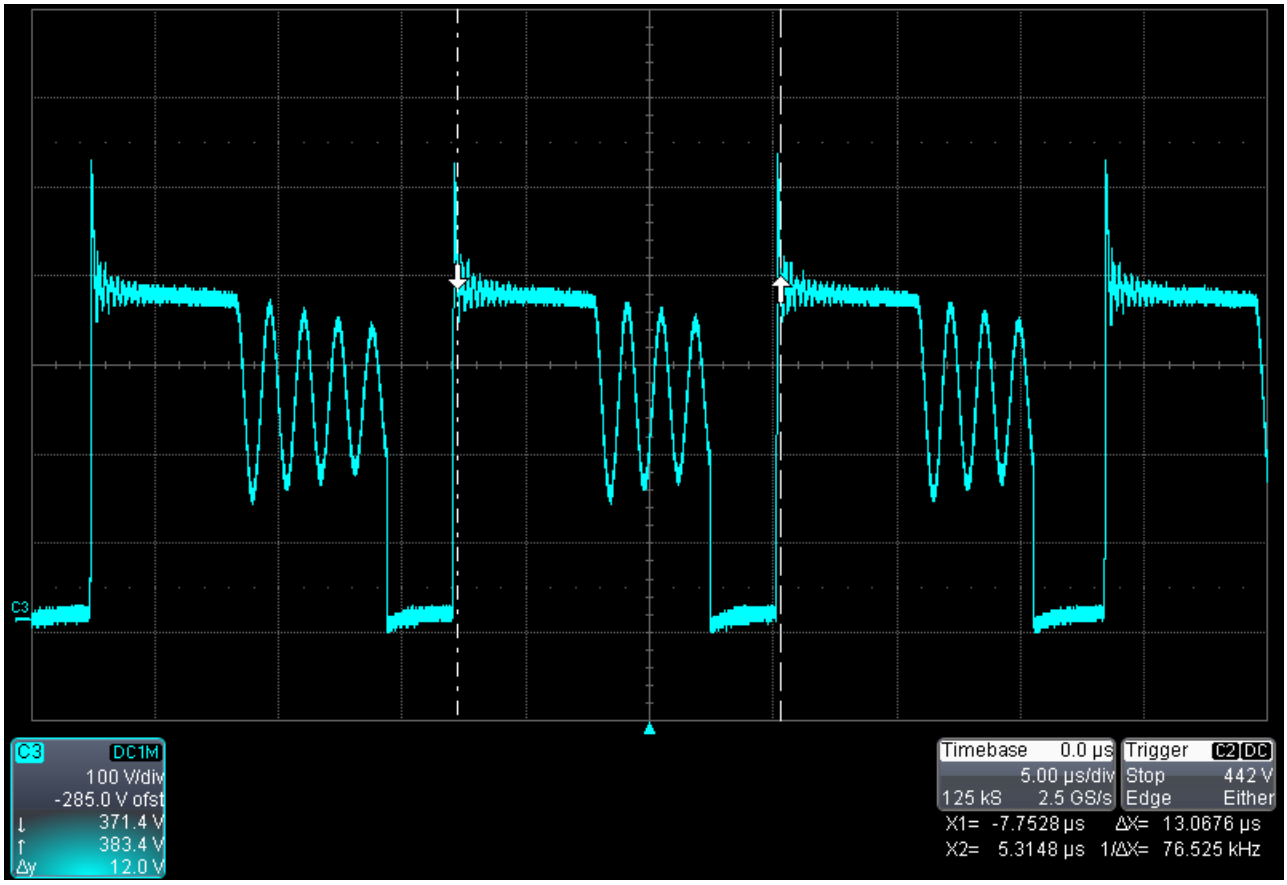

Figure 10. Primary Switch Node at 250 Vdc Input, 1 A out

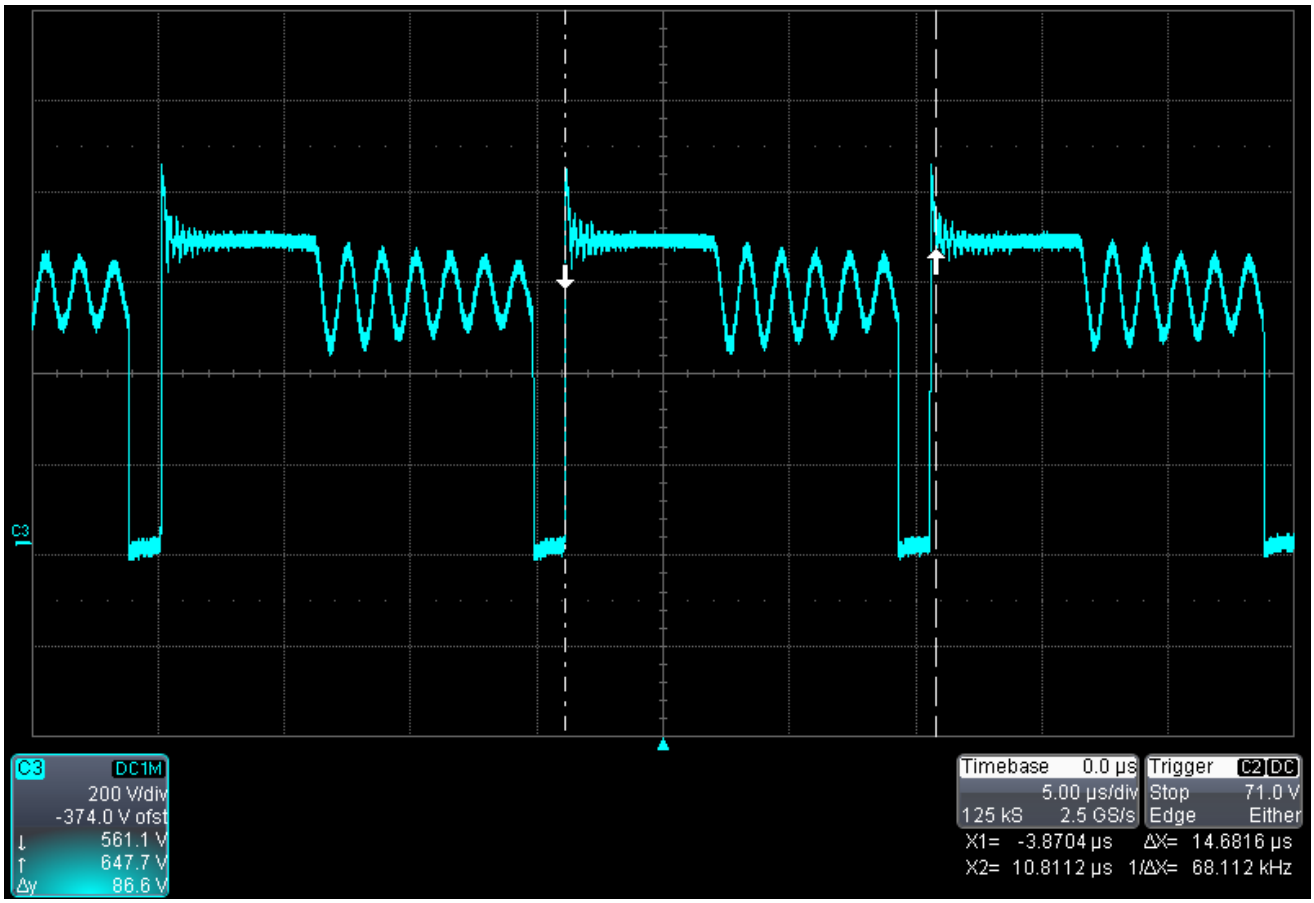

Figure 11. Primary Switch Node at 550 Vdc Input, 1 A out

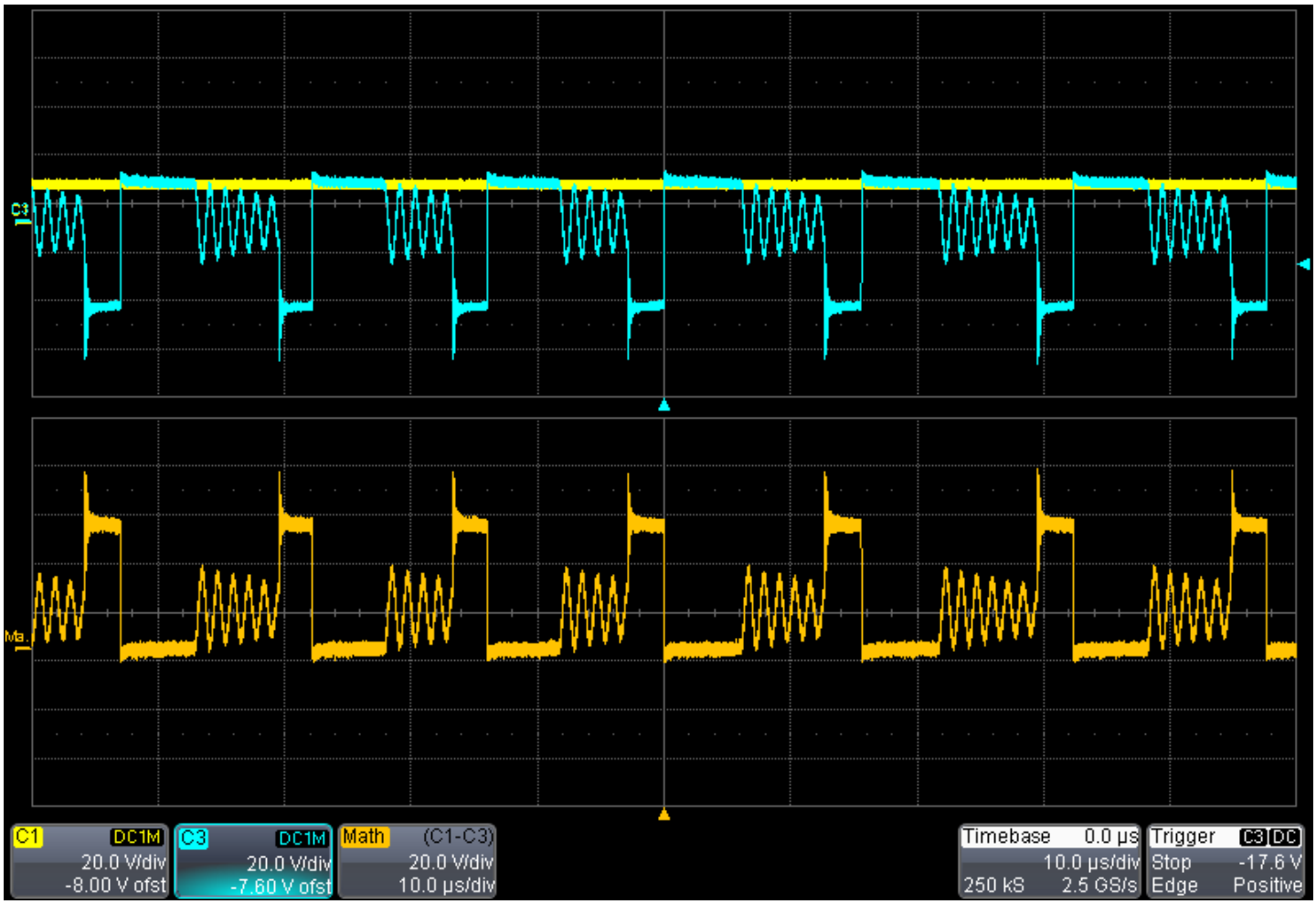

Figure 12. Secondary Switch Node at 250 Vdc Input, 1 A out

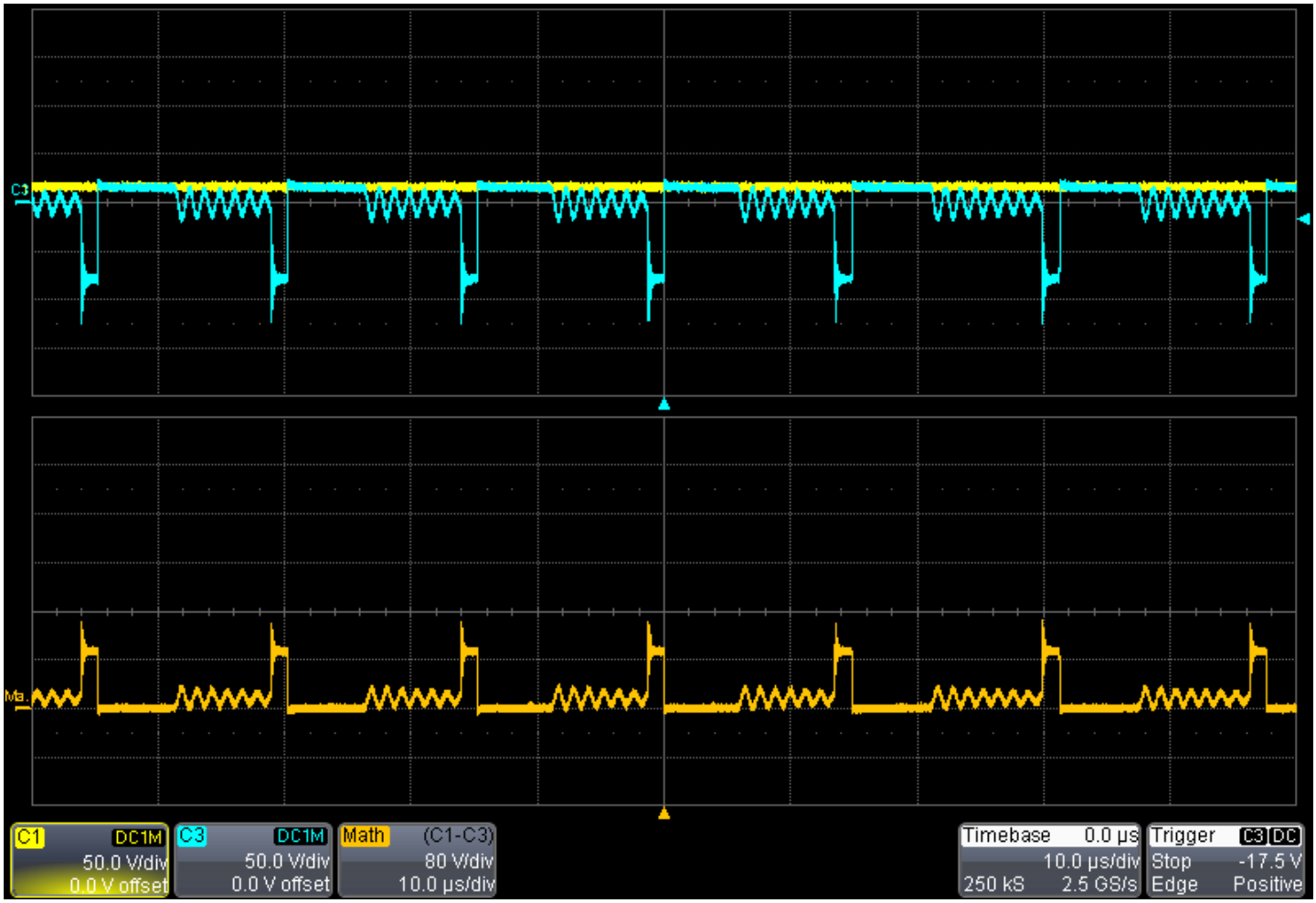

Figure 13. Secondary Switch Node at 550 Vdc Input, 1 A out

1.3.2 Output Voltage Ripple

Measurements were taken from Pin 2 of D1 to GND. The ripple measurements shown are with a 0 Ohm resistor (R1) at the output. The schematic has a placeholder for an output inductor (L1) to reduce ripple, if needed.

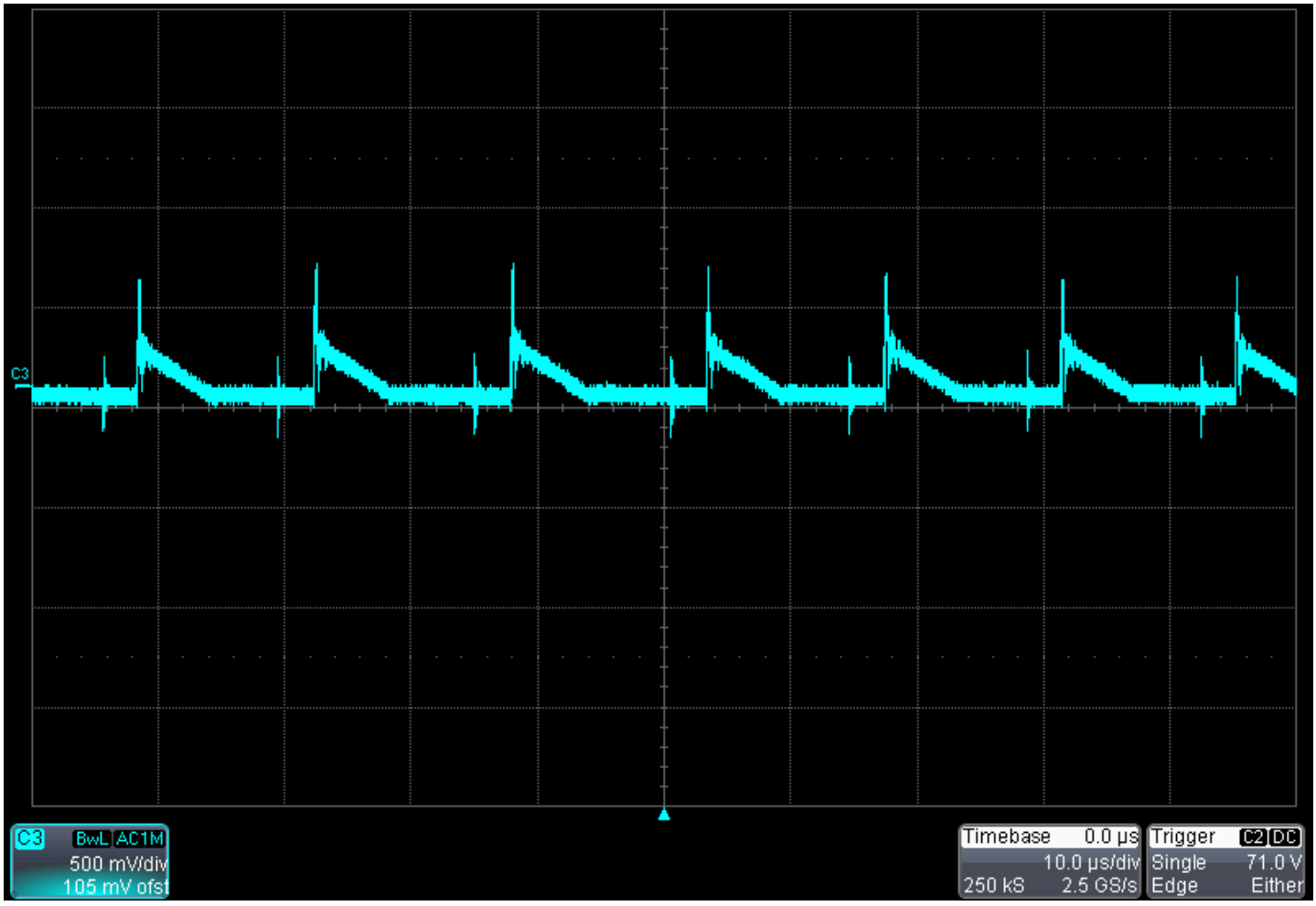

Figure 14. Output Ripple at 250 Vdc Input, 1 A out

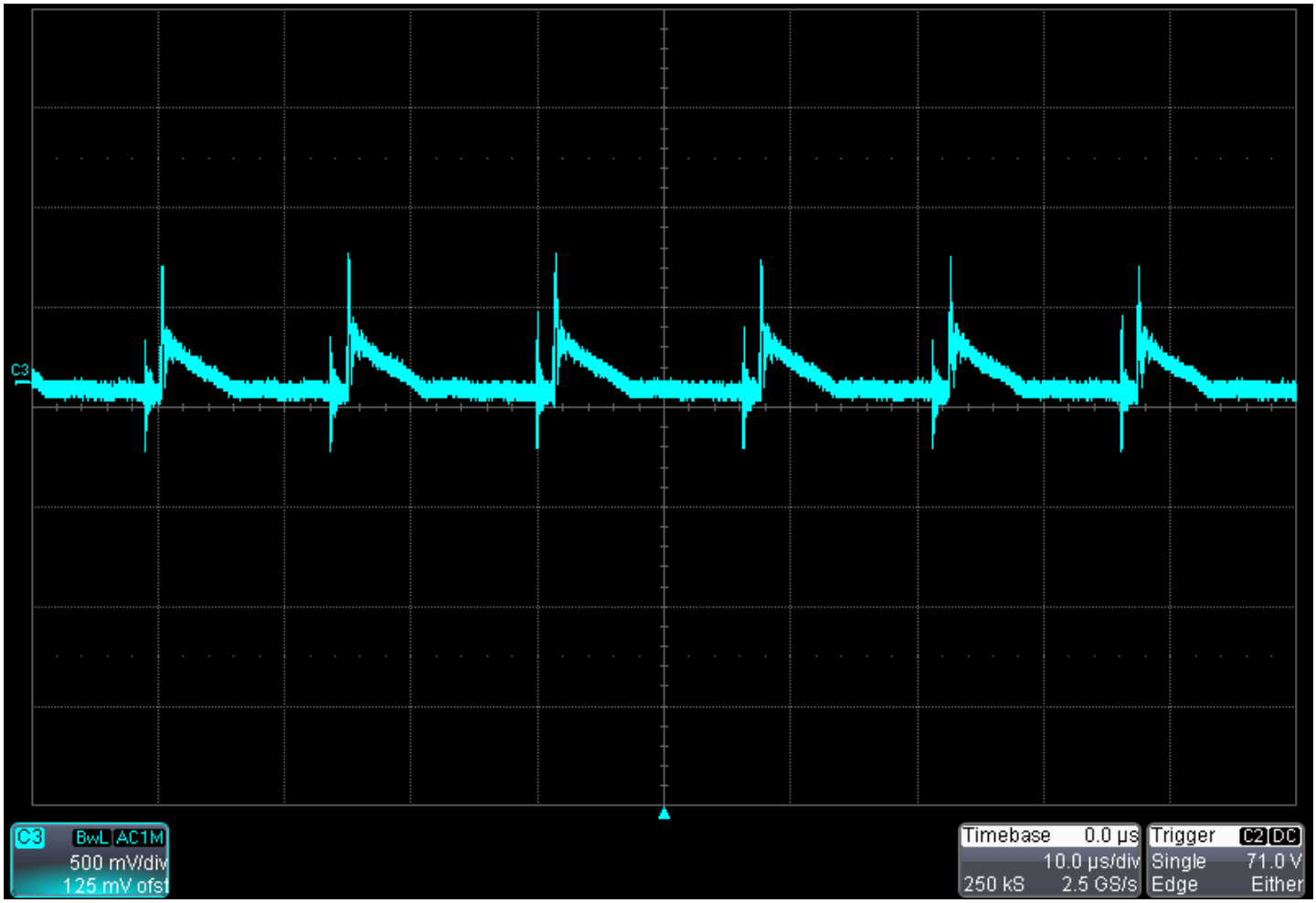

Figure 15. Output Ripple at 550 Vdc Input, 1 A out

1.3.3 Load Transients

The load step applied is between 0.25 A and 0.75 A (25% to 75% of full load). The slew rate is 4.000 A/uS. The output voltage (AC coupled) was measured at the output of D1 (pin 2).

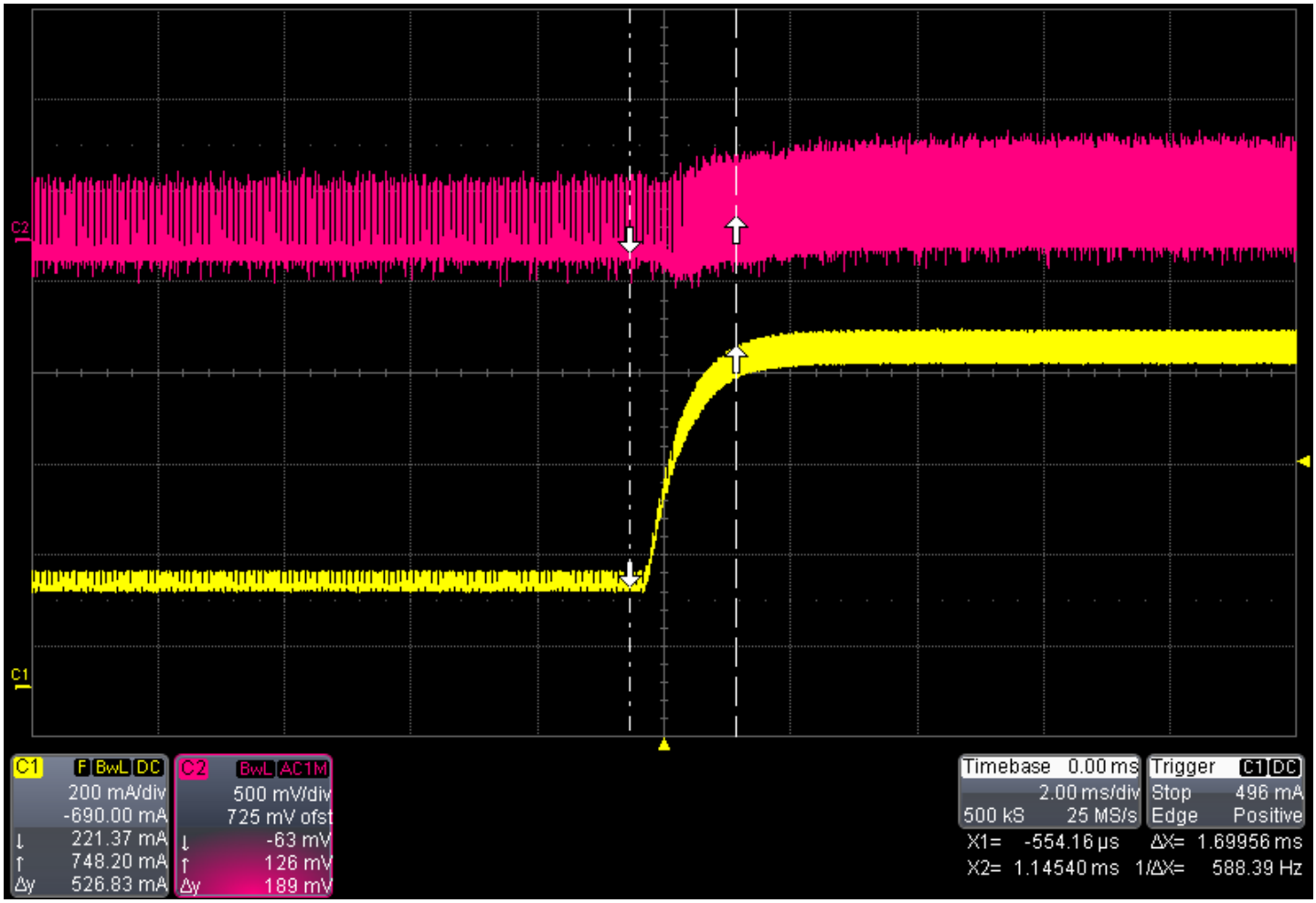

Figure 16. Load transient rising edge, 250Vin

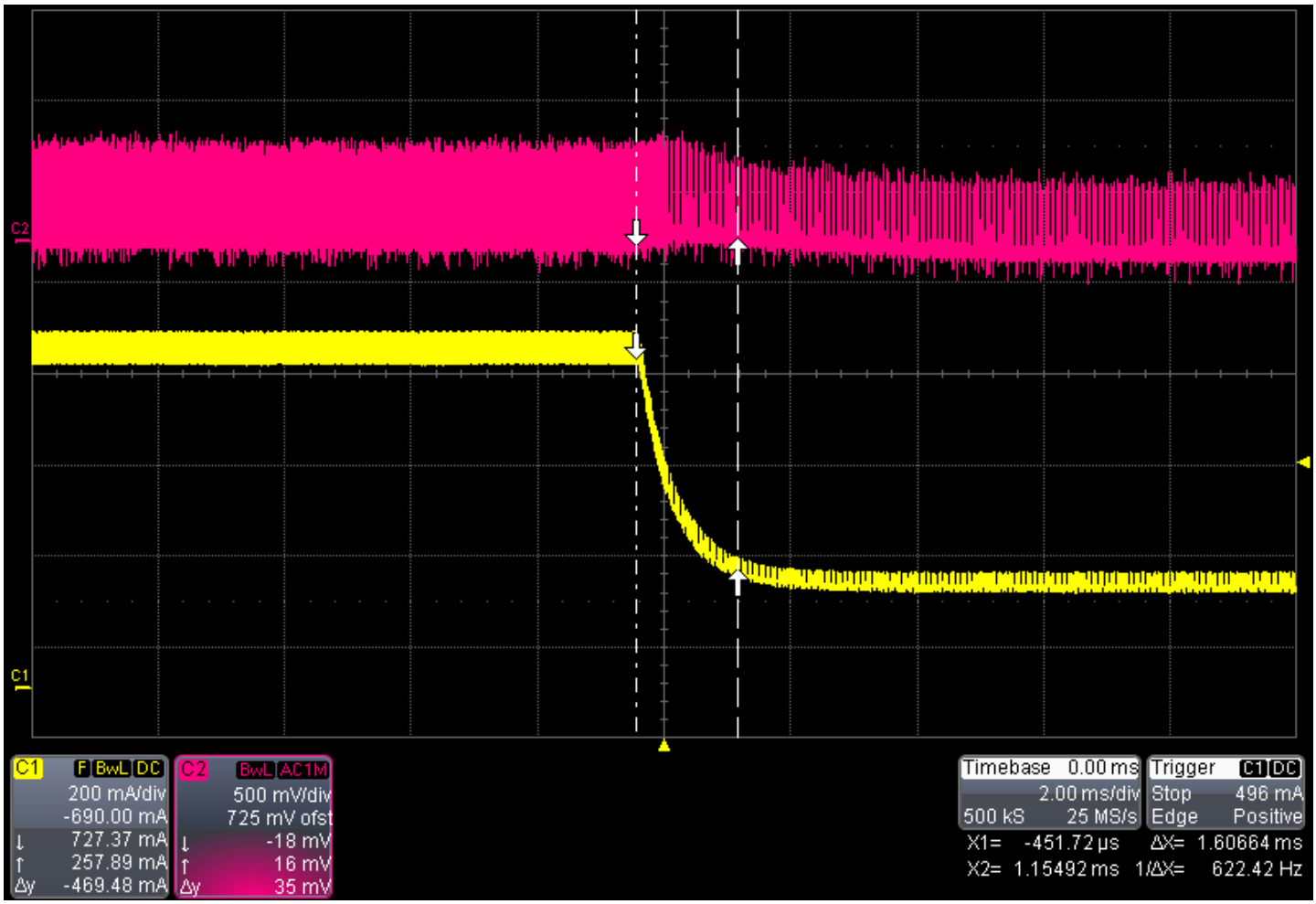

Figure 17. Load transient falling edge, 250Vin

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