Test Report: PMP31177

18 V_{DC} – 32 V_{DC} to 24 V and 3.3 V, 1-W Isolated Primary-Side Regulated Flyback Reference Design

Description

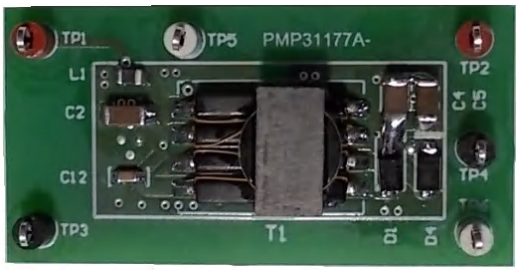
This 26.54 mm × 11.68 mm × 5.6-mm height board is optimized to leverage the performance of the LM5181 PSR Flyback converter. The board operates over an input voltage range of 18 V to 32 V to deliver a 24-V and 3.3-V outputs at currents up to 40 mA and 15 mA, respectively. Operating without an auxiliary winding or optocoupler, the LM5181 provides very tight output voltage regulation. The LM5181 offers several protection features, like undervoltage lockout to provide proper operation during voltage-sag conditions, programmable soft-start to reduce inrush current, hiccup-mode overcurrent protection, and thermal shutdown.

Features

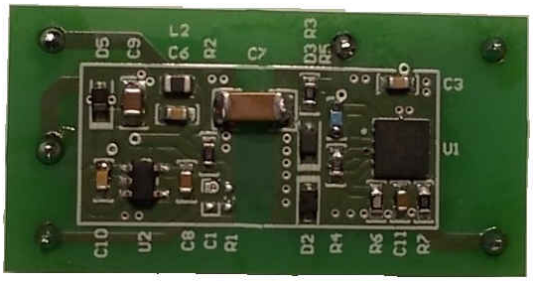
- 18-V to 32-V input voltage range
- 24-V and 3.3-V output voltages
- Up to 1-W total output power
- High-voltage isolation
- Fully assembled and tested PCB layout with small footprint and low profile

Applications

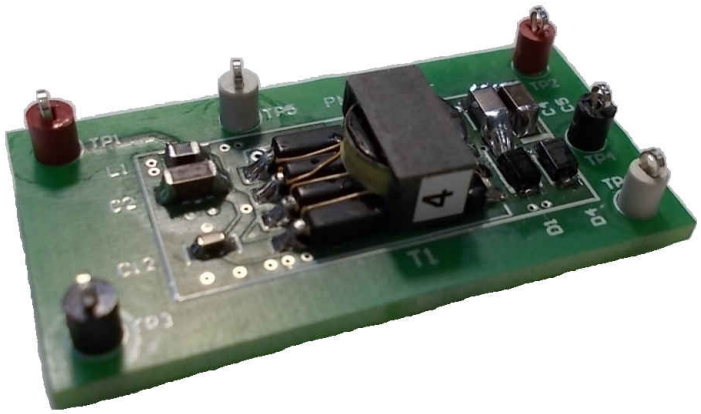
- Mixed module (AI,AO,DI,DO)



Top View



Bottom View



Angled View

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage	18 V_{DC} – 32 V_{DC}
Output-1 Voltage	24 V_{DC}
Output-1, Current	40 mA
Output-2, Voltage	3.3 V_{DC}
Output-2, Current	15 mA

1.2 Required Equipment

- 0…35 V_{DC} constant voltage source (VS1)
- Two electronic loads, (constant current range 0…100 mA minimum)
- Oscilloscope (minimum 100-MHz bandwidth)
- Current probe (minimum 100-kHz bandwidth)

1.3 Considerations

The reference design PMP31177 Rev_B was built on the PMP31177 Rev_A PCB.

1.4 Dimensions

The net PCB (containing all components) board dimensions are 26.54 mm × 11.68 mm, height 5.6 mm (T1) .

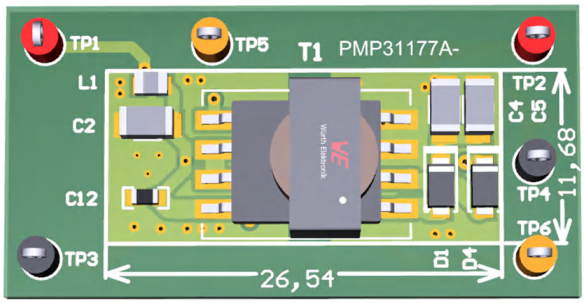


Figure 1-1. 3D-Image of the Board

1.5 Test Setup

1. Connect the source VS1 to TP1 (positive) and TP3 (negative)
2. Connect the first load to terminals TP2 (positive) and TP4 (negative)
3. Connect the second load to terminals TP6 (positive) and TP4 (negative)
4. Turn on VS1 (accepted range: 18 V_{DC} – 32 V_{DC})
5. Increase the load on each output

2 Testing and Results

2.1 Efficiency Graph

The efficiency graph in Figure 2-1 shows the converter efficiency, versus total output power.

The input voltage has been set to 18 V_{DC}, 24 V_{DC}, and 32 V_{DC}, while the load on each output has been increased at the same ratio.

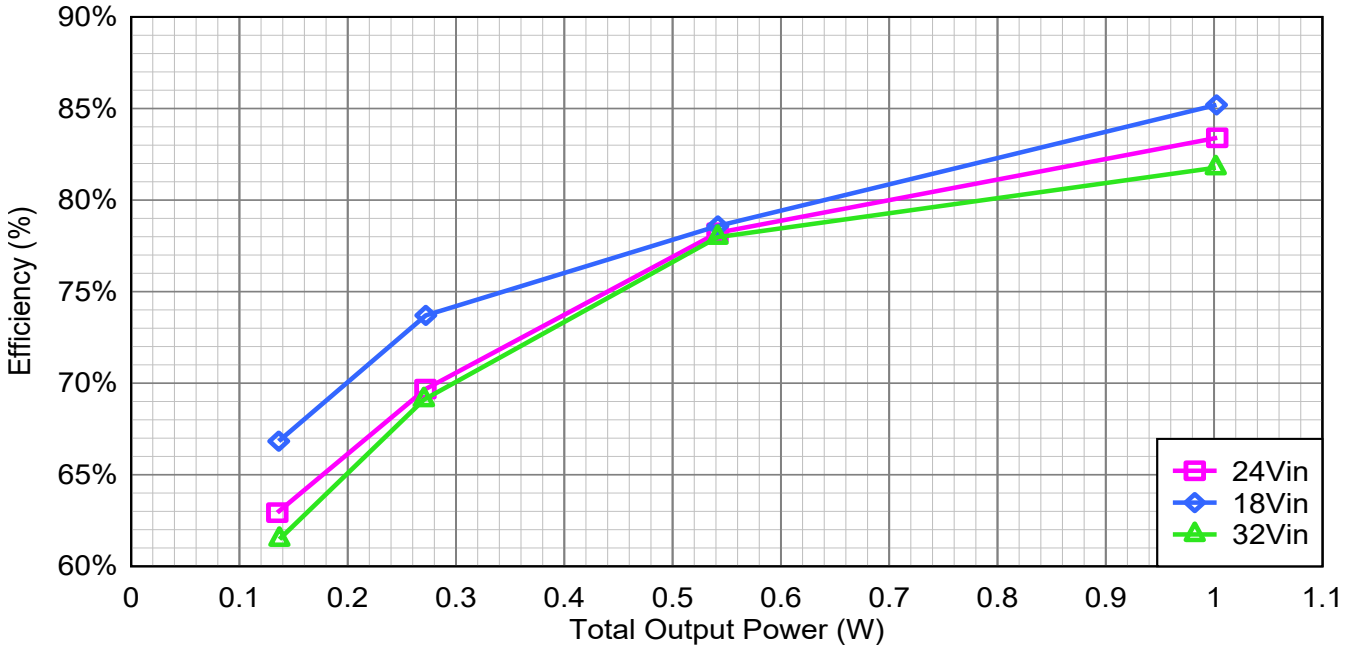


Figure 2-1. Efficiency Graph

2.2 Efficiency Data

The efficiency graph in Figure 2-1 reports the data, taken from the following tables.

Table 2-1. Efficiency Data for 24-V Input Voltage

V_{IN} (V)	I_N (mA)	P_{IN} (W)	24 V-V_{OUT} (V)	24 V-I_{OUT} (mA)	4 V-V_{OUT} (V)	3.3 V-V_{OUT} (V)	3.3 V-I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
24.00	1.43	0.034	23.72	0.0	4.576	3.307	0.0	0.000	0.00%
23.99	8.94	0.214	23.71	5.4	4.591	3.300	2.1	0.135	62.93%
23.99	16.26	0.390	23.70	10.8	4.595	3.299	4.8	0.272	69.68%
23.97	28.88	0.692	23.68	21.5	4.587	3.299	9.8	0.541	78.22%
24.05	50.00	1.203	23.65	40.3	4.593	3.298	15.1	1.003	83.40%

Table 2-2. Efficiency Data for 18-V Input Voltage

V_{IN} (V)	I_N (mA)	P_{IN} (W)	24V-V_{OUT} (V)	24V-I_{OUT} (mA)	4V-V_{OUT} (V)	3.3V-V_{OUT} (V)	3.3V-I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
18.03	1.61	0.029	23.72	0.0	4.577	3.307	0.0	0.000	0.00%
18.03	11.31	0.204	23.71	5.4	4.585	3.300	2.5	0.136	66.83%
18.02	20.49	0.369	23.70	10.8	4.594	3.299	4.9	0.272	73.70%
18.00	38.3	0.689	23.68	21.5	4.586	3.299	9.9	0.542	78.59%
17.96	65.5	1.176	23.65	40.3	4.602	3.298	14.9	1.002	85.20%

Table 2-3. Efficiency Data for 32-V Input Voltage

V_{IN} (V)	I_N (mA)	P_{IN} (W)	24 V-V_{OUT} (V)	24 V-I_{OUT} (mA)	4 V-V_{OUT} (V)	3.3 V-V_{OUT} (V)	3.3 V-I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
32.19	1.28	0.041	23.71	0.0	4.592	3.307	0.0	0.000	0.00%
32.19	6.92	0.223	23.71	5.4	4.603	3.300	2.7	0.137	61.48%
32.18	12.16	0.391	23.70	10.7	4.618	3.299	5.1	0.270	69.11%
32.17	21.6	0.695	23.67	21.5	4.618	3.299	9.9	0.542	77.97%
32.15	38.1	1.225	23.66	40.2	4.628	3.298	15.3	1.002	81.77%

2.3 Static Output Voltage Variation vs Load Current and V_{IN}

2.3.1 24-V Output Voltage

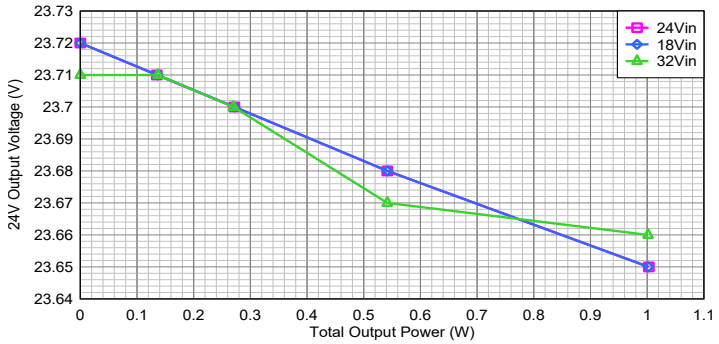


Figure 2-2. Static Output Voltage Variation of the 24-V Output

2.3.2 3.3-V Output Voltage

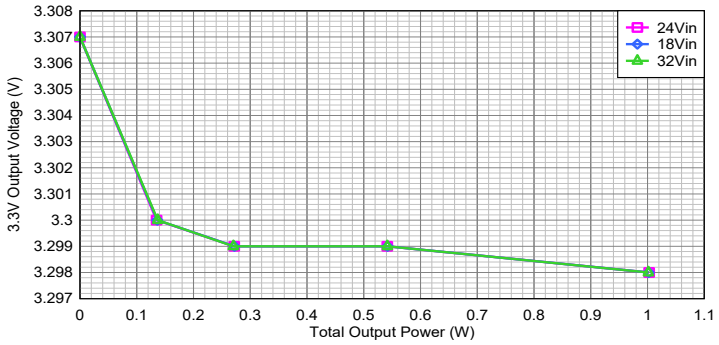


Figure 2-3. Static Output Voltage Variation of the 3.3-V Output

2.3.3 U2 Input Voltage

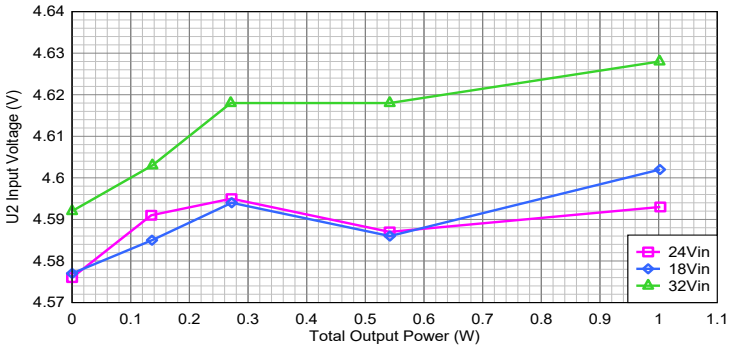


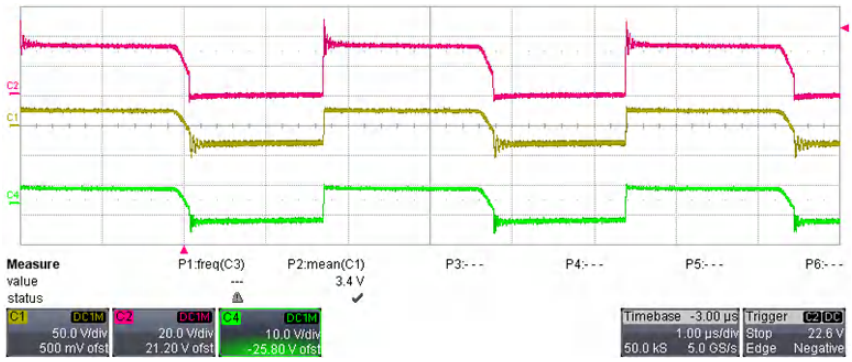
Figure 2-4. Static Output Voltage Variation of the U2 Input

3 Waveforms

3.1 Switching Waveforms on Pin 1 of U1 (SW), Anodes of D1 and D4, at Full Load

The switching waveforms were measured by supplying the converter at 96 V_{AC}, 400 Hz at full load. For all switch-node waveforms the bandwidth limit has been removed.

3.1.1 18-V Input Voltage



C1: D1 Anode
(50 V / div)

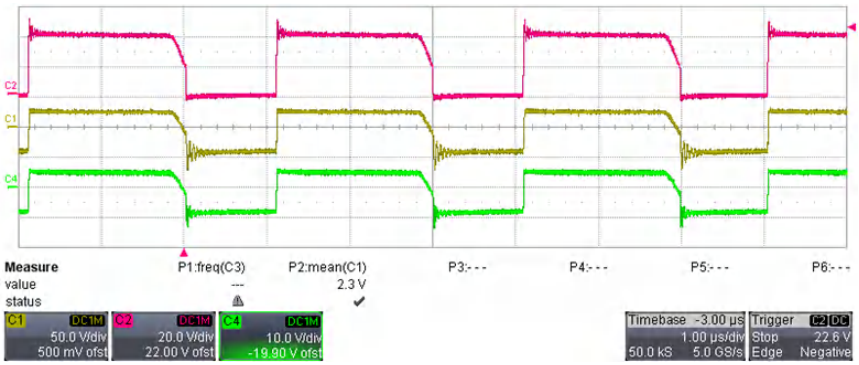
C2: SW
(20 V / div)

C4: D4 Anode
(10 V / div)

1 µs / div

Figure 3-1. Switching Waveforms at 18-V Input Voltage

3.1.2 24-V Input Voltage



C1: D1 Anode
(50 V / div)

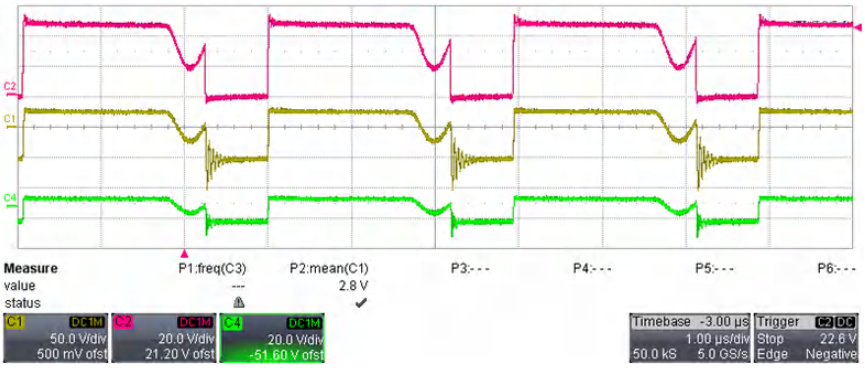
C2: SW
(20 V / div)

C4: D4 Anode
(10 V / div)

1 µs / div

Figure 3-2. Switching Waveforms at 24-V Input Voltage

3.1.3 32-V Input Voltage



C1: D1 Anode
(50 V / div)

C2: SW
(20 V / div)

C4: D4 Anode
(10 V / div)

1 µs / div

Figure 3-3. Switching Waveforms at 32-V Input Voltage

3.2 Output Voltage Ripple

The 3.3-V and 24-V outputs, as well as input voltage and ripple were measured by supplying the converter at 24 V_{DC} with both outputs loaded at nominal current. The bandwidth limit of the scope was set to 20 MHz, and the coupling to AC.

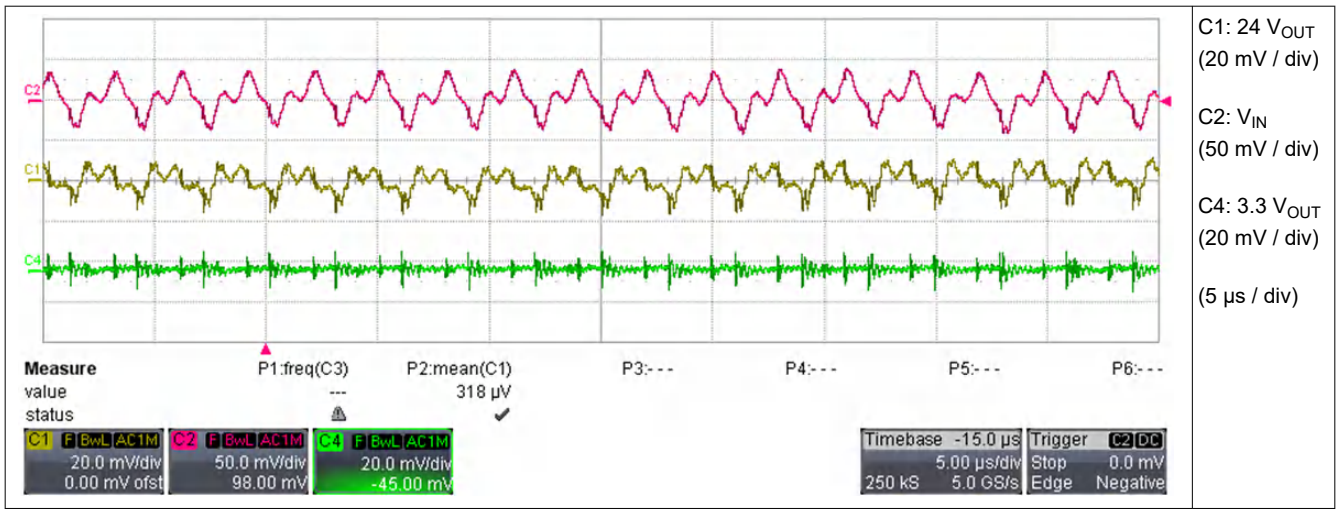


Figure 3-4. Output Voltage Ripple With 5 µs / div

Figure 3-5 is the same waveform as in Figure 3-4 but with longer time division for showing details about low-frequency ripple.

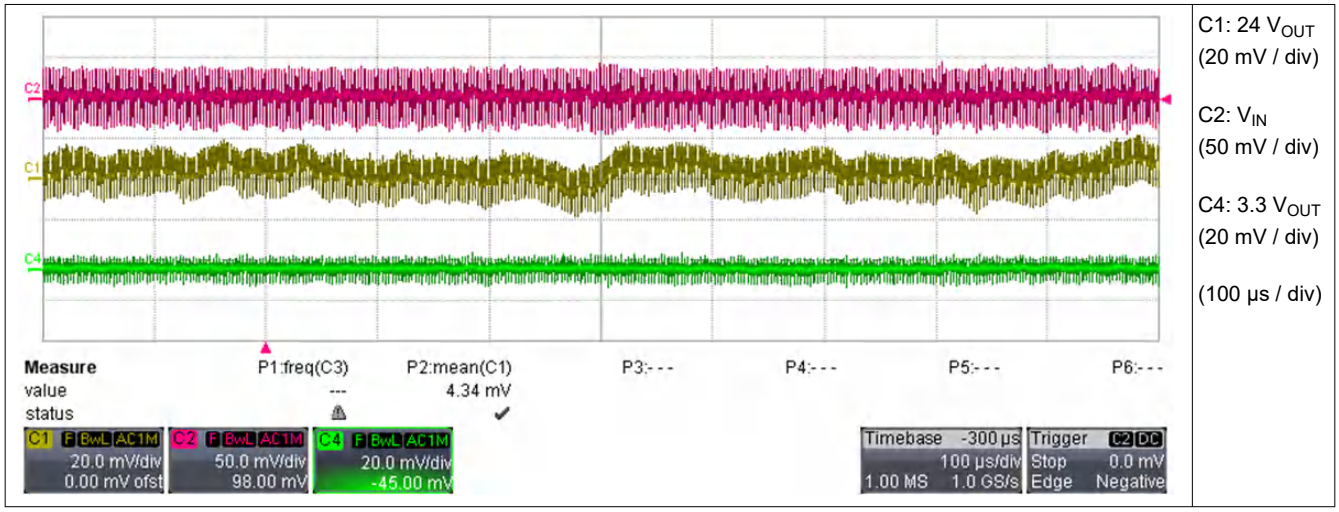


Figure 3-5. Output Voltage Ripple With 100 µs / div

3.3 Load Transients

During load transients, the outputs of the board were measured by supplying the converter at 24 V_{DC} while the load on 24 V_{OUT} was switched between 20 mA and 60 mA; the load on 3.3 V_{OUT} was constant at 15 mA. For all waveforms the bandwidth limit of the oscilloscope was set to 20 MHz.

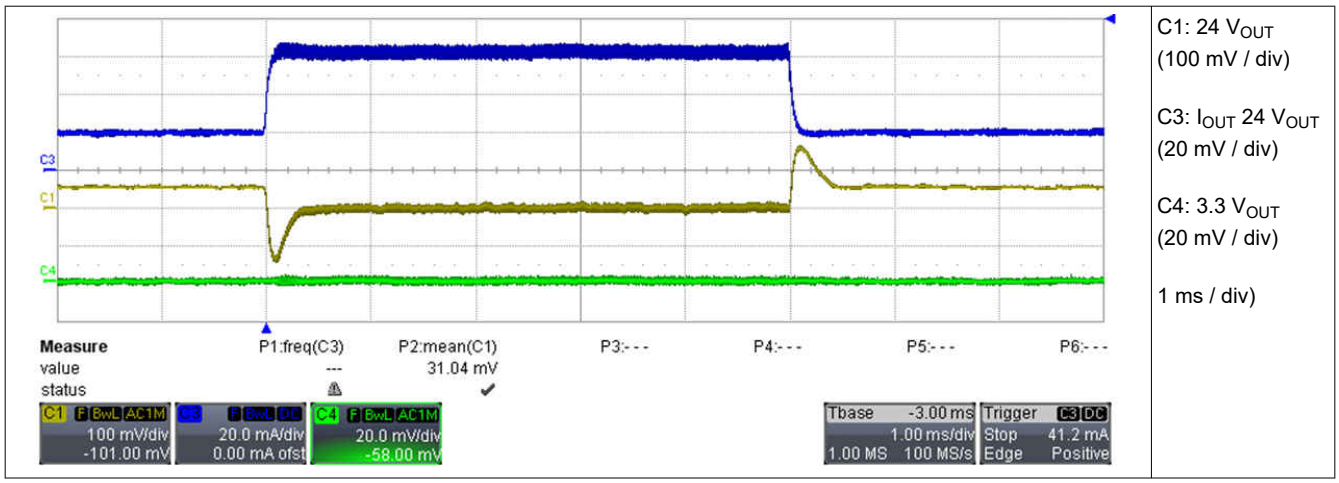


Figure 3-6. Load Transient

3.4 Start-Up Sequence

The start-up phase of the converter has been analyzed by supplying the circuit with 24 V_{DC} at zero load and full-load conditions. All waveforms were taken at 20 MHz bandwidth limit and DC coupling.

3.4.1 No Load

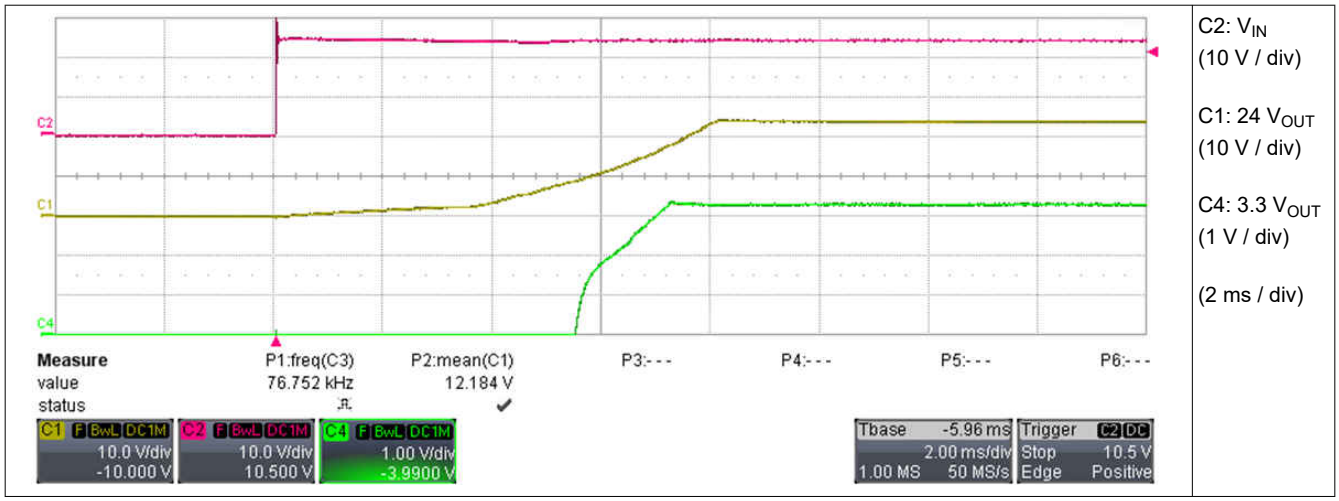


Figure 3-7. Start-Up With No Load

3.4.2 Full Load

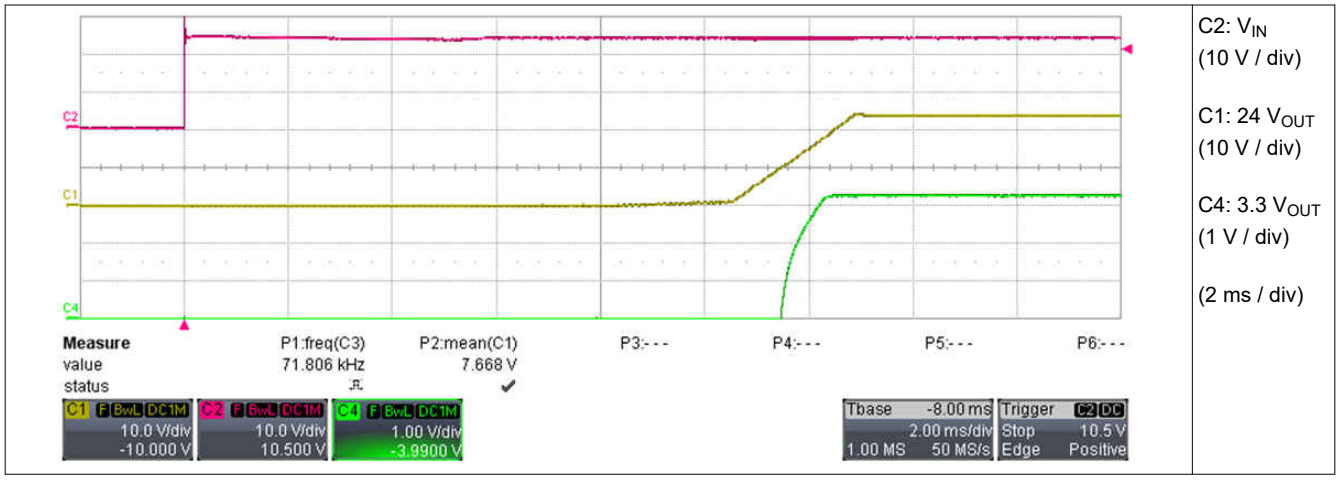


Figure 3-8. Start-Up With Full Load (at Both Outputs)

3.5 Shutdown Sequence

The shutdown phase of the converter was analyzed by supplying the circuit with 24 V_{DC} but only at full-load condition. All waveforms were taken at 20-MHz bandwidth limit and DC coupling.

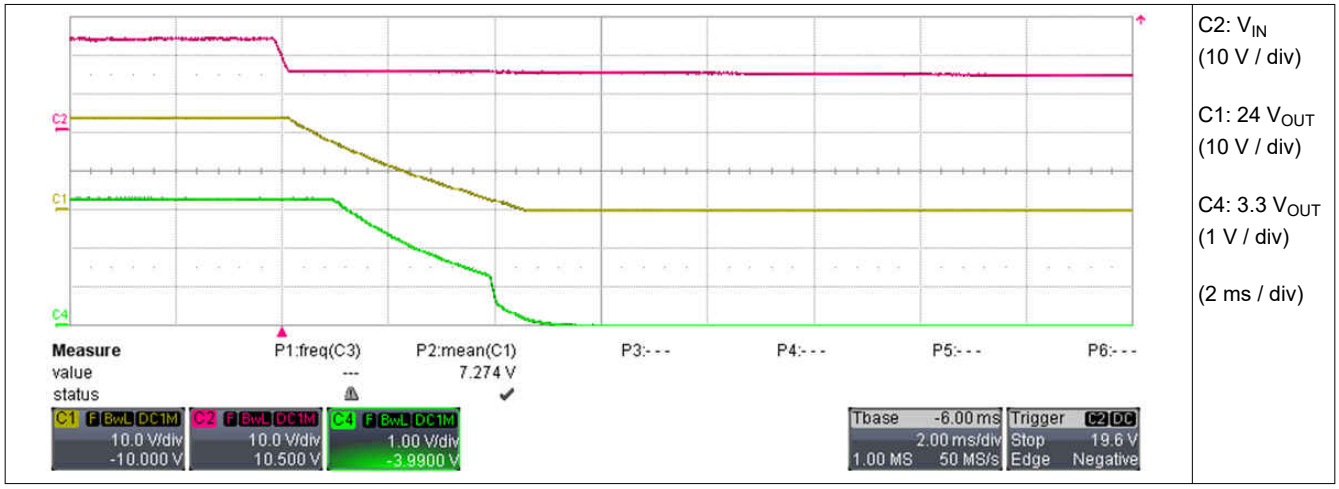


Figure 3-9. Shutdown with Full Load (at both Outputs)

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