1A, Single Cell LiFePO$_4$ Linear Battery Charger with 4.9 V, 50 mA LDO

This user's guide describes the bq25070 evaluation module (EVM), how to perform a stand-alone evaluation or interface with a host or system. The converter is designed to deliver up to 1 A of continuous current to the battery and/or system. The device has a 4.9 VDC, 50 mA max internal LDO that can be used for USB applications or any other need.

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1 Introduction

The bq25070 is a highly integrated $LiFePO_4$ linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell $LiFePO_4$ battery with up to 1 A of charge current. The 30 V maximum input voltage rating with 10.5 V input overvoltage protections supports low-cost unregulated adapters.

The bq25070 has a single power output that charges the battery and powers the system. The charge current is programmable up to 1 A using the CTRL input. Additionally, a 4.9 V ±10% 50 mA LDO is integrated into the IC for supplying low power external circuitry.

The $LiFePO_4$ charging algorithm removes the constant voltage mode control usually present in Li-Ion battery charge cycles. Instead, the battery is fast-charged to the overcharge voltage and then allowed to relax to a lower float charge voltage threshold. The removal of the constant voltage control reduces charge time significantly. During the charge cycle, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, and charge status display.

2 Considerations With Evaluating the bq25070

Read the complete data sheet (SLUSA66) to fully understand detailed information that may be useful in operating and evaluating this EVM.

This EVM can be used as a stand alone evaluation module using the hardware, on sheet 2 of the EVM schematic, that generates the pulses to program the IC's CTRL pin. Placing a single shunt on JP101 through JP113 programs the hardware to deliver pulses via JP3 to the CTRL pin on the IC. Toggling switch S101 from the down position up then back down sends the programmed pulses to the IC via JP3, if the input power is present. Potentiometer, R109, can be used to adjust the width of the pulse if it is out of specification.

A 10k NTC thermistor is required for charging, connected between TS and GND on J2 or the "on-board" 10k resistor can be substituted by placing a shunt on JP1. Using both the external thermistor and internal 10k resistor may cause a hot temperature fault due to the low parallel resistance. No connection to the TS pin will cause a cold temperature fault. During a temperature fault condition the OUT charge current is disabled.

The EVM can interface with a micro-processor from your system that can be connected by removing the JP3 shunt (disconnecting the EVM hardware producing the pulses) and applying the processor control signal to JP3-1 (right pin) with the processor ground connected to the ground of the EVM. Note that when JP3 is removed, the CTRL pin is pulled high by R6 and disables the IC. The micro-processor signal will pull the CTRL pin low when not delivering the pulses, allowing proper operation.

The optional Battery Cell Replacement Circuit allows quick adjustment to the battery voltage. To check the short circuit operation below 0.7V, the Cell P/S must be reduced to less than 1V. The programmed current will have to be reduced so the OUT voltage can drop below 0.7V or the charge current will have to be disabled and re-enabled.

3 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	UNIT
Input dc voltage, V_{IN}	Recommended input voltage range	5.1		5.5	V
Reduced performance, V_{IN} (1)	Input voltage too low to maintain output regulation	3.75		10.2	V

(1) As the input voltage drops near 5.1 VDC, the 4.9 V LDO may start to enter dropout.
As the input voltage drops near 3.75 V, the charge current may start to roll off.
Any input voltage near 10.2 V may put the device in OVP. See the data sheet for complete specifications.

4 Test Summary

The bq25070EVM-740 board requires an adjustable 5 VDC, ≥ 1250 mA Current Limited power source to provide input power and a $LiFePO_4$ battery as a load. The test setup connections and jumper settings selections are configured for a stand-alone evaluation, but can be changed to interface with external hardware such as a microcontroller.

4.1 Equipment

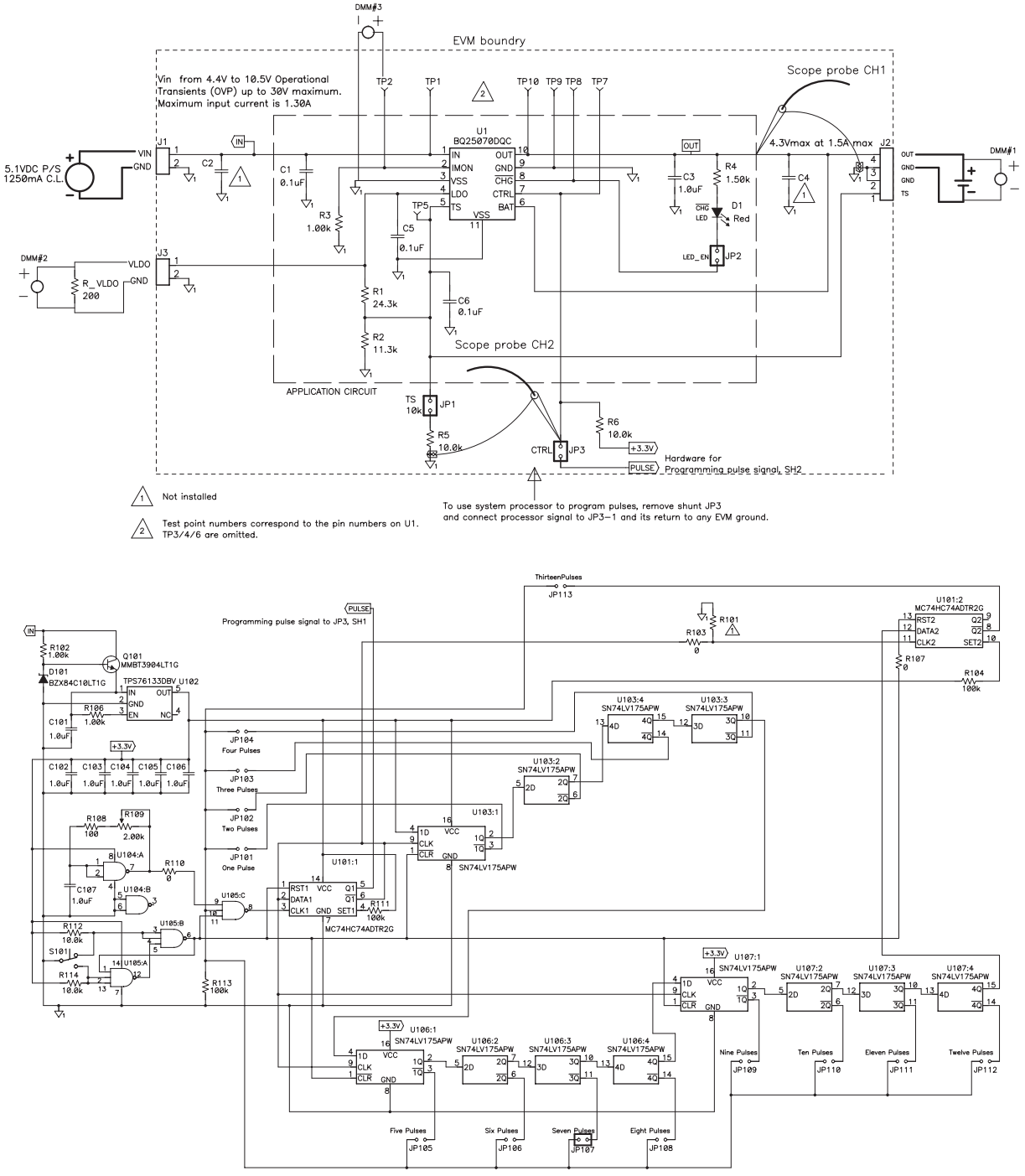
- Adjustable dc power supply with current meter, set between 5.1 V and 5.3 VDC with adjustable current limit set to between 1200 and 1300 mA
- Load **OUT**: $LiFePO_4$ battery charged up between 3 V and 3.3 V, with > 1F of capacity
  - See Figure 3 for an alternative “simulated battery replacement”.
- Load VLDO: 200 Ω resistor, 0.25W
- Three Fluke 75 DMMs (equivalent or better)
- Oscilloscope Model TDS222 (equivalent or better)

4.2 Equipment and EVM Setup

Table 1. Setup I/O Connections and Configuration for Evaluation of bq25070 EVM

Jack/Component (Silk Screen)	Connect or Adjustment TO:
J1-1 (VIN)	P/S positive lead, P/S preset to 5.1VDC; 1250mA current limit.
J1-2 (GND)	P/S negative lead, P/S preset to 5.1VDC;
J3-1/2 (VLDO/GND)	Connect 200 Ω resistor between pins
J2-1 (OUT)	Positive $LiFePO_4$ battery lead
J2-2 (GND)	Negative $LiFePO_4$ battery lead
S101 (Delivers Programmed Pulses)	Set in down position
JP1-1/2 (TS 10k “on board” pull-down)	Apply shunt to across pins 1 and 2 to connect 10k pull-down.
JP2-1/2 (CHG LED)	Apply shunt to across pins 1 and 2 to connect LED to CHG pin.
JP3-1.2 (Connects “Pulsed Hardware” to CTRL pin on IC)	Apply shunt to across pins 1 and 2 to connect pulse hardware to CTRL pin.
JP1xx-1/2 (Number of Pulse Selection)	Place only one shunt on JP101 to JP113 (Set to JP107 from factory) to select desired number of pulses.

Connect the meters, scope probes, output loads, shunt, and input power supply as listed in Table 1 and set scope to 2 ms/div, single sequence positive trigger; CH1 set to 500 mV/div and CH2 to 2 V/div; DC coupled on CH1 and CH2.



The circuit on this sheet is typically not part of the charger design.

This circuit generates the pulses to program the charge, which is normally done by the host. Use only one Shunt on JP101 through JP113. Place shunt according to desired program pluses. The 100 numbered components are part of the hardware for creating the programming pulses and are not typically part of an application.

Figure 1. EVM Schematic and Evaluation Setup
Top Schematic: Application Circuit
Bottom Circuit: Hardware Evaluation/Test Circuit to Generate Pulses to Program IC, done by host in Typical Application.

4.3 Test Procedure

1. Make sure that the EVM is set up according to Table 1 and Figure 1, and the power supply is preset to 5.1 VDC at ~1250 mA current limit.
2. Turn on input supply and verify the power supply current meter is between 0.26 A and 0.31 A. Note that this is a linear charger so the input current is approximately the output current minus any current going to VLDO. The battery voltage, DMM#1, should have increased slightly (few mV) due to the IR drop in the battery (I_{OUT} times mΩ of the cell).
3. Verify that the IMON pin is between 270 mV and 310 mV, DMM#3. The IMON output current is 1/1000 of the OUT current and is converted to a voltage using a 1k IMON resistor (1 V/1 A).
4. Verify that the CHG LED is lit.
5. Program the charger for ~0.95 A by placing a shunt on JP-111 (11 pulses - only one shunt on the JP1xx connectors at the bottom of the EVM) and toggling S100 From: Down TO: Up To: Down position.
6. Verify the power supply input current is between 0.93 and 0.98A. If current does not change, verify that the 11 pulses were generated and the pulse frequency is ~500 Hz, 50% duty cycle (see data sheet specification for further details). R106 can be adjusted to vary frequency (pulse width). See Figure 2 for example of transition. The figure was captured using a 4 quadrant supply (sinks and sources). See optional battery cell replacement in Figure 3.
7. Verify that the IMON pin is between 930mV and 980 mV, DMM#3.
8. Verify that the VLDO output, DMM2, is between 4.4 V and 5.4 V.
9. Remove Shunt JP1 and verify that charging stops (input current reduces to near 3mA due to VLDO load) and LED is flashing. This simulates a cold temperature fault.
10. Replace the JP1 shunt and verify the current returns to the default setting between 0.26 A and 0.31 A, (270 - 310 mV on DMM#3).
11. Short between J2 TS and GND and verify a hot temperature fault with the LED flashing. Remove short and verify that the current returns to the default setting between 0.26 A and 0.31 A.
12. Toggle S101 again to program the charge current to ~0.95A and let cell charge to completion. The OUT should charge to 3.6 V then go into float mode where the regulation will be reduced to 3.5 VDC, allowing the cell voltage to relax. This method of charging allows faster bulk charge.

NOTE: If the battery cell replacement circuit is used, the Cell voltage should be adjusted higher slowly, via the Battery P/S, until the OUT voltage reaches ~3.6 V and the charge current drops off. The OUT pin should relax some depending on the impedance of the diode in the battery cell replacement circuitry. The Battery P/S voltage may have to be lowered slightly, after output OV is reached, to get the OUT voltage to drop to the 3.5 V regulation

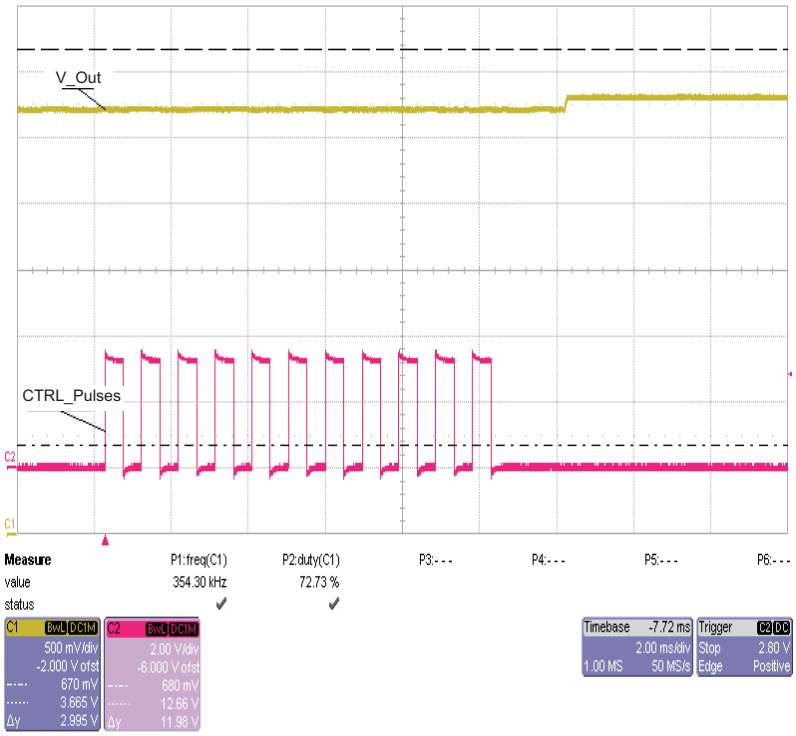


Figure 2. Pulse Programming – CH2: 11 pulses; CH1: V_{OUT} IR change due to increased charge current.

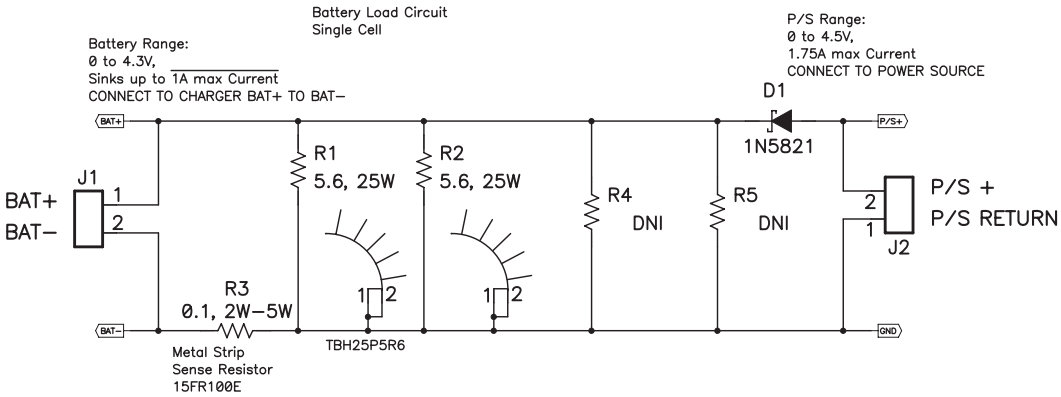


Figure 3. Battery cell Replacement – Allows quick battery adjustment

The P/S input to the right sets the BAT+ to BAT– voltage one diode drop below V_P/S,

R1 and R2 typically sink more than the charge current allowing the BAT+ voltage to drop unless pulled up by the P/S source thus allowing the P/S to set the battery voltage.

If a higher charge current is required, then a lower resistance is needed to adjust the battery voltage lower.

5 Schematic, Physical Layouts and Bill of Materials

5.1 Schematic

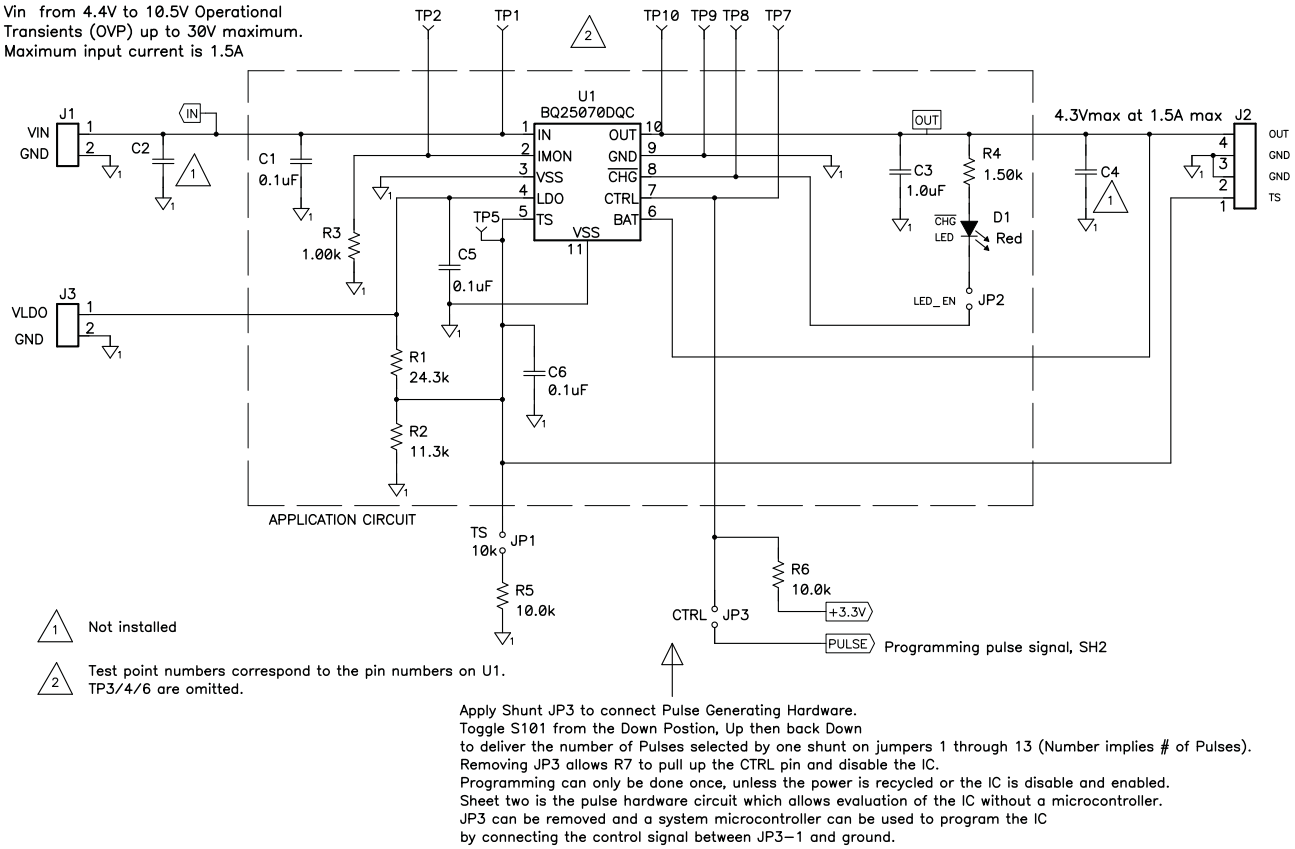


Figure 4. bq25070 EVM Board Schematic (Sheet 1 of 2)

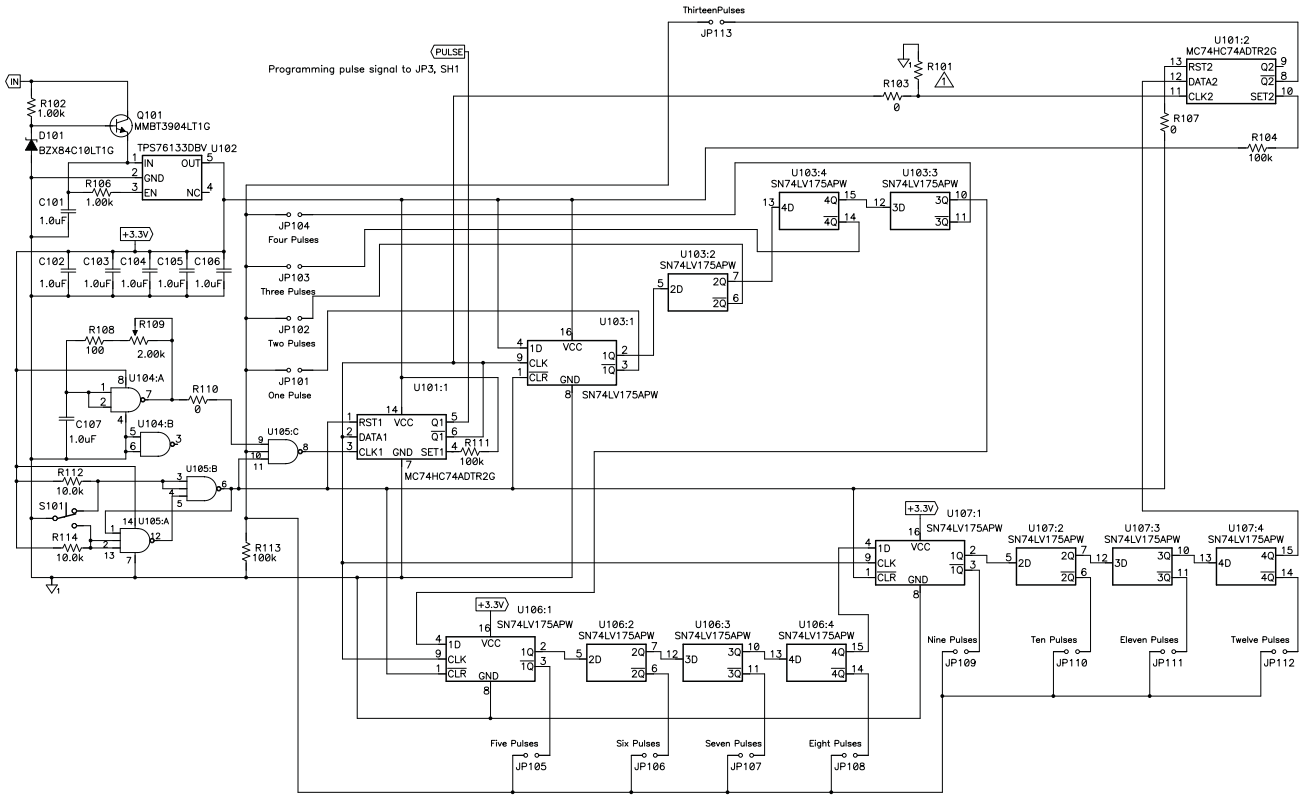


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Figure 5. bq25070 EVM Board Schematic (Sheet 2 of 2)

5.2 Physical Layouts

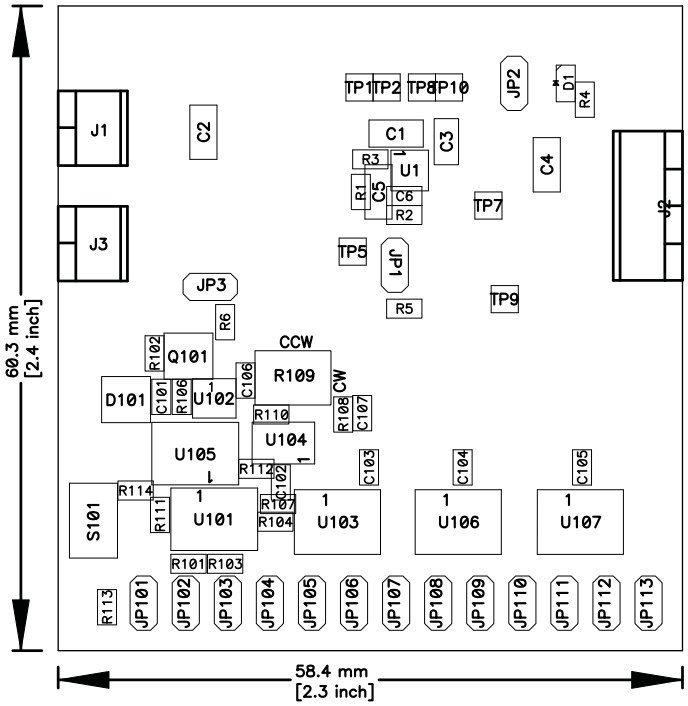

Figure 6. Assembly Layer

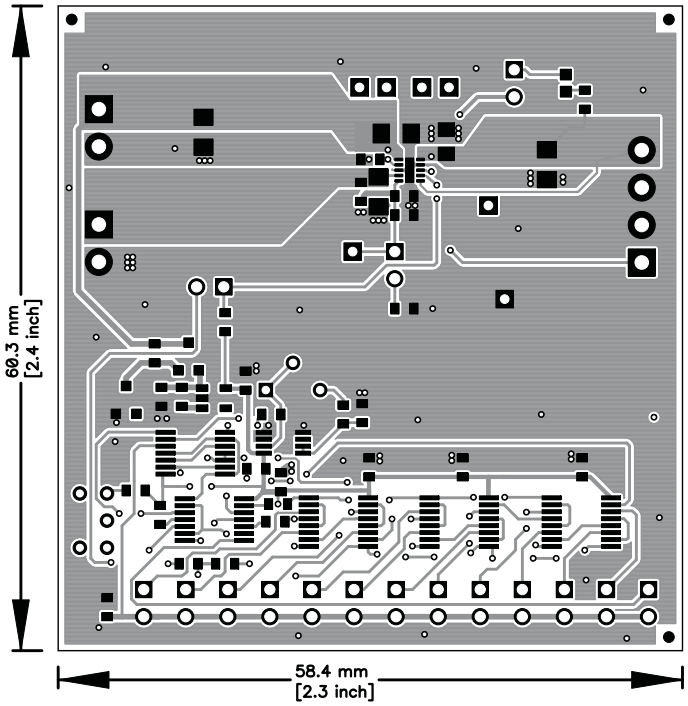

Figure 7. Top Layer

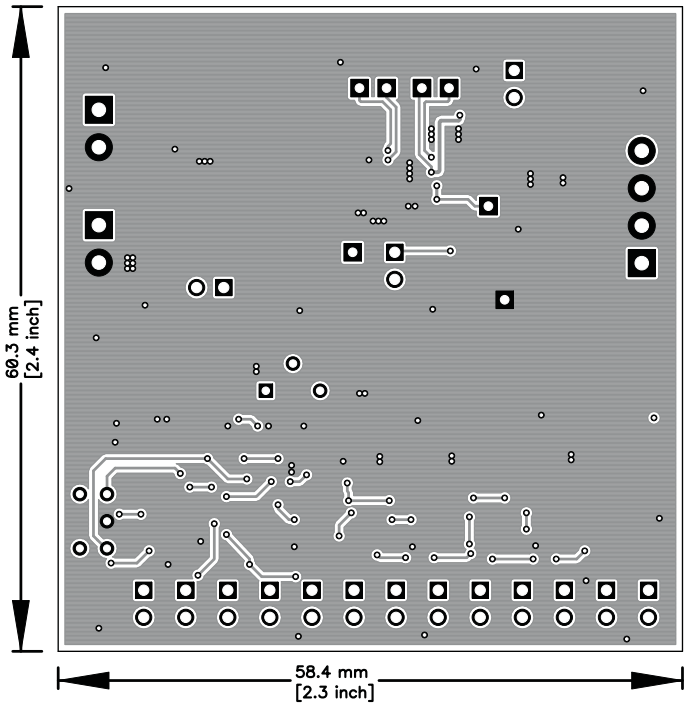

Figure 8. Bottom Layer

5.3 Bill of Materials

Table 2. HPA740A Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C5	0.1 µF	Capacitor, Ceramic, 25V, X7R, 10%	1206	Std	Std
0	C2, C4	Open	Capacitor, Ceramic, 25V, X7R, 10%	1206	Std	Std
1	C3	1 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
1	C6	0.1 µF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
7	C101, C102, C103, C104, C105, C106, C107	1 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	ECJ-1VB1A105K	Panasonic
1	D1	Red	Diode, LED, Red, 1.8-V, 20-mA, 20-mcd	0603	LTST-C190CKT	Liteon
1	D101	BZX84C10LT1G	Diode, Zener, 10-V, 350-mW	SOT-23	BZX84C10LT1G	On Semi
2	J1, J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	ED555/2DS	OST
1	J2	ED555/4DS	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25 inch	ED555/4DS	OST
16	JP1, JP2, JP3, JP101, JP102, JP103, JP104, JP105, JP106, JP107, JP108, JP109, JP110, JP111, JP112, JP113	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	Q101	MMBT3904LT1G	Bipolar, NPN, 40-V, 200-mA,225-mW	SOT23	MMBT3904LT1G	On Semi
1	R1	24.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R101		Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R102, R106, R3	1.00k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R103, R107, R110	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R104, R111, R113	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R108	100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R109	2.00k	Potentiometer, 1/4 in. Cermet, 12-Turn, Top-Adjust	0.25x0.17	3266W-1-202LF	Bourns
1	R2	11.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	1.50k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R5, R6, R112, R114	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	S101	G12AP	Switch, ON-ON Mini Toggle	0.28 x 0.18 inch	G12AP	NKK
0	TP1, TP2, TP5, TP7, TP8, TP9, TP10	Open	Test Point, O.032 Hole		STD	STD
1	U1	BQ25070DQC	IC, 1A, Single-Input, Single Cell LiFePO4 Linear Battery Charger with 50mA LDO	TDFN-10	BQ25070DQC	TI
1	U101	MC74HC74ADTR2G	IC, Dual D Flip Flop with Set and Reset	TSSOP	MC74HC74ADTR2G	On Semi
1	U102	TPS76133DBV	IC, Low-Power 100 mA LDO Regulator	SOT23-5	TPS76133DBV	TI
3	U103, U106, U107	SN74LV175APW	IC, Quad D-Flip Flop with Clear	TSSOP	SN74LV175APW	TI
1	U104	SN74LVC2G132DCTR	IC, Dual 2-Input NAND Gate With Schmitt-Trigger Inputs	SSOP-8	SN74LVC2G132DCTR	TI
1	U105	SN74HC10QPWREP	IC, Triple 3-Input Positive NAND Gate	TSSOP	SN74HC10QPWREP	TI
4	—		Shunt, 100-mil, Black	0.1	929950-00	3M
1	—		PCB, 2.4 In x 2.3 In x 0.031 In		HPA740	Any

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3.75 V to 10.3 V and the output voltage range of 0 V to 3 V and VLDO of 0 V to 5.4 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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