TIDA-00336: Design Considerations

Basics of Operation

The rolling LED design utilizes a TLC6C5912 shift register operated via two 555 timers contained in the TLC556 - one for the Shift Register Clock input and the other for the Serial-data Input. The duration of a single shift or step in the output pattern is defined by the period of the shift register clock, designed with an approximately 50% duty cycle. The output states of the shift register are regulated by the serial-data input from the second 555 timer. Utilizing two 555 timers for the logic inputs allow the LED patterns to remain periodic while still adjustable by the user.

The logic state of the serial-data input loads into the shift register on each rising edge of the shift register clock. Adjusting the external resistors of the 555 timer for serial-data will alter the output pattern of the shift register. The duty cycle of the serial-data signal defines the number of consecutive logic values in the output pattern, whereas the period of the serial-data input will define when the output pattern repeats. Adjusting the external resistors of the 555 timer for the shift register clock will alter the speed of the output pattern.

The TLC6C5912 has a maximum of 12 open drain outputs. In this application, a logic low on the serial input will result in a high output, as each drain is pulled high with 10k resistors.

Synchronization

To keep the two 555 timers synchronized, the shift register clock is designed to reset on each falling edge of the serial-data input signal via a coupling capacitor. This helps reduce undesirable behaviors in the output pattern occurring from variations in component tolerances. The value of this capacitor can be adjusted depending upon the desired frequencies of the two clocks. Omitting this capacitor could result in dropped or doubled sequencing in the output pattern, depending upon the external timing components.

Duty Cycle

This application utilizes a diode in parallel with R_b of the 555 circuit to reduce duty cycle restrictions. The following equations apply to both timers, where C is the timing capacitor.

$$T_H = .693 * R_a * C$$

$$T_L = .693 * R_b * C$$

Supply Voltage

Running the design at higher or lower supply voltages may alter the output frequencies and affect the output pattern. With a higher running frequency, the shift register clock is most susceptible to slight variations in timing. Maximum and minimum supply voltages and operating frequencies should be taken into consideration when selecting a pattern and designing for specific applications.

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