TIDA-00417 DS125BR820 40GbE/10GbE QSFP Reference Design – User's Guide

Version 2
May 2015

Table of Contents

1 Document Revision History

Revision	Comment	Date
1	• Initial creation of user's guide.	16-Dec-2014
2	• Added note regarding high-speed layout and the importance of avoiding crosstalk.	05-May-2015

2 Important Note Regarding TIDA-00417 PCB Routing

This PCB's high-speed signals have been routed using a trace width and trace spacing of ~7 mils and ~15 mils, respectively. As such, the inter-pair coupling (i.e. coupling from one differential pair to an adjacent differential pair) on this PCB is relatively high, which can lead to unwanted crosstalk.

It is therefore recommended to use more tightly-coupled routing with accordingly smaller trace width and spacing. For example, ~6 mil trace width and ~5 mil trace spacing would allow for better inter-pair isolation and reduced crosstalk. Steps should be taken to ensure the desired impedance (i.e. 100Ω differential) is maintained when adjusting the trace width and spacing.

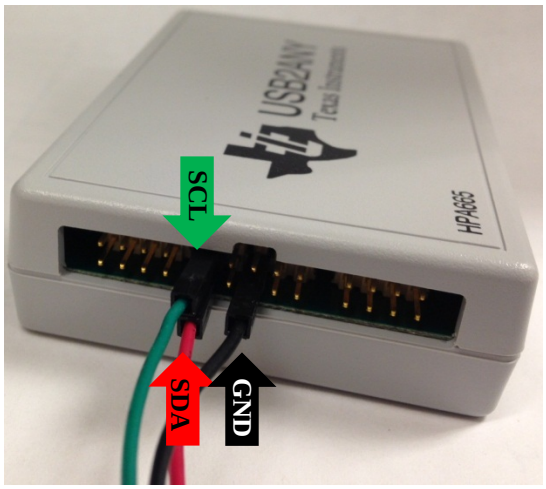
3 Software/Hardware Description and Setup

3.1 Procedure

The general procedure for setting up and testing with the TIDA-00417 Reference Design is as follows:

1. **(One-time step)** Install the TI SigCon Architect GUI software:
   a. If your PC already has the National Instruments runtime library, then you can download and install the stand-alone TI SigCon Architect: *http://www.ti.com/lit/zip/snlc055*
   b. If your PC *does not* have the National Instruments runtime library, then you can download and install the combined package: http://www.ti.com/lit/zip/snlc054

2. Connect the EVM to a PC and to the board (connector J1) using a USB2ANY dongle. The pins on the USB2ANY which correspond to I2C/SMBus are highlighted below. Connector J1 on the board has GND on pin 1, SCL on pin 3, and SDA on pin 4.



3. Connect power to the board. The DS125BR820 supports either 2.5V or 3.3V supply.
   a. 3.3V use case instructions:
      i. VDD_SEL pin on the DS125BR820 devices must be connected to GND. **Do this by setting SW9 position 1 to ON.**
      ii. Connect VIH to the VIN pins on the DS125BR820 devices. **Do this by placing a jumper between pins 1&2 on header J3.**
      iii. **Connect a 3.3V DC power supply (500mA max) between TP1 (VIN) and TP2 (GND)**

b. 2.5V use case instructions:
   i. VDD_SEL pin on the DS125BR820 devices must be floating. **Do this by setting SW9 position 1 to OFF.**
   ii. Connect VIH to the VDD pins on the DS125BR820 devices. **Do this by placing a jumper between pins 2&3 on header J3.**
   iii. **Connect a 2.5V DC power supply (650mA max) between TP3 (VDD) and TP2 (GND)**

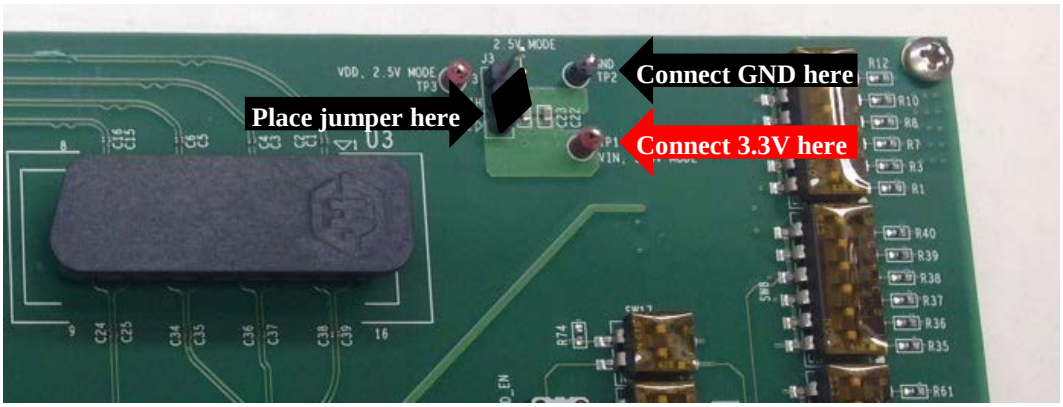


Figure 1: 3.3V mode connections (Note: SW9 position 1 must also be set to ON)

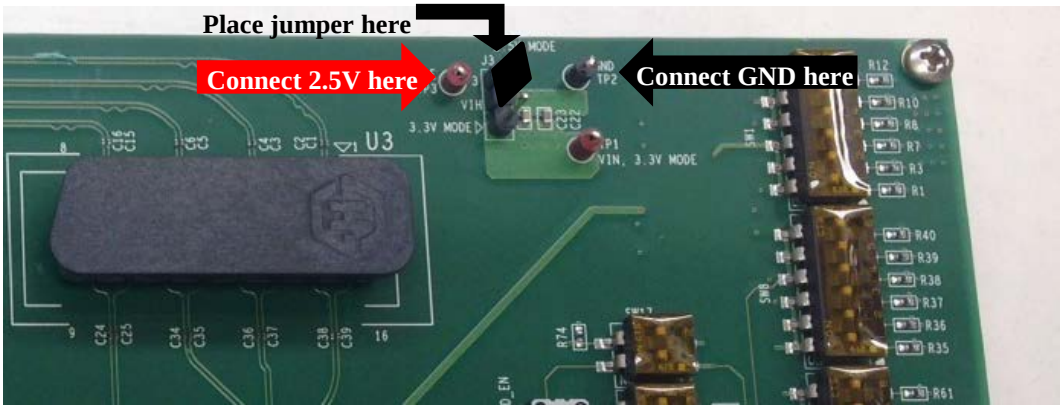


Figure 2: 2.5V mode connections (Note: SW9 position 1 must also be set to OFF)

4. Connect the high-speed signals between the QSFP+ port and the ASIC or scope. Likewise, connect the high-speed signals between the Huber+Suhner connectors and the ASIC or scope. This connection requires a Huber+Suhner 2x8 MXP cable assembly. Refer to Section 5 for more details.

This reference board has two 8-channel DS125BR820 devices, one to support all ingress signals, and one to support all egress signals from a stacked QSFP+ cage. The following table explains the mapping:

Table 1: Mapping between QSFP+ port and high-speed connectors

QFSP Port	QSFP Lane	Direction	Host-side Huber+Suhner connector pin P / N	Repeater channel	GUI Repeater address / channel
Top	1	Ingress	U4.4 / U4.3	U1.INB_3	0xB2, Ch3
		Egress	U4.13 / U4.14	U2.INA_0	0xB0, Ch4
	2	Ingress	U4.6 / U4.5	U1.INB_2	0xB2, Ch2
		Egress	U4.9 / U4.10	U2.INA_2	0xB0, Ch6
	3	Ingress	U4.2 / U4.1	U1.INA_0	0xB2, Ch4
		Egress	U4.11 / U4.12	U2.INA_1	0xB0, Ch5
	4	Ingress	U4.8 / U4.7	U1.INB_1	0xB2, Ch1
		Egress	U4.15 / U4.16	U2.INB_3	0xB0, Ch3
Bottom	1	Ingress	U3.15 / U3.16	U1.INA_3	0xB2, Ch7
		Egress	U3.5 / U3.6	U2.INB_2	0xB0, Ch2
	2	Ingress	U3.11 / U3.12	U1.INA_1	0xB2, Ch5
		Egress	U3.3 / U3.4	U2.INB_1	0xB0, Ch1
	3	Ingress	U3.13 / U3.14	U1.INA_2	0xB2, Ch6
		Egress	U3.8 / U3.7	U2.INA_3	0xB0, Ch7
	4	Ingress	U3.9 / U3.10	U1.INB_0	0xB2, Ch0
		Egress	U3.1 / U3.2	U2.INB_0	0xB0, Ch0

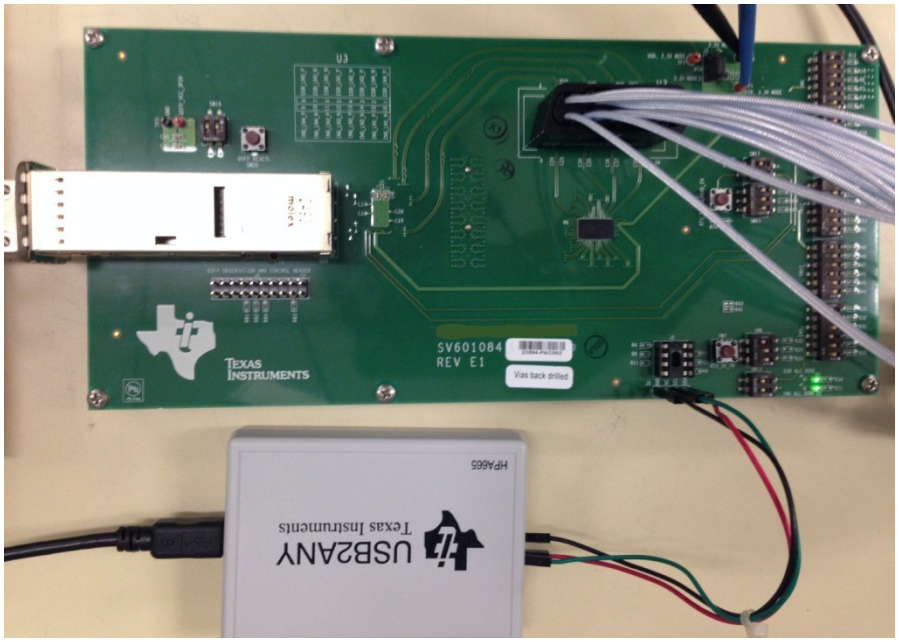


Figure 3: Example of Power, USB2ANY, and high-speed connections to the board

1. Launch the TI SigCon Architect GUI to control the two DS125BR820 devices on the board. As shown in Table 1, the Repeater at address 0xB0 is responsible for all the Egress channels (top and bottom port), and the Repeater at address 0xB2 is responsible for all the ingress channels (top and bottom port). Figure 4 shows an example of the SigCon architect GUI with the recommended default configuration for EQ and VOD.

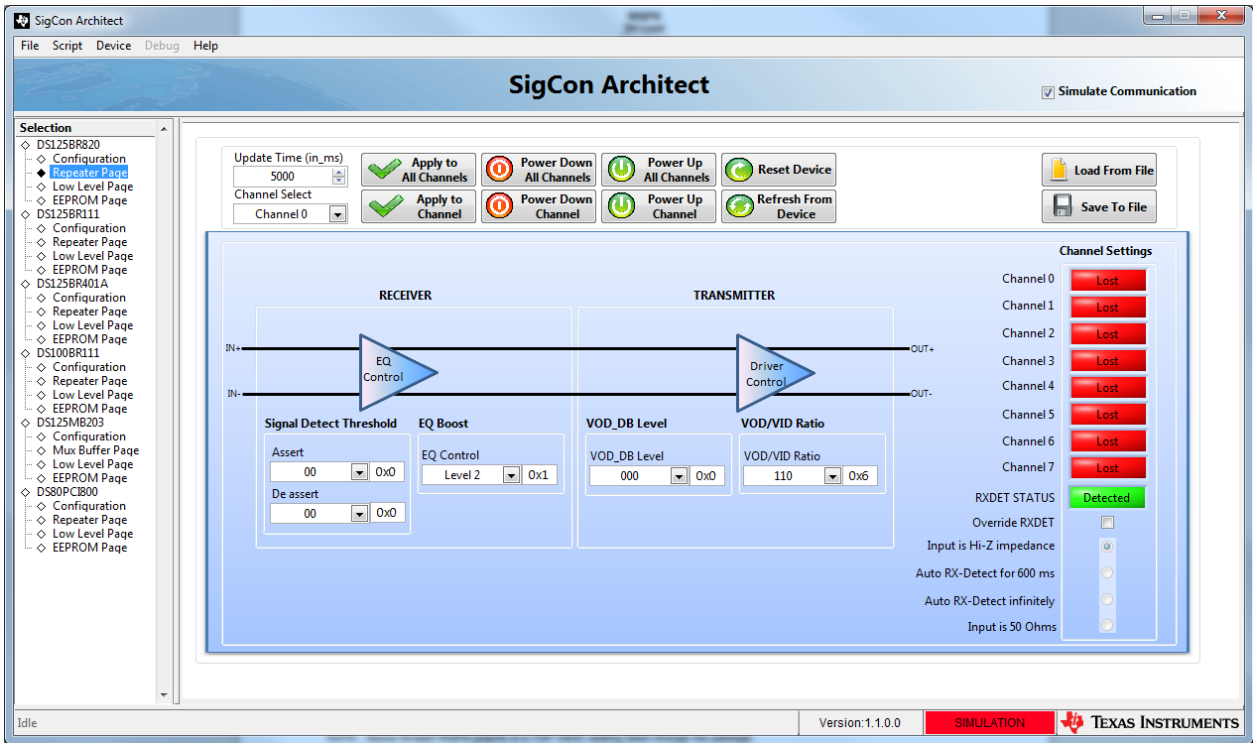


Figure 4: Example of TI SigCon Architect GUI, showing the recommended default configuration for EQ and VOD

3.2 Hardware notes

TI SigCon Architect GUI is the recommended means of configuring the devices on the board. The devices can also be configured via pin strapping using the switches available on the board. Table 2 lists the switches available, their function, and their recommended default state.

Table 2: Pin control switches

Switch #	Switch position(s)	Function	Recommended default state	Comment
SW1	1-3	Egress repeater AD3 / EQB pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
	4-6	Egress repeater AD2 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode. This must be 1K to GND in pin mode (OFF-OFF-**ON**)
SW2	1-2	Connects board I2C bus to Egress repeater I2C pins	**ON**-**ON**	Set to OFF if you want to disconnect the Egress repeater from the board I2C bus.
SW3	1-3	Egress repeater AD1 / VODB0 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
	4-6	Egress repeater AD0 / VODB1 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
SW4	1-3	Egress repeater VODA0 pin control	OFF-OFF-OFF	Floating by default since these pins are used as I2C in SMBus slave mode.
	4-6	Egress repeater VODA1 pin control	OFF-OFF-OFF	
SW5	1-3	Egress repeater EQA pin control	OFF-OFF-**ON**	EQ will be controlled in registers in SMBus slave mode.
	4-6	Egress repeater RESERVED3 pin control	OFF-OFF-**ON**	Can be floating, 1K to VDD, or 1K to GND
SW6	1-3	Egress repeater SD_TH pin control	OFF-OFF-**ON**	This pin not used in SMBus slave mode. Triggers EEPROM read in SMBus Master mode.
SW8	1-3	Egress repeater EN_SMB pin control	**ON**-OFF-OFF	EN_SMB=1 by default, to configure for SMBus slave mode. Set this to OFF-OFF-**ON** to enter pin control mode.
	4-6	Egress repeater RESERVED2 pin control	OFF-OFF-OFF	Pin is floating by default.
SW9	1	VDD select. ON : VDD_SEL=GND → 3.3V mode OFF: VDD_SEL=Float → 2.5V mode	**ON**	3.3V mode by default.
	2	Egress repeater PWDN pin control	**ON**	Set to ON for normal operation, OFF for powerdown.
SW10	1-3	Ingress repeater AD3 / EQB pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
	4-6	Ingress repeater AD2 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode. This must be 1K to GND in pin mode (OFF-OFF-**ON**)

Switch #	Switch position(s)	Function	Recommended default state	Comment
SW11	1-3	Ingress repeater VODA0 pin control	OFF-OFF-OFF	Floating by default since these pins are used as I2C in SMBus slave mode.
	4-6	Ingress repeater VODA1 pin control	OFF-OFF-OFF	
SW12	1-3	Ingress repeater AD1 / VODB0 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
	4-6	Ingress repeater AD0 / VODB1 pin control	OFF-OFF-**ON**	Used to set SMBus address since default is SMBus slave mode.
SW13	1-2	Connects board I2C bus to Ingress repeater I2C pins	**ON**-**ON**	Set to OFF if you want to disconnect the Ingress repeater from the board I2C bus.
SW14	1-3	Ingress repeater EQA pin control	OFF-OFF-**ON**	EQ will be controlled in registers in SMBus slave mode.
	4-6	Ingress repeater RESERVED3 pin control	OFF-OFF-**ON**	Can be floating, 1K to VDD, or 1K to GND
SW15	1-3	Ingress repeater SD_TH pin control	OFF-OFF-OFF	This pin not used in SMBus slave mode.
SW17	1	Connects Egress repeater ALL_DONE signal to Ingress repeater READ_EN signal so that repeaters can read from EEPROM in succession in SMBus Master mode	**ON**	
	2	Ingress repeater PWDN pin control	**ON**	Set to ON for normal operation, OFF for powerdown.
SW18	1-3	Ingress repeater EN_SMB pin control	**ON**-OFF-OFF	EN_SMB=1 by default, to configure for SMBus slave mode. Set this to OFF-OFF-**ON** to enter pin control mode.
	4-6	Ingress repeater RESERVED2 pin control	OFF-OFF-OFF	Pin is floating by default.
SW19	1-2	Connects QSFP I2C signals to the board I2C bus	OFF-OFF	QSFP I2C not connected by default.

4 Recommended DS125BR820 settings

In general, the Egress repeater is used to compensate for a portion of the host channel loss, specifically the loss which exceeds the SFF-8431 host channel specification. The Ingress repeater is also used to compensate for the host channel loss. If necessary, the Ingress repeater can be used to compensate for a portion of the passive copper cable. To avoid having to use settings specific to cable length, it is recommended that the Ingress repeater be configured to compensate only for the host channel loss.

The following settings have been shown to be generally good for most front-port QSFP+ applications.

Table 3: DS125BR820 settings used for Egress and Ingress testing

EQ Setting			VOD Setting			Comments
Value	**Pin strap**	**Equivalent register setting[1]**	**Value**	**Pin strap**	**Equivalent register setting[2]**	
Level 1	**0**: 1 kΩ to GND	Reg_0xF = 0x00	Level 6	VODA1= VODB1=**1** (1 kΩ to VIH) VODA0= VODB0=**0** (1 kΩ to GND)	Reg_0x10 = 0xAE	Different EQ settings used for different input channel length. VOD Level 6 used for all channels.
Level 2	**R**: 20 kΩ to GND	Reg_0xF = 0x01				
Level 3	**F**: Floating	Reg_0xF = 0x02				
Level 4	**1**: 1 kΩ to VIH	Reg_0xF = 0x03				

[1]Each channel has its own EQ control register. Reg_0x0F controls channel 0, Reg_0x16 controls channel 1, and so on.
[2]Each channel has its own VOD control register. Reg_0x10 controls channel 0. Reg_0x17 controls channel 1, and so on.

5 EVM Cable Assemblies

This reference design uses Huber+Suhner 2x8 MXP cable assemblies to access the host-side signals.

Contact Huber+Suhner to inquire about cable assembly availability and pricing.

There are two part numbers that TI suggests using with this EVM:

1. 84098901, MF53/2x8A_21MXP/11SK/229. This cable assembly is 9in long and terminates in "male" SMA connectors.
2. 84098908, MF53/2x8A_21MXP/21SK_ergo/305. This cable assembly is 9in long and terminates in "female" SMA connectors.

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