Test Data
For PMP9476 RevC
1/23/2015

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1. Design Specifications

Vin Minimum	**4VDC**
Vin Maximum	**40VDC**
Vout	**+5VDC @ 3A**
Nominal Switching Frequency	**≈ 300kHz**

2. Circuit Description

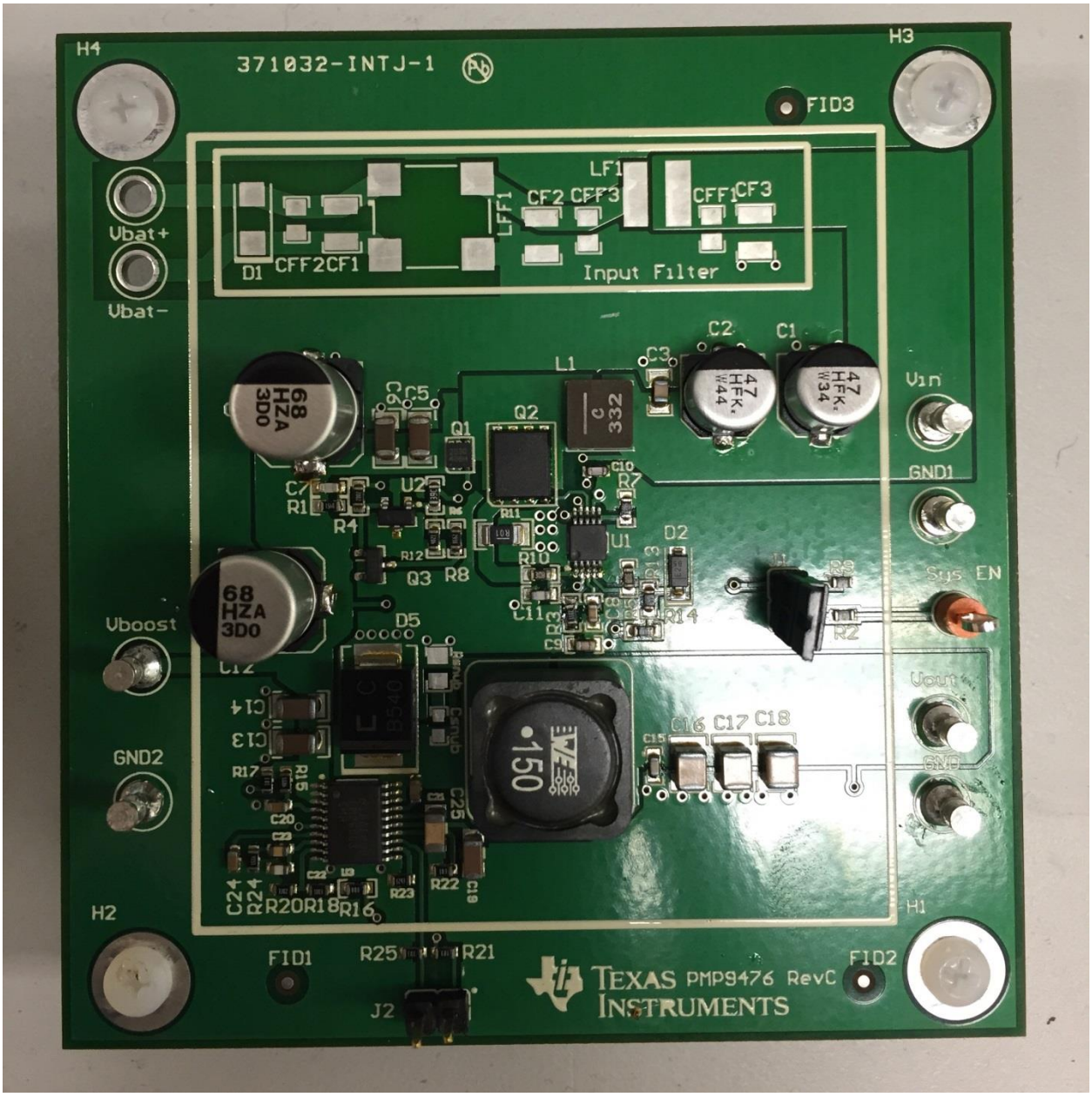
PMP9476 is a non-synchronous buck converter with integrated high side FET, using the LM26003 regulator IC. The design accepts an input voltage of 4V to 40V and provides one output of +5V, capable of supplying 5A current. The nominal switching frequency of the design is 300kHz. The board is a 4-layer PCB with 1oz copper on all 4 layers. All tests for oscilloscope waveform captures were performed between 4Vin and 12Vin. Efficiency testing was performed at 4Vin, 12Vin. The design incorporates an LM3481 boost controller acts as a pre-boost stage for the LM26003 buck when start-stop occurs.

The high side rectifier diode of LM3481 is replaced with a PFET, the turn on and turn off of the PFET is controlled by the input voltage. LMV431 controls the gate of the synchronous PFET Q1, when Vin is above 9V, the LMV431 is turned on and the gate of Q1 is pulled to GND which turns on the PFET. When Vin drops below 9V, the LMV431 turns off and the PFET gate is floating to the same potential as the source with some leakage. Which means only the body diode is conducting. The PFET Q1 turns off before the LM3481 exits out OVP and start switching, which ensures no short circuit happens. The resistor divider network between the source and gate sets the Vgs threshold of PFET Q1. Additional logic NFET Q3 and R8 are added to incorporate a hysterias to the LMV431 turn on threshold when Vin rises. When the Q1 gate is floating, the NFET Q3 is on, where R8 and R12 are in parallel which alters the turn on threshold of LMV431. The LMV431 will conduct (pull the Q1 gate low) at a higher voltage of 9.4V to ensure the LM3481 stops switching before PFET Q1 conducting.

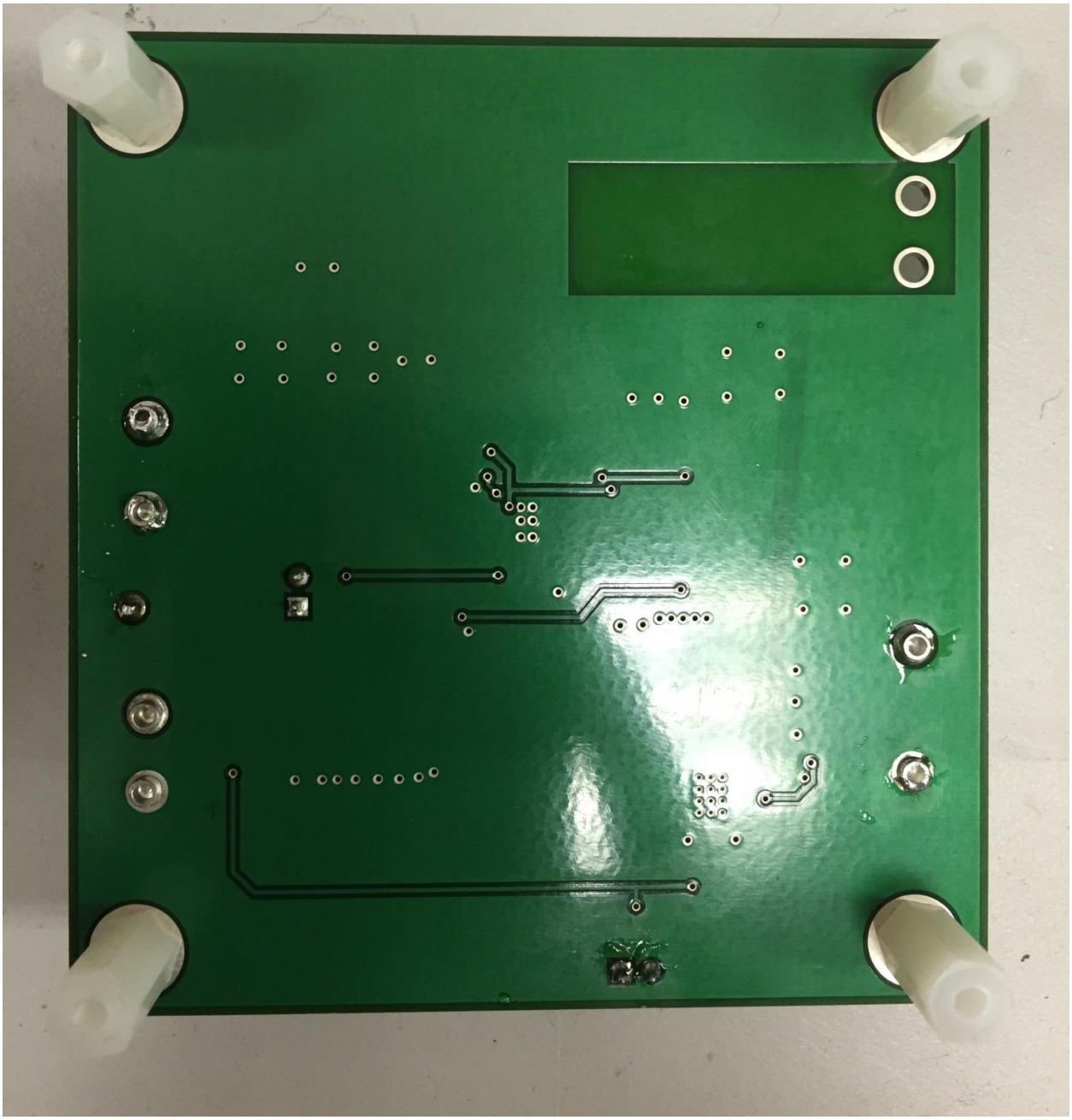
Since an external flag signal from the processor can trigger the wake up of LM3481 when start-stop sequence is initialized. A system enable jumper is implemented to the design to improve robustness of the design. 1.43V of LM3481UVLO enable threshold allows 3.3V flag signal to wake up the device properly.

3. PMP9476 Board Photos

Board Dimensions: 77mm x 79mm



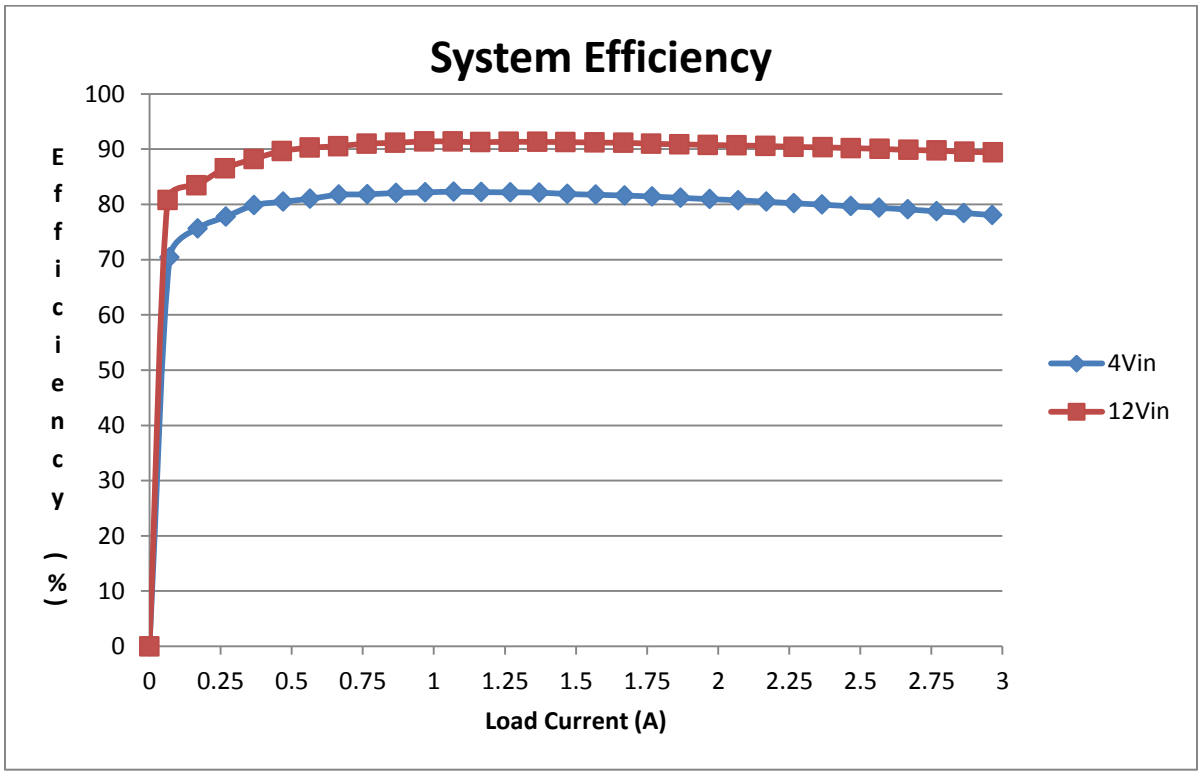
Board Photo (Top)



Board Photo (Bottom)

4. Efficiency

4.1 Efficiency Chart



4.2 Efficiency Data

Vin(V)	Iin(A)	Vout(V)	Iout(A)	Efficiency(%)
4.003	0.004	4.999	0	0
4.003	0.126	5.001	0.071	70.398
4.003	0.281	5.004	0.17	75.627
4.003	0.43	4.977	0.269	77.78
4.003	0.573	4.977	0.368	79.85
4.003	0.726	4.977	0.47	80.49
4.002	0.867	4.976	0.565	81.028
4.002	1.013	4.976	0.666	81.746
4.002	1.164	4.976	0.766	81.824
4.003	1.313	4.976	0.867	82.082
4.003	1.467	4.975	0.97	82.177
4.002	1.616	4.975	1.07	82.311
4.002	1.764	4.974	1.167	82.224
4.002	1.919	4.974	1.269	82.189
4.002	2.073	4.973	1.37	82.123
4.002	2.229	4.973	1.469	81.894

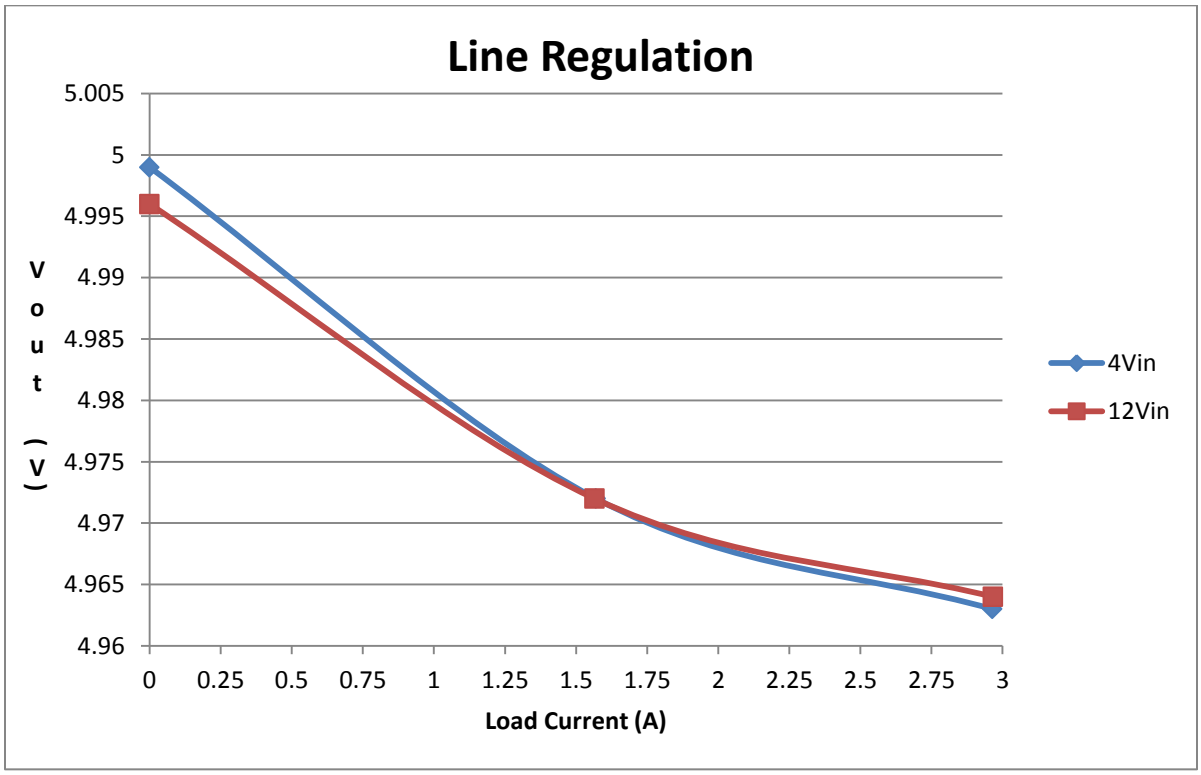
4.002	2.386	4.972	1.57	81.749
4.002	2.544	4.972	1.671	81.604
4.002	2.697	4.971	1.768	81.427
4.002	2.858	4.971	1.868	81.186
4.002	3.022	4.97	1.97	80.956
4.002	3.183	4.969	2.07	80.747
4.002	3.346	4.969	2.169	80.487
4.002	3.507	4.968	2.266	80.21
4.002	3.671	4.967	2.365	79.958
4.002	3.841	4.966	2.466	79.667
4.002	4.011	4.966	2.566	79.384
4.002	4.184	4.965	2.667	79.081
4.002	4.36	4.964	2.768	78.747
4.002	4.528	4.963	2.864	78.439
4.002	4.708	4.963	2.964	78.074

12.002	0.004	4.996	0	0
12.002	0.033	5	0.064	80.795
12.002	0.082	4.976	0.165	83.425
12.002	0.127	4.976	0.265	86.511
12.002	0.172	4.976	0.366	88.223
12.002	0.215	4.975	0.465	89.651
12.002	0.259	4.975	0.564	90.265
12.002	0.304	4.975	0.664	90.539
12.001	0.348	4.975	0.764	91.01
12.002	0.393	4.975	0.864	91.13
12.001	0.438	4.974	0.966	91.41
12.001	0.484	4.974	1.067	91.371
12.001	0.528	4.973	1.163	91.274
12.001	0.573	4.973	1.263	91.338
12.001	0.619	4.973	1.364	91.311
12.001	0.664	4.972	1.463	91.283
12.001	0.711	4.972	1.565	91.192
12.001	0.757	4.971	1.666	91.16
12.001	0.803	4.971	1.764	90.993
12.001	0.849	4.97	1.863	90.875
12.001	0.896	4.97	1.964	90.776
12.001	0.943	4.969	2.065	90.669
12.001	0.99	4.969	2.166	90.589
12.001	1.037	4.968	2.265	90.418

12.001	1.085	4.967	2.368	90.329
12.001	1.132	4.967	2.467	90.199
12.001	1.18	4.966	2.568	90.054
12.001	1.229	4.966	2.669	89.864
12.001	1.276	4.965	2.768	89.746
12.001	1.324	4.964	2.866	89.537
12.001	1.372	4.964	2.966	89.419

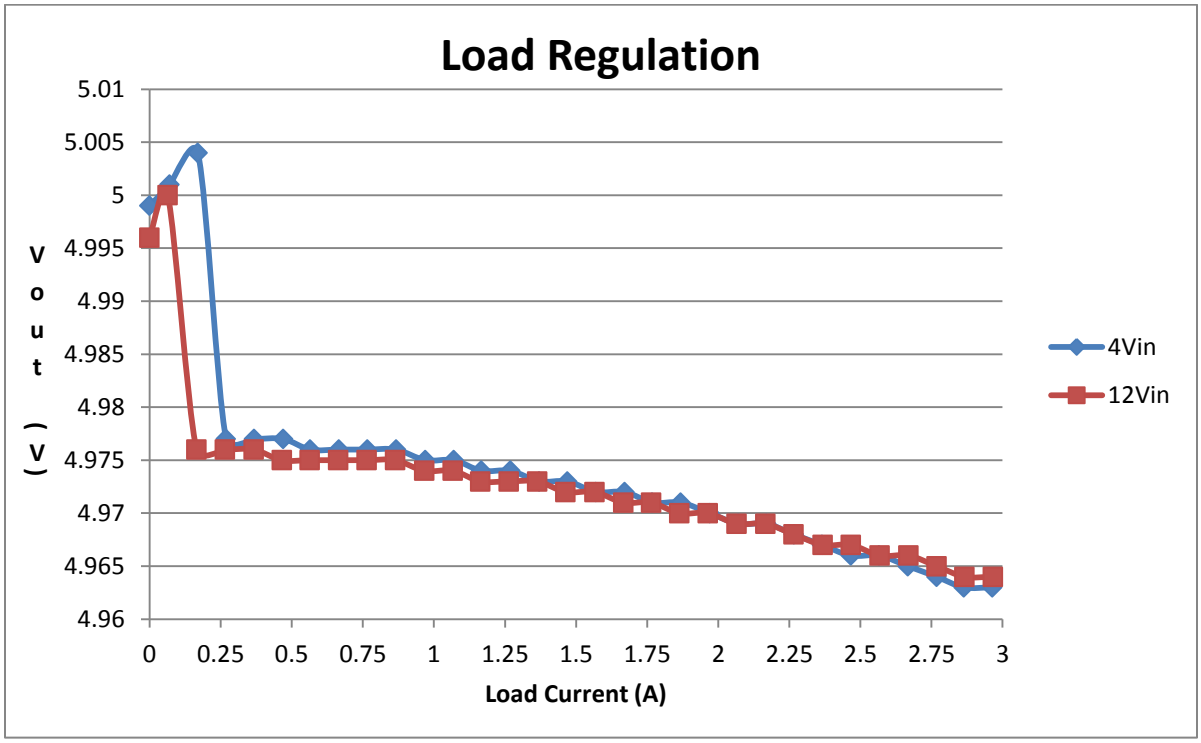
5 Output Voltage Regulation

5.1 Line Regulation

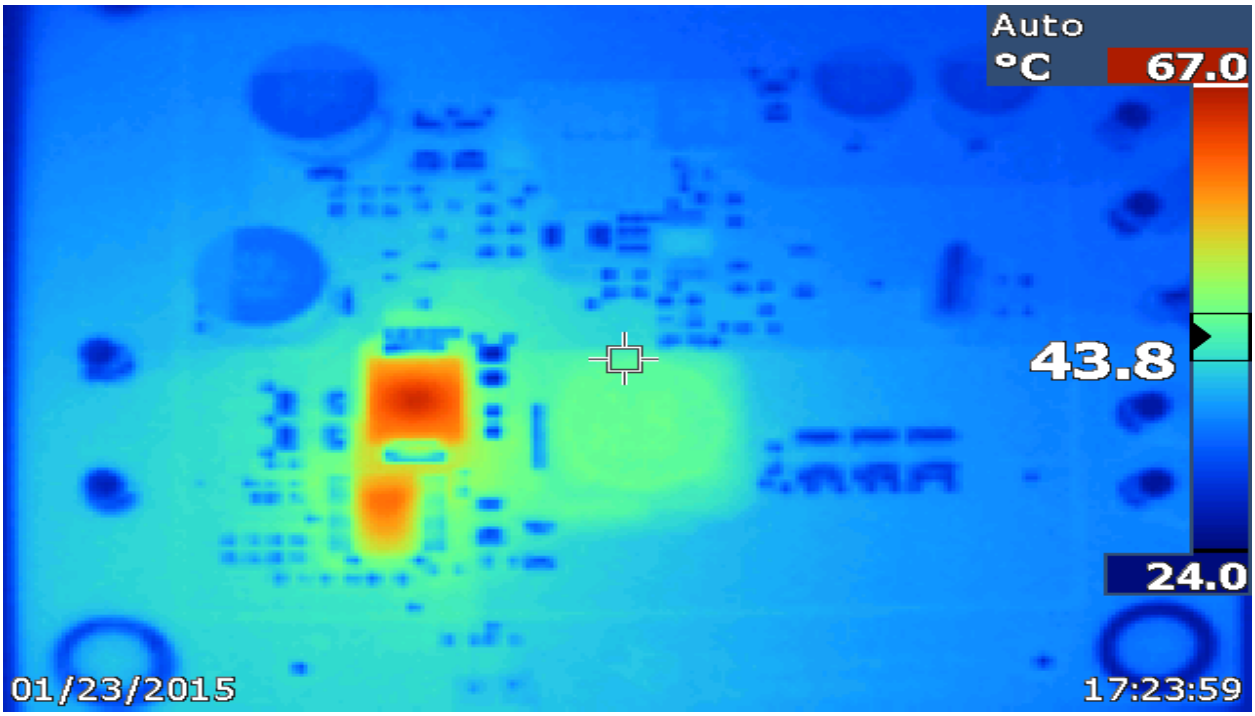


4Vin	Iout(A)	12Vin	Iout(A)
4.999	0	4.996	0
4.972	1.57	4.972	1.565
4.963	2.964	4.964	2.966

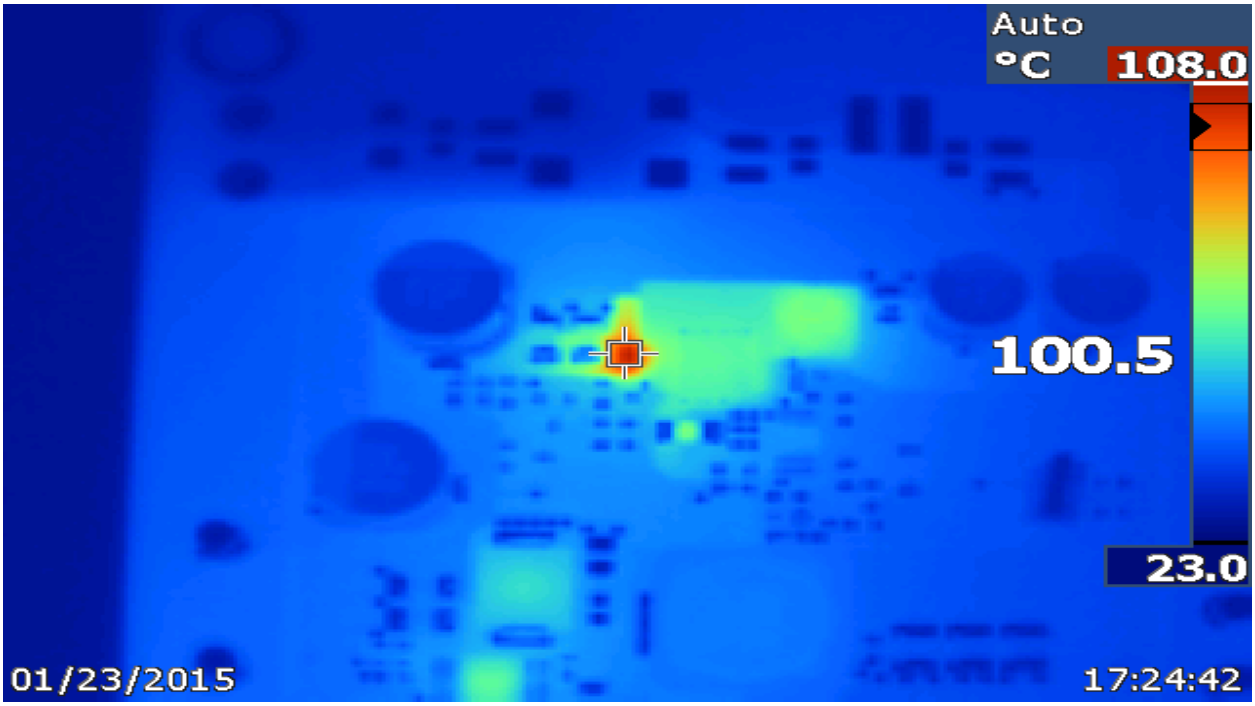
5.2 Load Regulation



6 Thermal Images



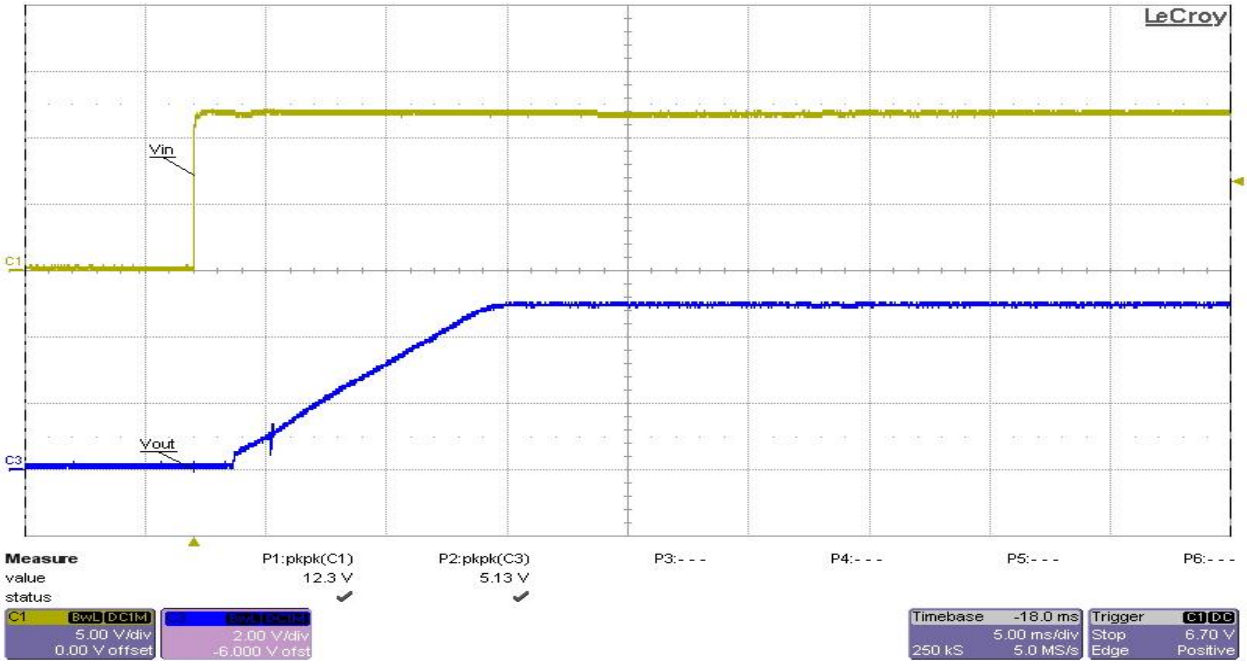
IR Thermal Image Taken at Steady State at 12Vin and Output at Full Loads



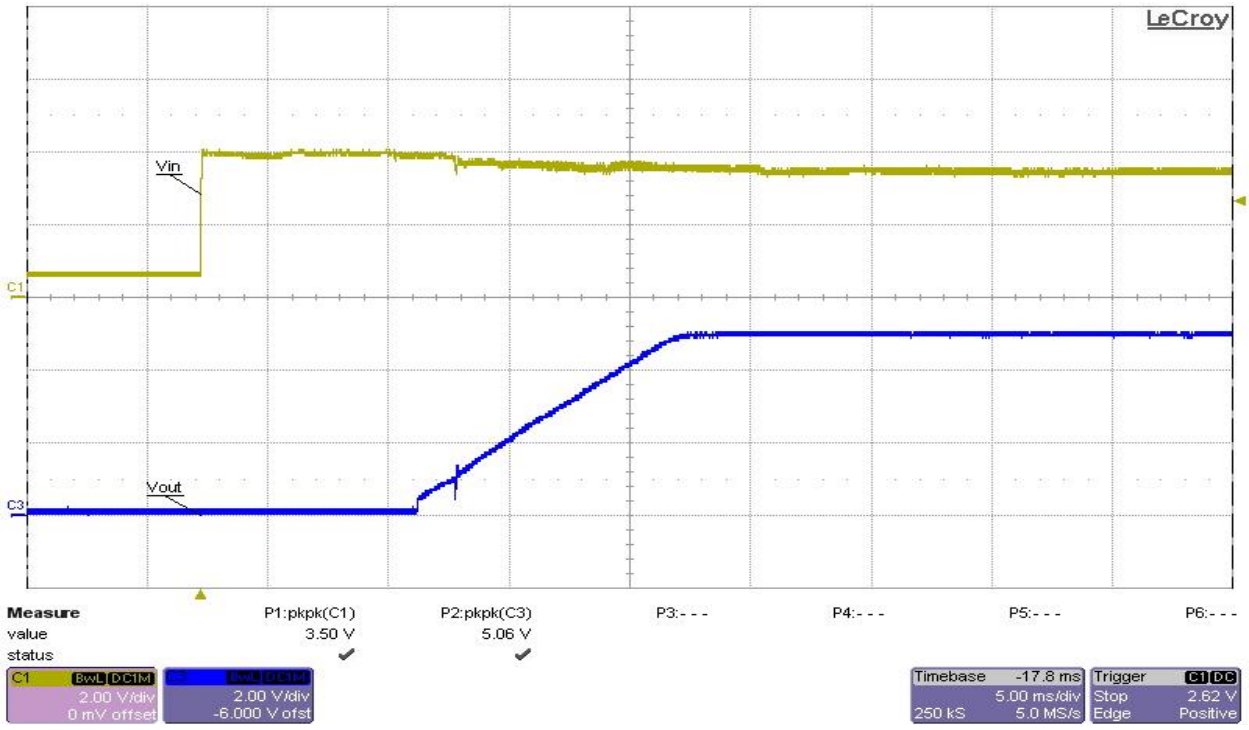
IR Thermal Image Taken at 4Vin and Output at Full Load for 10s.

7 Waveform

7.1 Start-Up

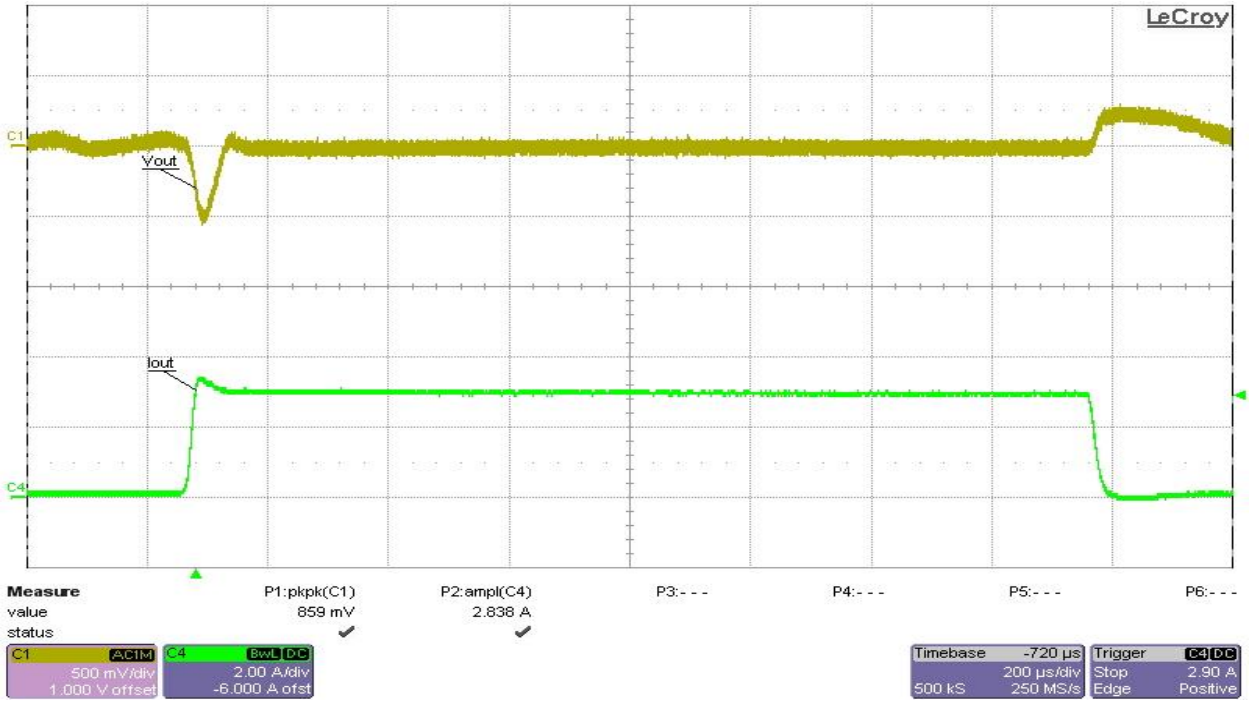


Startup into Full Load at 12Vin, Ch1 input, Ch3 Vout.

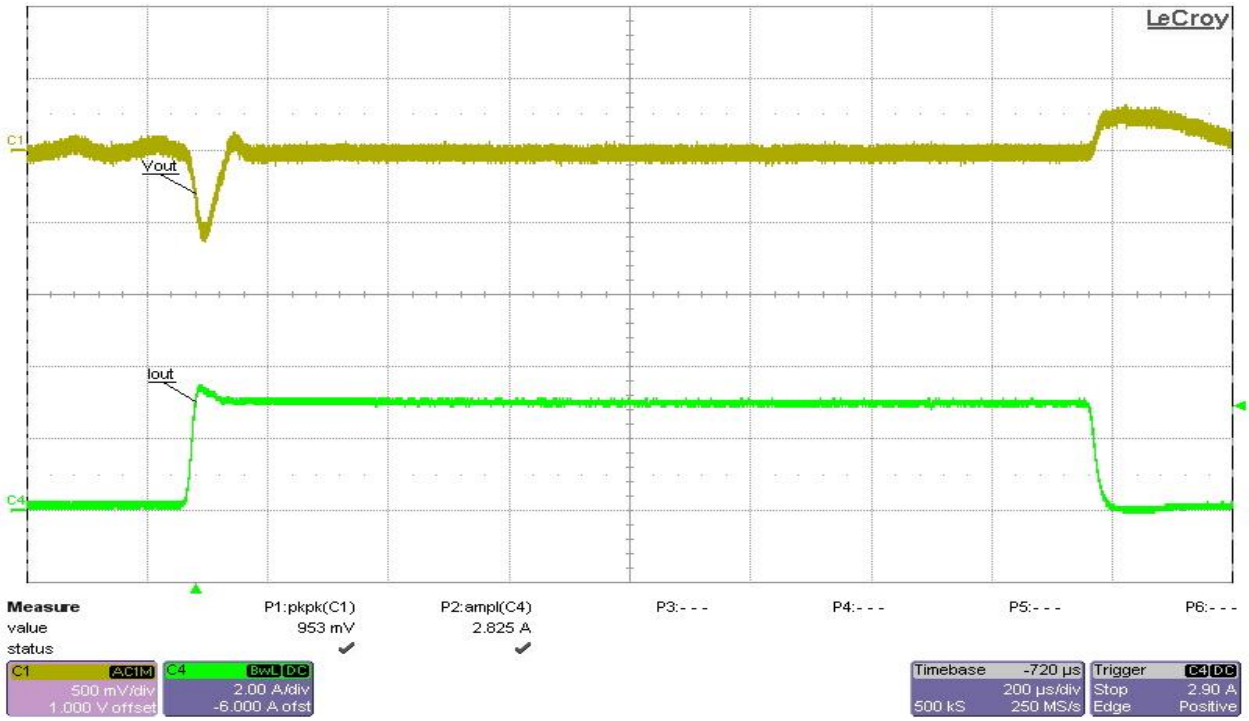


Startup into Full Load at 4Vin, Ch1 input, Ch3 Vpri.

7.2 Load-Transient

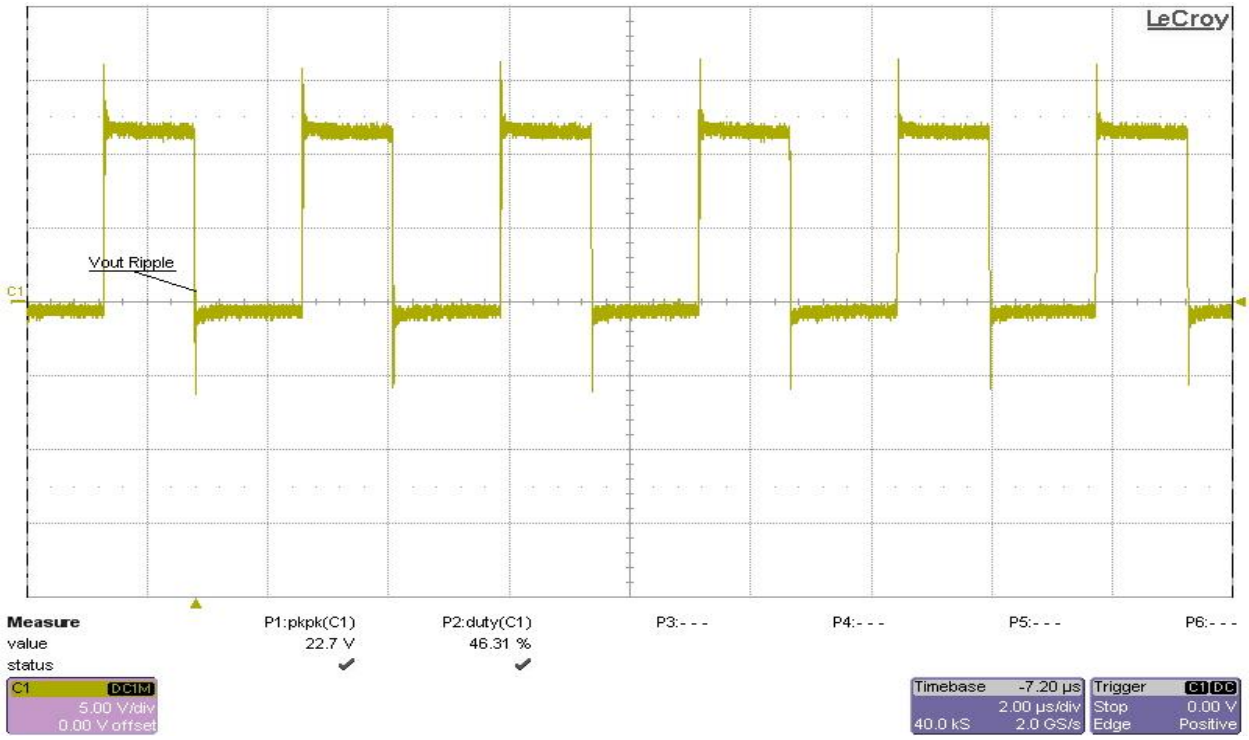


Load Transient Response of Vout Rail Undergoing 0% to 100% Load Step at 12Vin. Ch4 is load current, Ch1 is Vout AC coupled.

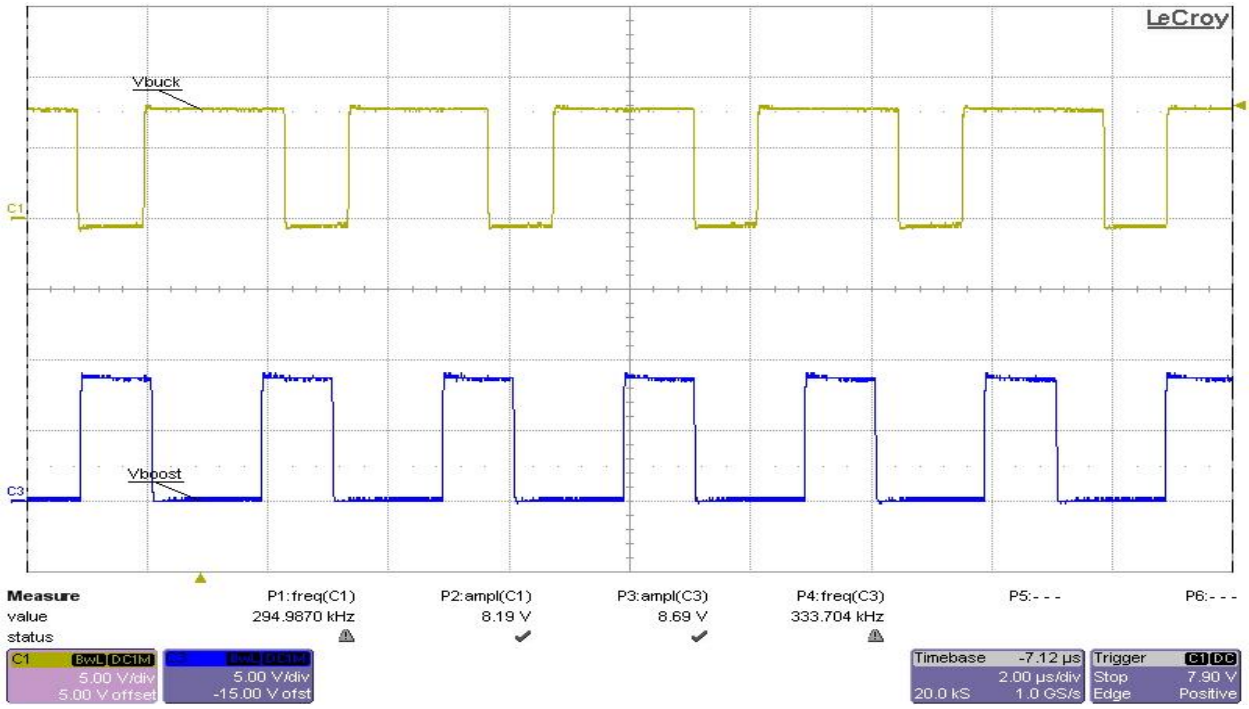


Load Transient Response of Vout Rail Undergoing 0% to 100% Load Step at 4Vin. Ch4 is load current, Ch1 is Vout AC coupled.

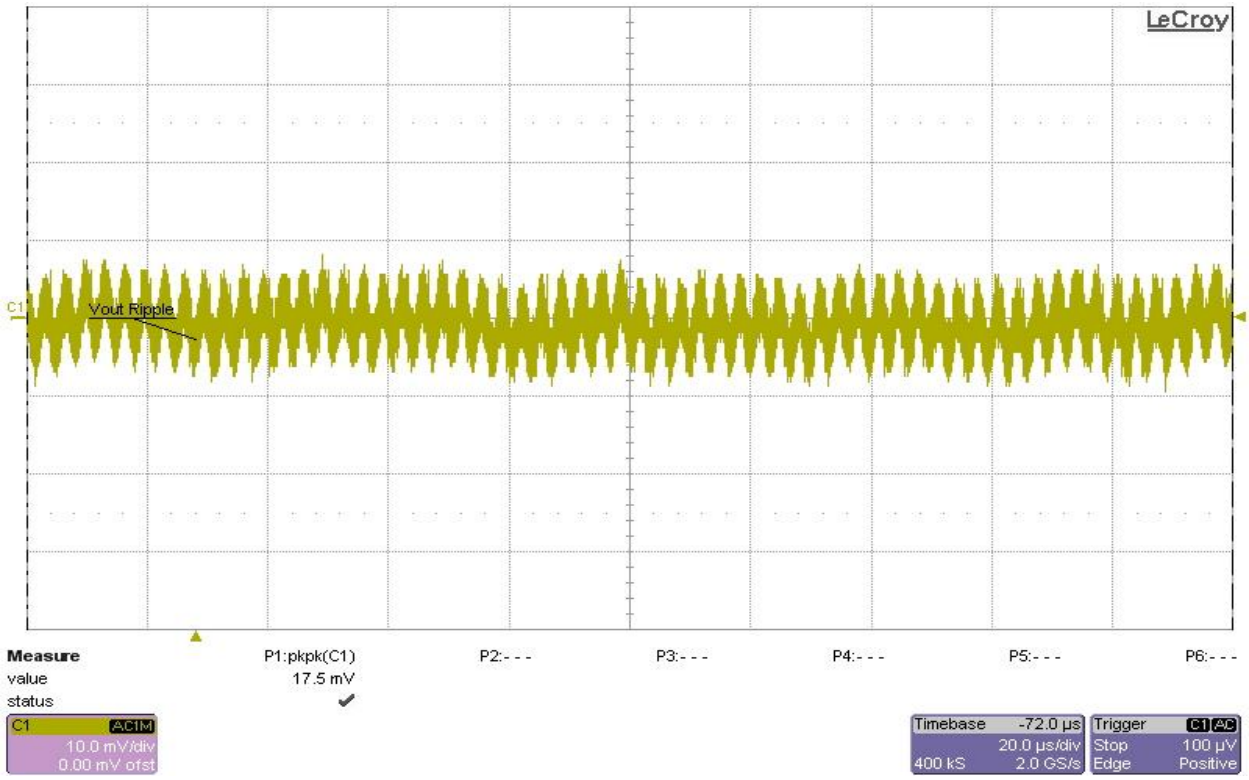
7.3 Switching Waveform and Output Ripple



12Vin, 100% load. Ch1 measures LM26003 switching waveform

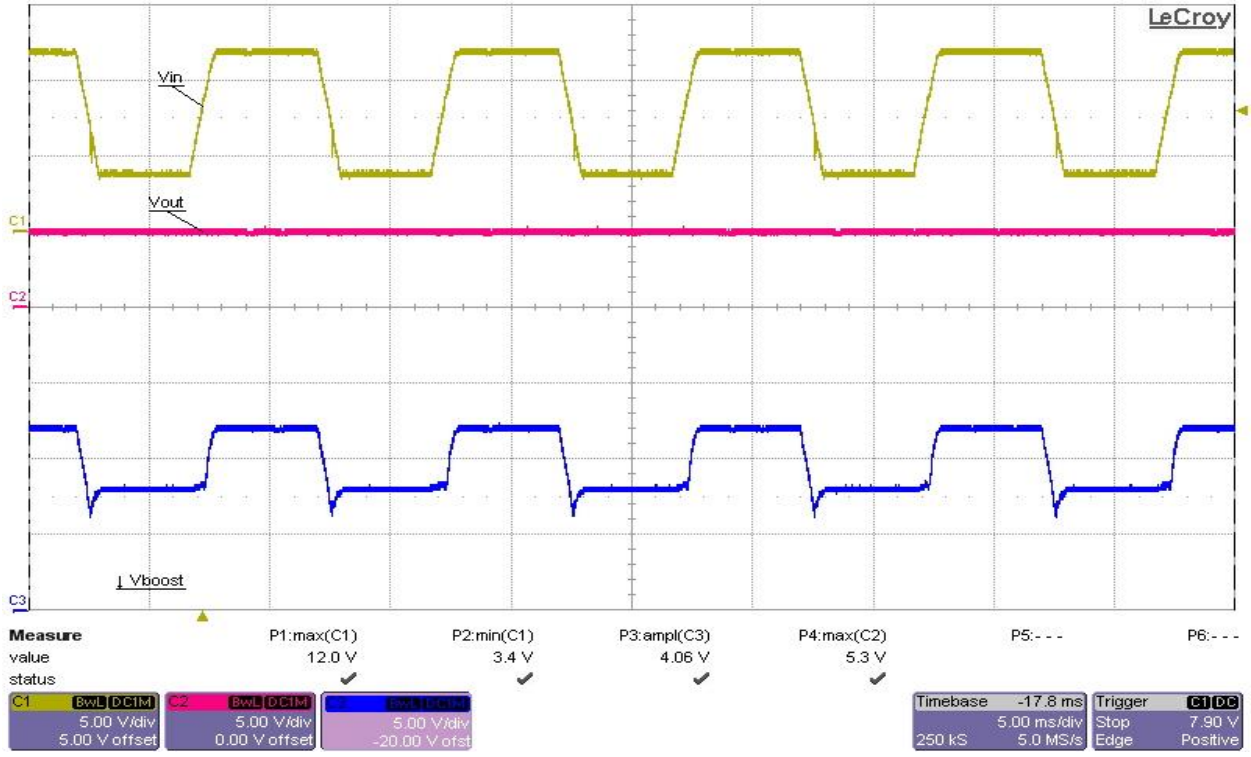


4Vin, 100% load. Ch1 measures LM26003 buck switch waveform, Ch3 measures LM3481 boost switch waveform.



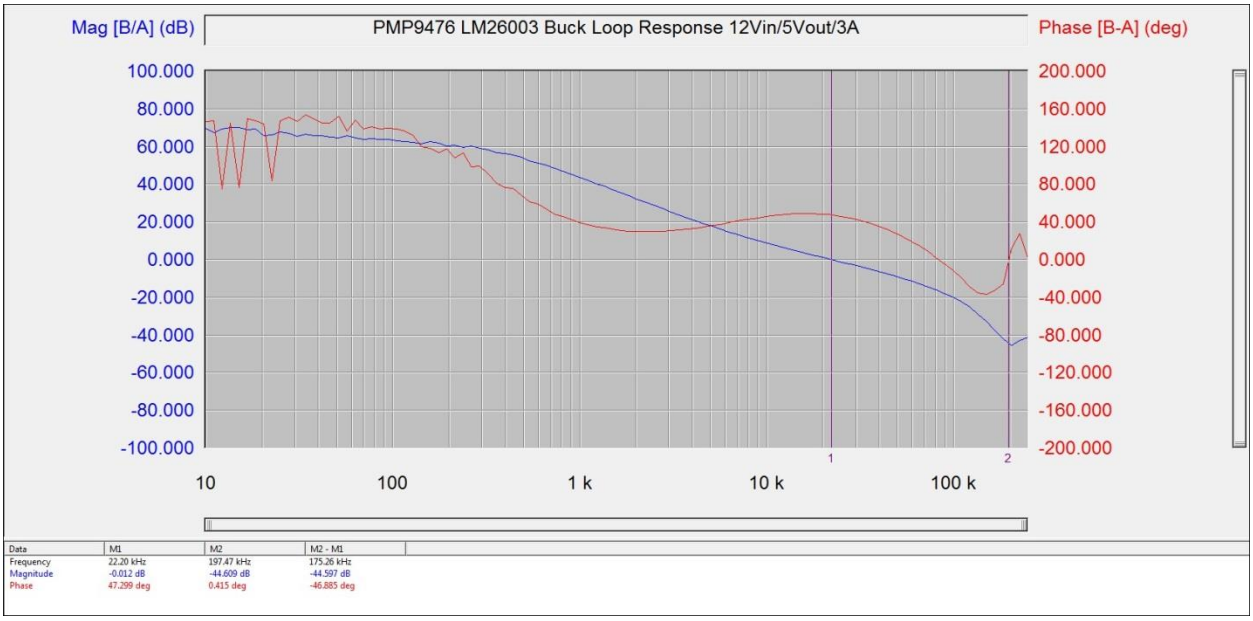
12Vin, 100% load. Ch1 measures LM26003 buck output ripple.

7.4 Line Transient



Ch1 measures input voltage, Ch2 measure buck output, Ch3 measures boost output. Output is 100% loaded, and input rise time and fall time are set at 1ms.

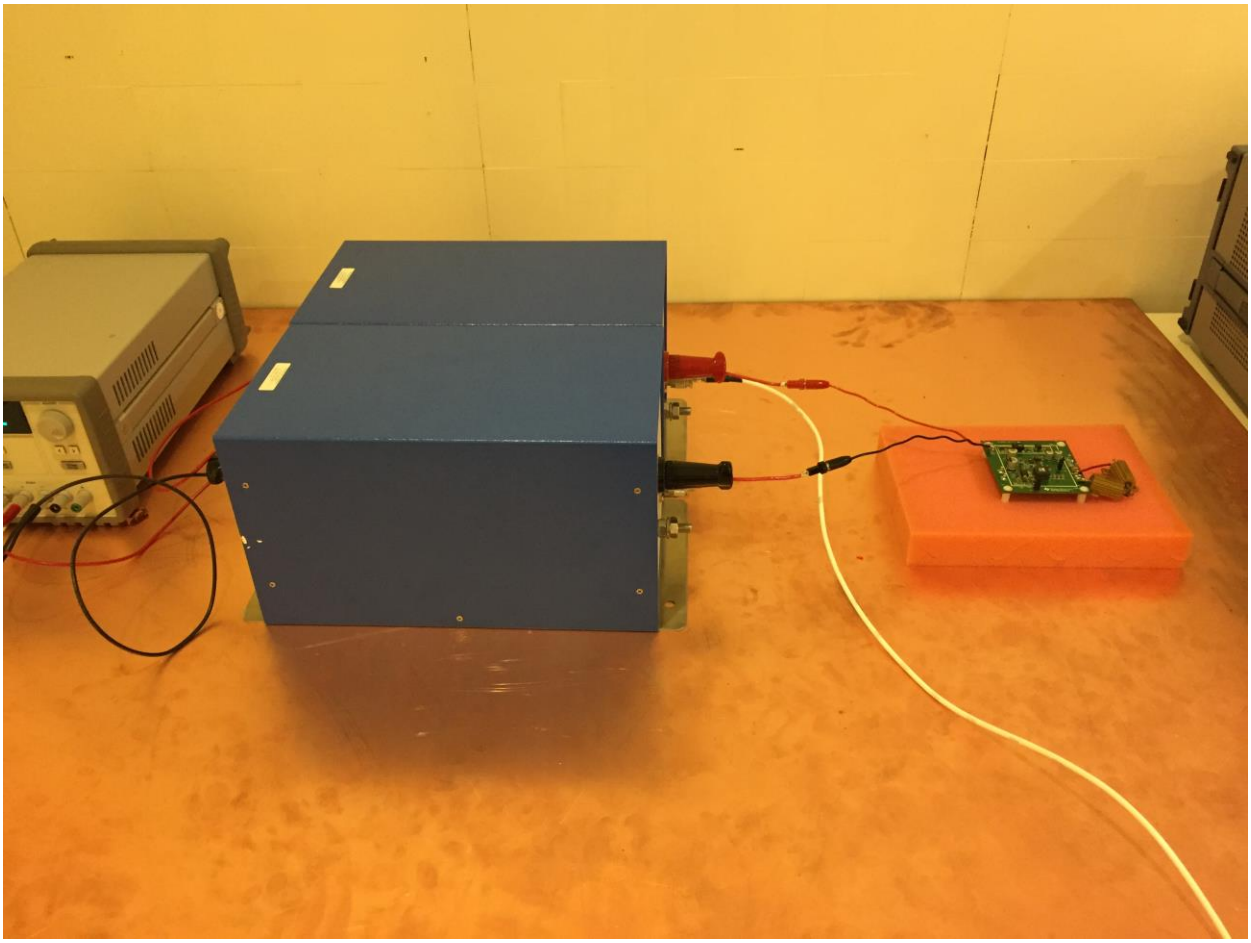
7.5 LM26003 Loop Response



LM26003 loop response is measured at 12Vin, 5Vout, fully loaded at 3A.

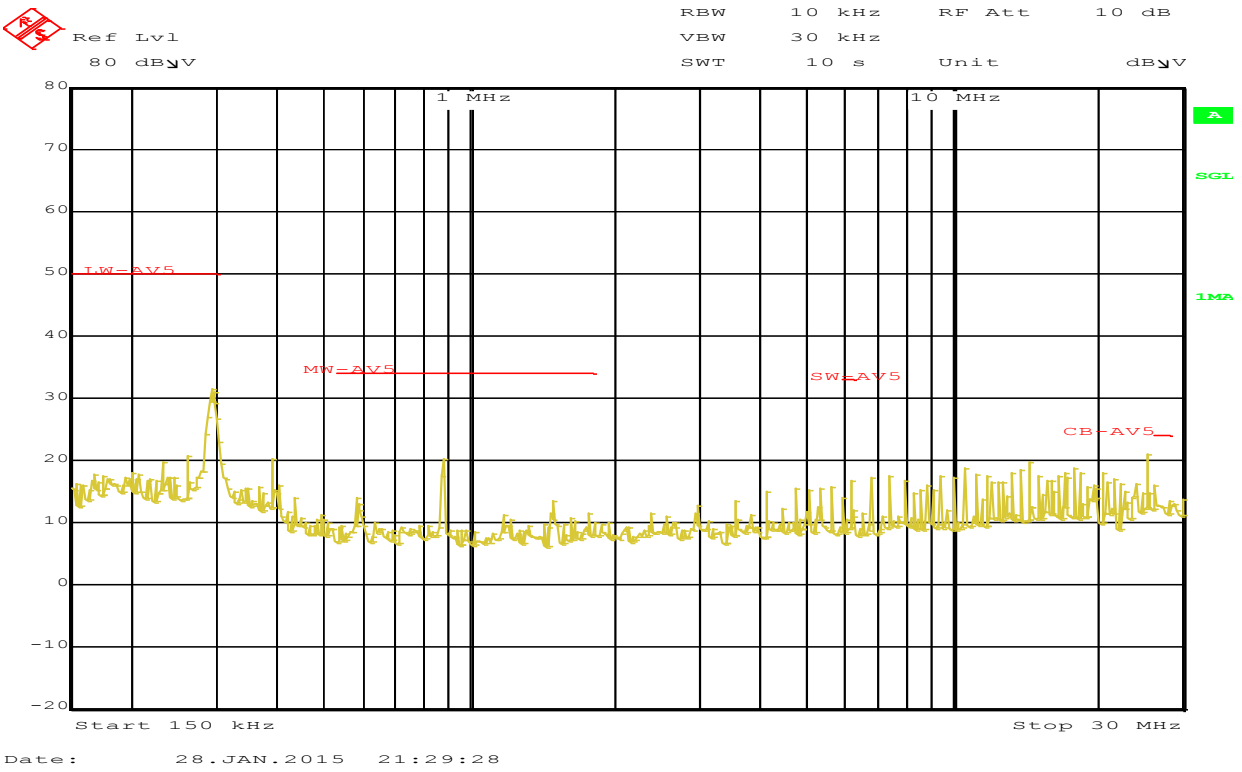
7.6 Conducted EMI

The tested board has the common mode choke and the filter inductor bypassed. The conducted emissions are tested under the CISPR 25 standards. The frequency band examined spans from 150 kHz to 108 MHz covering the AM, FM radio bands, VHF band, and TV band specified in the CISPR 25. The test setup is shown below: the input voltage is fed to the test board through two CISPR 25 compliant LISNs (Line Impedance Stabilization Networks), and the resistor loads are soldered on the output terminals of the test board.

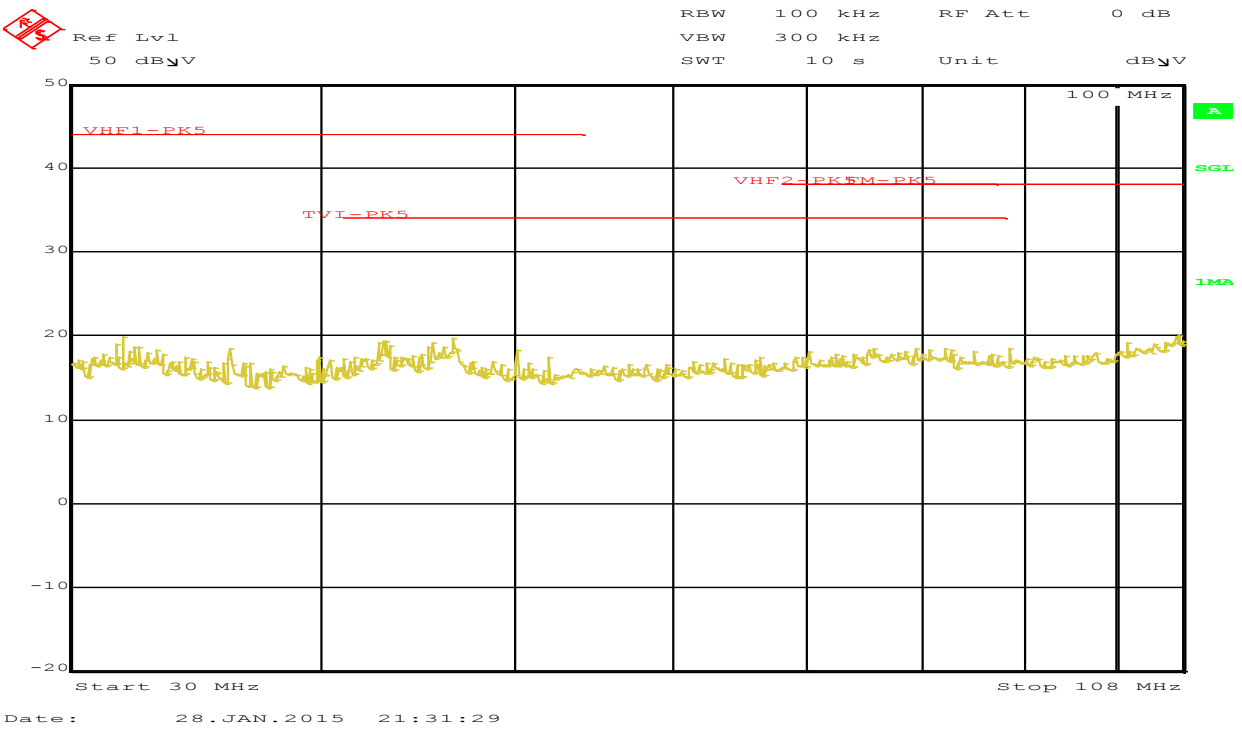


Test Setup

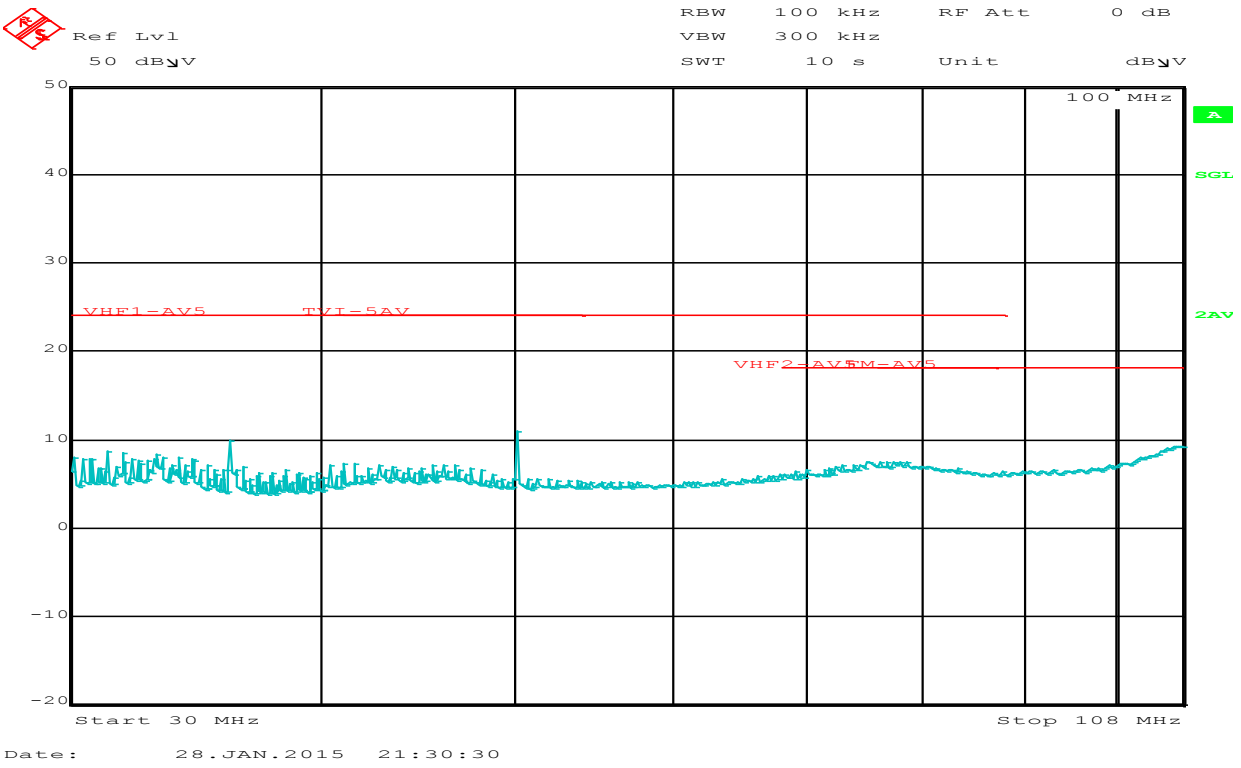
The test results are shown below. The limit lines in red are the Class 5 limits for conducted disturbances specified in the standard. The first waveform shows the conducted EMI noise from 150kHz to 30MHz using peak detector, and the limit lines are the Class 5 average limits. It can be seen the peak measurement result is well below the average limits. The next two waveforms show the noise scan result from 30MHz to 108MHz using peak and average detector, with the Class 5 peak and average limits respectively. It can be seen the peak/average noise is lower than the corresponding peak/average limits. Therefore, the power supply board is in compliance with the CISPR 25 Class 5 conducted emissions standard.



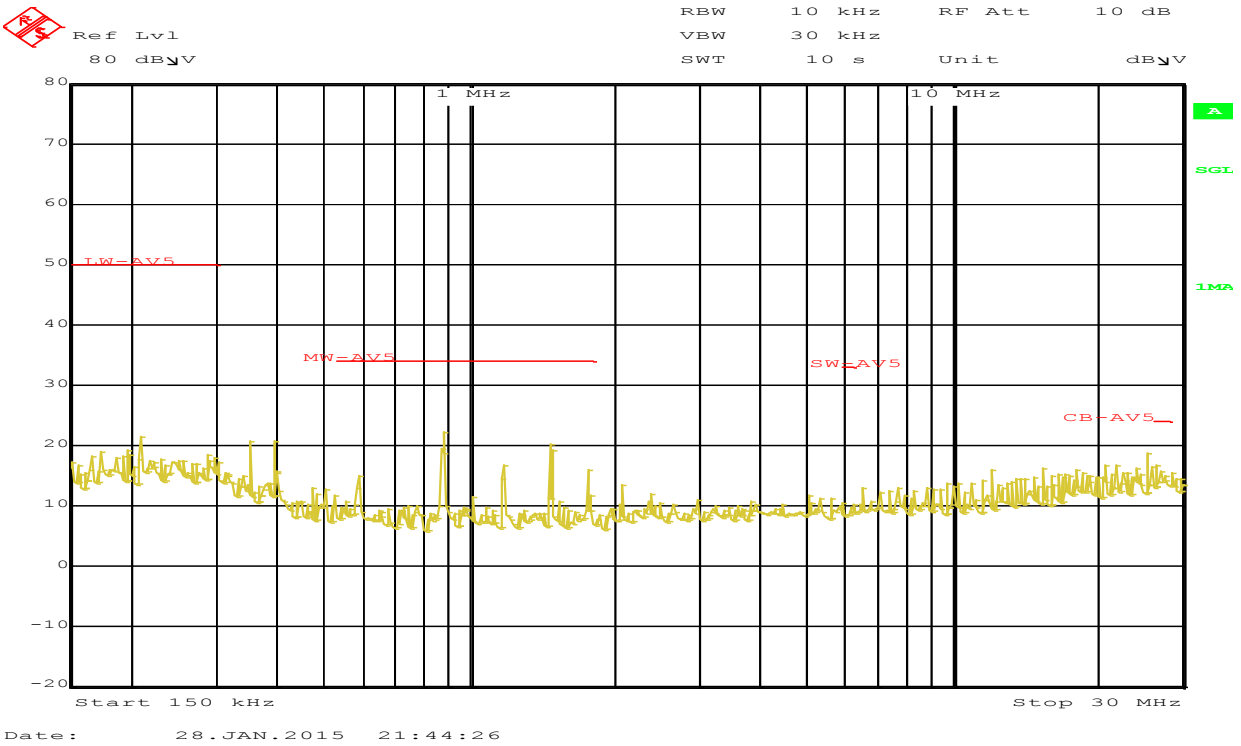
Peak detect, 150kHz-30MHz, with EMI filter.



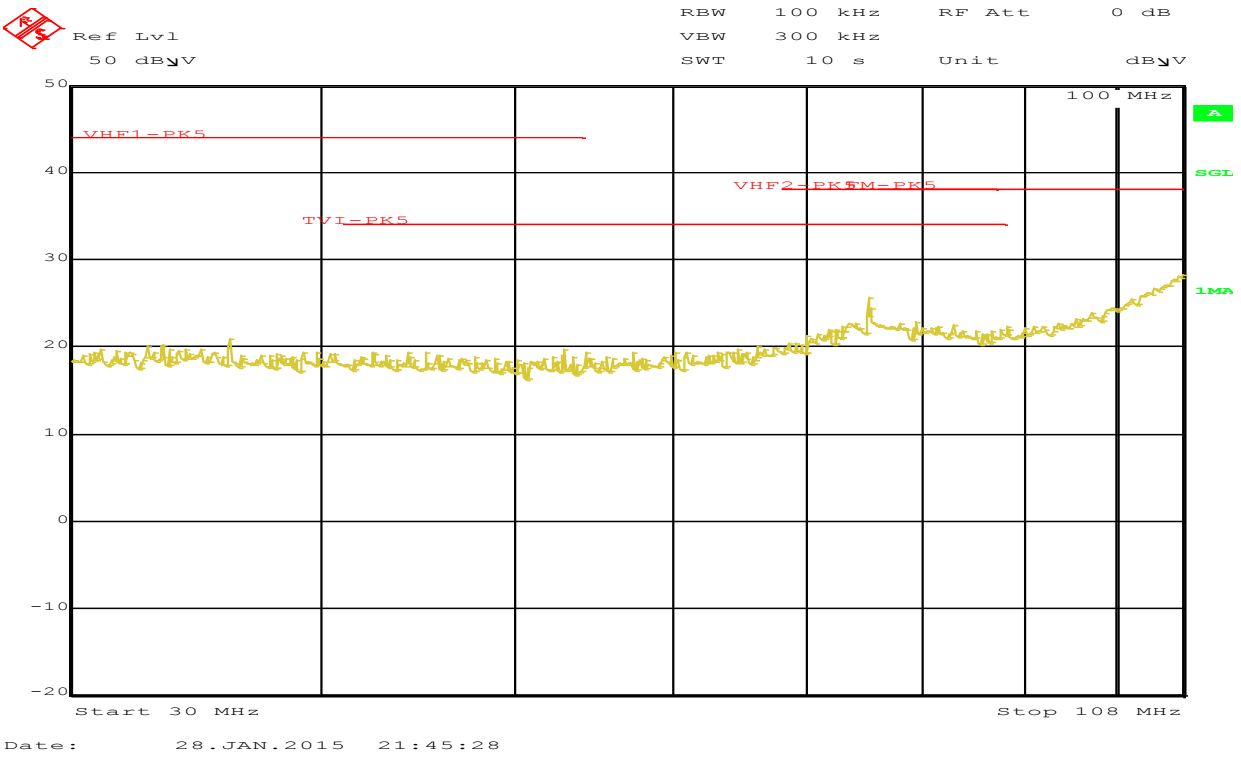
Peak detect, 30MHz – 108MHz, with EMI filter.



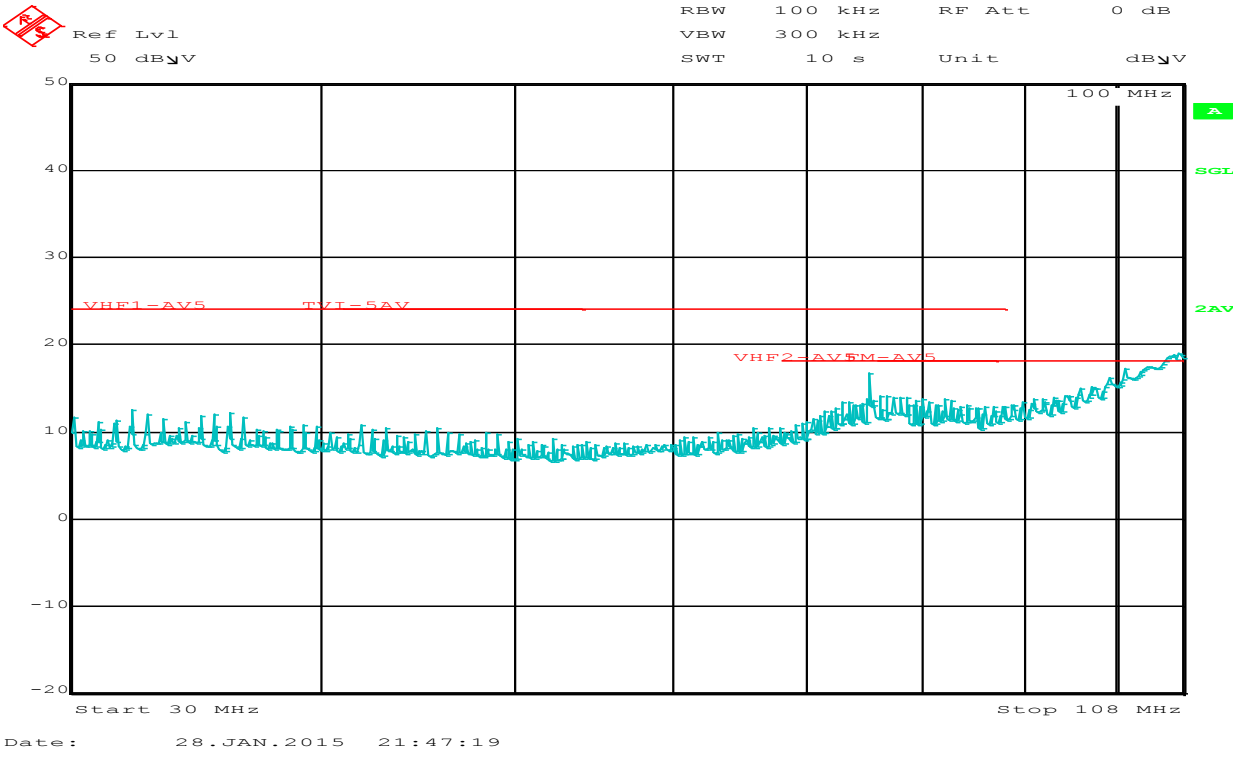
Averagedetect, 30MHz - 108MHz, with EMI filter.



Peak detect, 150kHz-30MHz, without EMI filter.



Peak detect, 30MHz – 108MHz, without EMI filter.



Averagedetect, 30MHz - 108MHz, without EMI filter.

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