TI Designs

Optimal Clock Sources for GSPS ADCs Design Guide

TI Designs High Speed

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Design Resources

TIDA-00479	Tool Folder Containing Design Files
ADC08Dxxxx	Family Product Folder
ADC10Dxxxx	Family Product Folder
ADC12Dxxxx	Family Product Folder
ADC12DxxxxRF	Family Product Folder
ADC12D1600RFRB	EVM Product Folder
LMX2531	Product Folder

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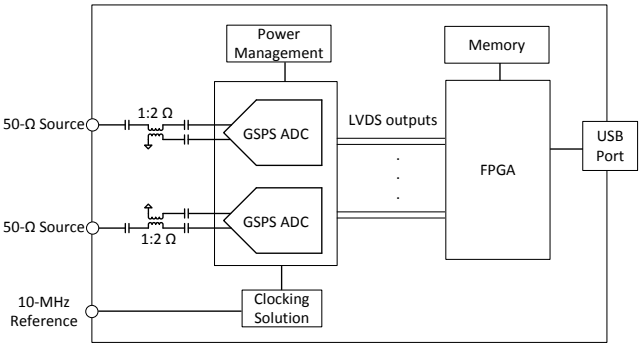
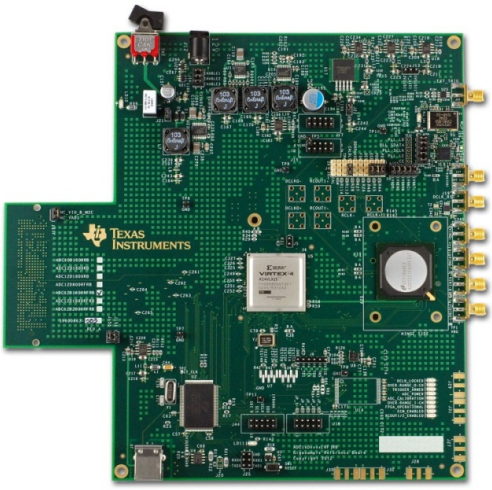
Clocking GSPS ADCs

Texas Instruments offers a large family of gigasample-per-second (GSPS) converters with sampling speeds ranging from 500 megasamples per second (MSPS) to 3.6 GSPS and 8 to 12 bits. The devices in the ADCxxDxxxx(RF) family operate using a folding-interpolating ADC architecture, which can achieve such performance, but the architecture inherently generates higher order harmonics that are treated as noise when considering the signal-to-noise ratio (SNR). Separating and quantifying all of the contributors to SNR is important to understand how to select the optimal clock source for a given system SNR budget. This report explores the effect of various clock sources on the performance of the ADC12D1600RF and provides a baseline understanding for the rest of the family.

The key applications that this family of products enables are high-speed digitizers, wideband microwave backhaul, RF sampling, software-defined radio, RADAR and LIDAR, and test and measurement. A 12-bit high-speed digitizer typically requires more than nine effective number of bits (ENOB) over a wide input bandwidth, which is only possible with the proper selection of clock source.





1 Introduction

Clocking performs a necessary function for every analog-to-digital converter (ADC), but the criteria for selecting the optimal clock source varies depending on application, ADC architecture, sample rate, resolution, and input frequency. A 12-bit high-speed digitizer typically requires a sample rate faster than 1 GSPS with more than 9 ENOB over a wide input frequency range. The ADC1xDxxxx(RF) family of devices utilizes a folding-interpolating architecture with high-bandwidth input buffers, which well suits this type of application. A balun front-end is typically used for RF sampling applications, which ideally does not contribute noise or distortion, leaving the clock source as the main contributor to performance degradation. With improper clocking, the overall system performance (specifically the signal-to-noise ratio (SNR) and ENOB) can fall below the requirement. Figure 1 shows a typical diagram of an AC coupled dual channel high speed digitizer.

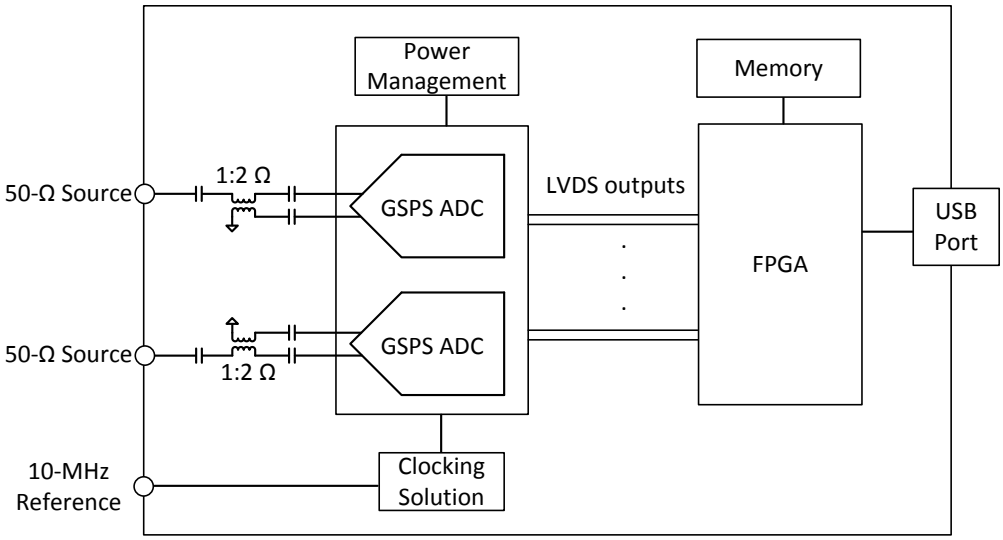


Figure 1. Dual Channel High-Speed Digitizer Block Diagram

2 Calculating System SNR

The ADCxxDxxxx(RF) family of ADCs have four main factors limiting the SNR: quantization noise, thermal noise, jitter, and higher-order harmonics. The fourth term is typically neglected for most ADC architectures because the harmonic distortion rolls off by the 9th harmonic and is represented by total harmonic distortion (THD). However, the transfer function of the folding and interpolating architecture inherently has points of discontinuity, which translates into higher-order harmonics that can show up in spectral analysis (see Figure 2). These higher-order harmonics are not encapsulated by the standard nine harmonics of the THD, and as a result, must be included when discussing SNR. For a further understanding on the sources of harmonics and methods of mitigation, please view the SLAA617 application report (SLAA617).

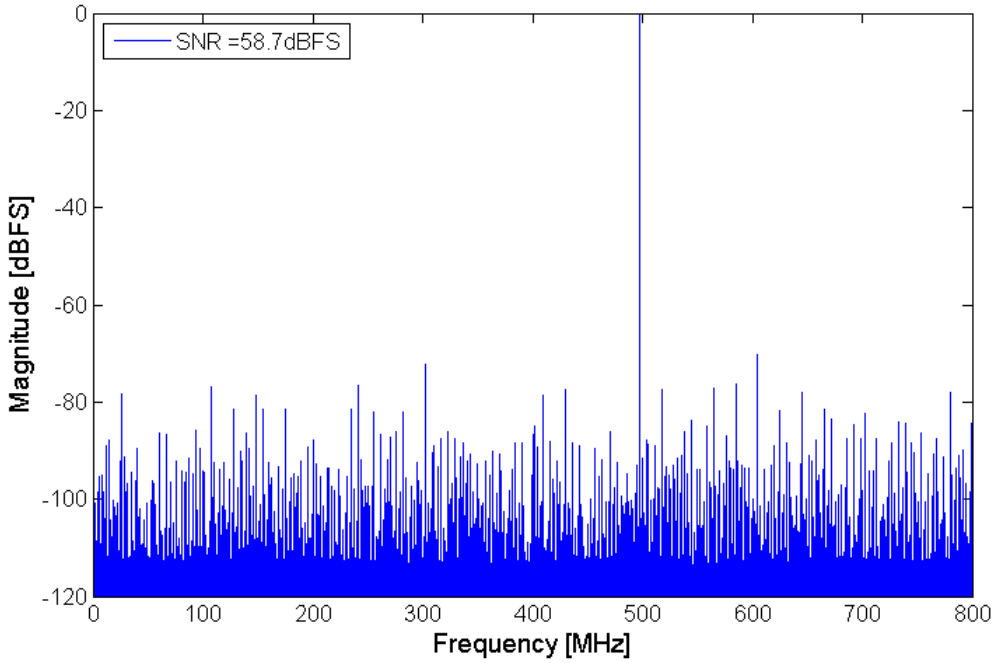


Figure 2. ADC12D1600RF Higher-Order Harmonics

All four sources of SNR can be combined to calculate the total SNR with the following formula in Equation 1:

$$SNR_{Total} = -10\log_{10}\left(10^{\left(\frac{-SNR_{Quantization}}{10}\right)} + 10^{\left(\frac{-SNR_{Thermal\_Noise}}{10}\right)} + 10^{\left(\frac{-SNR_{Higher\_Order\_Harmonics}}{10}\right)} + 10^{\left(\frac{-SNR_{Jitter}}{10}\right)}\right) \quad (1)$$

To approximate the total SNR for the ADC12D1600RF for a given clock jitter and input frequency, see Equation 13.

2.1 SNR as Result of Quantization Noise

For an N-bit data converter, the contribution to SNR from quantization noise can be approximated with the following Equation 2:

$$SNR_{Quantization} = 6.02\ N + 1.76 \quad (2)$$

For most data converters this is not the limiting factor for SNR and the ADC12D1600RF has an SNR as a result of quantization noise of 74 dBFS. Measuring the quantization noise becomes problematic because its contribution is typically masked by the thermal noise; therefore, a value of 74 dBFS is assumed throughout the guide.

2.2 SNR as Result of Thermal Noise

Thermal noise comes from several sources including input termination, ADC input buffer noise, and sampling switch resistance, as Figure 3 shows.

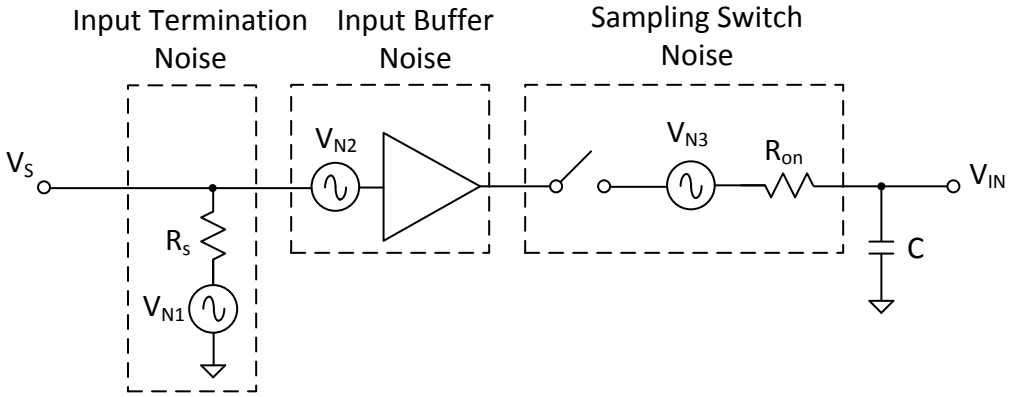


Figure 3. Thermal Noise Sources

These noise sources are typically lumped together and represented in the datasheet as noise spectral density (NSD) or noise floor density, as the following Table 1 shows.

Table 1. ADC12D1600RF Noise Floor Density

PARAMETER	CONDITIONS	ADC12D1600RF		ADC12D1000RF		UNITS (LIMITS)
		TYP	LIM	TYP	LIM	
Noise floor density	50-Ω single-ended termination, DES mode	–154.6		–154.0		dBm/Hz
		–153.6		–153.0		dBFS/Hz

The value in dBFS/Hz can be integrated over the Nyquist bandwidth to get the thermal noise contribution to SNR with the following Equation 3:

$$SNR_{Thermal\_Noise} = -NSD_{dBFS/Hz} - 10\log_{10}\left(\frac{f_{Sample}}{2}\right) \quad (3)$$

For the ADC12D1600RF the measurement was performed with the dual edge sampling (DES) mode, so f_{Sample} is 3200 MHz and the $NSD_{dBFS/Hz}$ is given as −153.6 dBFS/Hz. From Equation 3, the calculated $SNR_{Thermal\ Noise}$ is 61.6 dBFS, which remains constant across the input frequency.

2.3 SNR as Result of Higher Order Harmonics

To reiterate, the higher-order harmonics are inherent to the folding and interpolating architecture and do not linearly decrease with the harmonic index and have little dependency on the input amplitude, as the following Figure 4 shows.

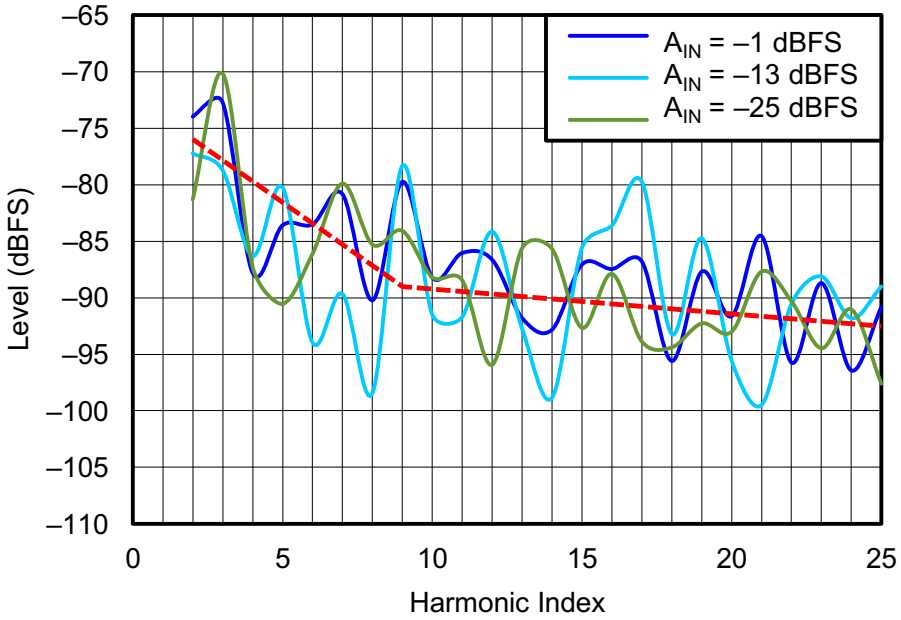


Figure 4. ADC12D1600RF Harmonic Index Versus Level (3)

The first nine harmonics are the most dominant and are represented by THD, while the remaining harmonics are combined with the noise floor. The ADCxxDxxxx(RF) family includes internal calibration to help linearize the transfer curve, which reduces the source of higher-order harmonics and maintains a relatively constant performance across the input frequency. Therefore, to a first order, the SNR contribution as a result of the higher-order harmonics can be approximated by the RMS of the integral non linearity (INL) with the following Equation 4:

$$SNR_{Higher\_Order\_Harmonics} = -20\log_{10}\left(\frac{V_{FSR\_RMS}}{INL_{RMS}}\right) \quad (4)$$

For the ADC12D1600RF the INL_{RMS} is about 170 μV_{RMS}. Compared to 283 mV_{RMS} at full scale, the SNR contribution as a result of higher-order harmonics is about 64.4 dBFS. This number works well for a first-order approximation, but in a real system measuring at the desired frequency is important because there is still a dependency on the input configuration and thus the input frequency. To measure the real effect of higher-order harmonics for a given input frequency, a fast Fourier transform (FFT) can be taken where the harmonics greater than the 9th (as well as the remaining harmonics) are isolated from the spectrum with a post-processing tool such as Matlab. The impact of the harmonics on the SNR can then be directly computed by taking a power sum of the resulting vector.

To accurately separate the harmonics from the noise floor, the harmonic and spur magnitudes must be 10 dB larger than the noise floor for ±0.5-dB accuracy. Therefore, the designer can utilize the processing gain by increasing the number of samples in the FFT to spread out the noise floor into adjacent bins, which effectively lowers the noise floor without affecting the spur magnitude. As the sample size is increased by a factor of 2, the NSD per bin drops by 3 dB without affecting the magnitude of the spur. For this report, a sample size of 1,048,576 has been used to create the most separation between the higher-order harmonics and the noise floor while maintaining coherent sampling.

Figure 5 shows that for an input frequency of 498 MHz, the higher-order harmonics account for approximately 63.3 dBFS of the SNR. The remaining 60.5 dBFS is a combination of the thermal noise, quantization noise, and jitter. Using a power sum to combine these two SNR numbers gives a total SNR of 58.7 dBFS, which is the same SNR that results by integrating the entire spectrum (see Figure 2). Additionally, with an input signal of −0.5 dBFS, the total SNR relative to the carrier is 58.2 dBc, which matches the typical value for SNR in the datasheet, as Table 2 shows. Note that the 2nd through 9th harmonics are not counted as higher-order harmonics in the preceding Figure 5 measurement, as these are included in THD.

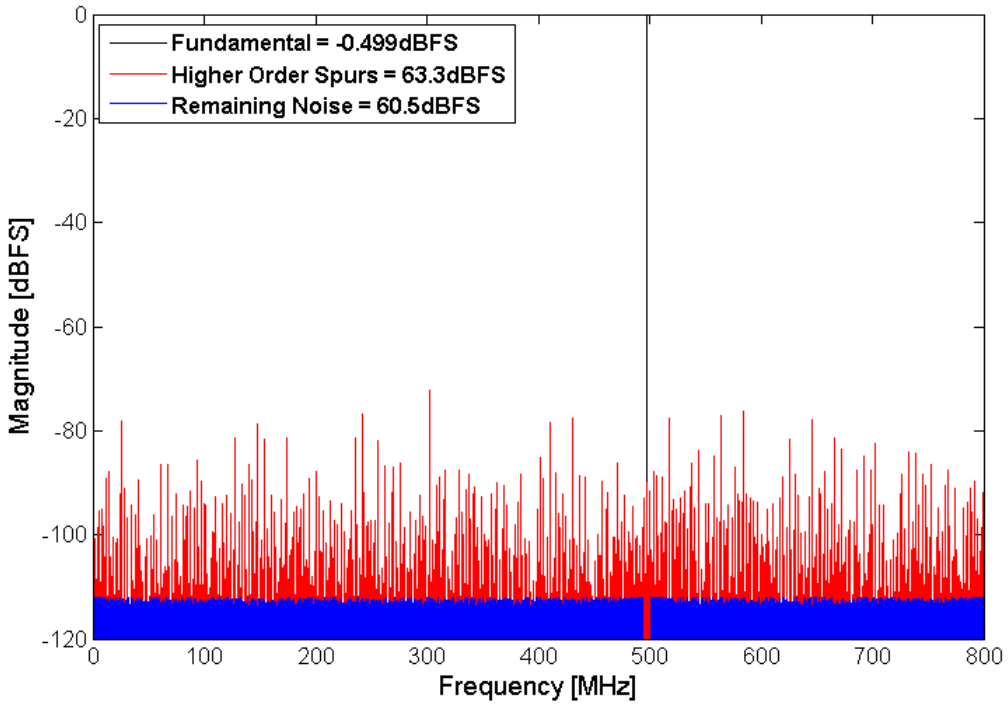


Figure 5. Higher Order Harmonics Separated from Noise Floor With 1,048,576 Samples

Table 2. ADC12D1600RF Datasheet SNR in Non-DES Mode

SYMBOL	PARAMETER	CONDITIONS	ADC12D1600RF		ADC12D1000RF		UNITS (LIMITS)
			TYP	LIM	TYP	LIM	
Non-DES Mode							
SNR	Signal-to-noise ratio	A_{IN} = 125 MHz at –0.5 dBFS	59		60.1		dB
		A_{IN} = 248 MHz at –0.5 dBFS	58.6		60		dB
		A_{IN} = 498 MHz at –0.5 dBFS	58.2	**54.6**	58.8	**55.1**	dB (min)
		A_{IN} = 998 MHz at –0.5 dBFS	57		58.2		dB
		A_{IN} = 1448 MHz at –0.5 dBFS	55.4		56.1		dB

2.4 SNR as Result of Jitter

Jitter is essentially the time variation of the sampling instant, which results in sampling error. Both the ADC and the clock source have jitter. ADC jitter results from the timing uncertainty of the aperture, which is commonly given in the datasheet as aperture jitter (t_{AJ}). Table 3 shows that the typical aperture jitter for the ADC12D1600RF device is 0.2 ps or 200 fs.

Table 3. Aperture Jitter in ADC12D1600RF Datasheet

SYMBOL	PARAMETER	CONDITIONS	ADC12D1600RF		ADC12D1000RF		UNITS (LIMITS)
			TYP	LIM	TYP	LIM	
t_{AJ}	Aperture jitter	See (1)	0.2		0.2		ps (rms)

(1) This parameter is specified by design and/or characterization and is not tested in production.

The clock source typically has random jitter, which is specified as integrated phase noise over a given frequency range in fs (rms) or in dBc/Hz for several offset frequencies as the Clock Phase Noise in LMX2531 Datasheet shows.

Clock Phase Noise in LMX2531 Datasheet

SYMBOL	PARAMETER	TEST CONDITIONS		TYP	UNITS (LIMITS)
$L(f)_{Fout}$	Phase noise (LMX2531LQ1570E)	f_{Fout} = 1583 MHz DIV2 = 0	10-kHz offset	–93	dBC/Hz
			100-kHz offset	–118	
			1-MHz offset	–140	
			5-MHz offset	–154	
		f_{Fout} = 791.5 MHz DIV2 = 1	10-kHz offset	–99	
			100-kHz offset	–122	
			1-MHz offset	–144	
			5-MHz offset	–155	

A solid understanding of jitter and its effects on ADCs is important to accurately compute the jitter contribution of the clock (refer to the following data acquisition articles in [4] SLYT379, SLYT389, and SLYT422 for more information). The jitter from the clock input must be measured and integrated over the proper frequency range. In an RF sampling application where the clock frequency can be greater than 1 GHz, the ADC clock receiver must have a bandwidth of several GHz to accommodate the signal without attenuation or degrading the slew rate at the zero crossing. The resulting effect of accommodating a higher clock bandwidth is an increase of the wideband noise. Figure 6 shows the result of integrating the single-side band phase noise profile of a 1600-MHz sine-wave clock source by decade. The data in Figure 6 clearly shows that the integrated noise above 100 MHz is the dominant source of jitter.

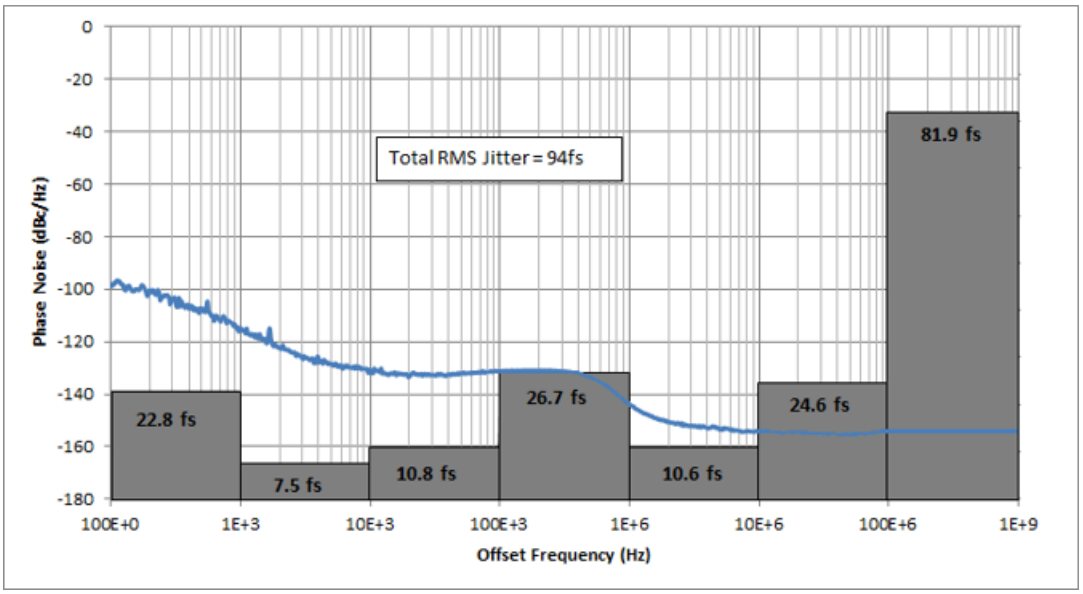


Figure 6. Integrated Clock Jitter Per Decade With No Filtering

Filtering can help reduce the effects of wideband noise. Figure 7 shows the drastic difference that filtering the wideband noise can make to the overall jitter contribution.

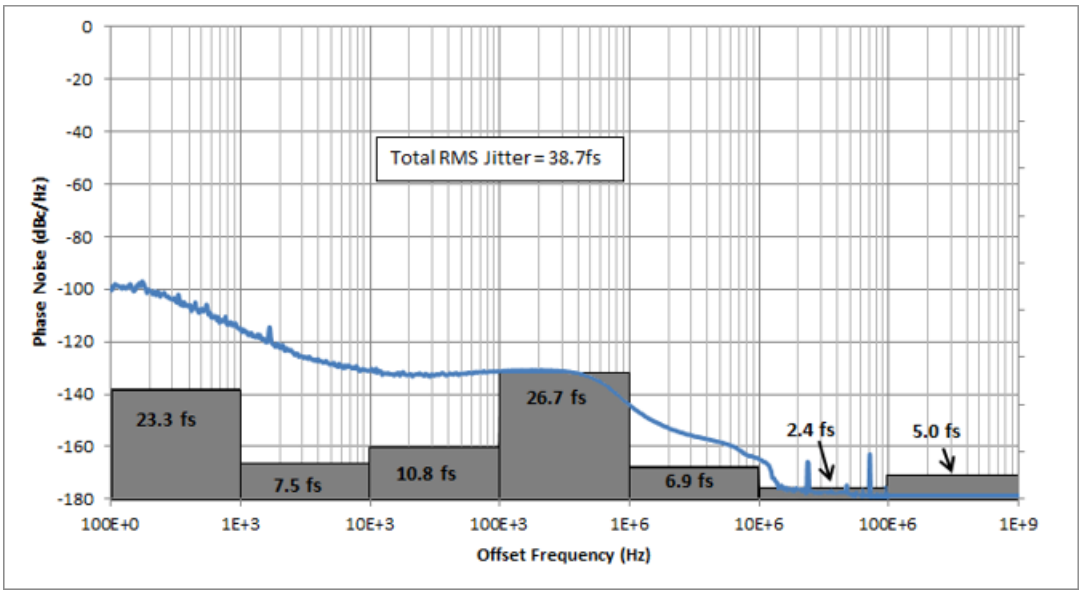


Figure 7. Integrated Clock Jitter Per Decade With Filtering

Filtering may not be practical in applications where the insertion loss is too great or a variable frequency clock source is required. Also note that, because the phase noise is measured in dBc/Hz, reducing the amplitude effectively increases the wideband noise. Figure 8 shows the effect of reducing the clock amplitude of a filtered signal on the wideband noise. The curves are measured to 100 MHz and extrapolated to 1 GHz.

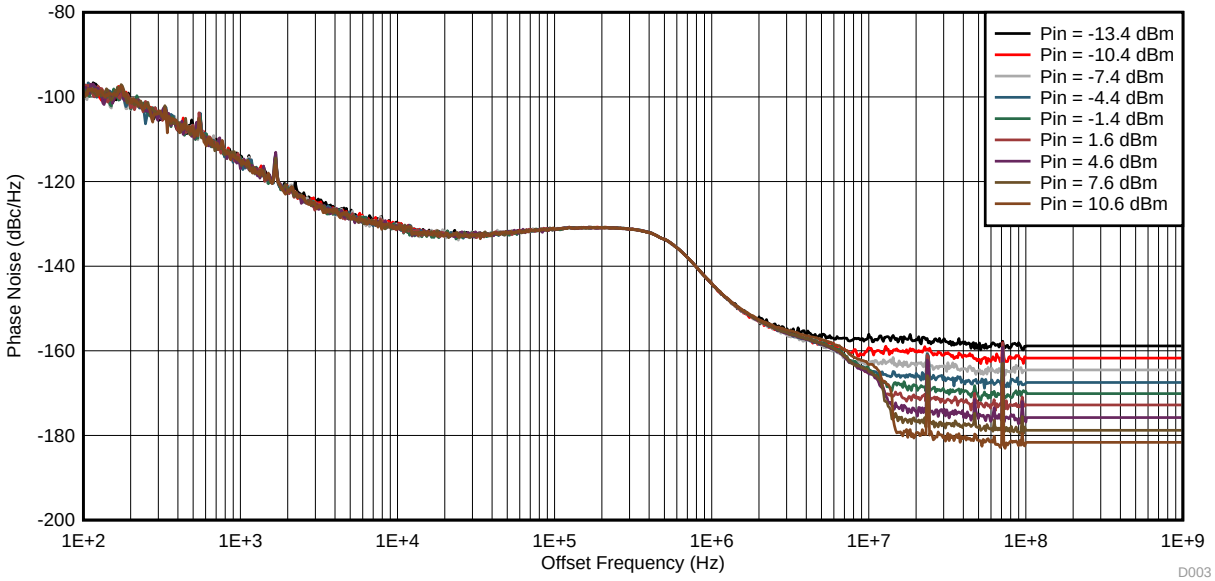


Figure 8. Effects of Amplitude on Wideband Clock Phase Noise in dBc/Hz

Table 4 shows that for smaller clock amplitudes the integrated jitter increases. The effect appears to be small until the wideband noise is high enough to make an impact, which can be attributed to the extremely low noise floor of the phase noise analyzer equipment of about −172 dBm/Hz.

Table 4. Effects of Amplitude on Integrated Clock Jitter

CLOCK SOURCE AMPLITUDE (dBm)	INTEGRATED PHASE NOISE 100 Hz TO 1 GHz (fs)
10.6	38.6
7.6	38.7
4.6	39.0
1.6	39.8
–1.4	40.7
–4.4	42.8
–7.4	46.4
–10.4	53.5
–13.4	64.2

Converting the curves from Table 4 from dBc/Hz to dBm/Hz can be helpful to identify the source of the wideband noise. This is accomplished by adding the input power (P_{in}) to each respective curve, as in the following Figure 9 shows. Note that the absolute noise floor limit is −174 dBm/Hz, which comes from the inherent kT noise referenced to 1 mW, assuming a temperature of 290° Kelvin and a Boltzmann's constant of 1.38×10^{-23} Joules per Kelvin.

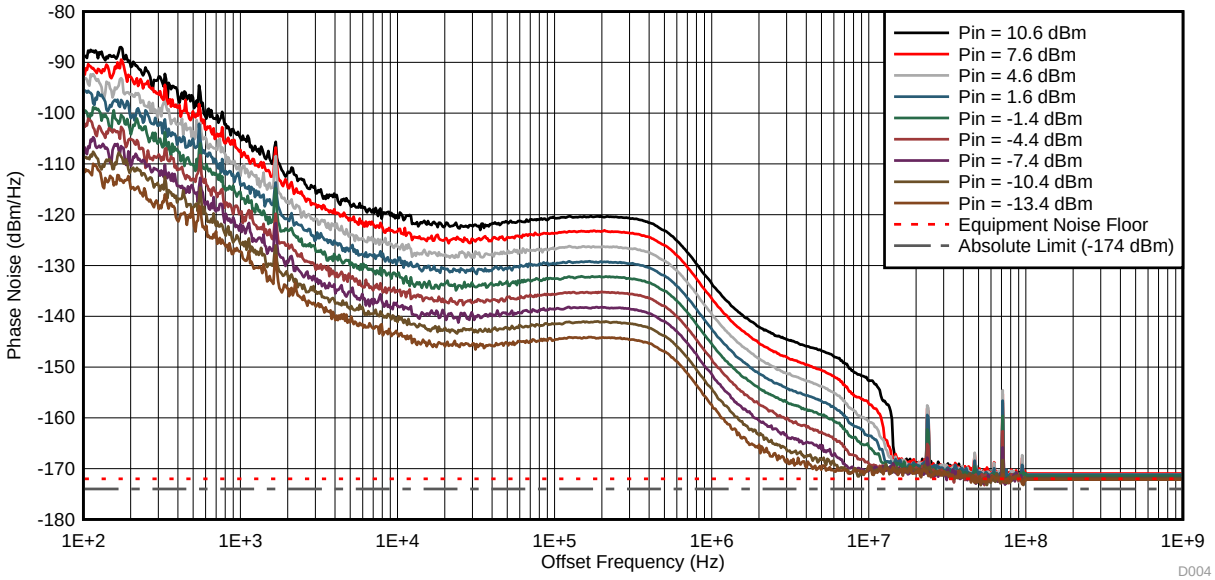


Figure 9. Phase Noise in dBm/Hz With Equipment Limitation

In a real scenario, the limiting noise floor is much higher than that used with expensive equipment. Therefore, to calculate the impact that results from jitter when clocking an ADC, the measurement must be extrapolated to use the noise floor of the clock receiver. For the ADC12D1600RF, the clock receiver has a noise floor of about −162 dBm/Hz. Additionally, the power seen by the clock receiver is likely to be less because of insertion losses on the board, including baluns and other series components. The following Equation 5 can be used to extrapolate the actual phase noise curves in a system.

$$\text{Phase\_Noise}_{\text{dBm/Hz}} = -10\log_{10}\left(10^{-\left(\frac{\text{Phase\_Noise}_{\text{dBc/Hz}} + P_{\text{in\_dBm}} - P_{\text{Loss\_dB}}}{10}\right)} + 10^{-\left(\frac{P_{\text{Noise\_Floor\_dBm/Hz}}}{10}\right)}\right) \quad (5)$$

Figure 10 uses Equation 5 and takes into account the ADC12D1600RF noise floor (dotted red line) as well as the 3.4 dB of insertion loss from the onboard balun of the ADC12D1600RFRB (5).

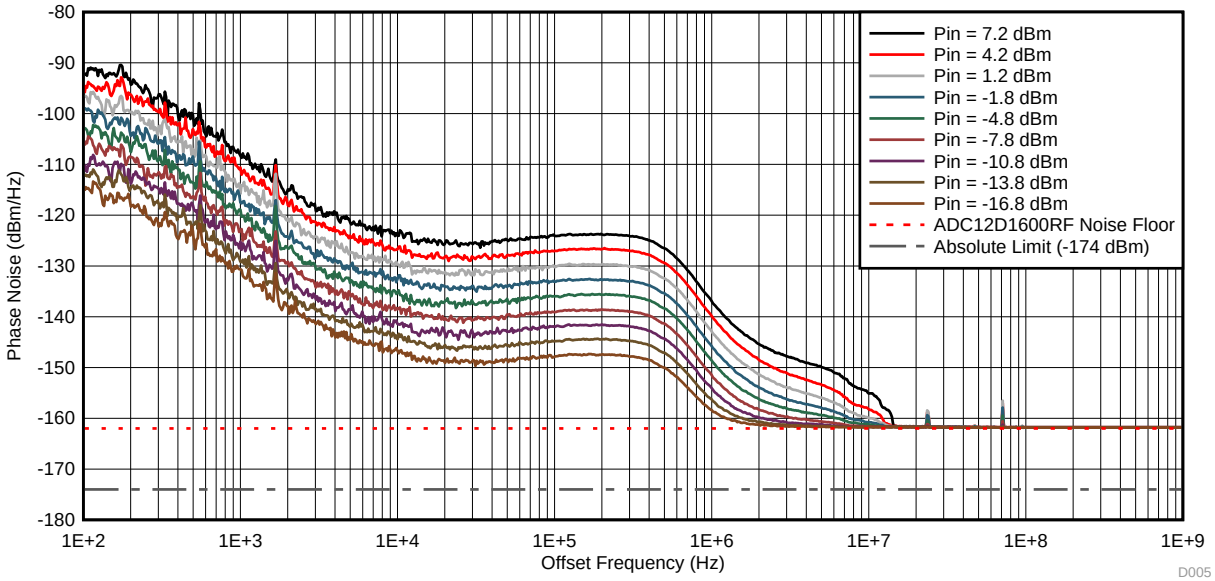


Figure 10. Phase Noise in dBm/Hz With ADC12D1600RF Clock Receiver

From a dBm/Hz standpoint, everything has shifted down 3.4 dB and the curves now intersect the noise floor of the ADC12D1600RF clock receiver at −162 dBm/Hz. Table 5 shows the results of converting back to dBc/Hz and integrating from 100 Hz to 1 GHz for each respective clock source amplitude.

Table 5. Effects of Amplitude on Integrated Clock Jitter

CLOCK SOURCE AMPLITUDE (dBm)	CORRECTED CLOCK SOURCE AMPLITUDE (dBm)	INTEGRATED PHASE NOISE 100 Hz TO 1 GHz (fs)
10.6	7.2	41.4
7.6	4.2	44.8
4.6	1.2	50.0
1.6	–1.8	59.3
–1.4	–4.8	74.3
–4.4	–7.8	97.4
–7.4	–10.8	132.1
–10.4	–13.8	182.9
–13.4	–16.8	255.1

For the ADC12D1600RF, the full-scale clock amplitude is 2 V_{PP} into 100 Ω or 7 dBm. For full-scale and close to full-scale clock signals, reducing the clock amplitude has a marginal effect. However, because of the wideband noise limitation of the clock receiver, even a very clean filtered clock source can have a substantial jitter impact to the system if the amplitude drops low enough. Therefore, the tradeoffs between filtering, clock amplitude, and selecting a large amplitude GHz clock source with inherently low wideband phase noise are important and must be considered.

2.4.1 Determining Limits of Integration

For the ADC12D1600RF, the clock receiver bandwidth is approximately 3.5 GHz. Because of the clock path not being a simple first order system, the −3-dB bandwidth and the equivalent noise bandwidth are approximately identical at 3.5 GHz. In an ideal situation, the phase noise is broken up into different sections and integrated across the entire noise bandwidth (DC to 3.5 GHz); however, most equipment measures single side-band phase noise up to a couple hundred MHz offset. The phase noise outside of this range can be assumed to be uniformly at the noise floor and the single side-band profile can be extrapolated to half of the clock receiver bandwidth to encompass the entire noise bandwidth of the ADC12D1600RF clock receiver. The close in phase noise is captured by the lower frequency integration limit, which greatly depends on the end application. For triggered systems such as high-speed digitizers, the capture length (or number of samples) determines how much low-frequency clock jitter (or wander) shows up as a sampling error relative to the initial capture. For systems with multiple repeated captures, this effect can be calibrated out by measuring relative to a trigger point, leaving just the reference accuracy and the integrated jitter where the low frequency wander is bounded by the capture length. Equivalently, for spectral analysis, the capture depth and sample rate determine the low frequency limit, which is half of the FFT bin width or resolution bandwidth (RBW), as Figure 11 shows. Increasing the number of samples reduces the RBW, effectively exposing more of the inband phase noise, which is considered part of the noise of the system. The phase noise that falls within ½ of the bin width of a bin-centered coherent signal is lumped with the fundamental bin and has a negligible impact on the fundamental amplitude. Therefore, for a high-speed digitizer application, the lower limit of single side-band integration can be determined by ½ of the RBW, which is a function of the sample rate and number of samples in the FFT.

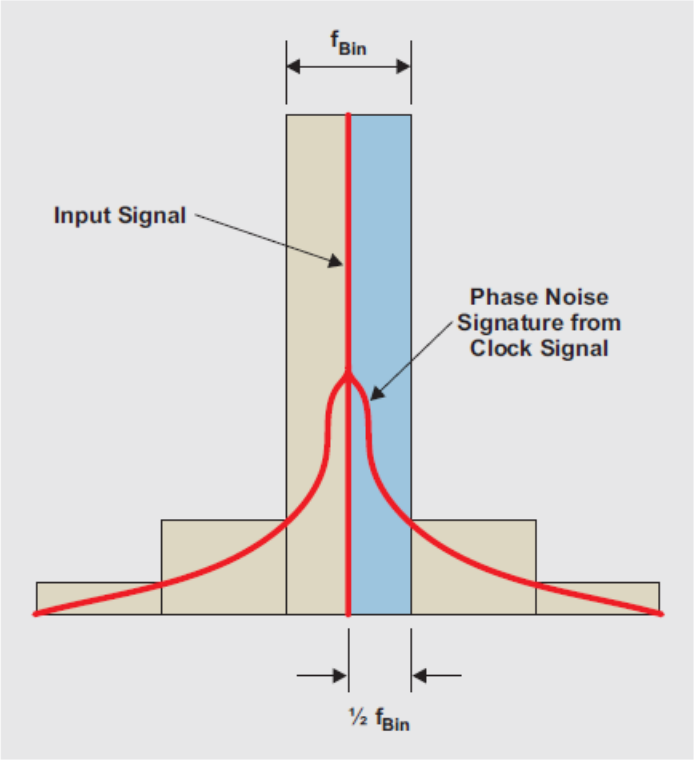


Figure 11. Half-Bin Width of FFT (4)

Figure 12 shows the single side-band phase noise of four different clock sources with varying degrees of inband and wideband noise measured to a 100-MHz offset and extrapolated to 1.75 GHz.

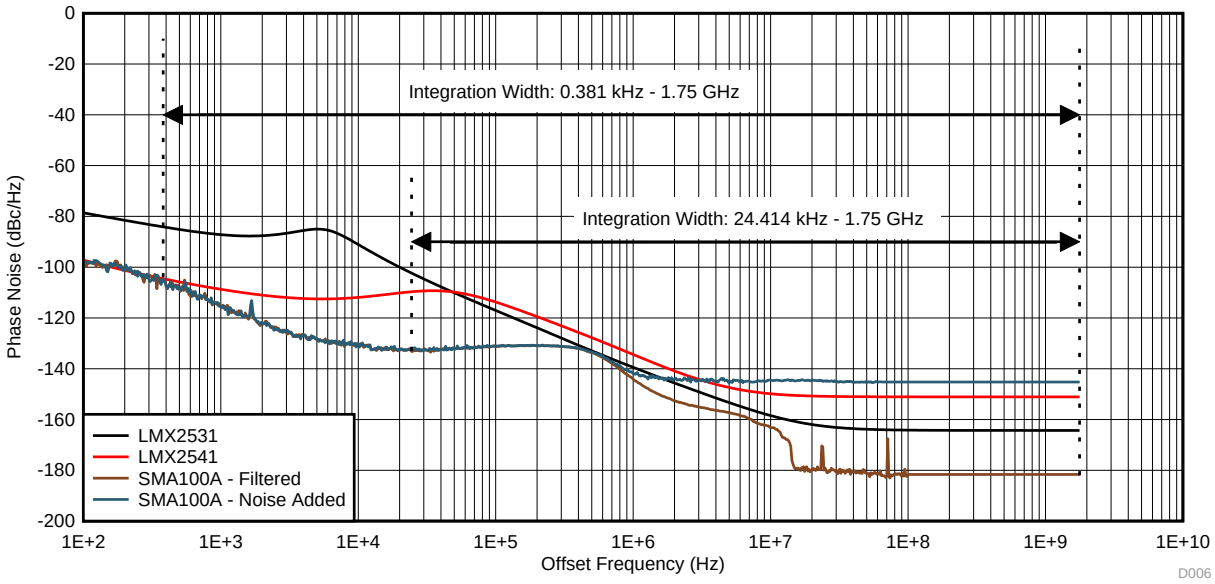


Figure 12. Integration Limits for Different Sample Sizes

Table 6 shows the impact that changing the lower integration limit can have. By decreasing the number of samples in the FFT, clock sources with poor inband phase noise but good wideband phase noise, such as the LMX2531, start to out-perform those with good inband but low wideband performance, such as the LMX2541.

Table 6. Integrated Jitter from ½ Bin Width to 1.75 GHz for 1600-MHz Clock Sources

FFT SIZE (POINTS)	½ BIN WIDTH (kHz)	LMX2531 JITTER (fs)	LMX2541 JITTER (fs)	SMA100A JITTER – NOISE ADDED (fs)	SMA100A JITTER – FILTERED (fs)
1048576	0.381	698.0	229.5	328.4	33.0
524288	0.763	682.8	229.1	328.2	31.5
262144	1.526	661.5	228.7	328.1	30.8
131072	3.052	618.1	228.2	328.1	30.5
65536	6.104	453.0	227.5	328.1	30.3
32768	12.207	239.5	225.7	328.1	30.2
16384	24.414	144.3	220.8	328.0	29.9
8192	48.828	94.1	207.5	328.0	29.5

Also note that the results from Table 6 are for coherent sampling. For windowed sampling, the fundamental power is spread out across several bins essentially masking the inband phase noise and making its effect almost completely negligible, even for larger sample sizes. The quality of the wideband noise is the dominant factor for windowed sampling, which makes the choice of a clock source with good wideband performance like the LMX2531 even more important.

As soon as the clock jitter has been calculated with the appropriate limits, the clock jitter can be combined with the ADC aperture jitter using the following formula in Equation 6, where $t_{Jitter,ADC\_Aperture}$ is the value given in the ADC datasheet and $t_{Jitter,Clock\_Input}$ is the integrated RMS jitter from the preceding Table 6:

$$t_{Jitter\_Total} = \sqrt{\left(t_{Jitter\_Clock}\right)^2 + \left(t_{Jitter\_ADC_{Aperture}}\right)^2} \quad (6)$$

Using the ADC12D1600RF with a $t_{Jitter,ADC\_Aperture}$ of 200 fs and the LMX2531 with a coherent sample size of 16,384 and $t_{Jitter,Clock}$ of 144.3 fs, the $t_{Jitter,Total}$ is calculated to be 246.6 fs. In this case, the LMX2531 adds about 46.6 fs of jitter to the total system.

The effect that jitter has on the ADC performance varies over input frequency and can be quantified with the following Equation 7:

$$SNR_{Jitter} = -20\log\left(2\pi f_{In} \times t_{Jitter\_Total}\right) \quad (7)$$

Figure 13 shows the effect that input frequency has on the calculated SNR with varying levels of total jitter.

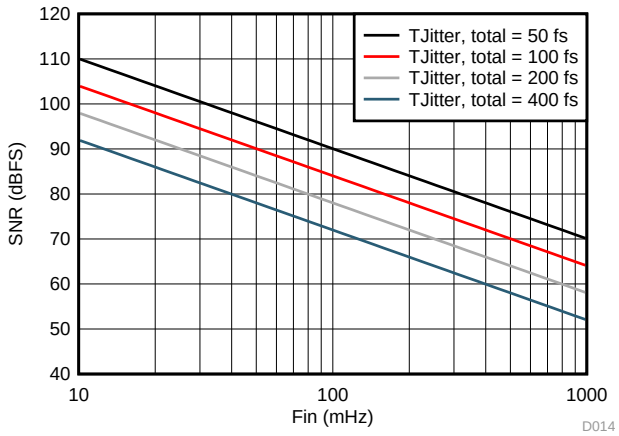


Figure 13. SNR as Result of Jitter versus Input Frequency

2.4.2 Extracting the Clock Jitter Requirements

Because quantization noise, thermal noise, and higher-order harmonics are predetermined by the ADC, the only parameter that designers can control is the contribution as a result of clock jitter. To determine the maximum amount of tolerable jitter for a required SNR_{Total}, Equation 1 and Equation 8 can be combined and rearranged to give the following formula:

$$t_{Jitter\_Total} = \frac{10^{\left(\frac{10\log_{10}\left(10^{\left(\frac{-SNR_{Quantization}}{10}\right)} - 10^{\left(\frac{-SNR_{Quantization}}{10}\right)} - 10^{\left(\frac{-SNR_{Thermal\_Noise}}{10}\right)} - 10^{\left(\frac{-SNR_{Higher\_Order\_Harmonics}}{10}\right)}\right)}{20}\right)}}{2\pi \times f_{In}} \quad (8)$$

By rearranging Equation 6, the sole contribution as a result of the clock source can be calculated as Equation 9.

$$t_{Jitter\_Clock} = \sqrt{\left(t_{Jitter\_Total}\right)^2 - \left(t_{Jitter\_ADC\_Aperture}\right)^2} \quad (9)$$

With these two equations and the proper inputs, the maximum allowable jitter contributed by the clock source can be calculated for a required SNR_{Total}.

3 Experimental Results

SNR can be calculated with estimations, but verifying and updating the constants with measurements is important for the most accuracy. For the ADC12D1600RF, this process can be accomplished with the ADC12D1600RFRB (5), a clean clock source, and by sweeping the input frequency to isolate each parameter.

A low-noise clock source is used to have a minimal contribution to the total jitter so that ADC aperture jitter can be extracted and verified. The clock path insertion losses and the ADC12D1600RF clock receiver noise floor have been taken into account with Equation 5, converted back to dBc/Hz, and plotted in the following Figure 14. The corrected RMS jitter is 39 fs integrated from 0.381 kHz to 1750 MHz.

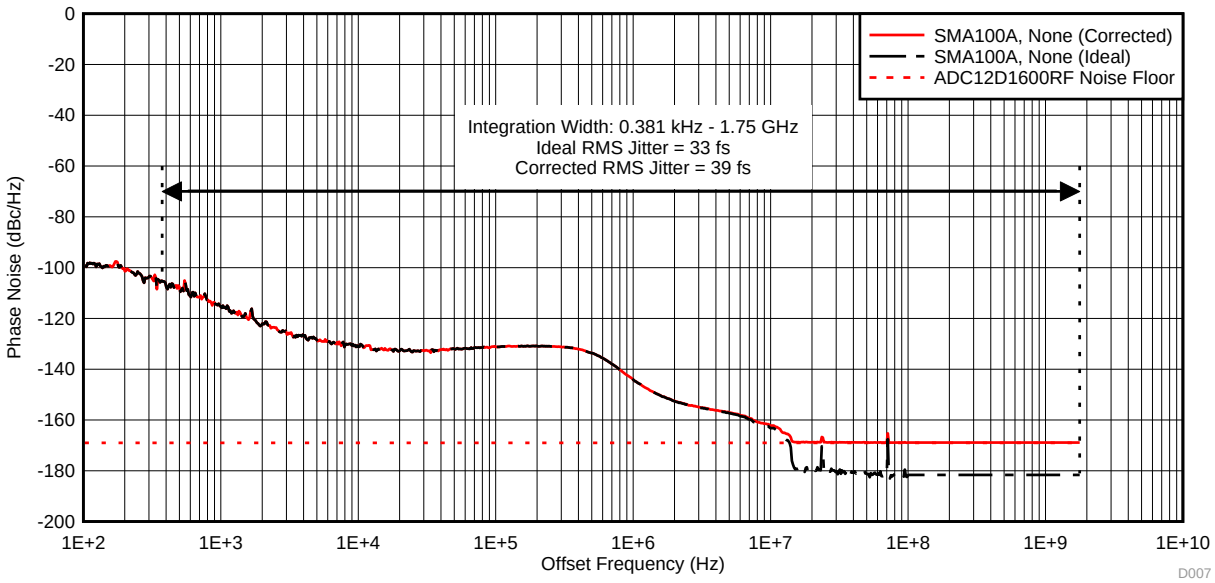


Figure 14. Phase Noise of Low Noise Clock Source With Filtering

3.1 Measuring Thermal Noise and Higher-Order Harmonics

The effect of thermal noise and higher-order harmonics is easy to observe at low input frequencies where clock jitter does not have an impact on the spectrum. Using a large sample size and utilizing the processing gain to obtain enough separation between the noise floor and the higher-order harmonics is important. An FFT sample size of 1,048,576 has been used for the majority of this design guide.

Figure 15 shows that, with a 100-MHz input signal measured on the ADC12D1600RFRB, the SNR contribution as a result of higher-order harmonics is 65.312 dBFS. This calculation is obtained by isolating and integrating the harmonics with amplitudes 10 dB larger than the average NSD per bin. The 2nd through 9th harmonics are not counted in the process and are replaced with the average NSD per bin. Similarly, each higher-order harmonic is removed and replaced with the average NSD per bin so that the remaining integrated noise can be properly analyzed. Integrating the remaining wideband noise gives an SNR of about 61.152 dBFS, which can be assumed to consist solely of contributions from thermal noise and quantization noise. Removing the 74-dBFS contribution from $SNR_{Quantization}$ leaves an $SNR_{Thermal\_Noise}$ of 61.384 dBFS, which this design guide assumes as a fixed value across the input frequency for the remainder of the guide. The SNR_{Total} is given by integrating the original spectrum, not including the fundamental or 2nd through 9th harmonics, resulting in 59.7 dBFS.

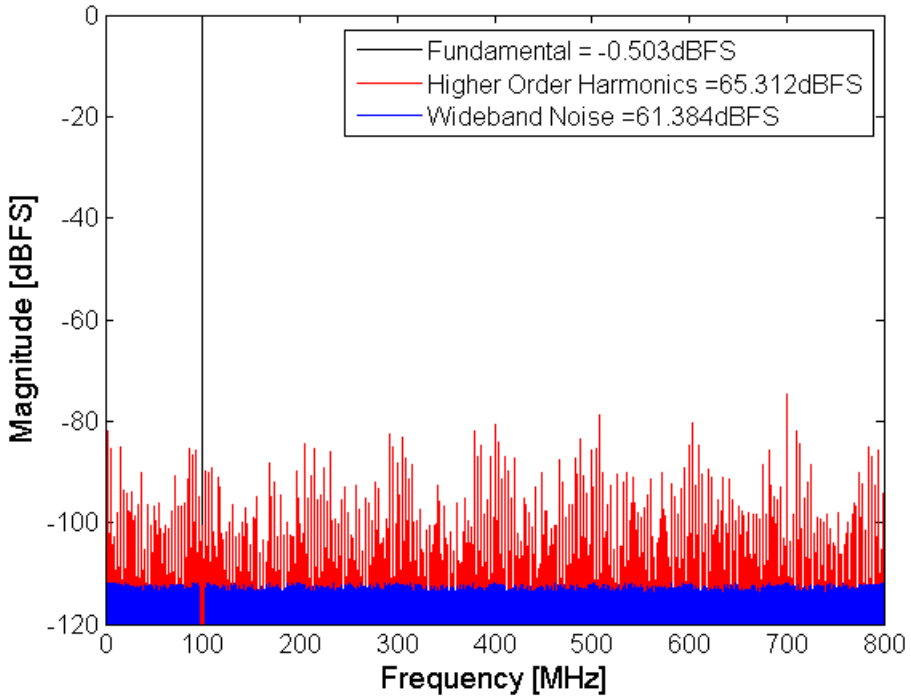


Figure 15. Isolating Wideband Noise and Higher Order Harmonics at Low Input Frequency

3.2 Measuring Clock Jitter

To isolate impact of jitter, the user can sweep the input frequency and calculate the jitter at each point with the following Equation 10:

$$SNR_{Jitter} = -10\log_{10}\left(10^{\left(\frac{-SNR_{Total}}{10}\right)} - 10^{\left(\frac{-SNR_{Quantization}}{10}\right)} - 10^{\left(\frac{-SNR_{Thermal\_Noise}}{10}\right)} - 10^{\left(\frac{-SNR_{Higher\_Order\_Harmonics}}{10}\right)}\right) \quad (10)$$

Figure 16 shows that jitter contribution to SNR starts to dominate at higher input frequencies.

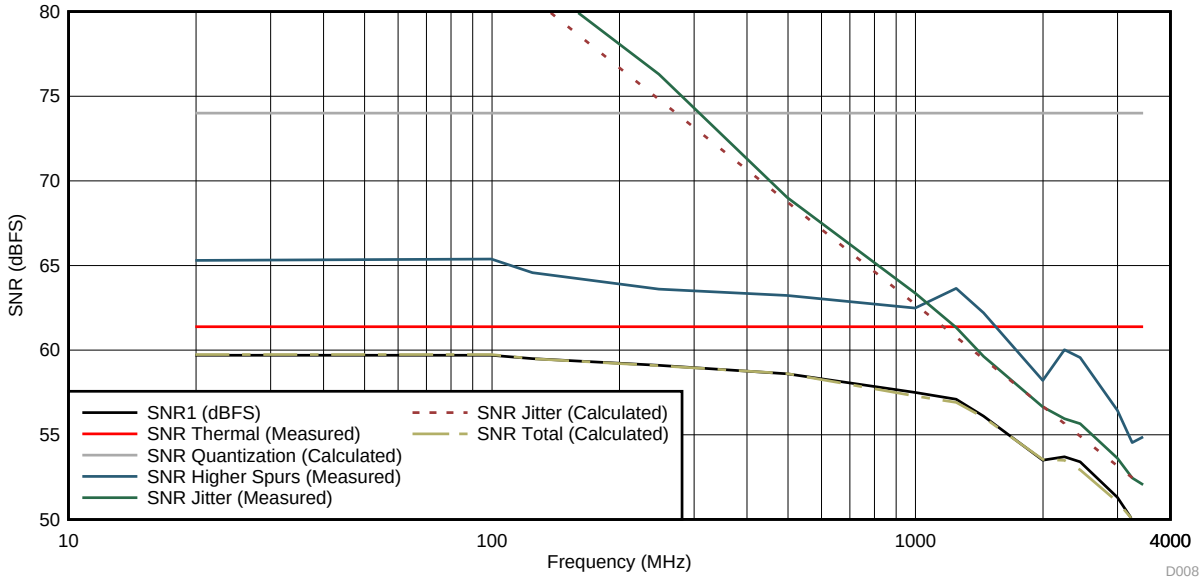


Figure 16. Measured and Calculated SNR and Contributors

With all four contributions known across the input frequency, the measured SNR as a result of jitter can be used to extract the actual ADC aperture jitter by combining Equation 6 and Equation 7 into the following Equation 11:

$$t_{Jitter\_ADC\_Aperture} = \sqrt{\left(\frac{10^{\frac{-SNR_{Jitter}}{20}}}{2\pi \times f_{In}}\right)^2 - \left(t_{Jitter\_Clock}\right)^2} \quad (11)$$

By inserting the 39-fs integrated value for $t_{Jitter,Clock}$ and the measured SNR_{Jitter} from the preceding Figure 16, the ADC aperture jitter can be extracted and calculated at each frequency as the following Table 7 shows.

Table 7. Measured and Calculated SNR and Contributors

$f_{in\ (MHz)}$	EXTRACTED $t_{Jitter,ADC\_Aperture}$ (fs)
20	83.7
100	88.7
125	93.9
248	90.3
497	106.3
998	101.0
1248	102.2
1448	107.8
1998	110.5
2248	105.9
2448	99.9
2998	103.6
3248	110.2
3448	108.5

As the frequency increases the extracted value becomes more accurate; therefore, the ADC aperture jitter can be approximated to 110 fs. Inserting this value back into Equation 6 and Equation 7 leads to the following Equation 12:

$$SNR_{Jitter\_(Calculated)} = -20\log_{10}\left(2\pi \times f_{In} \times \sqrt{\left(t_{Jitter\_Clock}\right)^2 + \left(110\ fs\right)^2}\right) \quad (12)$$

With a value of 39 fs for the $t_{Jitter,Clock}$ (and plotting versus input frequency), Figure 17 shows that the calculated SNR as a result of jitter is a very close approximation to the measured SNR as a result of jitter.

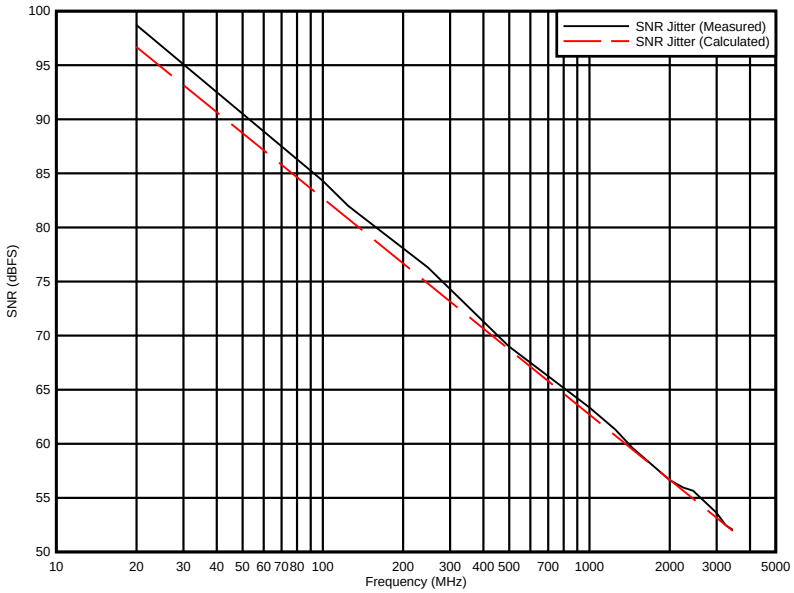


Figure 17. Calculated and Measured SNR as Result of Jitter

3.2.1 Quantifying Impact of Wideband Phase Noise

To clearly see the impact of wideband phase on the overall SNR, use a clean clock generator such as the SMA100A with varying amounts of wideband noise injected into the clock path, as Figure 18 shows.

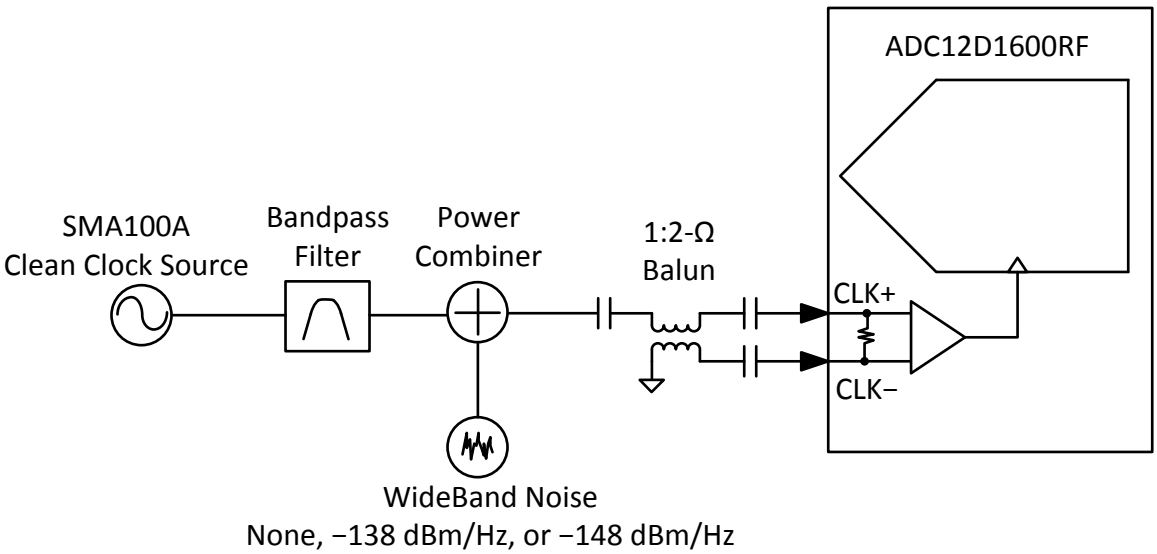


Figure 18. Clock Signal Source With Varying Amounts of Wideband Noise

Figure 19 shows the integrated jitter for three clock sources with varying amounts of wideband noise. Note that the curves have been measured by high-end equipment and corrected by using Equation 5 to account for the insertion losses and ADC12D1600RF noise floor.

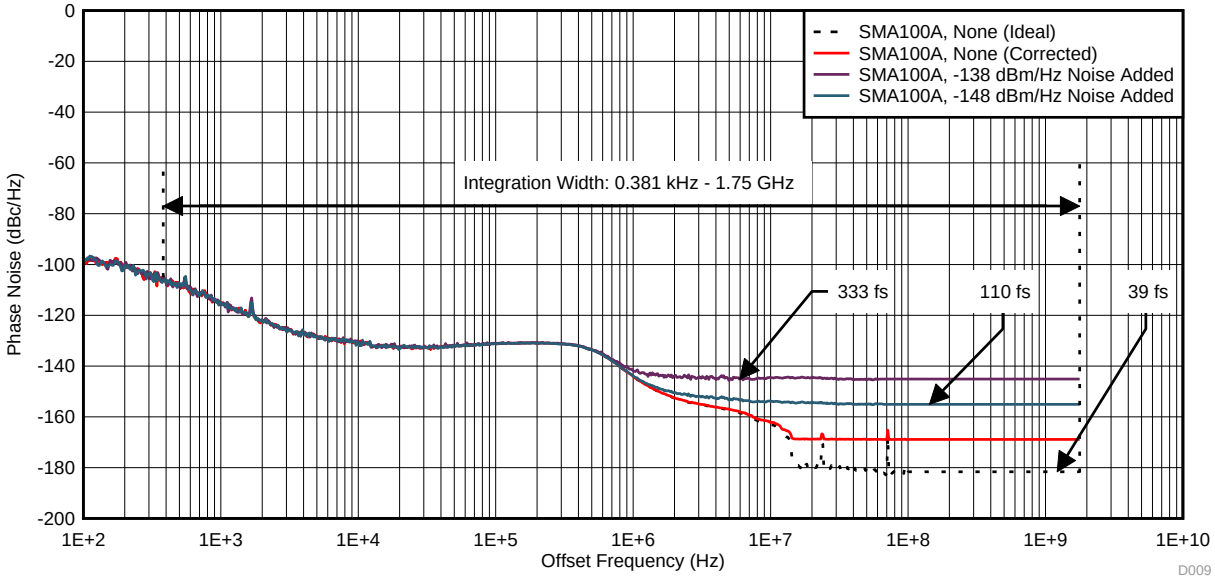


Figure 19. Various Clock Sources With Integrated Jitter

Using the integrated jitter for the three clock sources in the preceding Figure 19 and utilizing Equation 12, the SNR as a result of jitter can be calculated across the input frequency. Using this value along with 74 dBFS for the $SNR_{Quantization}$, 61.384 dBFS for $SNR_{Thermal\_Noise}$, and the measured $SNR_{Higher\_Order\_Harmonics}$ from Figure 16, the SNR_{Total} can be calculated with Equation 1 and plotted in the following Figure 20. Figure 20 shows the plots of the measured SNR for all three conditions, which shows that the calculations approximate the measured SNR very closely.

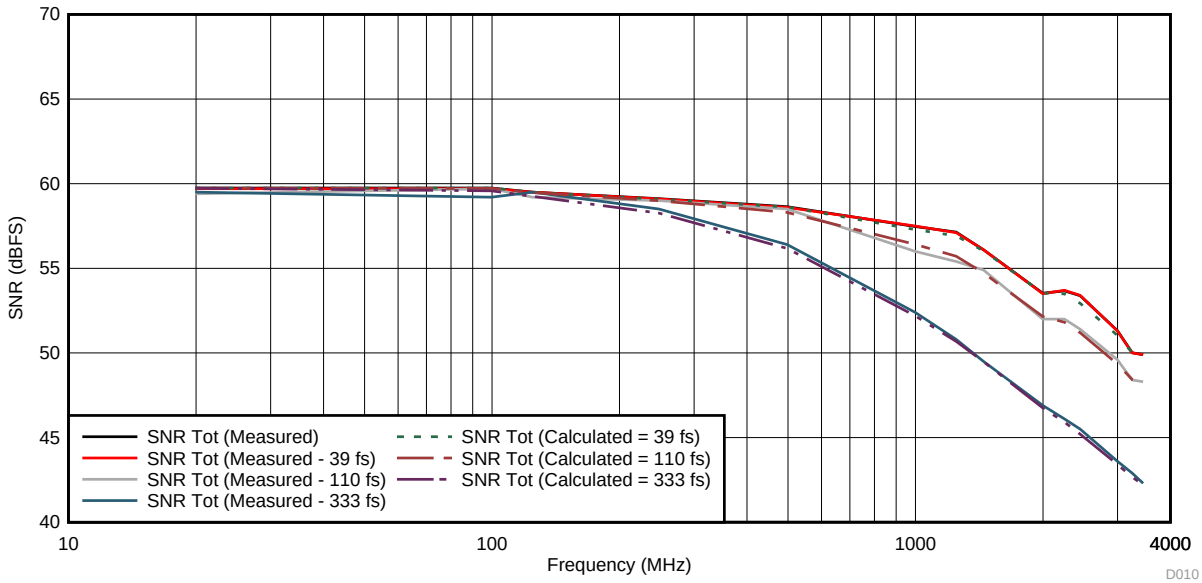


Figure 20. Measured and Calculated SNR versus Input Frequency

3.3 Effect of Clock Amplitude on SNR as Result of Jitter

Verifying the effects of the clock amplitude is also important. For a sine wave clock source, decreasing the amplitude essentially decreases the slew rate at the zero crossing where the clock receiver is most sensitive to noise coupling in as sampling error. Figure 21 shows the phase noise for nine different clock amplitudes. Equation 5 was used to approximate the amount of jitter present at the ADC clock inputs by taking into account the 3.4 dB of insertion loss from the onboard clock balun, as well as the −162-dBm/Hz noise floor of the clock receiver.

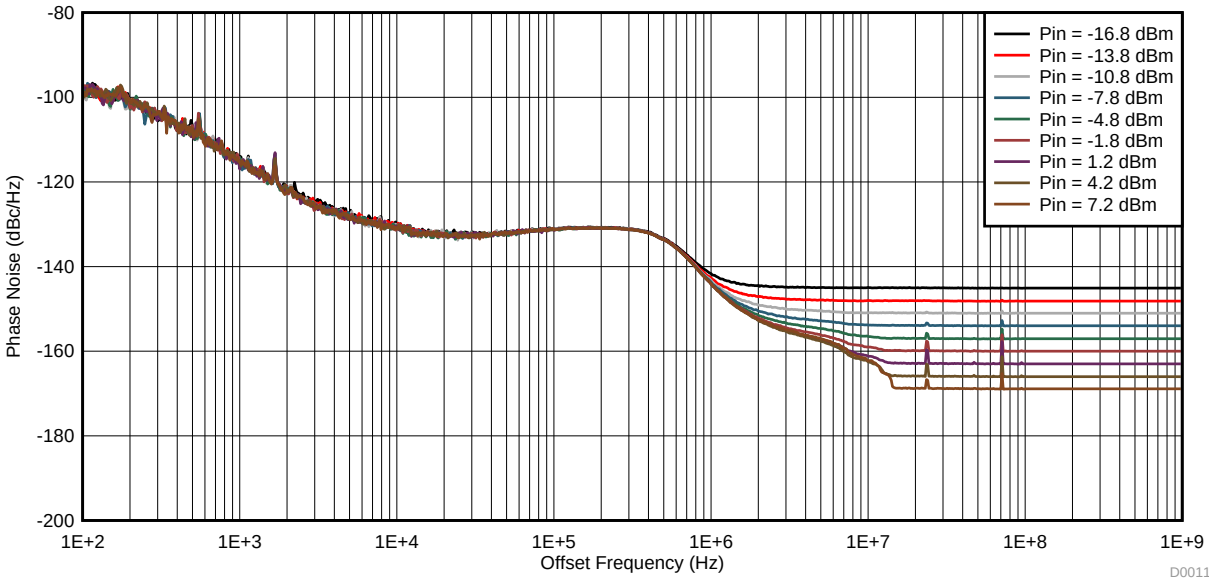


Figure 21. Phase Noise of Various Clock Amplitudes

Table 8 shows the calculated RMS jitter for each of the corrected clock amplitudes.

Table 8. Effects of Clock Amplitude on Integrated Jitter

CLOCK SOURCE AMPLITUDE (dBm)	CORRECTED CLOCK SOURCE AMPLITUDE (dBm)	INTEGRATED PHASE NOISE 381 Hz TO 1.75 GHz (fs)
10.6	7.2	38.7
7.6	4.2	44.4
4.6	1.2	53.6
1.6	–1.8	68.4
–1.4	–4.8	90.7
–4.4	–7.8	123.6
–7.4	–10.8	171.5
–10.4	–13.8	240.1
–13.4	–16.8	337.0

Selecting a high input frequency of 1448 MHz shows the clearest impact where the SNR curve is mostly dominated by jitter.

Figure 22 shows that by using Equation 12 and the values from Table 8, the calculated SNR as a result of jitter lines up very closely with the measured SNR as a result of jitter. Therefore, the effects of the clock amplitude can also be taken into account if the phase noise profile of the clock source is known.

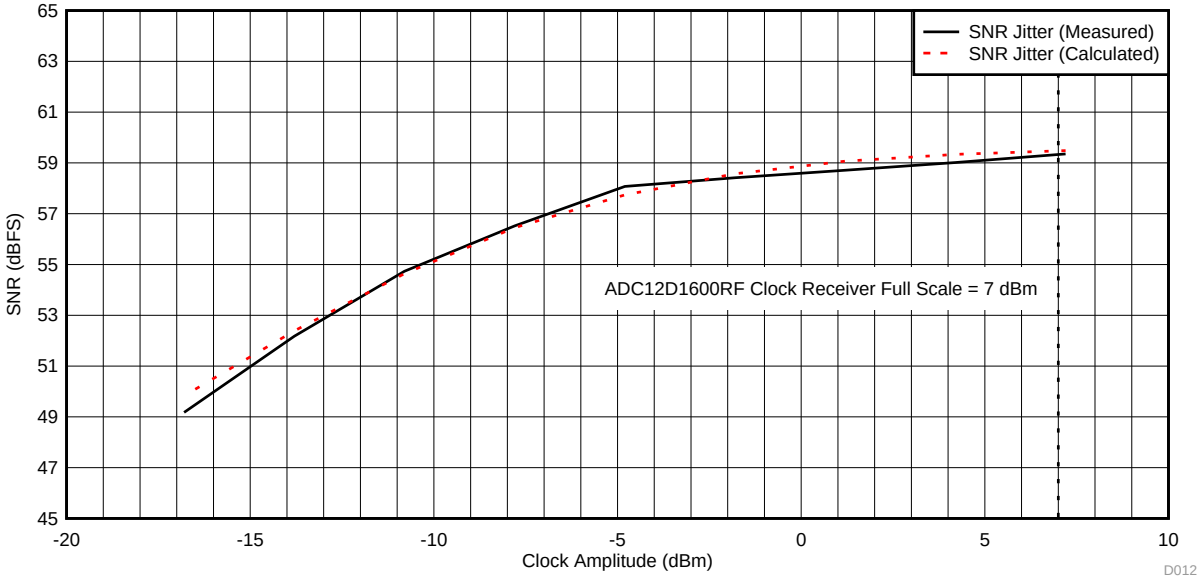


Figure 22. Measured and Calculated SNR as Result of Jitter versus Clock Amplitude

3.4 Approximating SNR in Closed Form

Using Equation 4 and the measured values established earlier in the guide to estimate the SNR impact as a result of higher-order harmonics (64.422 dBFS), approximate the total SNR for the ADC12D1600RF with the following Equation 13:

$$SNR_{Total\_Approx\_dBFS} = -10\log_{10}\left(10^{\left(\frac{-74\ dBFS}{10}\right)} + 10^{\left(\frac{-61.384\ dBFS}{10}\right)} + 10^{\left(\frac{-64.422\ dBFS}{10}\right)} + 10^{\left(\frac{20\log_{10}\left(2\pi \times f_{In} \times \sqrt{\left(t_{Jitter\_Clock}\right)^2 + (110\ fs)^2}\right)}{10}\right)}\right) \quad (13)$$

The SNR is typically given in dBc, so Equation 13 is easy to modify with the following form in Equation 14:

$$SNR_{Total\_Approx\_dBc} = SNR_{Total\_Approx\_dBFS} + P_{In\_dBFS} \quad (14)$$

Figure 23 shows the plot of Equation 14 versus the input frequency with various values for $t_{Jitter,Clock}$ and an input power of –0.5 dBFS. Note that even with an ideal case of 0 fs for the clock jitter, the SNR curve still rolls off because of the ADC aperture jitter.

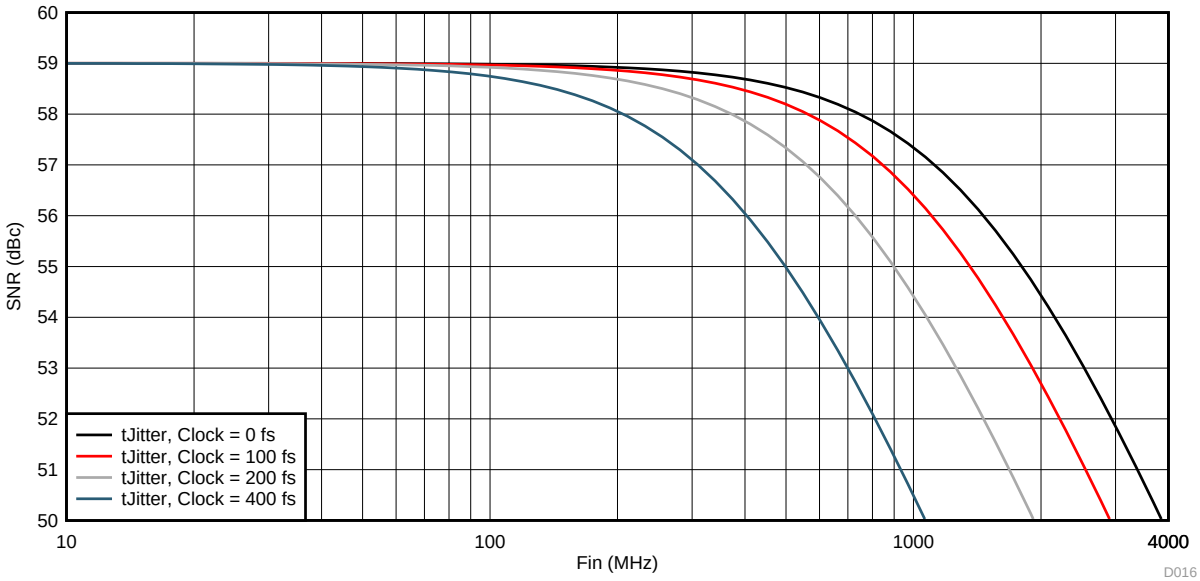


Figure 23. Generalized SNR for ADC12D1600RF versus Input Frequency

Table 9. SNR Compared Against Datasheet, Measured, and Estimated

f_{in} (MHz)	A_{in} (dBFS)	$SNR_{Datasheet}$ (dBc)	$SNR_{Measured}$ (dBc)	$SNR_{Approximated}$ (dBc)
125	–0.5	59	59	59
248	–0.5	58.6	58.6	58.9
498	–0.5	58.2	58.2	58.5
998	–0.5	57	57	57.2
1448	–0.5	55.4	55.6	55.9

Using Equation 14 and the frequencies and amplitudes from Table 9, the approximated SNR compares well to both the measured SNR and datasheet SNR.

4 Requirements for High-Speed Digitizer

The main requirement for a 12-bit high-speed digitizer is to maintain greater than 9-bits ENOB over the entire 1st Nyquist zone, which is 800 MHz for a sample rate of 1600 MSPS. For spectral analysis, the resolution bandwidth (RBW) must be less than 50 kHz, which means an FFT size of 16384 may be used, which has an RBW of 48.88 kHz.

To maintain this performance, the user must understand how to estimate ENOB for a given clock jitter. ENOB can be calculated from SNR, signal-to-noise and distortion ratio (SINAD), and THD with the following Equation 15 and Equation 16.

$$\text{SINAD} = -10\log_{10}\left(10^{\left(\frac{-\text{SNR}}{10}\right)} + 10^{\left(\frac{-\text{THD}}{10}\right)}\right) \quad (15)$$

Because of the folding and interpolating architecture of the ADC12D1600RF, the THD remains relatively constant across the input frequency and can be approximated to 64 dBFS.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (16)$$

Using Equation 13, Equation 15, Equation 16, and a value of 64 dBFS for THD, Figure 24 shows the approximated ENOB versus input frequency with various clock sources integrated from 24.414 kHz to 1.75 GHz.

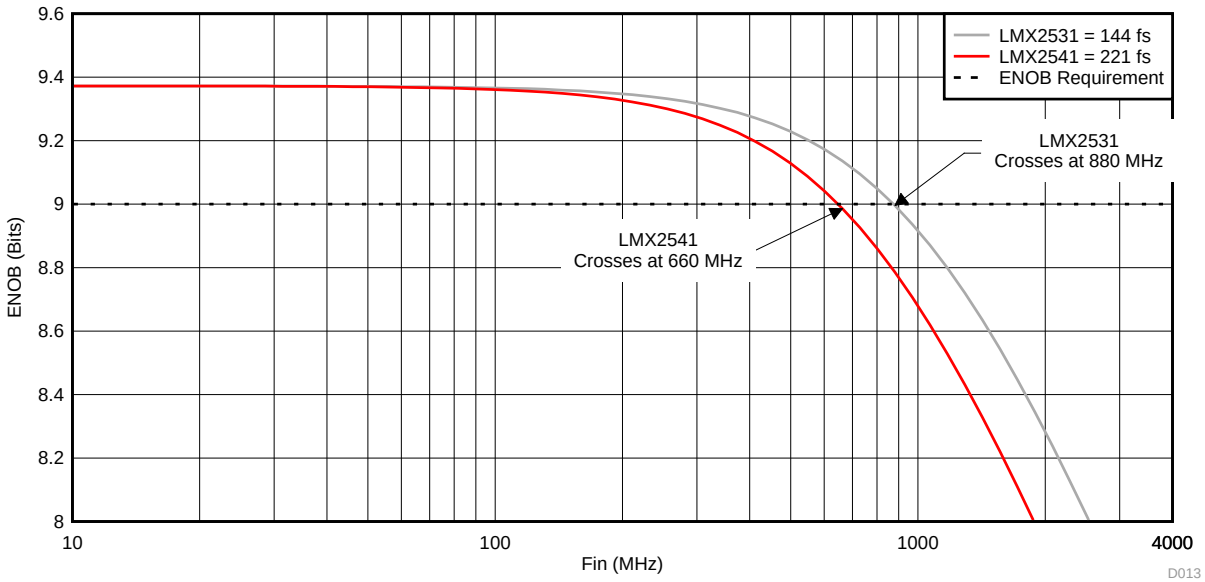


Figure 24. Calculated ENOB versus Input Frequency

The LMX2531 has an integrated phase noise of 144 fs, which can maintain 9-bit ENOB up to an input frequency of 880 MHz and satisfies the requirements of a 1st Nyquist 12-bit high-speed digitizer, whereas the LMX2541 falls short at 660 MHz. Additionally, if coherent sampling is not required, then a windowing function can be used and the sample size may be further increased with little degradation because of the low wideband performance of the LMX2531 device.

Using the ADC12D1600RFRB and the LMX2531, signals can be effectively digitized to 9 bits of effective resolution over the specified range, as the following Figure 25 and Figure 26 show.

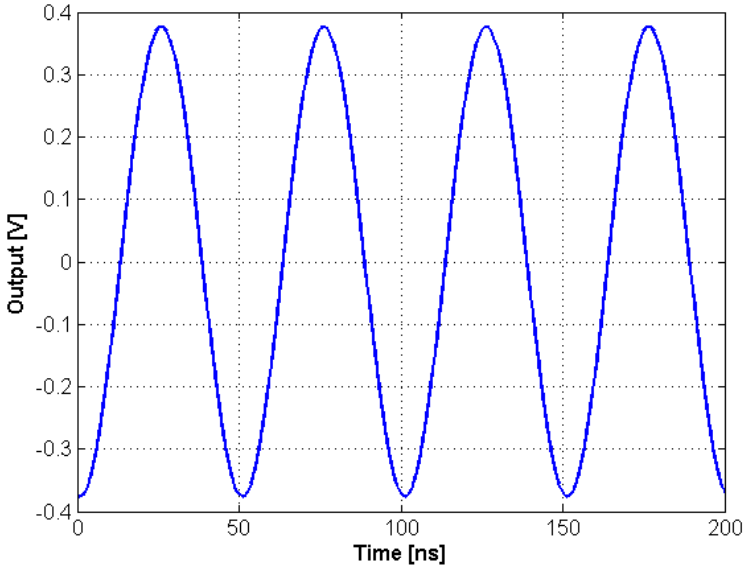


Figure 25. 20-MHz Input Signal Digitized in Time Domain With ADC12D1600RFRB and LMX2531

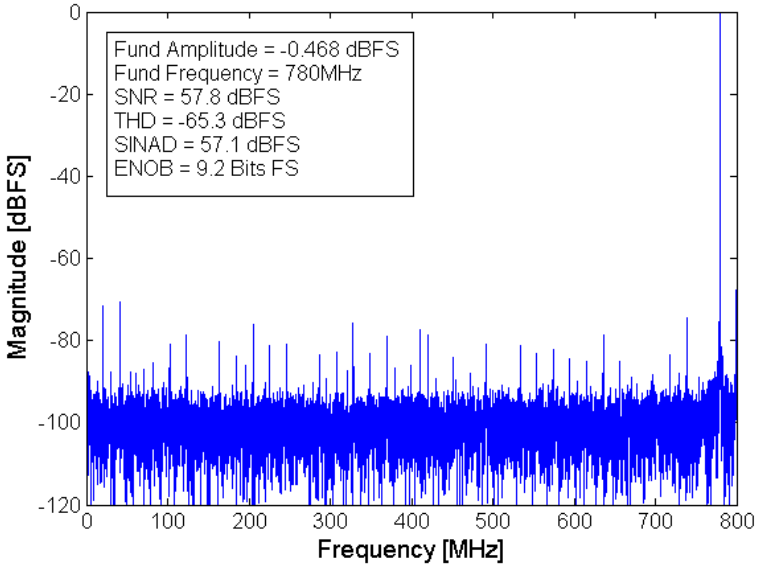


Figure 26. 780-MHz Input Signal Digitized FFT With ADC12D1600RFRB, LMX2531, and 16384 Points

5 Summary

When considering which GHz clock source to use, understanding all of the individual SNR contributors allows the designer to establish how much jitter budget is available for the clock source. Equation 13 represents a closed-form approximation of the ADC12D1600RF SNR versus the input frequency, which can be manipulated to approximate other important AC parameters, such as the SINAD or ENOB. Recreating the results for the other ADCs in this product family and computing the clock jitter requirements for a high-speed digitizer application are possible when using the techniques described in this design guide.

6 References

1. Texas Instruments, *ADC12D1000RF, ADC12D1600RF ADC12D1600/1000RF 12-Bit, 3.2/2.0 GSPS RF Sampling ADC*, ADC12D1600RF Datasheet (SNAS519)
2. Texas Instruments, *LMX2531 High-Performance Frequency Synthesizer System With Integrated VCO*, LMX2531 Datasheet (SNAS252)
3. Texas Instruments, *Maximizing SFDR Performance in the GSPS ADC: Spur Sources and Methods of Mitigation*, Application Report (SLAA617)
4. Texas Instruments, *Clock Jitter Analyzed in the Time Domain*, Data Acquisition Articles Parts 1–3 (SLYT379, SLYT389, SLYT422)
5. National Semiconductor, *ADC12D1X00RFRB Reference Board Users' Guide*, ADC12D1X00RFRB Datasheet (SNAU017)

7 About the Author

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