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Class 0.5 Three-Phase Energy Measurement System With Enhanced ESD Protection

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Design Resources

TIDM-3PH-ENERGY5-ESD	Tool Folder Containing Design Files
MSP430F67641A	Product Folder
TPS54060	Product Folder
CC2530	Product Folder
CC2530EMK	Product Folder
TIDM-LOWEND-IHD	Product Folder

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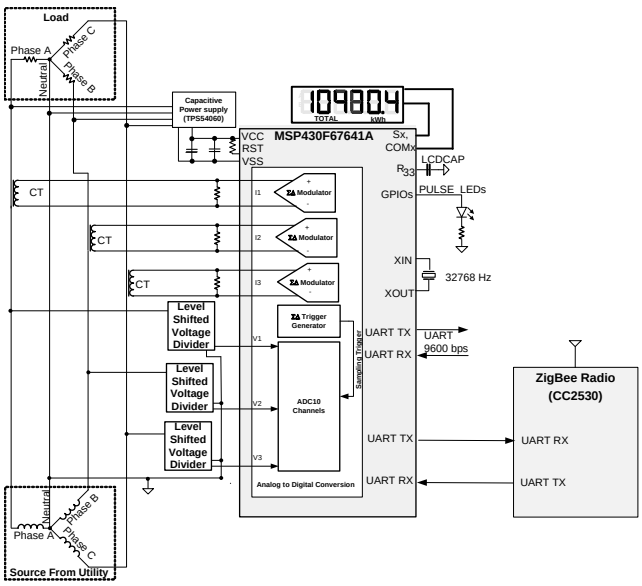
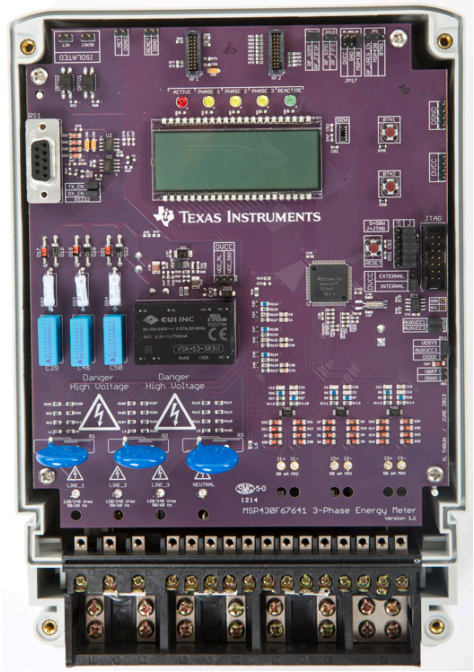
Design Features

- Three-Phase Energy Measurement System Which Exceeds Class 0.5 Accuracy Requirements from ANSI and IEC
- Passed IEC 61000-4-2 Level-4 Air Discharge Tests [1]
- TI Energy Library Firmware Calculates All Energy Measurement Parameters Including Active and Reactive Power; Active and Reactive Energy; Root Mean Square (RMS) Current and Voltage; Power Factor; and Line Frequency
- Support for ZigBee® Communication to In-Home Display or Connections to Wi-Fi®, Wireless M-Bus, and IEEE-802.15.4g Add-On Communications Modules
- Automated or Manual Switching Between Main and Auxiliary Power Sources for Metrology Engine

Featured Applications

- Metering
- Street Lighting





1 System Description

This design implements an ANSI/IEC Class 0.5 three-phase energy measurement system with enhanced electrostatic discharge (ESD) protection. The design also features communications through ZigBee® connectivity. The energy measurement system on chip (SoC) is used to perform all metrology functions and sends active power results to the CC2530EM add-on board. Developers can use the companion In-Home Display TI Design (TIDM-LOWEND-IHD) to display results remotely [2].

The design guide has a complete metrology source code provided as a downloadable *.zip* file.

1.1 MSP430F67641A

For sensing and calculating the metrology parameters, the MSP430F67641A energy measurement SoC is used. This device is the latest metering SoC that belongs to the MSP430F67xxA family of devices. This MSP430F67xxA family of devices offers enhancements when compared to the previous non-A MSP430F67xx devices, such as the MSP430F67641. One of these enhancements addresses improved ESD robustness (see the *Differences Between MSP430F67xx and MSP430F67xxA Devices* application note (SLAA666) for more details on this change as well as other changes compared to the non-A MSP430F67xx devices). These ESD enhancements can enable increased ESD immunity when compared to the previous meters that are based on the non-A MSP430F67xx devices.

In regard to metrology, the MSP430F67641A energy library software has support for calculation of various parameters for three-phase energy measurement. The key parameters calculated during energy measurements are: RMS current and voltage; active power, reactive power, and energies; power factor; and frequency. The user can view these parameters from the calibration graphical user interface (GUI) or liquid crystal display (LCD).

1.2 CC2530

For ZigBee communication, the CC2530EMK evaluation kit is used. Place the board of the kit into the EVM's RF connector to enable ZigBee communication. The F67641A e-meter software automatically packages the active power readings into a packet. This packet is then sent to the CC2530 evaluation kit that is connected to the RF connector of the design.

The TIDM-LOWEND-IHD TI design can be used as a receiver. When using this as a receiver, the CC2530 on the IHD430 in-home display (IHD) receives the packet from the CC2530 on the design and displays the packet on the IHD430's LCD.

1.3 TPS54060

The TPS54060 device is used in the power supply to help provide a 3.3-V output from an input mains voltage of 120- to 230-$V_{AC,RMS}$ at 50/60 Hz. Figure 8 shows how the TPS54060 is used to create the 3.3-V output from the 120- to 230-$V_{AC,RMS}$ input.

2 Block Diagram

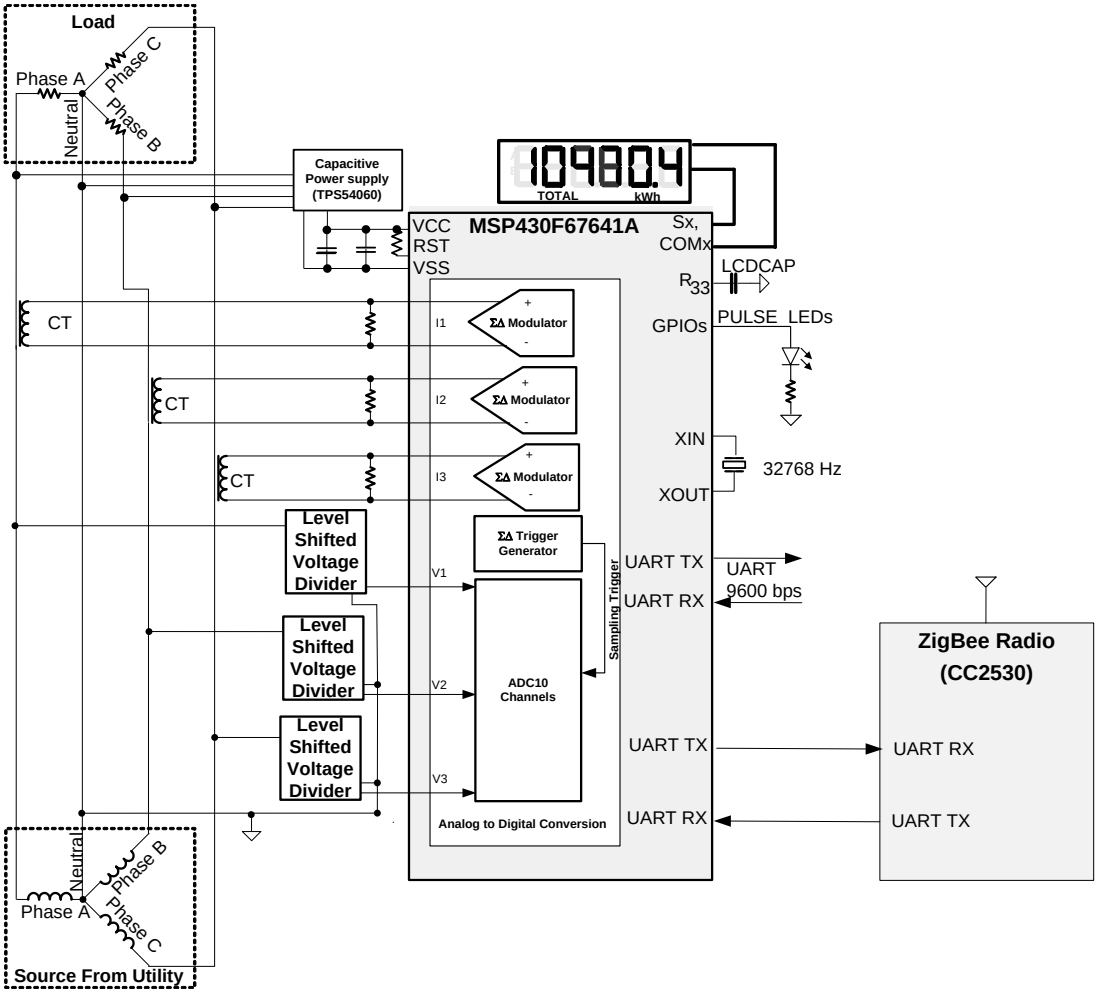


Figure 1. System Block Diagram

Figure 1 shows a block diagram that displays the high-level interface used for a three-phase energy meter application that uses the MSP430F67641A device. shows a three-phase, four-wire star connection to the AC mains in this case. In the diagram, a current sensor connects to the current channel. The current transformer (CT) has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is based on the manufacturer and current range required for energy measurements.

The trigger generator of the ΣΔ triggers the ADC10 to perform conversions, thereby synchronizing it with the ΣΔ converter's timings. For the voltage sensor, this design uses a combination of a voltage divider and level shifter to ensure that the input voltage to the ADC fits within the single-ended voltage range of operation. The chosen reference voltage source of the SAR ADCs determines this range of operation. The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to the normal input ranges that are valid for the SAR ADC, based on the selected reference voltage. Refer to the MSP4305xx/6xx user's guide (SLAU208) and device specific datasheet (SLASE50) for the ADC input voltage range.

Other signals of interest in Figure 1 are the PULSE LEDs, which are used to transmit active and reactive energy pulses used for accuracy measurement and calibration. The pulses are also used to transmit the active power consumed for each individual phase. In addition, the user can add ZigBee communication to an in-home display by connecting a CC2530EM board into the RF connectors of the design and flashing the CC2530 device with the proper software.

2.1 Highlighted Products

2.1.1 MSP430F67641A

Similar to the MSP430F67641, the MSP430F67641A belongs to the powerful 16-bit MSP430F6xx platform. This chip is intended for energy measurement applications and has the necessary architecture to perform this application. The F67641A has a powerful 25-MHz CPU with MSP430CPUx architecture. The analog front-end (AFE) consists of three independent 24-bit ΣΔ analog-to-digital converters (ADC) that are used for sensing current and a 10-bit SAR ADC for sensing phase voltages. The ΣΔ ADCs are based on a second-order sigma-delta architecture and they support differential inputs. The sigma-delta ADCs (SD24_B) operate independently and are capable of 24-bit results. The sigma-delta ADCs can be grouped together for simultaneous sampling of voltages and currents on the same trigger. In addition, SD24_B also has an integrated gain stage to support gains up to 128 for amplification of low-output current sensors.

In contrast, the 10-bit SAR supports single-ended inputs and performs sequential sampling of the three different phase voltages, the integrated temperature sensor, the voltage of the active supply powering the chip (VDSYS), and an additional optional auxiliary power supply (selected by the AUXADCSELx bits). The SD24_B on the F67641 module has a trigger generator that triggers the ADC10 to ensure that the timing between the ADC10 and ΣΔ modules are grouped and synchronized.

Additionally, a 32-bit x 32-bit hardware multiplier on this chip can be used to further accelerate math-intensive operations during energy computation. Using the multiplier, the software energy library supports calculation of various parameters for up to three-phase energy measurement.

Figure 2 shows a block diagram of the chip and displays the features of the MSP430F67641A.

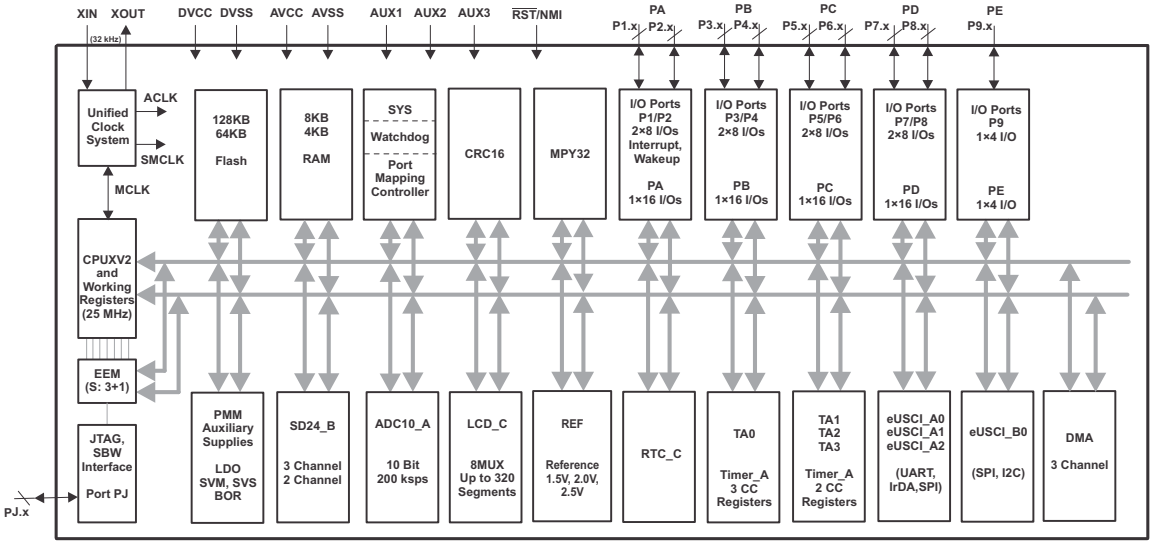


Figure 2. MSP430F67641 Block Diagram

CC2530

The CC2530 device is a true system on chip (SoC) solution for IEEE 802.15.4, ZigBee, and Radio Frequency for Consumer Electronics (RF4CE) applications. The CC2530 enables the building of robust network nodes with very-low bill of material costs. The CC2530 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful features. The CC2530 comes in four different flash versions: CC2530F32/64/128/256, with 32/64/128/256KB of flash memory, respectively. The CC2530 has various operating modes, making it highly suited for systems where ultra-low power consumption is required. Short transition times between operating modes further ensure low energy consumption. Combined with the industry-leading and golden-unit status ZigBee protocol stack (Z-Stack™) software from Texas Instruments, the CC2530F256 provides a robust and complete ZigBee solution.

2.1.2 TPS54060

The TPS54060 device is a 42-V, 0.5-A, step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the supply current to 116 µA when outputting regulated voltage without a load. Using the enable pin, shutdown supply current reduces to 1.3 µA when the enable pin is low.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The slow-start pin controls the output voltage start-up ramp. The output voltage startup ramp is controlled by the slow-start pin that can also be configured for sequencing or tracking. In addition, an open-drain, power good signal indicates the output is within 94% to 107% of its nominal voltage.

3 System Design Theory

3.1 ESD Introduction

Electrostatic discharge (ESD) is a single-event rapid transfer of electrostatic charge between two objects that are at different voltages. ESD events can have a negative effect on electronic systems such as e-meters. There can be many sources for ESD. For an e-meter in particular, a charged person that is in contact with the meter (such as the operator of a meter) can potentially subject the meter to ESD. Depending on the humidity of the environment, and the material used to charge the charged person, the voltage at which the person is charged varies.

Figure 3 shows the electrostatic voltages in relation to the humidity of the environment.

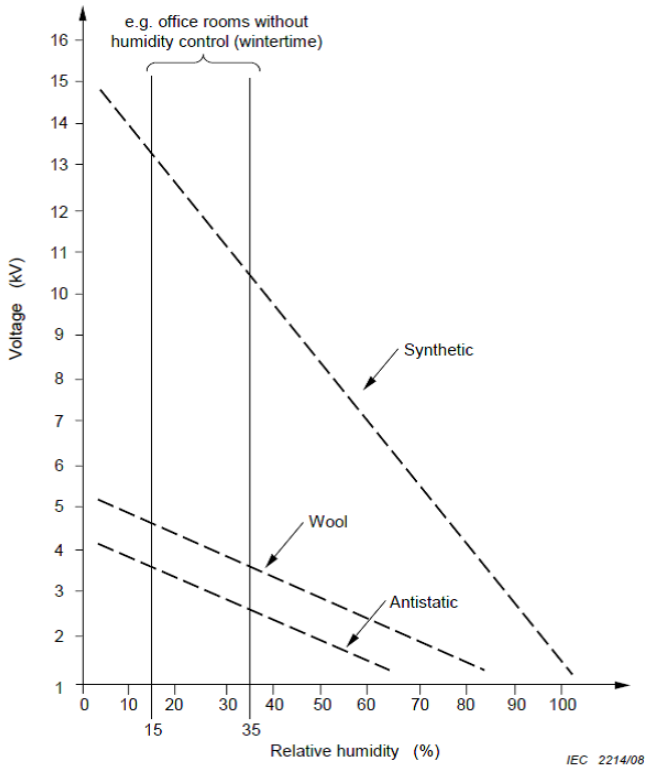


Figure 3. Maximum Values of Electrostatic Voltages People Can Be Charged to When in Contact With Different Materials [1]

Because these devices are used in billing applications and should always remain functional, e-meters must be designed with ESD immunity in consideration. The IEC 62052-11 standard accounts for this consideration by requiring all e-meters that adhere to this standard to pass ESD immunity tests according to IEC 61000-4-2.

The purpose of the IEC 61000-4-2 standard is to ensure that systems are tolerant of ESD exposure that may be present while a system is operating. The scope of the standard is to test electrical and electronic equipment that may be subjected to ESD from operators directly or from personnel to adjacent objects [1]. Depending on the equipment and environment in which the equipment operates, the amount of ESD exposure can vary. The IEC 61000-4-2 defines multiple levels to cover the different types of exposure levels. There are four standard levels; however, depending on special requirements, testing beyond these conditions may be conducted. Choose the selected level for testing based on the purpose of the implemented system and the environment where the tests are to be deployed. For each test, a special unit (sometimes referred to as an ESD gun), generates an ESD event that is meant to simulate the necessary ESD waveform.

Figure 4 shows an example of such an ESD waveform. Figure 5 shows this ESD gun, along with the entire setup for IEC 61000-4-2.

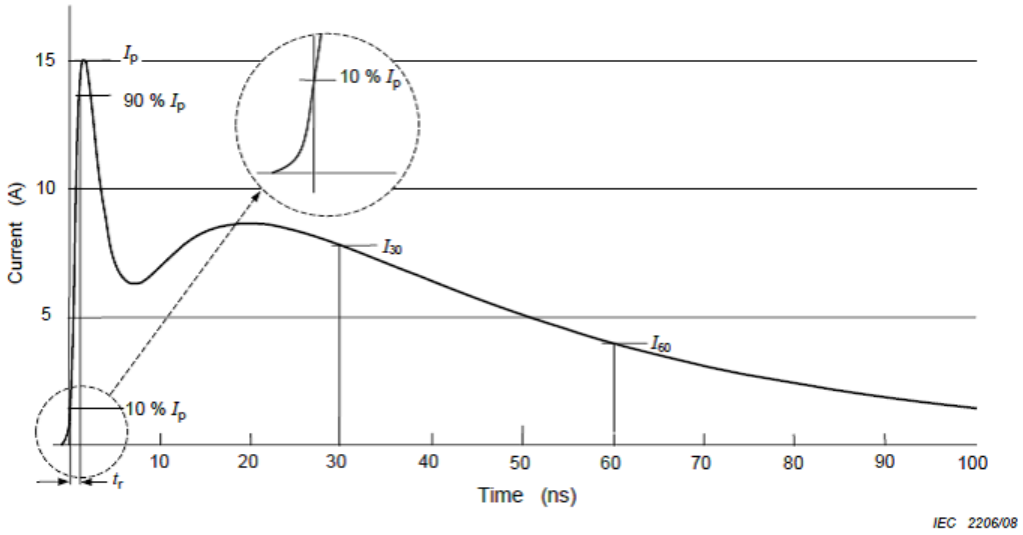


Figure 4. Ideal Contact Discharge Current Waveform at 4 kV (Taken from IEC 61000-4-2) [1]

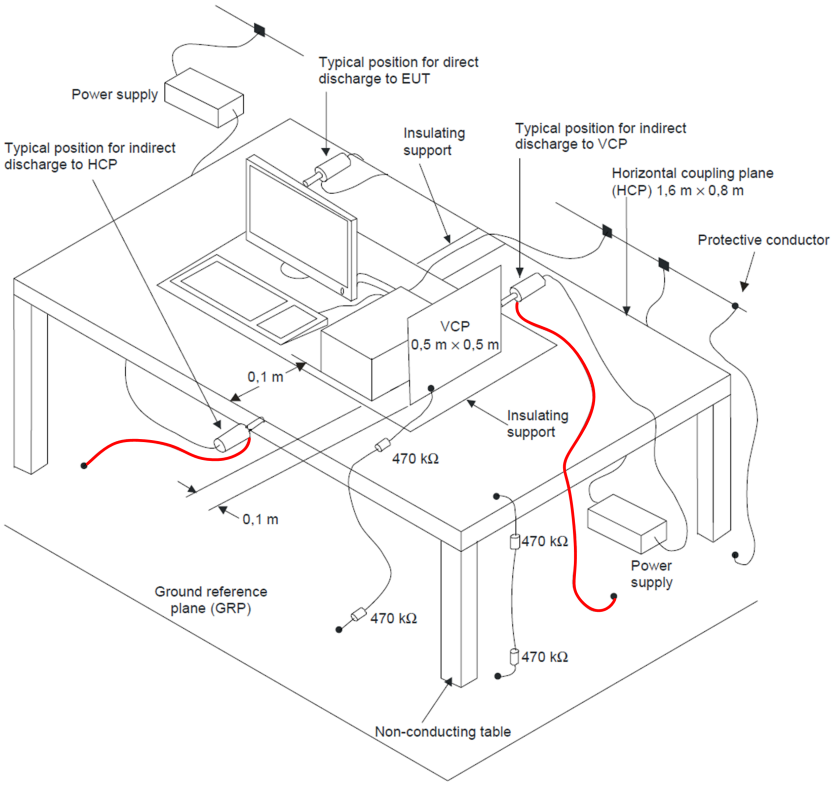


Figure 5. ESD Test Bench for Powered Condition [1] (Taken from IEC 61000-4-2)

For e-meters, IEC 62052-11 specifically mentions that IEC 61000-4-2 should be conducted with contact discharges (if applicable) of 8 kV and air discharges of 15 kV with ten discharge pulses at a rate of 1 Hz. However, based on different region requirements, sometimes a meter may have more stringent requirements and must pass immunity testing at higher ESD voltage levels or larger number of discharge pulses.

3.2 Design Hardware Implementation

3.2.1 Analog Inputs

The MSP430F6741A has a 10-bit SAR ADC (ADC10_A), three ΣΔ ADCs, and a mechanism to synchronize these two types of converters. Because the magnitude of the current waveform varies more than the magnitude of the voltage waveform, the higher accuracy ADCs must be used to sense current. As a result, the three ΣΔ ADCs should be used for measuring the phase currents. The SAR ADC can be used for measuring phase voltages.

The ΣΔ ADC is differential and requires that the input voltages at the pins do not exceed ±920 mV (gain = 1). To meet this specification, the current inputs must be divided down. In addition, the ΣΔ24 allows a maximum negative voltage of −1 V; therefore, the AC current signal from mains can be directly interfaced without the requirement for level shifters.

In contrast, the ADC10_A module has single-ended inputs. Therefore the ADC10_A requires that the sensed voltage is between 0-V_{REF} volts, with the option to select the V_{REF} source and voltage software. As a result, after the mains voltage is divided down for sensing, the voltage front-end circuitry requires a level shifter to properly interface to the ADC10_A module.

This sub-section describes the AFE used for voltage and current channels.

3.2.1.1 Voltage Inputs

The voltage from the mains is usually 230 V or 120 V and must be brought down to within V_{REF} volts. In the AFE for voltage, there consists a spike protection varistor, diodes, electromagnetic interference (EMI) filter beads (which help for ESD testing), a voltage divider and shifter network, and an RC low-pass filter that functions as an anti-alias filter.

Figure 6 shows the AFE for voltage inputs for a mains voltage of 230 V. In this circuitry, the voltage is brought down to within V_{REF} Volts, where V_{REF} is selected to be the 2.0-V reference produced by the chip's reference module. The maximum voltage that is fed to the ADC is usually a certain margin below the maximum V_{REF} voltage. As an example, when the 2.0-V reference is selected, the front-end may be built to produce a maximum voltage of 1.4 V to 1.6 V when the maximum mains voltage is applied. This margin helps prevents ADC clipping when the meter is exposed to harmonics or an overvoltage condition.

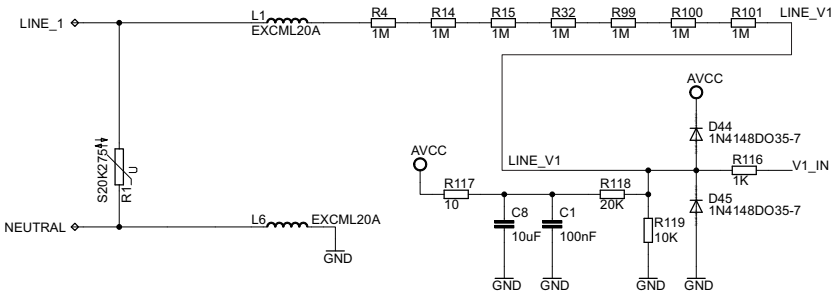


Figure 6. Analog Front End for Voltage Inputs

3.2.1.2 Current Inputs

The AFE for current inputs is slightly different from the AFE for the voltage inputs. Figure 7 shows the AFE used for a current channel. The AFE for current consists of diodes and transorbs for transient voltage suppression (TVS). In addition, the front-end consists of EMI filter beads (which help for ESD testing), burden resistors for current transformers, and also an RC low-pass filter that acts like an anti-alias filter.

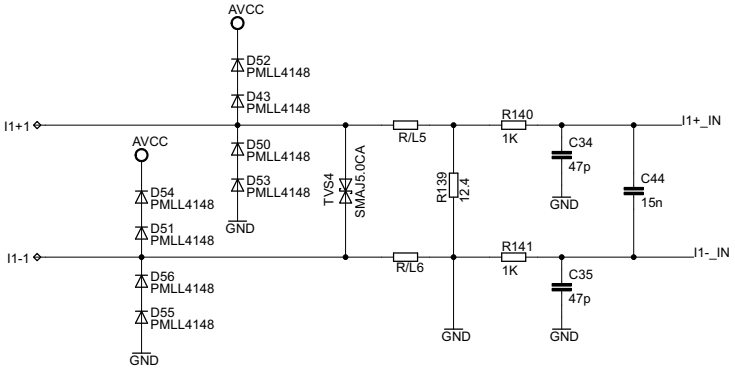


Figure 7. Analog Front End for Current Inputs

In Figure 7, resistor R139 is the burden resistor to select based on the current range used and the turns ratio specification of the current transformer or CT (CTs with a turns ratio of 2000:1 are used for this design). The value of the burden resistor for this design is 12.4 Ω. Based on the 100-A maximum current of this EVM, a CT turns ratio of 2000:1, and a burden resistor of 12.4 Ω, the input signal to the converter is a fully differential input with a voltage swing of ±877 mV maximum when the maximum current rating of the meter (100 A) is applied. Following the burden resistor is the anti-aliasing circuitry, which is implemented with resistors and capacitors.

3.2.2 Power Supply

The MSP430 family of microcontrollers support a number of low-power modes in addition to low-power consumption during active (measurement) mode when the CPU and other peripherals are active. Because an energy meter is always interfaced to the AC mains, deriving the DC supply required for the measuring element (MSP430F67641A) is easy using an AC-to-DC conversion mechanism.

The reduced power requirements of this device family allow design of power supplies to be small, extremely simple, and cost-effective. The power supply allows the operation of the energy meter by powering it directly from the mains.

Figure 8 shows a capacitor power supply that provides a single output voltage of 3.3 V directly from the mains of 120-$V_{AC,RMS}$ to 230-$V_{AC,RMS}$ at 50/60 Hz.

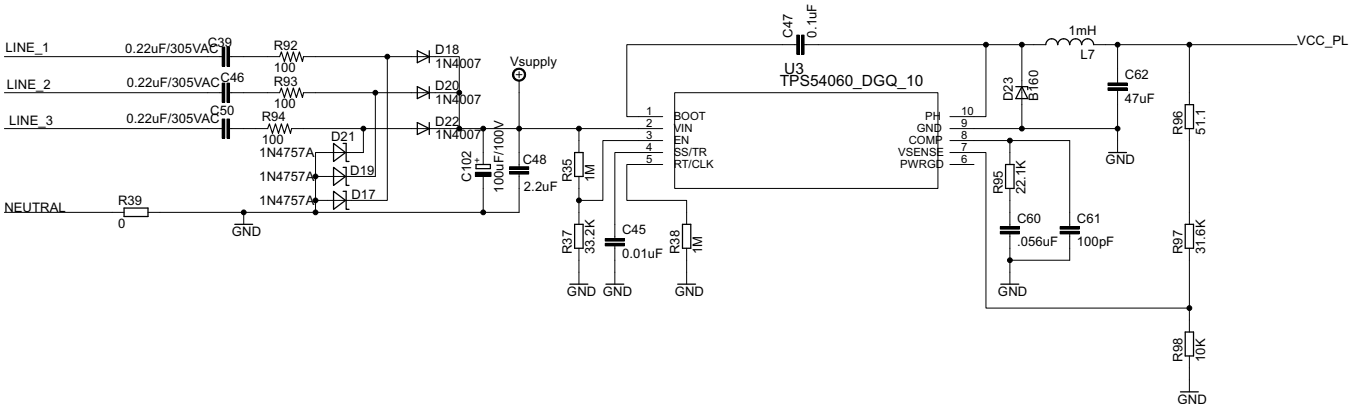


Figure 8. Simple Capacitive Power Supply for MSP430 Energy Meter

Figure 8 also shows how the voltage from the mains is directly fed to an RC-based circuit followed by a rectification circuit to provide a DC voltage for the operation of the MSP430 device. This DC voltage is regulated to 3.3 V for full-speed operation of the MSP430 device. The design equations for the power supply are given in the application report *Improved Load Current Capability for Cap-Drop Off-Line Power Supply for E-Meter* (SLVA491).

3.3 Metrology Software Implementation

This section discusses the software for the implementation of three-phase metrology. The first subsection discusses the setup of various peripherals of the MSP430 device. Subsequently, this section describes the entire metrology software as two major processes: the foreground process and background process.

3.3.1 Peripherals Setup

The major peripherals of the MSP430F67641A are the 24-bit sigma delta (SD24_B) ADC , the 10-bit SAR ADC (ADC10_A), auxiliary power supply module (AUX), clock system, real-time clock(RTC), LCD, and watchdog timer (WDT).

3.3.1.1 SD24_B Setup

The MSP430F67641A has three independent sigma-delta data converters, which measure the three currents in a three-phase system. In addition, the MSP430F67641A has a trigger generator module that triggers the ADC10, which senses the corresponding three voltages of the three-phase system. The code accompanying this design guide addresses the metrology for a three-phase system with limited discussion to anti-tampering.

The clock to the SD24 (f_M) ADCs and trigger generator derives from the digitally controlled oscillator (DCO) running at 25 MHz. The sampling frequency is defined as $f_s = f_M / OSR$, where the oversampling ratio (OSR) is chosen to be 256, and the modulation frequency, f_M, is chosen as 1.048576 MHz, resulting in a sampling frequency of 4.096 samples per second for the converters and a triggering frequency of 4096 Hz for the trigger generator. The SD24s are configured to generate regular interrupts every sampling instant.

The following are the ΣΔ channels associations:

A0.0+ and A0.0– → Current I1

A1.0+ and A1.0– → Current I2

A2.0+ and A2.0– → Current I3

3.3.1.2 ADC10_A Setup

The ADC10 samples the three mains voltages and is triggered by the ΣΔ's trigger generator. When triggered by the ΣΔ, the ADC10 enters autoscan mode and samples all of its 16 ADC channels once. In the software, the clock to the ADC10 is set to 4 MHz. The sample and hold time for each converter is 8 cycles and the conversion time is 12 cycles, which results in an approximate 20-cycle (approximately 5-µs) delay between conversion results of adjacent converters. In addition, the ADC10_A uses the 2.0-V reference from the REF module and is configured to output 10-bit results that are scaled to 16-bit twos complement numbers (ADC10DF = 1). This configuration allows the ADC results from the ADC10 to be treated as a 16-bit signed number when performing mathematical operations.

The following are the relevant ADC10 channel associations:

A12 (internal channel) → (AUXADC voltage) / 3, where AUXADC is selected to be DVCC

A11 (internal channel) → (VDSYS voltage) / 2

A10 (internal channel) → Temperature sensor

A5 → Voltage V1

A4 → Voltage V2

A3 → Voltage V3

3.3.1.3 AUX Module

To ensure that the 32-kHz oscillator is powered, the AUXVCC3 device must be powered. The AUXVCC3 powers through the use of software by powering it internally from DVCC using AUXVCC3's internal charger. Also, the ability to use the ADC10 to measure the primary or an auxiliary supply is enabled. In this software, the ADC10 is set to measure DVCC.

The AUX module is set so that hardware switching is enabled for DVCC, AUXVCC1, and AUXVCC2. In the software, the SVSMH voltage is set to level 4 (see the datasheet for the range of exact voltages that corresponds to a particular level). When VDSYS (the supply selected to power the chip), falls below this SVSMH level, the AUX module triggers for VDSYS to switch to another supply as long as the supply to switch to is above a user-defined threshold. The OK-voltage threshold for AUXVCC1 (AUX1LVL) and AUXVCC2 (AUX2LVL) is level 5. The OK-voltage level for DVCC (AUX0LVL) is level 6. Please note that if DVCC was previously not declared OK, but is later declared OK, the AUX module switches to DVCC even if VDSYS is not below the SVSMH level. This auto-switch behavior is only true for DVCC and is not applicable for AUXVCC1 or AUXVCC2. For more information about the AUX module, please consult the user's guide or the following TI design: http://www.ti.com/tool/TIDM-AUX-MODULE.

3.3.1.4 Real Time Clock (RTC_C)

The RTC_C is a real-time clock module that is configured to give precise one second interrupts. Based on these one second interrupts, the time and date are updated in the software, as necessary.

LCD Controller (LCD_C)

The LCD controller on the MSP430F67641A device can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to ACLK/64, which is 512 Hz.

3.3.2 Foreground Process

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. Figure 9 shows the flowchart for this process. The initialization routines involve the setup of the ADC, clock system, auxiliary supply system, general purpose input and output (GPIO) port pins, RTC module for clock functionality, LCD, and the USCI_A0 for universal asynchronous receiver and transmitter (UART) functionality. In addition, if ZigBee™ communication is enabled, the USCI_A2 is configured.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified to the foreground process to calculate new metering parameters. This notification is accomplished through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed current, voltage, and active and reactive quantities that have been accumulated for one second. This accumulation is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps tracks of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. The foreground process uses these dot products to calculate the corresponding metrology readings in real-world units. Processed voltages accumulate in a 48-bit register. In contrast, processed currents, active energies, and reactive energies accumulate in separate 64-bit registers to further process and obtain the RMS and mean values. Using the calculated values of active and reactive power from the foreground, the apparent power is calculated. The frequency (in Hz) and power factor are also calculated using parameters calculated by the background process using the formulas in Section 3.3.2.1.

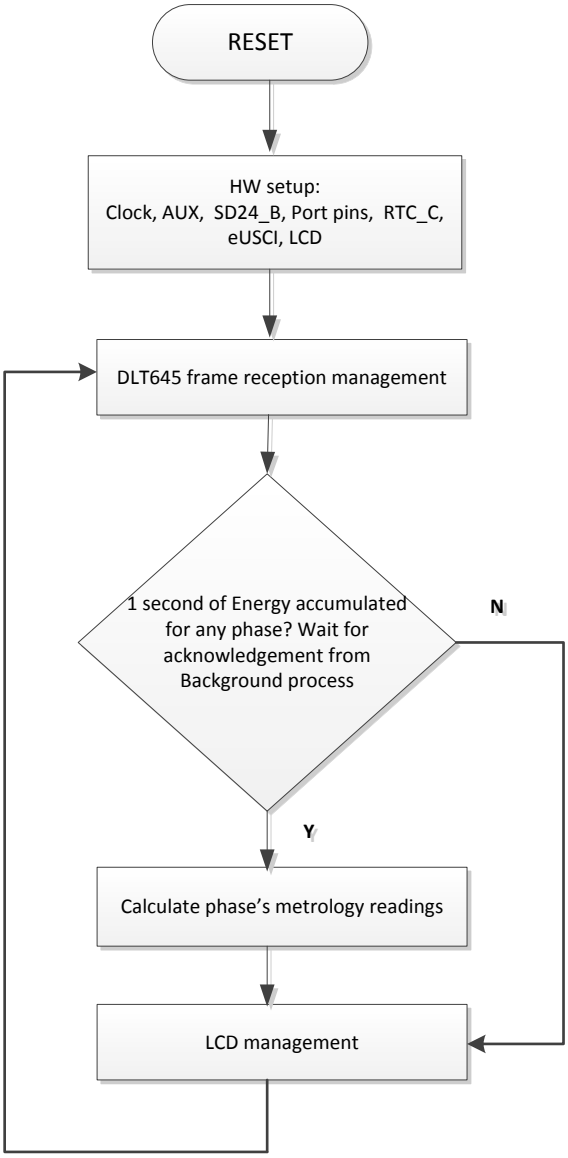


Figure 9. Foreground Process

3.3.2.1 Formulae

This section briefly describes the formulas used for the voltage, current, energy, and temperature calculations.

As previous sections describe, voltage and current samples are obtained at a sampling rate of 4096 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (1)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph}$$

where

- ph = Phase parameters that are being calculated [that is, Phase A(=1), B(=2), or C(=3)]
- $V_{ph}(n)$ = Voltage sample at a sample instant n
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ph}(n)$ = Each current sample at a sample instant n
- $I_{offset,ph}$= Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{v,ph}$ = Scaling factor for voltage
- $K_{i,ph}$ = Scaling factor for each current (2)

Power and energy are calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ph}(n)}{\text{Sample count}} \quad (3)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ph}(n)}{\text{Sample count}} \quad (4)$$

$$P_{APP,ph}{}^2 = \sqrt{P_{ACT,ph}{}^2 + P_{REACT,ph}{}^2}$$

where

- $V_{90}(n)$ = Voltage sample at a sample instant ‘n’ shifted by 90°
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power (5)

Please note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly (see Section 3.3.3.1.2 for details).

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90° before the current sample is used and a voltage sample slightly less than 90° before the current sample is used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the following Equation 6, Equation 7, and Equation 8:

$$P_{ACT,Cumulative} = \sum_{ph=1}^{3} P_{ACT,ph} \quad (6)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^{3} P_{REACT,ph} \quad (7)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^{3} P_{APP,ph} \quad (8)$$

Using the calculated powers, energies are calculated by the following formulas in Equation 9:

$$E_{ACT,ph} = P_{ACT,ph} \times Samplecount$$
$$E_{REACT,ph} = P_{REACT,ph} \times Samplecount$$
$$E_{APP,ph} = P_{APP,ph} \times Samplecount \quad (9)$$

From there, the energies are also accumulated to calculate the cumulative energies by the following Equation 10, Equation 11, and Equation 12:

$$E_{ACT,Cumulative} = \sum_{ph=1}^{3} E_{ACT,ph} \quad (10)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^{3} E_{REACT,ph} \quad (11)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^{3} E_{APP,ph} \quad (12)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since the system reset. Please note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by the following formula in Equation 13:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \tag{13}$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated by the following formula in Equation 14:

$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{ if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{ if inductive load} \end{cases} \tag{14}$$

In addition, temperature is also calculated in the software. The temperature is calculated using the TLV entries on the MSP430F67641 and in units of Celsius. The measured values for 30°C ±3°C and 85°C ±3°C for the 2.0-V reference are used for calculating temperature. The following Equation 15 shows the exact formula that is used to calculate temperature:

$$\text{Temp} = \left(\text{ADC(raw)} - \text{CAL\_ADC\_20T30}\right) \times \left(\frac{85 - 30}{\text{CAL\_ADC\_20T85} - \text{CAL\_ADC\_20T30}}\right) \tag{15}$$

3.3.3 Background Process

Figure 10 shows the background process, which mainly deals with timing critical events in software. The background process uses the SD24_B trigger generation to collect voltage and current samples. The ΣΔ interrupt occurs either when a new current sample is ready or when the trigger generator of the ΣΔ triggers the ADC10. As soon as the trigger to the ADC is generated, sample processing is done on the previously obtained voltage and current samples. This sample processing is done by the "per_sample_dsp()" function. After sample processing, the background process uses the "per_sample_energy_pulse_processing()" for the calculation and output of energy-proportional pulses. Figure 10 shows the flowchart for this process.

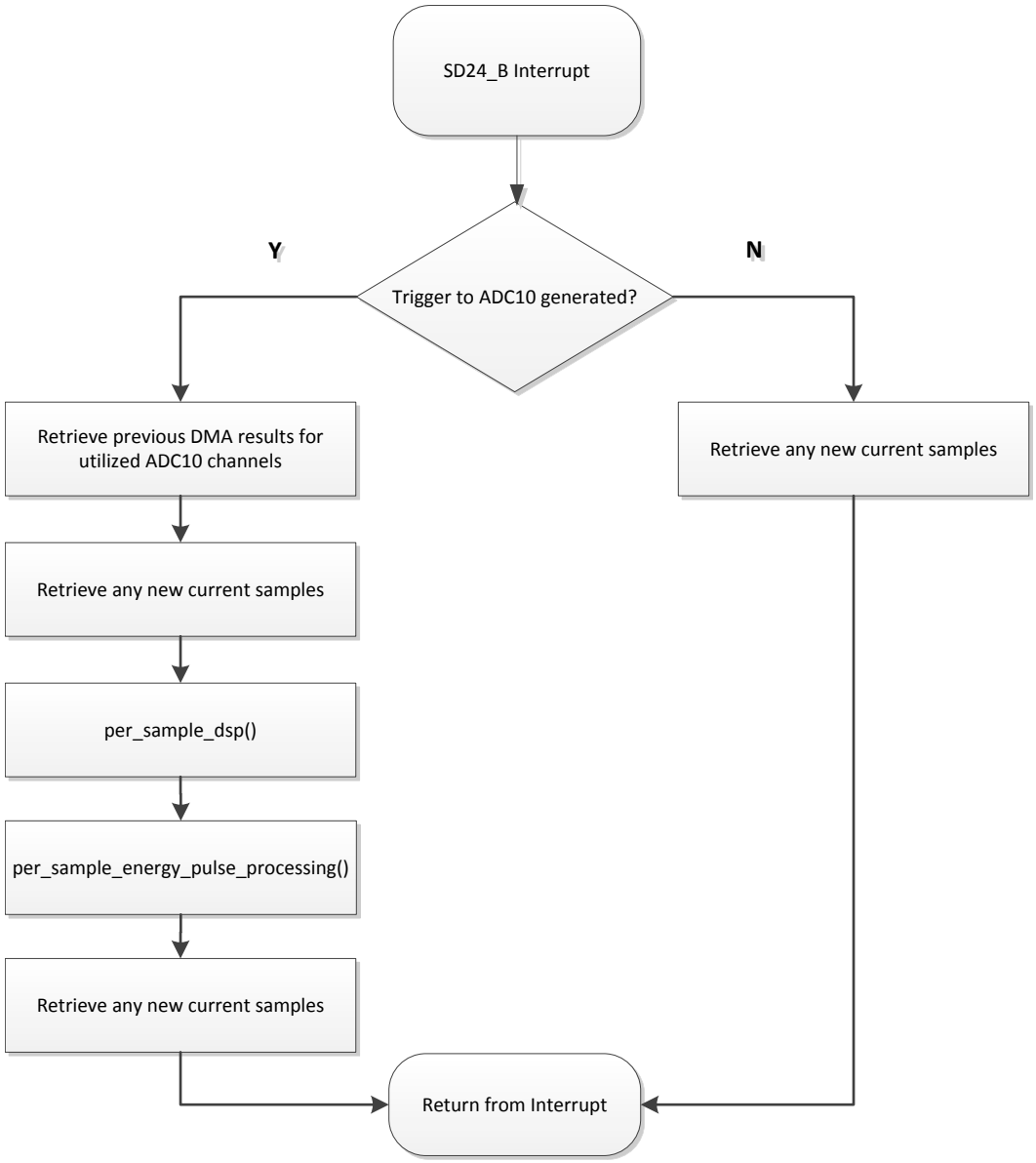


Figure 10. Background Process

When a trigger is generated, the next set of ADC10 conversions occur in parallel to the activity in the background process. Figure 11 shows this parallel activity. In Figure 11 the gray containers represent items that are done automatically by the configuration of the ADC10, DMA, and ΣΔ modules. For these gray items, CPU intervention is not required.

As Figure 11 represents, whenever the ADC10 is triggered, the ADC10 enters autoscan mode and samples all of its 16 ADC channels once. After each channel has a conversion result, the DMA automatically places these results in memory and the next channel's conversion is automatically started. For each converter, there is a memory location that stores the conversion results for that particular converter. The procedure of sampling a converter and storing the results in memory is repeated until the last converter (ADC10INCH = 0) is sampled. Because the clock to the ADC10 is set to 4 MHz, the sample and hold time for each converter is 8 cycles, and the conversion time is 12 cycles, there is an approximate 20-cycle (approximately 5-µs) delay between the conversion results of adjacent converters.

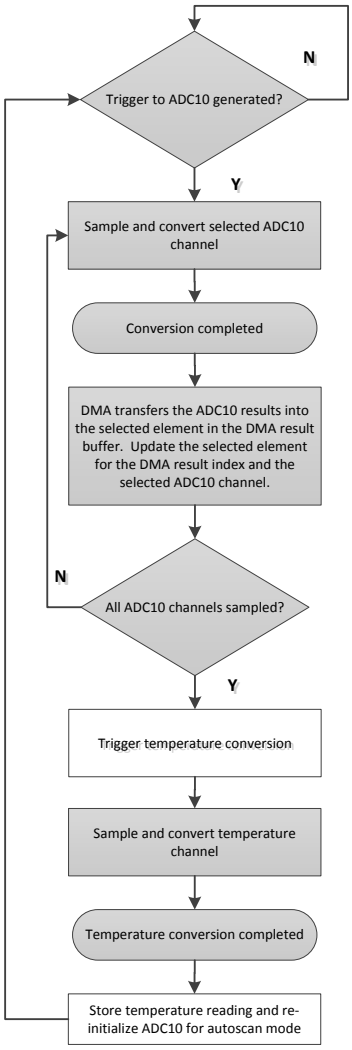


Figure 11. ADC10 Triggering Process

To sense the internal temperature sensor using the ADC10, a recommended sample period of at least 30 µs must be used. As a result, the temperature reading measured in the autoscan mode may be invalid because the sample time used is not sufficient. To mitigate this, a single conversion of the ADC10 temperature channel is triggered. This is triggered in the DMA ISR when all of the autoscan ADC results have been placed in the proper memory locations. After a temperature reading has been received, the ADC10 ISR is triggered. In this ISR, the temperature reading is stored and the ADC10 settings are then reset to support autoscan mode. The ADC10 enters autoscan mode again at the next trigger from the ΣΔ's trigger generator.

3.3.3.1 per_sample_dsp()

Figure 12 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. The ADC10 is configured to represent the 10-bit voltage results as a 16-bit signed result. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, as a result of using 24-bit current samples, the current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

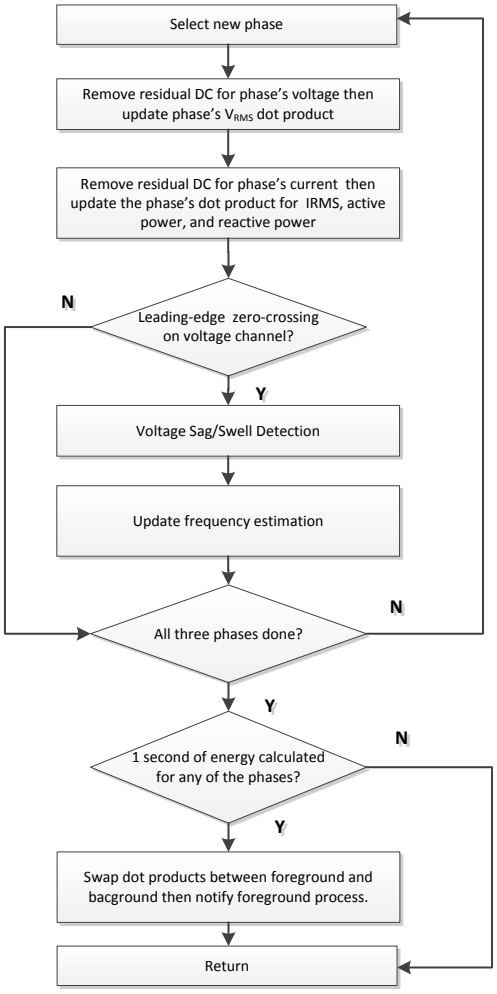


Figure 12. per_sample_dsp()

After sufficient samples (approximately one second's worth) have been accumulated, then the foreground function is triggered to calculate the final values of V_{RMS}; I_{RMS}; active, reactive, and apparent powers; active, reactive, and apparent energy; and frequency, temperature, and power factor. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products.

Whenever there is a leading-edge zero-crossing (− to + voltage transition) on a voltage channel, the per_sample_dsp() function is also responsible for updating the corresponding phase's frequency (in samples per cycle) and voltage sag and swell conditions. For the sag conditions, whenever the RMS voltage is below a certain user-defined threshold percentage, the number of mains cycles where this condition persists is logged as the sag duration. The number of periods in time where there was a sag condition is logged as the sag events count. Please note that the sag duration corresponds to the total number of cycles in a sag condition since being reset, and is therefore not cleared for every sag event. Also, when the RMS voltage is above a certain threshold percentage, swell events and duration are logged in a similar way.

The following sections describe the various elements of electricity measurement in the per_sample_dsp() function.

3.3.3.1.1 Voltage and Current Signals

The output of each SD24_B digital filter and ADC10 converter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. A separate DC estimate for all voltages and currents is obtained using the filter, voltage, and current samples, respectively. This estimate is then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active energy
- Accumulated energy samples using current and 90° phase-shifted voltage to calculate reactive energy

The foreground process processes these accumulated values.

3.3.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltages are accumulated in a 48-bit register. In contrast, the instantaneous currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one second's worth of samples have been accumulated, the background process stores these accumulation registers and notifies the foreground process to produce the average results, such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. Figure 13 shows the samples near a zero cross and the process of linear interpolation.

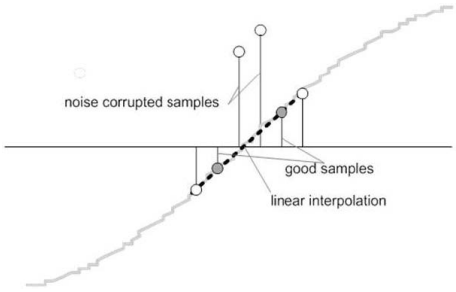


Figure 13. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points are interpolated from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair appear as if there is a zero crossing.

The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out any cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.3.3.2 LED Pulse Generation

In electricity meters, the energy consumption of the load is normally measured in a fraction of kilowatt-hour (KWh) pulses. This information can be used to accurately calibrate any meter for accuracy measurement. Typically, the measuring element (the MSP430 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, the pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, time jitters give a negative indication of the overall accuracy of the meter. The jitter must be averaged out due to this negative indication of accuracy.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates at every ΣΔ interrupt, thereby spreading the accumulated energy from the previous one-second time frame evenly for each interrupt in the current one-second time frame. This accumulation process is equivalent to converting power to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of the threshold in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy “tick” specified by meter manufacturers and is a constant. The “tick” is usually defined in pulses per kWh or just in KWh. One pulse must be generated for every energy “tick”. For example, in this application, the number of pulses generated per KWh is set to 1600 for active and reactive energies. The energy “tick” in this case is 1 KWh/1600. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO pins are used to produce the pulses.

In the EVM, the LEDs that are labeled “Phase 1”, “Phase 2”, “Phase 3”, and “Active” correspond to the active energy consumption for phase A, phase B, phase C, and the cumulative three-phase sum, respectively. “Reactive” corresponds to the cumulative three-phase reactive energy sum. The number of pulses per kWh and each pulse duration can be configured in software. Figure 14 shows the flow diagram for pulse generation. This flow diagram is valid for pulse generation of individual or accumulative phase active, reactive, and apparent energy

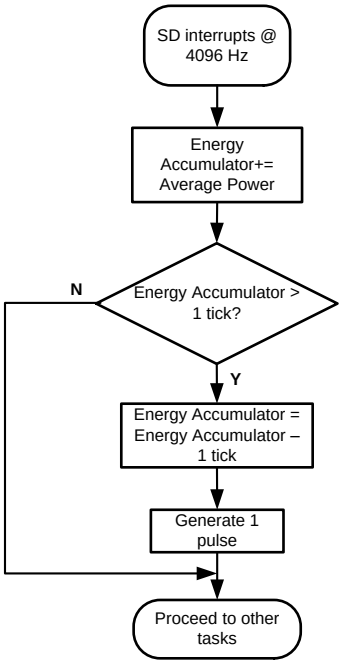


Figure 14. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and a 1-KWh threshold is defined as:

1-KWh threshold = 1 / 0.001 × 1 KW × (Number of interrupts per sec) × (number of seconds in one hour) = 1000000 × 4096 × 3600 = 0xD693A400000

3.3.3.3 Phase Compensation

When a CT is used as a sensor, it introduces additional phase shift on the current signals. Also, the passive components of the voltage and current input circuit may introduce another phase shift. Another source of phase shift is the sequential sampling on the voltage channel. The user must compensate the relative phase shift between voltage and current samples to ensure accurate measurements. The ΣΔ converters have programmable delay registers (ΣΔ24PREx) that can be applied to a particular channel. The use of this built-in feature (PRELOAD) is to provide the required phase compensation. Figure 15 shows the usage of PRELOAD to delay sampling on a particular channel.

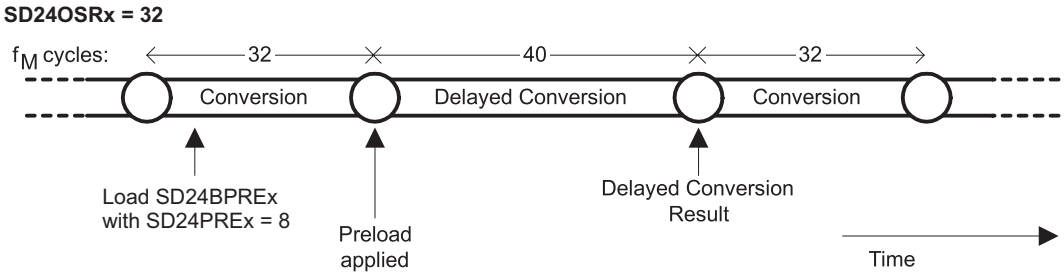


Figure 15. Phase Compensation Using PRELOAD Register

The fractional delay resolution is a function of input frequency (f_{IN}), OSR, and the sampling frequency (f_s).

$$\text{Delay resolution}_{\text{Deg}} = \frac{360^\circ \times f_{IN}}{OSR \times f_s} = \frac{360^\circ \times f_{IN}}{f_M} \quad (16)$$

In the current application, for an input frequency of 60 Hz, OSR of 256, and sampling frequency of 4096, the resolution for every bit in the preload register is about 0.02° with a maximum of 5.25° (maximum of 255 steps).

3.4 ESD Test Software

When exposing equipment to ESD testing, failures can be classified into three categories:

- Temporary loss of function or degradation of performance that ceases after the disturbance ceases. The equipment under test recovers its normal performance without operator intervention. This is an acceptable failure for an e-meter in IEC 62052-11, assuming the energy readings were not affected by an amount greater than a certain threshold.
- Temporary loss of function or degradation of performance. Recovery requires operator intervention.
- Temporary loss of function or degradation of performance that is not recoverable.

To better diagnose ESD failures from passes (and also distinguish the different failures into the three types of failures), a separate code example was loaded on the MSP430F67641A when performing ESD testing. In this code example, the RST/NMI pin is configured to NMI mode. Additionally, whenever a brownout reset occurs, the red light of the EVM blinks three times before staying ON. Afterward, the green LED of the EVM constantly blinks. If this green LED stops blinking, this indicates that the meter has temporarily stopped working. If the red LED starts blinking again after previously being ON, then a brownout reset event has reoccurred.

4 Getting Started Hardware

For testing this design, the EVM430-F67641 is used and its MSP430F67641 is replaced with a MSP430F67641A. The following figures of the EVM best describe the hardware: Figure 16 shows the top view of the energy meter and Figure 17 shows the location of various pieces of the EVM based on functionality.

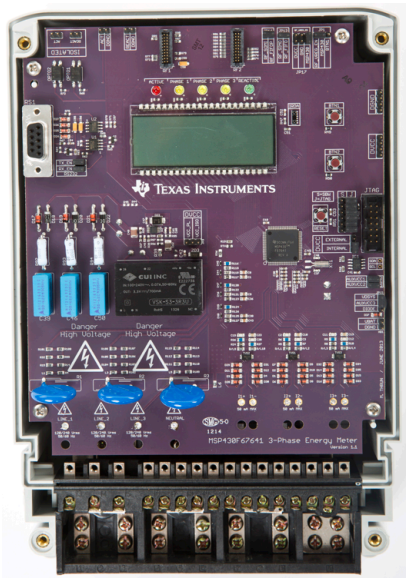


Figure 16. Top View Three-Phase Energy Meter EVM

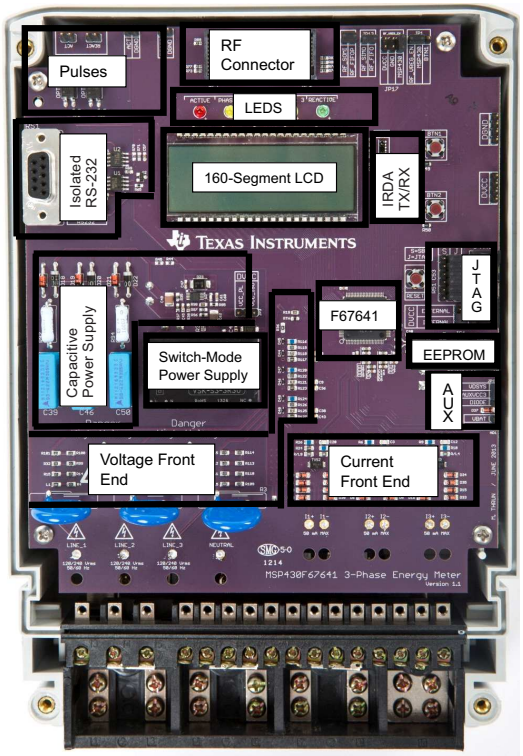


Figure 17. Top View Three-Phase Energy Meter EVM With Components Highlighted

4.1 Connections to the Test Setup for AC Voltages

AC voltage or currents can be applied to the board for testing purposes at these points:

- Pad “LINE_1” corresponds to the line connection for phase A.
- Pad “LINE_2” corresponds to the line connection for phase B.
- Pad “LINE_3” corresponds to the line connection for phase C.
- Pad “NEUTRAL” corresponds to the neutral voltage. The voltage between any of the three line connections to the neutral connection must not exceed 230-V AC at 50/60 Hz.
- I1+ and I1− are the current inputs after the sensors for phase A. When a current sensor is used, make sure that the voltage across I1+ and I1− does not exceed 920 mV. This is currently connected to a CT on the EVM.
- I2+ and I2− are the current inputs after the sensors for phase B. When a current sensor is used, make sure that the voltage across I2+ and I2− does not exceed 920 mV. This is currently connected to a CT on the EVM.
- I3+ and I3− are the current inputs after the sensors for phase C. When a current sensor is used, make sure that the voltage across I3+ and I3− does not exceed 920 mV. This is currently connected to a CT on the EVM.

Figure 18 and Figure 19 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. Figure 18 shows the connections from the top view. VA+ , VB+, and VC+ correspond to the line voltage for phases A, B, and C, respectively. VN corresponds to the neutral voltage from the test AC source.

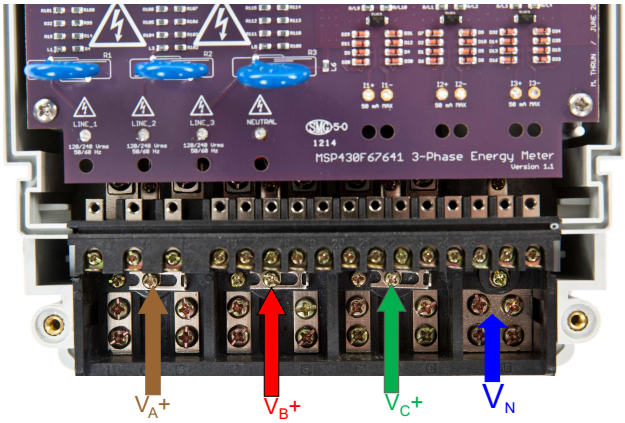


Figure 18. Top View of the EVM With Test Setup Connections

Figure 19 shows the connections from the front view. IA+ and IA− correspond to the current inputs for phase A; IB+ and IB− correspond to the current inputs for phase B; and IC+ and IC− correspond to the current inputs for phase C. VN corresponds to the neutral voltage from the test setup.

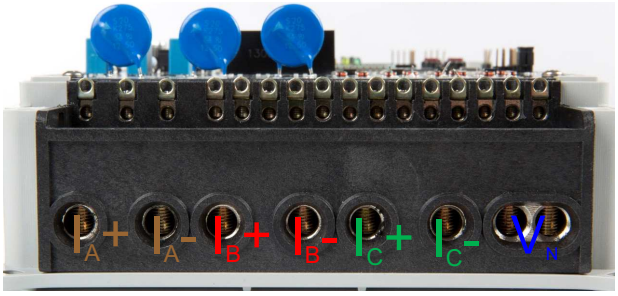


Figure 19. Top-Front View of the EVM With Test Setup Connections

4.2 Power Supply Options and Jumper Settings

A single DC voltage rail (DVCC) powers the entire board and the UART communication. DVCC can be derived either through JTAG, external power, or the AC mains through either the capacitive power supply or switching power supplies. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for blocks to function correctly. Table 1 shows the functionality of each jumper on the board and the associated functionality.

Table 1. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE CASE	COMMENTS
ACT/RTCCLK (Not isolated, do not probe)	2-pin header	Active energy pulses and RTC calibration (WARNING)	Probe between here and ground for cumulative three-phase active energy pulses. Alternatively, enable port mapping to connect this pin instead to RTCCLK. When connected to RTCCLK, probe here to measure the frequency of RTCCLK, which is used for calibrating the RTC.	This header is not isolated from AC voltage, so do not connect measuring equipment unless isolators external to the EVM are available. See the ISOLATED ACT header, instead. Please note that by default this pin is configured for outputting active pulses. The software must be modified to output RTCCLK.
AUXVCC1 (Not isolated, do not probe)	2-pin header	AUXVCC1 Selection and external power (WARNING)	Place a jumper here to connect AUXVCC1 to GND. This jumper must be present if AUXVCC1 is not used as a backup power supply. Alternatively, the header can be used to provide a backup power supply to the MSP430. To do so, connect the alternative power supply to this header. In addition, on the bottom of the board, a footprint is present that allows the addition of a supercap.	
AUXVCC2 (Not isolated, do not probe)	2-pin jumper header	AUXVCC2 selection; AUXVCC2 external power (WARNING)	Place a jumper here to connect AUXVCC2 to GND. This jumper must be present if AUXVCC2 is not used as a backup power supply. Alternatively, it can be used to provide a backup power supply to the MSP430. To do so, simply connect the alternative power supply to this header.	
AUXVCC3 (Not isolated, do not probe)/JP15	3-pin humper header option	AUXVCC3 selection and external power (WARNING)	To power the RTC externally regardless of whether DVCC is available, provide external voltage at AUXVCC3, disable the internal AUXVCC3 charger in software, and do not connect a jumper at this header. Alternatively, place a jumper at the “VDSYS” option to connect AUXVCC3 to VDSYS so that it is powered from whichever supply (DVCC, AUXVCC1, or AUXVCC2) is powering the chip. To power the RTC externally only when DVCC is not available, enable the internal charger, place a jumper at the “Diode -”, option and apply external voltage at the Diode + pin of the HD1 header.	
DGND (Not isolated, do not probe)	Header	Ground voltage header (WARNING)	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated. This voltage can be hot or neutral if AC wall plug is connected to the meter.
DVCC (Not isolated, do not probe)	Header	VCC voltage header (WARNING)	Not a jumper header; probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if board is powered from AC mains, unless the AC mains are isolated.
DVCC EXTERNAL (Do not connect JTAG if AC mains is the power source ;isolated JTAG or supply is fine)	Jumper header option	JTAG external power selection option (WARNING)	Place a jumper at this header option to select external voltage for JTAG programming.	This jumper option and the DVCC INTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
DVCC INTERNAL (Do not connect JTAG if AC mains is the power source)	Jumper header option	JTAG internal Power selection option (WARNING)	Place a jumper at this header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.	This jumper option and the DVCC EXTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
DVCC VCC_ISO	Jumper header option	Isolated power supply select	Place a jumper at this header position to power the board through AC mains using the switching power supply.	Place a jumper only if AC mains voltage is required to power the DVCC rail. This header option and the DVCC VCC_PL header option comprise one three-pin header that can be used to select either the capacitive power supply, isolated power supply, or neither (if jumper not present).
DVCC VCC_PL (Not isolated, do not probe)	Jumper header option	Capacitor power supply select (WARNING)	Place a jumper at this header position to power the board through AC mains using the capacitor power supply.	Place a jumper only if AC mains voltage is required to power the DVCC rail. Do not debug using JTAG unless AC source is isolated or JTAG is isolated. This header option and the DVCC VCC_ISO header option comprise one three-pin header that selects a capacitive power supply, an isolated power supply, or neither.
HD1	2-pin jumper header	AUXVCC3 External Power For AUXVCC3 “Diode” Option (WARNING)	When the “Diode −” option is selected for AUXVCC3, apply voltage at this header so that the RTC can still be powered when the voltage at DVCC is removed.	
ISOLATED ACT	1-pin header	Isolated active energy pulses	Not a jumper header, probe between here and ground for cumulative three-phase active energy pulses.	This header is isolated from AC voltage so it is safe to connect to scopes or other measuring equipment because isolators are already present.

Table 1. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE CASE	COMMENTS
ISOLATED REACT	1-pin header	Isolate reactive energy pulses	Not a jumper header, probe between here and ground for cumulative three-phase reactive energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present.
J (Do not connect JTAG if AC mains is the power source)	Jumper header option	4-wire JTAG programming option (WARNING)	Place jumpers at the J-header options of all of the six JTAG communication headers to select 4-wire JTAG.	Place jumpers at the six headers to select a JTAG communication option. Each of these six headers have a J option and an S option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, configure all of these headers for the J option. To enable SBW, configure all of the headers for the S option.
JP1	Jumper header option	MSP430 P1.7 connection selection	Place a jumper at the “BTN1” option to connect P1.7 of the MSP430 to the EVM’s “BTN1” button. Place a jumper at the “RF_VREG_EN” option to connect P1.7 of the MSP430 to the “MSP430” option of JP17 (RF_VREG_EN section).	When the BTN1 option is selected, pressing BTN1 makes P1.7 LOW. When the button is not pressed, P1.7 is HIGH. When the “RF_VREG_EN” is selected, the “MSP430” option must be selected from JP17 to connect P1.7 to the “RF_VREG_EN” of the radio module, which is connected to the board’s RF connectors.
JP13	Jumper Header	RF connector transmit enable	Place a jumper here to enable transmission to the radio module connected to the EVM’s RF connectors.	
JP14	Jumper header	RF connector receiver enable	Place a jumper here to enable receiving from the radio connected to the EVM’s RF connectors.	
JP17	Jumper header option (connect only one option to RF_VREG_EN)	RF connector’s RF_VREG_EN connection selection (WARNING)	Place a jumper between DVCC and RF_VREG_EN to connect the RF connector’s RF_VREG_EN connection to DVCC. Place a jumper between GND and RF_VREG_EN to connect the RF connector’s RF_VREG_EN connection to GND. Place a jumper between DVCC and RF_VREG_EN to connect the RF connector’s RF_VREG_EN connection to the “RF_VREG_EN” option of the JP1 header.	When the “MSP430” option is selected, the “RF_VREG_EN” option must be selected from JP1 to connect P1.7 to the “RF_VREG_EN” of the radio module connected to the board’s RF connectors.
REACT (Not isolated, do not probe)	1-pin header	Reactive energy pulses (WARNING)	Not a jumper header, probe between here and ground for cumulative three-phase reactive energy pulses.	This header is not isolated from AC voltage, so do not connect measuring equipment unless isolators external to the EVM are available. See the ISOLATED REACT header, instead.
RX_EN	Jumper header	RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232.	–
S (Do not connect JTAG if AC mains is the power source)	Jumper header option	SBW JTAG programming option (WARNING)	Place jumpers at the S-header options of all of the six JTAG communication headers to select SBW.	Place jumpers at the six headers to select a JTAG communication mode. Each of these six headers that have a J option and an S option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the J option. To enable SBW, all of the headers must be configured for the S option.
SCL (Not isolated, do not probe)	1-pin jumper header	I^2C/EEPROM SCL probe point (WARNING)	Probe here to probe the I^2C SCL line.	Probe only when AC mains is isolated.
SDA (Not isolated, do not probe)	1-pin jumper header	I^2C/EEPROM SDA probe point (WARNING)	Probe here to probe the I^2C SDA line.	Probe only when AC mains is isolated.
TX_EN	Jumper header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	–

5 Getting Started Firmware

The source code is developed in the IAR™ environment using the IAR Embedded Workbench® Integrated Development Environment (IDE) version 6.30.1 for the MSP430 IDE and version 7.2.0.3640 for IAR common components. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the IDE may prompt the user to create a backup. Click “YES” to proceed. The energy metrology software has four main parts:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for the host-processor functionality of the meter (that is communication, LCD display, RTC setup, and so forth)
- The GUI that is used for calibration

Figure 20 shows the contents of the source folder.

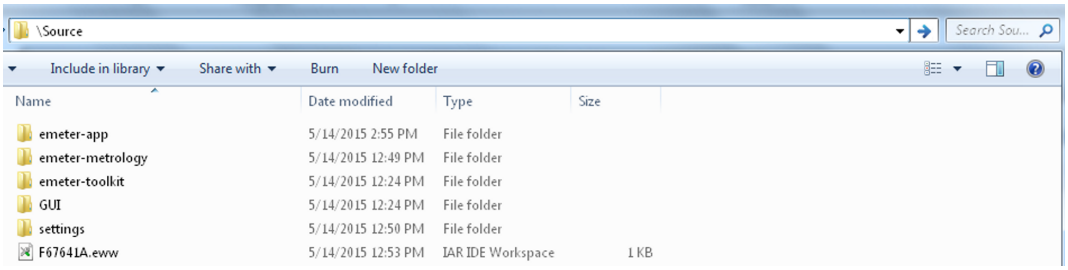


Figure 20. Source Folder Structure

Within the *emeter-app-67641A* folder in the *emeter-app* folder, the *emeter-app-67641A.ewp* project corresponds to the application code. Similarly, within the *emeter-metrology-67641A* folder in the *emeter-metrology* folder, the *emeter-metrology-67641A.ewp* project corresponds to the portion of the code for metrology. Additionally, the folder *emeter-toolkit-67641* within the emeter-toolkit has the corresponding toolkit project file *emeter-toolkit-67641A.ewp*. For first-time use, TI recommends to rebuild all three projects by performing the following steps:

- Open the IAR IDE.
- Open the F67641A workspace, which is located in the *Source* folder.
- Within IARs workspace window, click the *Overview* tab to have a list view of all the projects.
- Right-click the *emeter-toolkit-67641A* option in the workspace window and select *Rebuild All*, as Figure 21 shows.
- Right-click the e*meter-metrology-67641A* option in the workspace window and select *Rebuild All*, as Figure 22 shows.
- Within IARs workspace window, click the *emeter-app-67641A* tab.
- Within the workspace window, select *emeter-app-67641A*, click *Rebuild All* as Figure 23 shows, and then download this project onto the MSP430F67641A device.

Please note that if any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

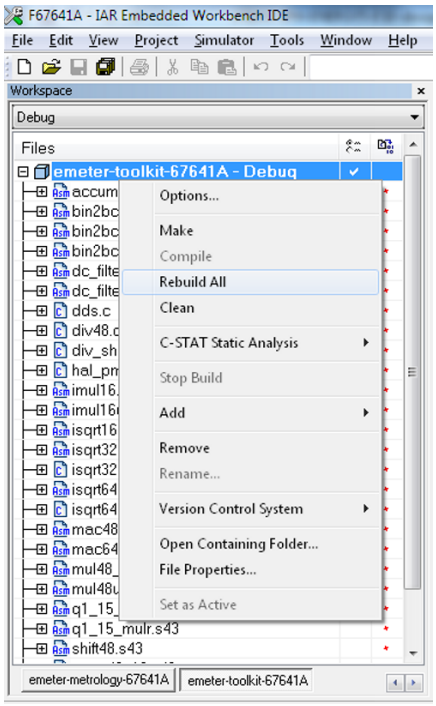


Figure 21. Toolkit Project Compilation

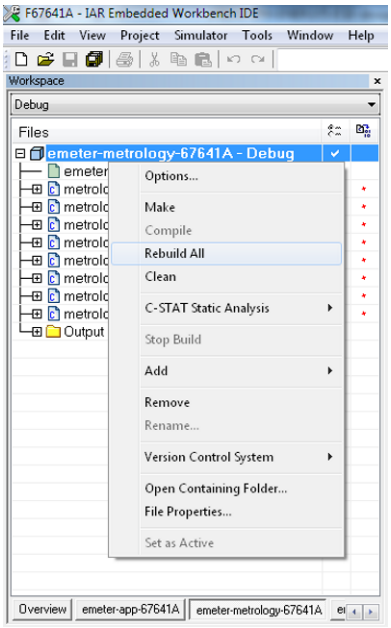


Figure 22. Metrology Project Compilation

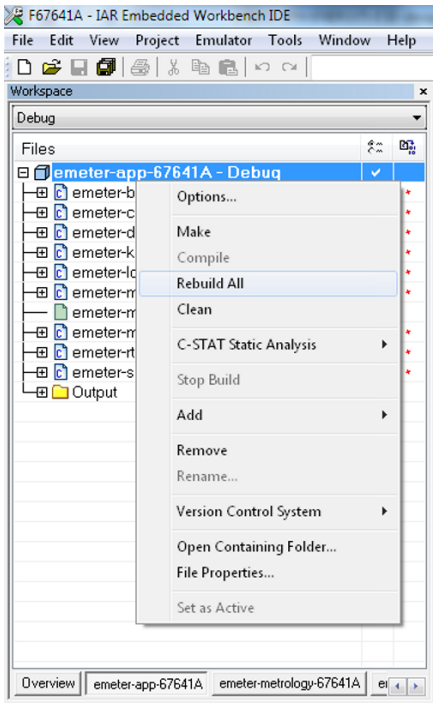


Figure 23. Application Project Compilation

6 Test Setup

6.1 Metrology Test Setup

For performing metrology testing, a source generator was used to provide the voltages and currents to the meter at the proper locations (see Section 4.1). The design tests used a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz. In the tests, current is varied from 50 mA to 100 A. For each current, a phase shift of 0°, 60°, and −60° is applied between the voltage and current.

When voltage and current are applied to the meter, the meter outputs active energy pulses at a rate of 1600 pulses/kWh. This pulse output feeds into a reference meter that determines the active energy % error (for the equipment used in this test, the reference meter was integrated in the same equipment used for the source generator). The active energy % error is based on the actual energy provided to the meter and the measured energy as determined by the active energy output pulse of the meter. Based on this energy pulse measurement, a plot of active energy % error versus current is created for 0°, 60, and −60° phase shifts, as Section 8.2 shows.

6.2 ESD Test Setup

When performing ESD testing, both a MSP430F67641-based meter and MSP430F67641A-based meter were tested to show the ESD improvements of the MSP430F67641A device. Both meters use the same board (EVM430-F67641). The only differences between the meters would be whether a MSP430F67641 or MSP430F67641A device was actually populated on the boards. Although this test shows the comparative behavior of the MSP430F67641 against the MSP430F67641A, please note that the ESD testing for e-meters is a system-level test. Therefore, improvements from selecting the MSP430F67641A varies based on layout and overall system design. Adhering to good ESD layout guidelines allows for maximum ESD immunity. The presence of the MSP430F67641A SoC cannot compensate for significant design weaknesses because the ESD testing is performed on a system level.

Each meter was tested by applying discharges on the coupling plane, as Figure 24 shows. For each test point, ten strikes were applied. The tested ESD voltages were 2 kV to 20 kV in 2-kV increments, with both positive and negative polarities. These voltages were applied from four different orientations with respect to the ESD gun, as Figure 25, Figure 26, Figure 27, and Figure 28 show.

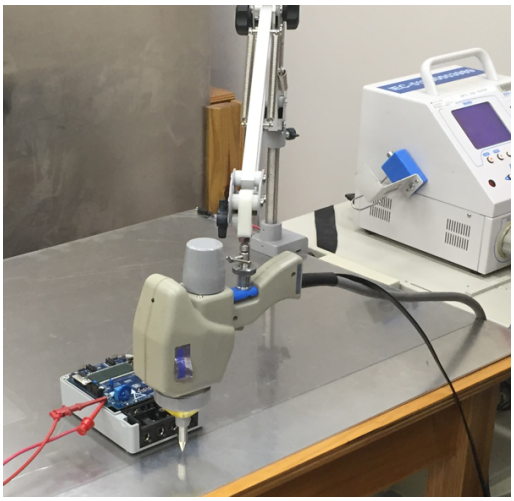


Figure 24. ESD Test Setup

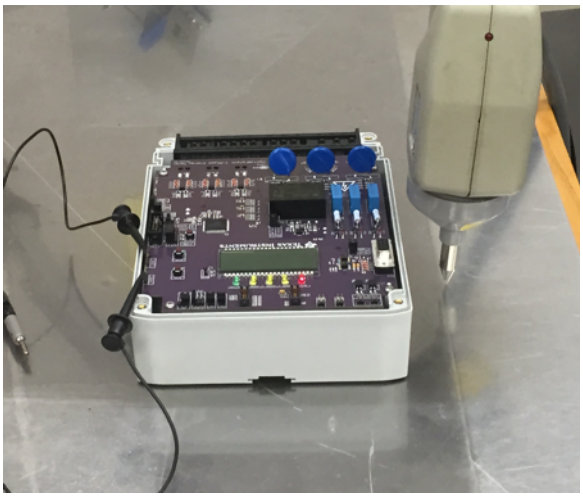


Figure 25. Left Orientation of E-Meter

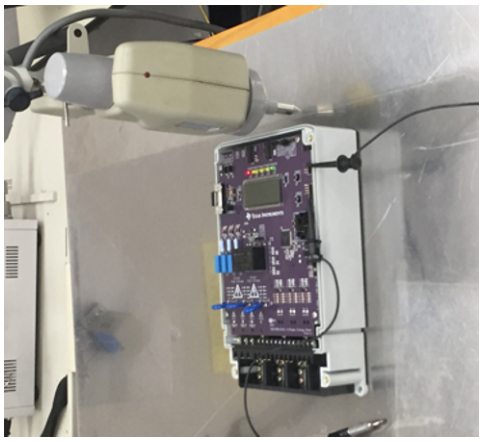


Figure 26. Top Orientation of E-Meter

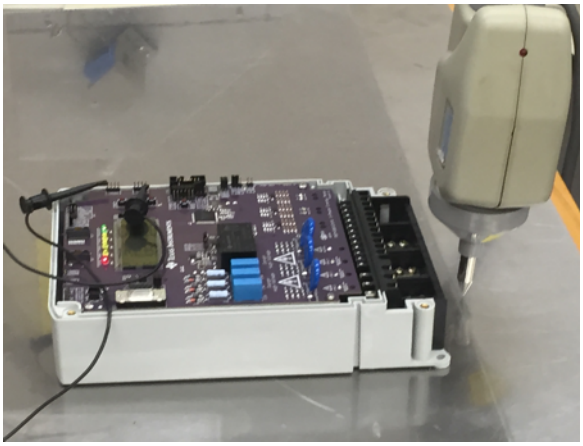


Figure 27. Bottom Orientation of E-Meter

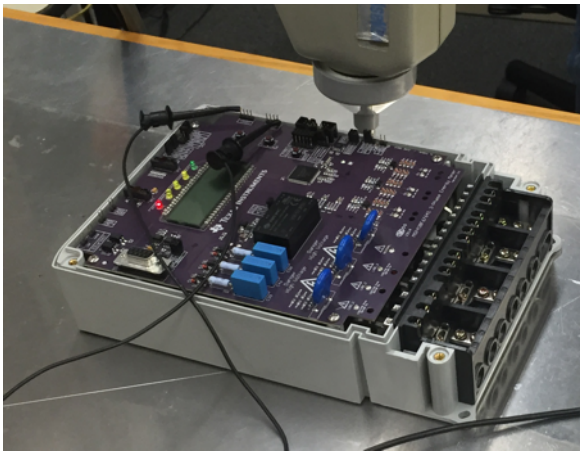


Figure 28. Right Orientation of E-Meter

To easily diagnose the state of the MSP430F67641A device when performing ESD testing, the EVM was loaded with software performing the functions that Section 3.4 lists. Using the software, the state of the MSP430F67641A can be determined by observing the LEDs of the EVM. In addition, the currents drawn by the microcontrollers were monitored to determine between latch-up or lock-up conditions.

Section 8 shows the results of these ESD tests.

7 Viewing Metrology Readings and Calibration

The values of the metrology parameters can be viewed on the LCD or the GUI. In addition, the active power reading can be viewed from an in-home display that communicates with the meter through ZigBee communication.

7.1 Viewing Results Through LCD

The LCD scrolls between metering parameters approximately every two seconds. For each metering parameter that shows on the LCD, three items usually display on the screen: a symbol used to denote the phase of the parameter, text to denote the parameter that is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. Figure 29, Figure 30, and Figure 31 show the mapping between the different orientations of the triangle and the phase descriptor:

Figure 29. Symbol for Phase A

Figure 30. Symbol for Phase B

Figure 31. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. Table 2 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The “DESIGNATION” column shows which characters correspond to which metering parameter.

Table 2. Displayed Parameters

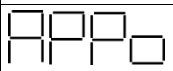
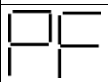
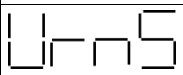
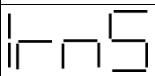
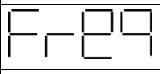
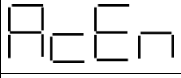
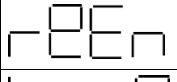
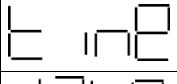
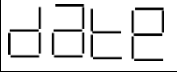
PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power		Watt (W)	This parameter displays for each phase. The aggregate active power is also displayed.
Reactive power		Volt-Ampere Reactive (var)	This parameter displays for each phase. The aggregate reactive power is also displayed.
Apparent power		Volt-Ampere (VA)	This parameter displays for each phase.
Power factor		Constant between 0 and 1	This parameter displays for each phase.
Voltage		Volts (V)	This parameter displays for each phase.
Current		Amps (A)	This parameter displays for each phase.
Frequency		Hertz (Hz)	This parameter displays for each phase.
Total consumed active energy		kWh	This parameter displays for each phase.
Total consumed reactive energy		kVarh	This parameter displays when the sequence of aggregate readings are displayed. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time		Hour:minute:second	This parameter displays when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date		Year:month:day	This parameter displays when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.

Figure 32 shows an example of phase B's measured frequency of 49.99 Hz displayed on the LCD.

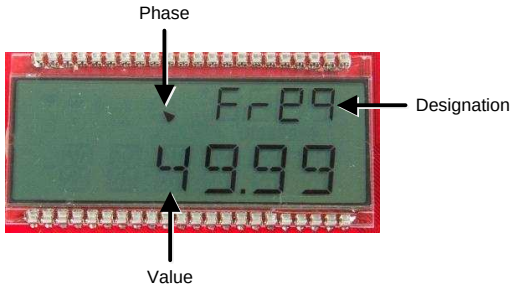


Figure 32. LCD Display

7.2 Viewing Results Using RF Technology (ZigBee)

The CC2530 evaluation module (EM) is an add-on and plug-in daughter card for ZigBee and IEEE 802.15.4 RF applications in the 2.4-GHz, unlicensed industrial, scientific, and medical (ISM) band. The communication interface to any host or application processor is through UART. The instantaneous power consumption sends periodically to the ZigBee module for wireless transmission.

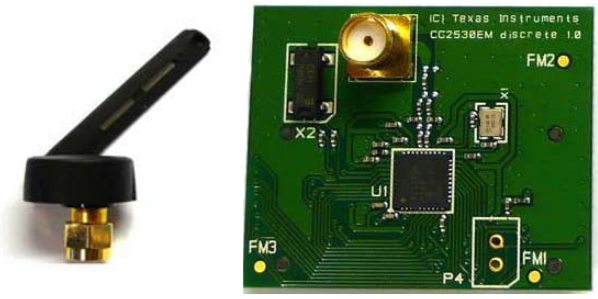


Figure 33. ZigBee Radio

This ZigBee module connects through the UART, which is configured to 115.2 kbaud on the transmit portion of the MSP430F67641A device and the receive portion of the MSP430F4618 device (IHD430).

7.2.1 In-Home Display

Most IHDs have their own setup mechanism and all of them tend to join the ZigBee network when turned ON. This section describes the in-home display using TI's IHD430 (TIDM-LOWEND-IHD), which Figure 34 shows. The IHD430 has an MSP430F461x device as an application or host processor.

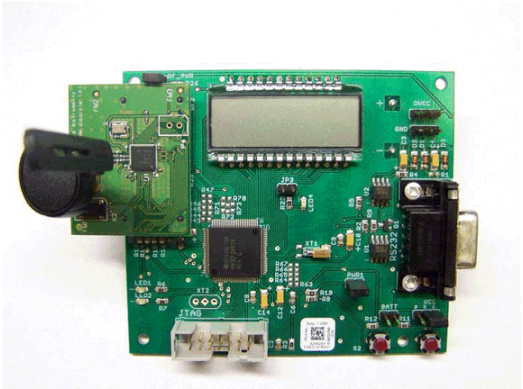


Figure 34. TIDM-LOWEND-IHD

Viewing active power readings on the IHD430

Place a CC2530 module in the RF connector socket of the meter EVM430-F67641, making sure that the module is properly oriented. This CC2530 is flashed with code to act as a transmitter. The IHD430 also has a corresponding CC2530 module that has been flashed to act as a receiver. Please note that the CC2530 cannot be powered from the cap drop supply; therefore, the entire EVM must be powered from an external power supply, as Section 4.2 mentions.

Initializing the IHD430

Power must be provided by two AAA batteries or an external supply. The power source is selected by configuring jumpers on the VCC and BATT headers and the power is supplied to the on-board MSP430 by placing a jumper on the PWR1 header. The power setup options are provided in the following list.

1. Jumper settings to provide battery power are:
   (a) Place jumper on BATT header
   (b) Place jumper on PWR1 header
2. Jumper settings to provide flash emulation tool power are:
   (a) Place jumper on pins [1-2] on VCC 3-pin header
   (b) Place jumper on PWR1 header
3. Jumper settings to provide external power are:
   (a) Place jumper on pins [2-3] on VCC 3-pin header
   (b) Place jumper on PWR1 header
4. Ensure jumper is placed on RF_PWR header, which has been provided to enable and disable power to CC2530

The “IHD430_SUPPORT” macro must be defined in the *emeter-1ph-neutral-67641(A)_shunt.h* file for the MSP430F67641A software to communicate the active power to the IHD430. When this macro is enabled, the active power reading sends to the on-board CC2530 transmitter through 8N1 UART communication at a baud rate of 115.2 kbaud. The CC2530 then sends the data to the CC2530 receiver. The IHD430 receives the active power readings and displays it on the LCD. Please note that the transmitter (meter) must be turned ON before the receiver to ensure proper ZigBee communication. In addition, modifications can be made to the MSP430F67641A software to send different parameters for display onto the IHD430.

7.3 Calibrating and Viewing Results Through PC

7.3.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As Figure 35 shows, this field is changed to *COM7*.

```
260        </correction>
261      </phase>
262      <temperature/>
263      <rtc/>
264    </cal-defaults>
265    <meter position="1">
266      <port name="com7" speed="9600"/>
267    </meter>
268    <reference-meter>
269      <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270      <type id="chroma-66202"/>
271      <log requests="on" responses="on"/>
272      <scaling voltage="1.0" current="1.0"/>
273    </reference-meter>
```

Figure 35. GUI Config File Changed to Communicate With Energy Measurement System

4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the EVM, the GUI opens (see Figure 36). If the GUI connects properly to the EVM, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

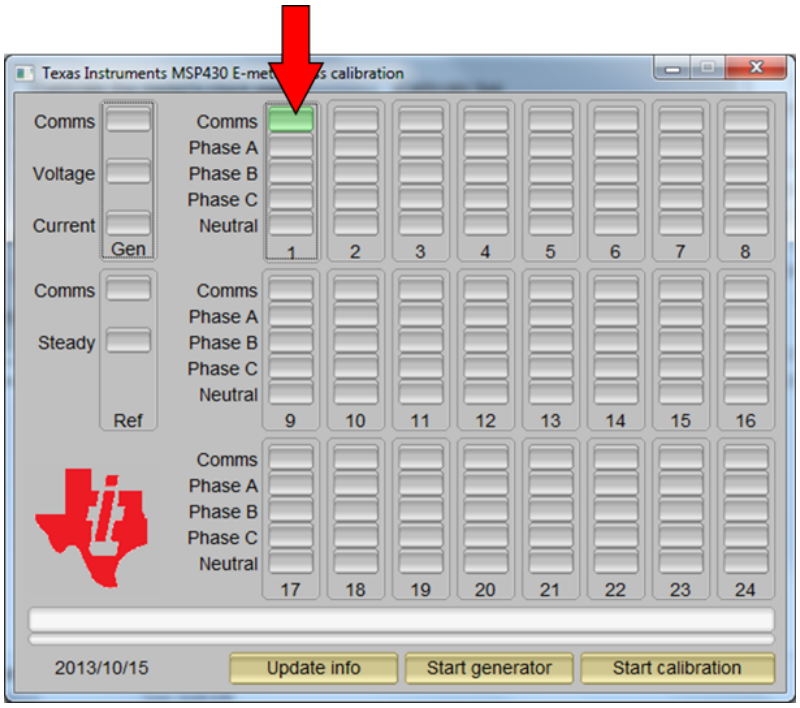


Figure 36. GUI Startup Window

Upon clicking on the green button, the results window opens (see Figure 37). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.

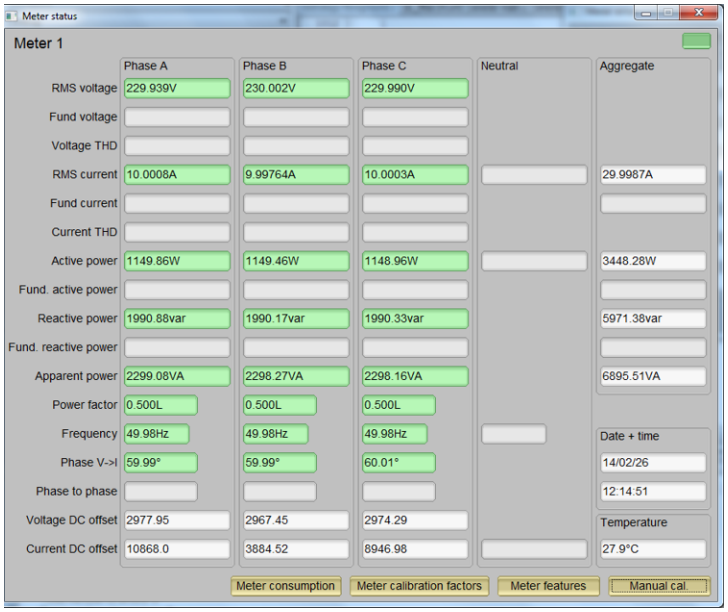


Figure 37. GUI Results Window

From the results window, the total-energy consumption readings and sag/swell logs can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as Figure 38 shows.

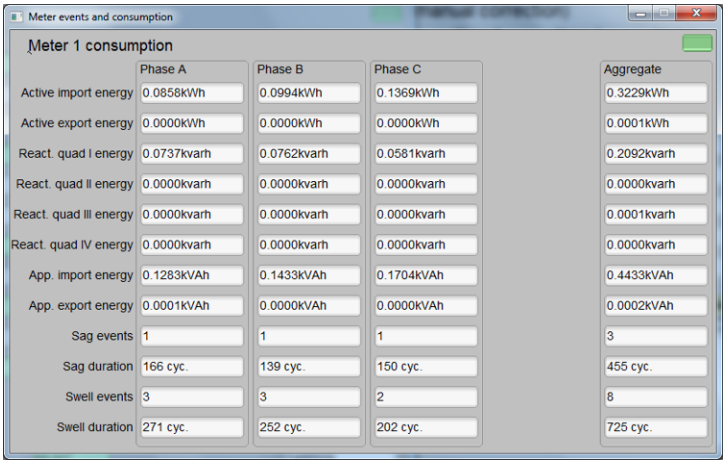


Figure 38. Meter Events and Consumption Window

From this *Meter events and consumption* window, the user can view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

7.3.2 Calibration

Calibration is key to any meter performance and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify these effects, every meter must be calibrated. To perform calibration accurately there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, voltage AC offset, current scaling factor, current AC offset, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Please note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed with the code (available in the **.zip* file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted. However, if the code is re-flashed during debugging, the calibration factors are replaced and the meter has to be recalibrated. One way to save the calibration values is by clicking on the *Meter calibration factors* button (see Figure 37). The *Meter calibration factors* window (see Figure 39) displays the latest values, which can be used to restore calibration values.

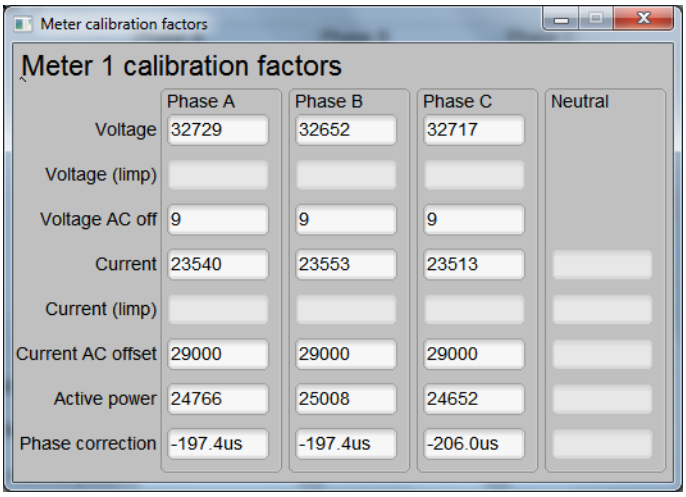


Figure 39. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Section 4.1, and the energy pulses connected to the reference meter.

7.3.2.1 Gain Calibration

Usually gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other two phases must be turned OFF. Typically, switching only the currents OFF is good enough for disabling a phase.

7.3.2.1.1 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 230 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that Figure 37 shows. The following screen pops up from Figure 40:

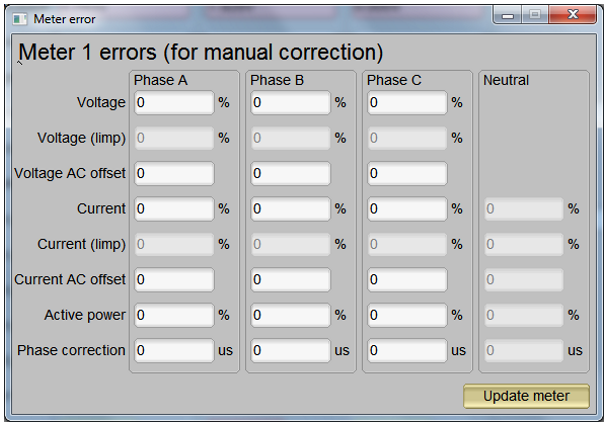


Figure 40. Manual Calibration Window

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (17)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter,
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source.

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage* and *Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

7.3.2.1.2 Active Power Gain Calibration

Note that this example is for one phase. Repeat these steps for other phases.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating using Step 4 with active power readings (displayed on the AC test source) can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction %* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, perform the following steps.

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source
3. Repeat Steps 1 to Steps 3 from the previous Section 7.3.2.1.1 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in the previous Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the *Correction %* value and does not require calculation.
6. Click on *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

7.3.2.2 Phase Correction

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 1−3 from Section 7.3.2.1.1 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If this error from the previous Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   (a) Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error would require a positive (negative) number as correction.
   (b) Click on the *Update meter* button and monitor the error values on the reference meter.

(c) If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on the previous Step 4a and Step 4b. Please note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.

(d) Change the phase now to −60° and check if this error is still acceptable. Ideally, errors should be symmetric for same phase shift on lag and lead conditions.

After performing phase correction, calibration is complete for one phase. Please note that the gain calibration and phase calibration are completed in sequence for each phase before moving on to other phases. These two procedures must be repeated for each phase, unlike voltage and current calibration.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see Figure 41) by clicking the *Meter calibration factors* button of the GUI metering results window in Figure 37.

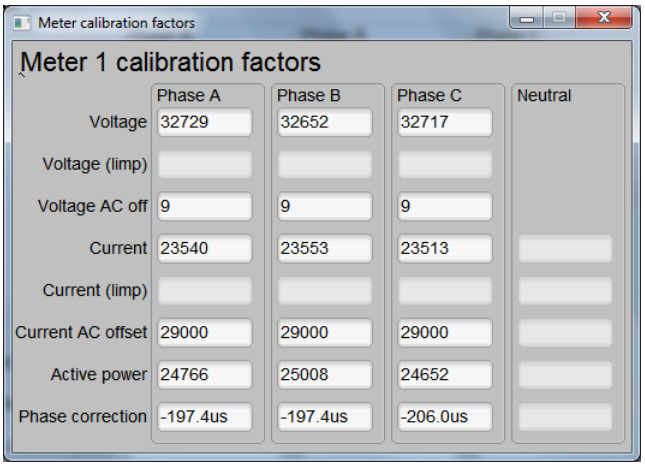


Figure 41. Calibration Factors Window

Also view the configuration of the system by clicking on the *Meter features* button in Figure 37 to get to the window that Figure 42 shows.

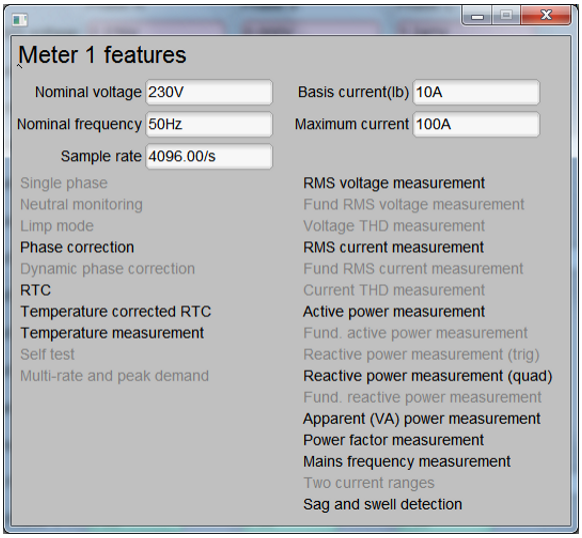


Figure 42. Meter Features Window

8 Test Data

8.1 ESD Results

To test the comparative ESD robustness between the MSP430F67641A and MSP430F67641 devices, an IEC 61000-4-2 test was performed on one EVM430-F67641 that had the MSP430F67641A as the metering SoC and another EVM430-F67641 that had the non-A MSP430F67641 as the metering SoC. Please note that for the EVM430-F67641, some ESD tradeoffs were made to support fully showcasing the features of the silicon and ease of use for evaluation purposes. However, the EVM can serve as a gauge to show the improvements in using the MSP430F67641A devices instead of the MSP430F67641.

For applying the ESD test on the two test EVMs, both positive and negative polarity discharges were applied on both test boards at the same location. In the tests, recoverable failures (for example, a reset), lock-ups, and latch-ups were logged as failures. Table 3, Table 4, Table 5, and Table 6 show the results of these tests. In these tests, voltage levels where both positive and negative polarity tests passed are colored green, tests where only either positive or negative polarity tests passed are colored yellow, and tests where both positive and negative polarity tests failed are colored red. To verify failures in some cases, a second trial of a test was performed, which means a particular test may have two results that correspond to different trials, as was done for the F67641 16-kV positive polarity test for the left orientation.

Table 3. IEC 61000-4-2 Test Results for MSP430F67641 and MSP430F67641A, Left Orientation

TEST VOLTAGE	F67641 RESULTS (+POLARITY/ –POLARITY)	F67641A RESULTS (+POLARITY/ –POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Pass/Pass	Pass/Pass
14	Pass/Fail-Fail	Pass/Pass
16	Fail-Pass/	Pass/Pass
18	Pass/	Pass/Pass
20	Fail-Fail/	Pass/Pass

Table 4. IEC 61000-4-2 Test Results for MSP430F67641 and MSP430F67641A, Right Orientation

TEST VOLTAGE	F67641 RESULTS (+POLARITY/ –POLARITY)	F67641A RESULTS (+POLARITY/ –POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Fail-Pass/Pass	Pass/Pass
14	Fail/Pass	Pass/Pass
16	/Fail-Fail	Pass/Pass
18	/Fail	Pass/Pass
20	/Fail	Pass/Pass

Table 5. IEC 61000-4-2 Test Results for MSP430F67641 and MSP430F67641A, Bottom Orientation

TEST VOLTAGE	F67641 RESULTS (+POLARITY/ –POLARITY)	F67641A RESULTS (+POLARITY/ –POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Pass/Pass	Pass/Pass
12	Pass/Pass	Pass/Pass
14	Pass/Pass	Pass/Pass
16	Fail-Fail/Fail-Fail	Pass/Pass
18		Pass/Pass
20		Pass/Pass

Table 6. EC 61000-4-2 Test Results for MSP430F67641 and MSP430F67641A, Top Orientation

TEST VOLTAGE	F67641 RESULTS (+POLARITY/ –POLARITY)	F67641A RESULTS (+POLARITY/ –POLARITY)
2	Pass/Pass	Pass/Pass
4	Pass/Pass	Pass/Pass
6	Pass/Pass	Pass/Pass
8	Pass/Pass	Pass/Pass
10	Fail-Fail/Fail-Fail	Pass/Pass
12		Pass/Pass
14		Pass/Pass
15 (extra test)		Pass/Pass
16		Fail-Fail/Pass
18		/Fail-Pass
20		/Fail-Pass

From these results, there is a clear improvement in selecting the MSP430F67641A devices over the MSP430F67641. The MSP430F67641A chips pass up to 20 kV in three of the four orientations tested. In the other orientation, there is still a 6- to 8-kV improvement and the board still passes level 4 testing standards. The reduced performance in this orientation is due to the ESD gun being in closer proximity to the LCD and its long LCD traces, which were sensitive to ESD. In this hardware, the LCD lines are not individually decoupled (doing so increases the system-level ESD performance).

8.2 Metrology Result Comparison

Regardless of the improvements made in the MSP430F67641A device, the metrology performance is still comparable to the non-A MSP430F67641. To show this, an EVM430-F67641 was tested with an MSP430F67641 and an MSP430F67641A device. Table 7, Figure 36, and Figure 37 show the results for these tests. The results from this test show that the MSP430F67641A can still meet the class 0.5% accuracy requirements fulfilled by the non-A MSP430F67641 device.

Table 7. Active Energy % Error for MSP430F67641 and MSP430F67641A

	MSP430F67641			MSP430F67641A		
CURRENT (AMPS)	0°	60°	−60°	0°	60°	−60 °
0.05	−0.04	0.005	−0.08	−0.012	−0.018	−0.038
0.1	−0.004	0.043	−0.06	0.003	0.018	−0.02
0.25	−0.003	0.044	−0.055	−0.008	0.01	−0.031
0.5	−0.008	0.051	−0.05	−0.022	0.002	−0.017
1	−0.002	0.053	−0.033	−0.0295	0.0085	−0.016
2	−0.00533	0.071667	−0.053	−0.014	−0.009	−0.024
5	−0.00533	0.018333	−0.02333	−0.0125	−0.01	−0.017
10	0.002	0.008333	0.01	0.0005	−0.013	0.021
20	−0.00967	−0.048	0.029667	0.0005	−0.032	0.039
30	−0.00767	−0.08267	0.065	0.0155	−0.0555	0.0725
40	−0.004	−0.106	0.107667	0.0115	−0.08	0.098
50	−0.00733	−0.14667	0.125	0.002	−0.1	0.112
60	−0.00367	−0.15967	0.14	−0.0015	−0.114	0.134
70	0.000333	−0.16233	0.155667	0.008	−0.109	0.142
80	−0.00133	−0.17033	0.161333	0.01	−0.159	0.134
90	0.001333	−0.17367	0.179333	0.008	−0.1615	0.177
100	−0.00033	−0.17067	0.172	0.011	−0.1755	0.184

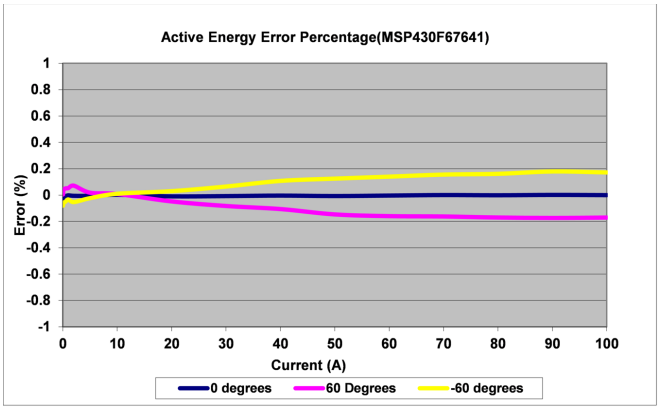


Figure 43. EVM430-F67641 Performance With MSP430F67641

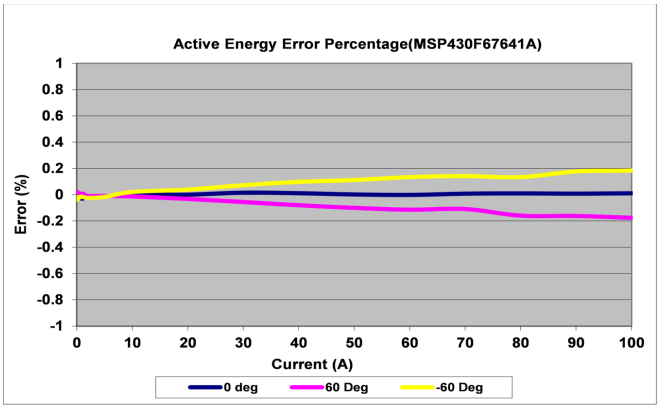


Figure 44. EVM430-F67641 Performance With MSP430F67641A

9 Design Files

9.1 Schematics

To download the schematics for each board, see the design files at TIDM-3PH-ENERGY5-ESD.

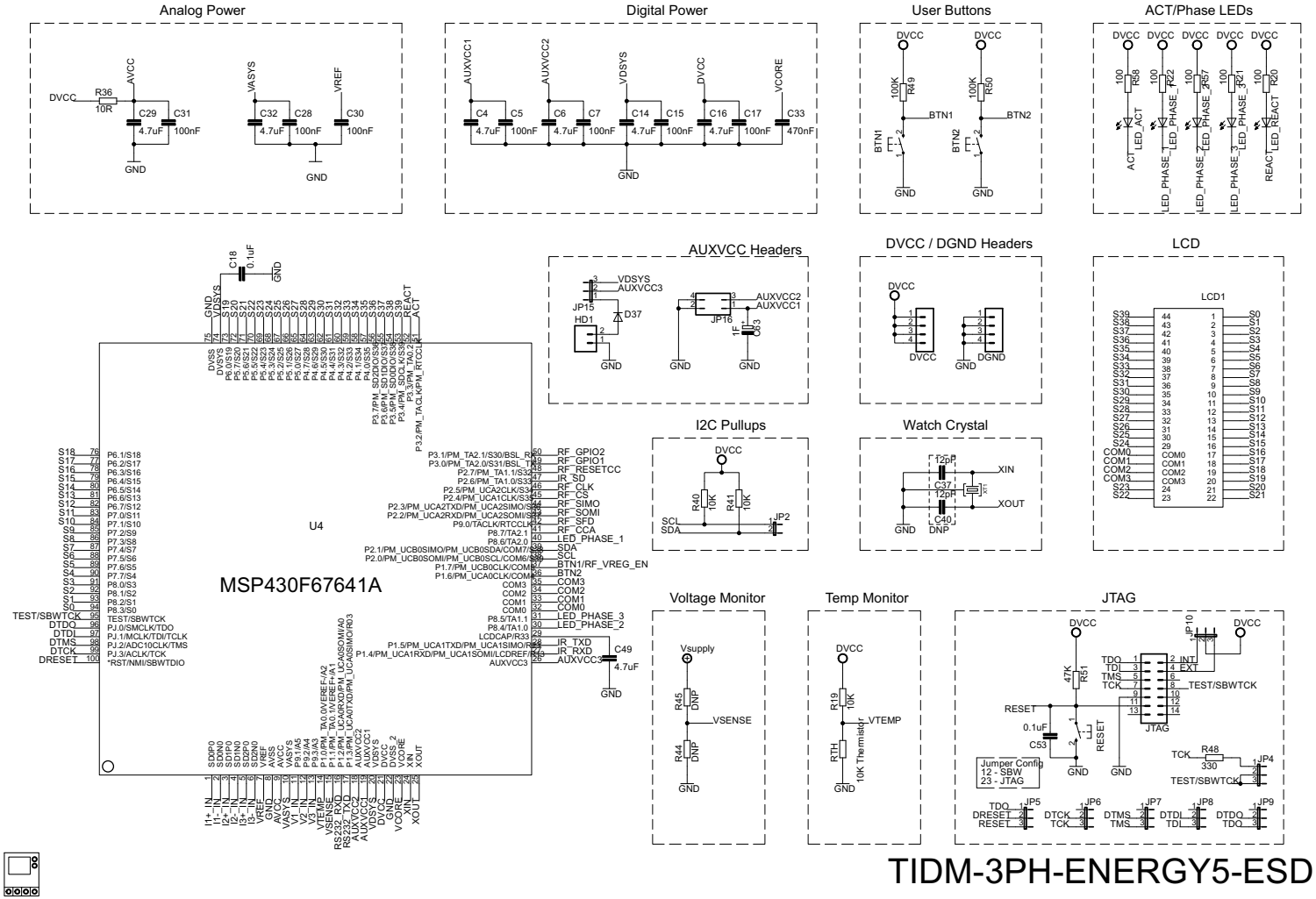


Figure 45. TIDM-3PH-ENERGY5-ESD Schematic Page 1

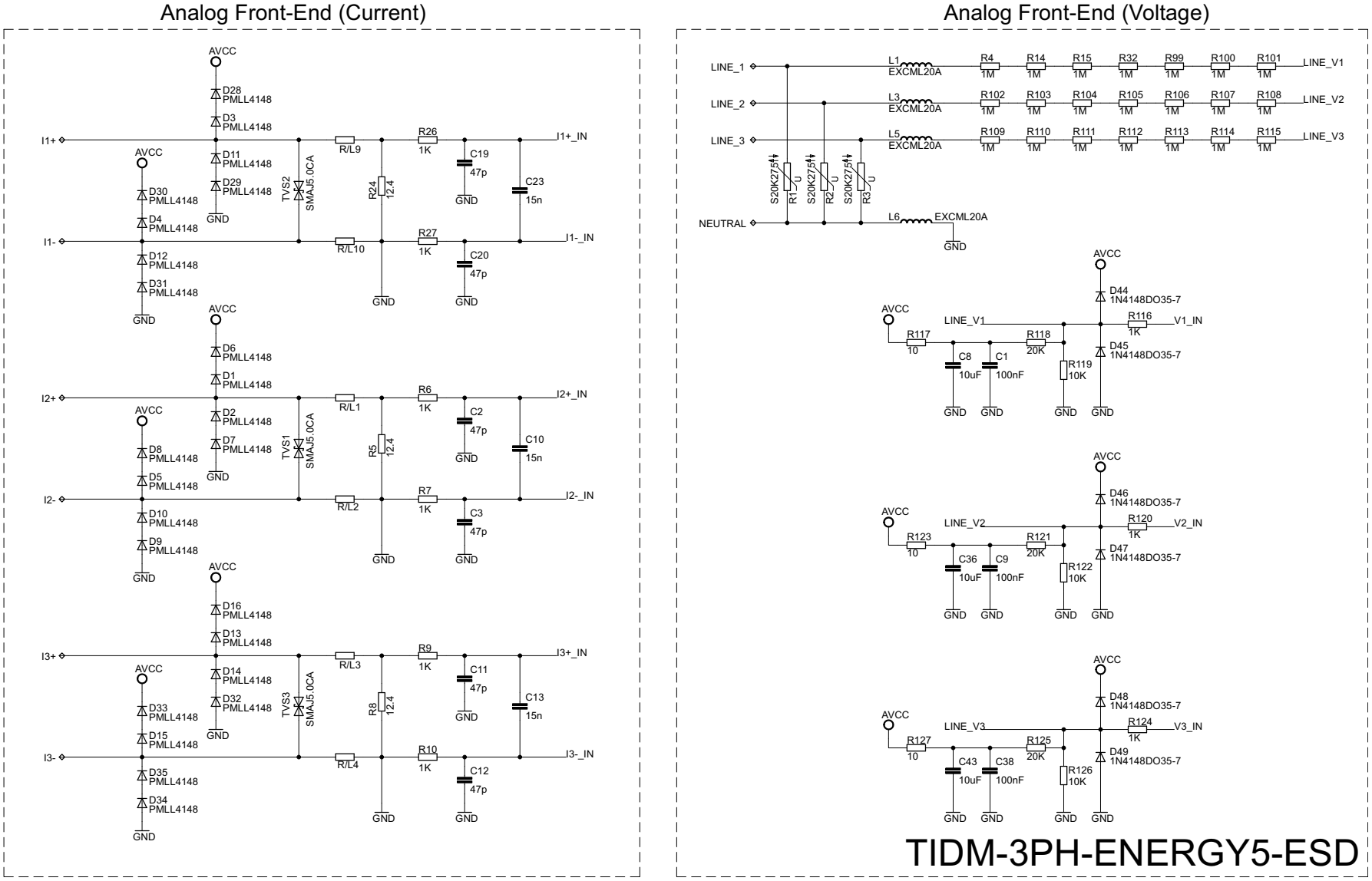


Figure 46. TIDM-3PH-ENERGY5-ESD Schematic Page 2

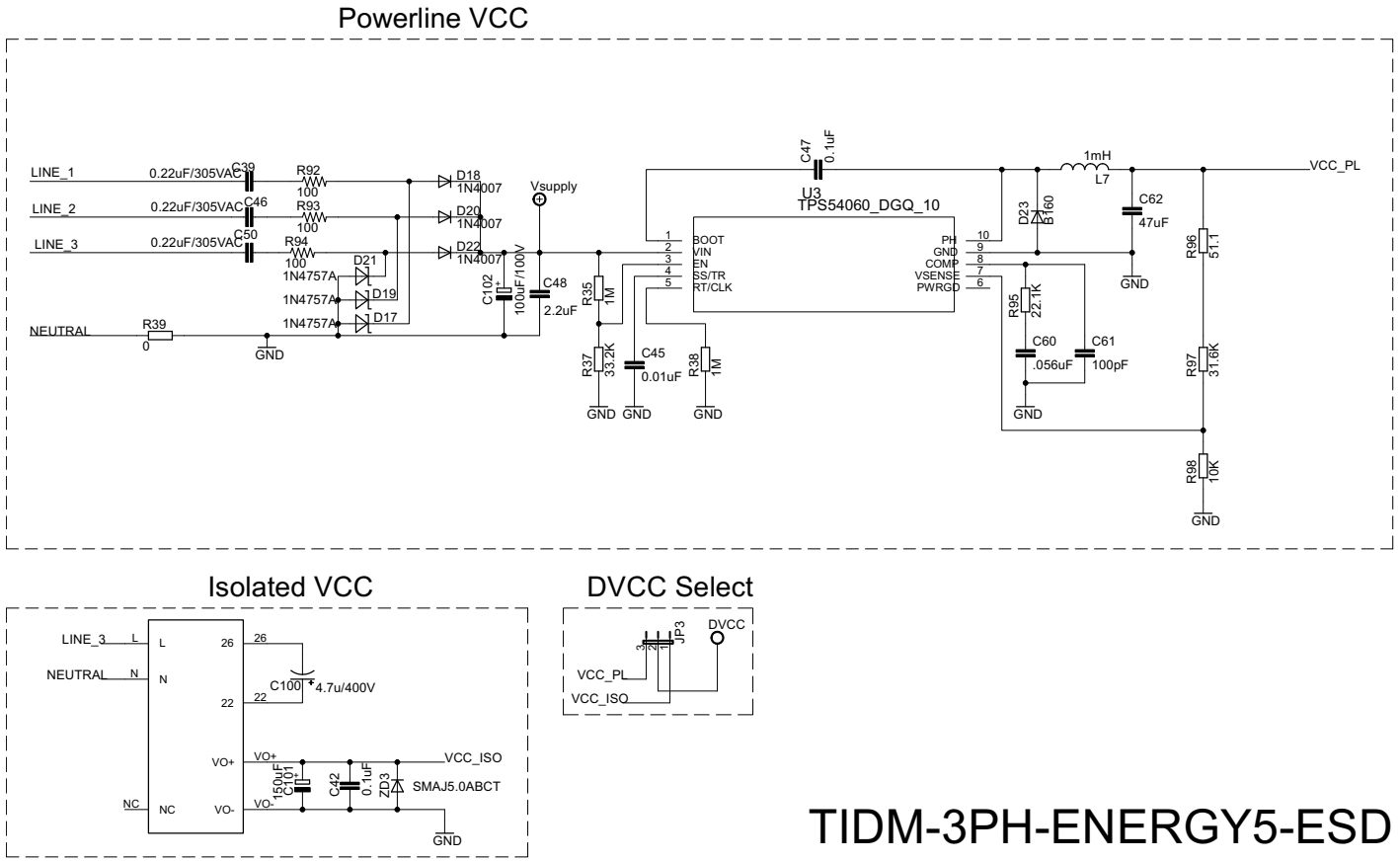
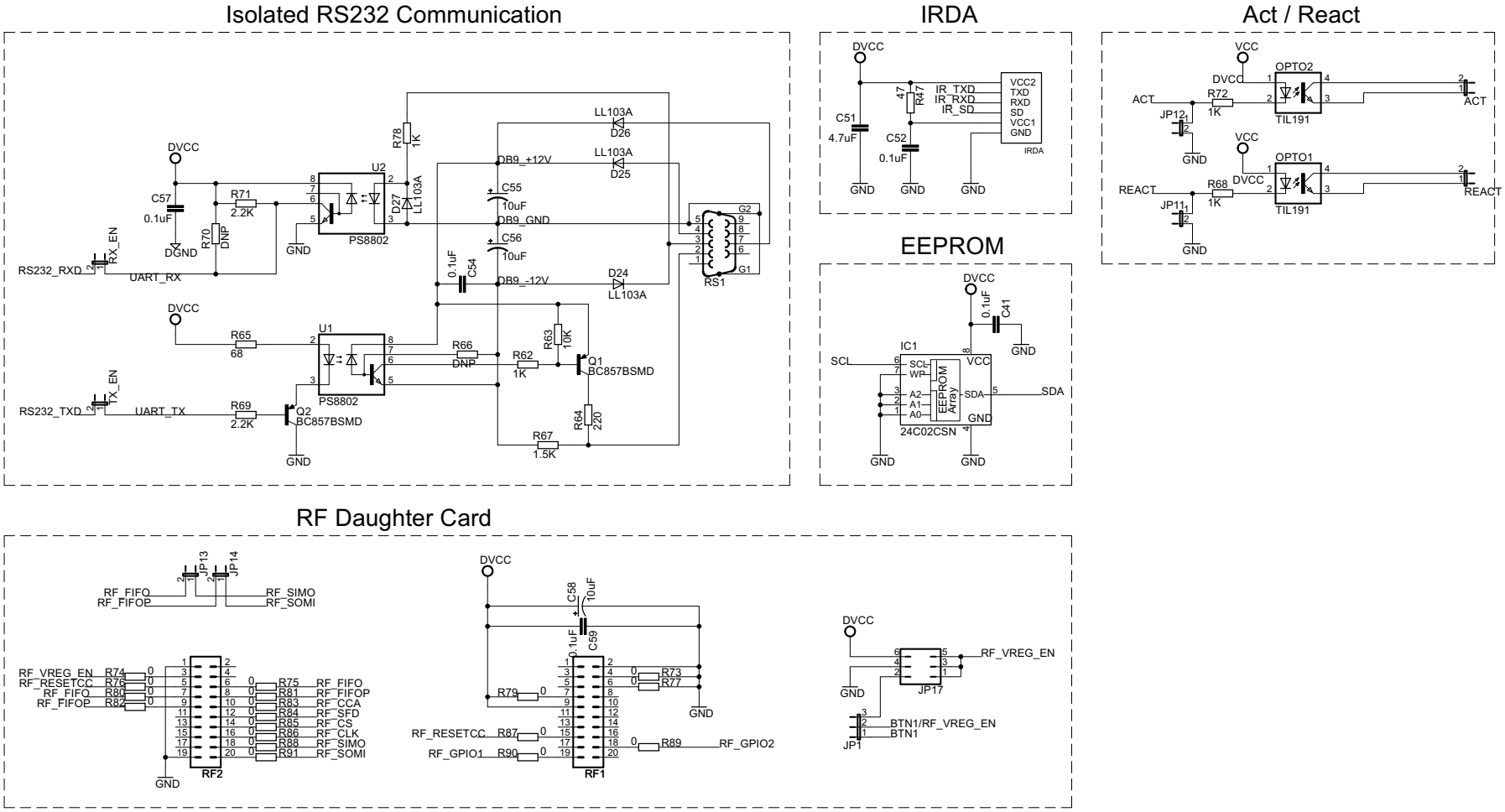


Figure 47. TIDM-3PH-ENERGY5-ESD Schematic Page 3



TIDM-3PH-ENERGY5-ESD

Figure 48. TIDM-3PH-ENERGY5-ESD Schematic Page 4

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-3PH-ENERGY5-ESD.

9.3 PCB Layout Recommendations

PCB layout is an important factor in a meter's ESD immunity performance. The EVM430-F67641 in particular was designed to make it easy to evaluate the MSP430F67641 as an e-meter SoC. As a result, in certain instances, ESD performance was traded off for ease of evaluation of the EVM. However, here are some general PCB layout guidelines for ESD performance:

- Use ground planes instead of ground traces where possible and minimize the cuts in these ground planes (especially for critical traces) in the direction of current flow. Ground planes provide a low-impedance ground path, which minimizes induced ground noise.; however, cuts in the ground plane can increase inductance. If there are cuts in the ground plane, they should be bridged on the opposite side with a 0-Ω resistor.
- When there is a ground plane on both the top and bottom layers of a board (such as in this EVM430-F67641) ensure there is good stitching between these planes through the liberal use of vias that connect the two planes.
- Keep traces short and wide to reduce trace inductance. If an LCD is used, place it near the microcontroller and prevent long LCD traces to the microcontroller.
- Use wide VCC traces and star-routing for these traces instead of point-to-point routing.
- Minimize the length of the microcontroller's reset trace and other critical edge-triggered traces.
- Isolate sensitive circuitry from noisy circuitry. For example, high voltage and low voltage circuitry must be separated.
- Use transient voltage suppressors, EMI suppressant ferrite beads, and other ESD protection devices to suppress the effects from an ESD discharge. The turn on time of these devices should be small since the rise time of ESD discharge waveform is also small. View further information on ESD protection devices at the following link: www.ti.com/esd.
- Keep sensitive circuitry away from PCB edges. If a ground plane is present, put sensitive circuitry near the center of these ground planes.
- Use decoupling capacitors with low effective series resistance (ESR) and effective series inductance. Place decoupling capacitors close to their associated pins.
- Place connectors all on one edge of the PCB, especially through-hole connectors because they cause breaks in the ground plane.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there should be clean ground underneath the crystal and placing any traces underneath the crystal should be prevented. Also, keep high frequency signals away from the crystal.

Please refer to SLAA530 for more ESD recommendations.

9.4 Layer Plots

To download the layer plots, see the design files at TIDM-3PH-ENERGY5-ESD.

9.5 CAD Project

To download the CAD project files, see the design files at TIDM-3PH-ENERGY5-ESD.

9.6 Gerber Files

To download the Gerber files, see the design files at TIDM-3PH-ENERGY5-ESD

10 Software Files

To download the software files, see the design files at TIDM-3PH-ENERGY5-ESD

11 References

1. International Electrotechnical Commission, *IEC 61000-4-2 – Electromagnetic capability (EMC) Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*, Ed. 2.0
2. Texas Instruments, *Segment LCD-Based Low-End In-Home Display with Wireless RF Communication*, User's Guide (TIDU203)

12 About the Author

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