TI Designs

24-V DC, 100-W/30-W Dual Sensorless Brushless DC Motor Drive Reference Design

TI Designs

The TIDA-0447 is a 24-V, dual brushless motor drive platform to be used in dishwashers to drive the water circulation pump and drain pump. The drive stage for circulation pump is designed for 100-W continuous operation, and the drain pump drive stage is designed for 30-W continuous operation. The design is tested for full load operation, overcurrent, and motor stall protection.

Design Resources

TIDA-00447	Design Folder
MSP430G2744	Product Folder
CSD88539ND	Product Folder
DRV8303	Product Folder
DRV10983	Product Folder
TPD4S009	Product Folder
LMT84	Product Folder
TLV803S	Product Folder
CSD17304Q3	Product Folder
ISO7421D	Product Folder

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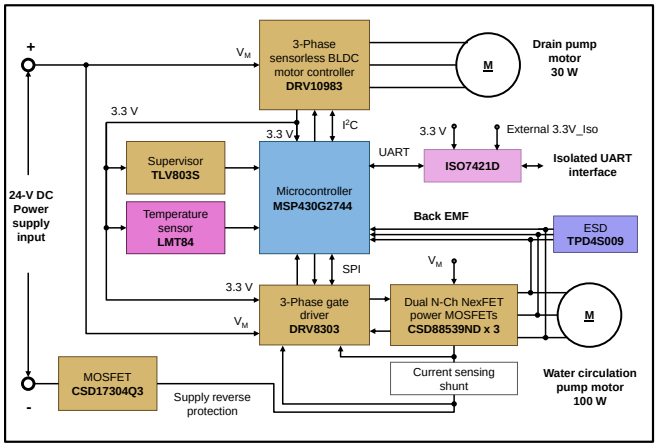
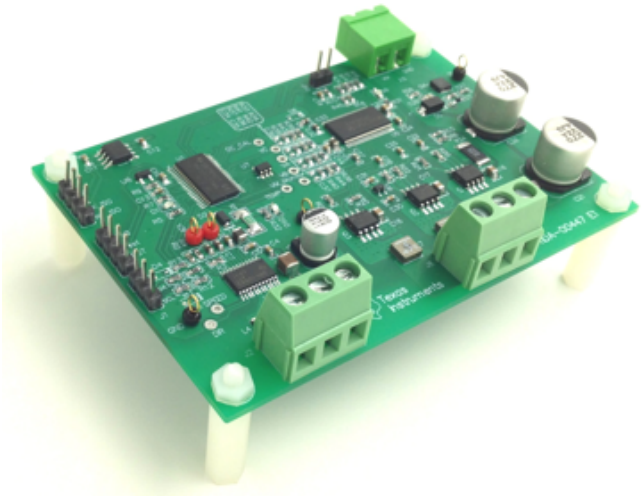
Design Features

- Enables Safer, Noiseless Operation and Small Form Factor
- Circulation Pump Drive Designed for up to 100-W Continuous Operation Using Discrete Approach Having an MCU, External MOSFET Driver With Built-in Protections and Current Sensing Amplifier, and External Power MOSFETs
- MCU Software Implements InstaSPIN-BLDC, Sensorless Trapezoidal Control of BLDC Motor Using Back-EMF (BEMF) Integration Method Offering Robust Low Speed Operation, and Finer Control Over Entire Speed Range
- Drain Pump Designed for up to 30-W Continuous Operation Based on a Single-Chip, 3-Phase Motor Driver With Integrated Power MOSFETs
  - Offers Proprietary Sensorless Control Scheme to Provide Continuous Sinusoidal Drive
  - Integrates 5-V/3.3-V Buck/Linear Converter and Protection Functions Such as Overcurrent, Voltage Surge Protection, UVLO Protection, and Motor Lock Detection
- Designed to Operate at Ambient Temperatures of –20°C to 55°C

Featured Applications

- Dishwashers
- Appliances With 24-V DC Pumps or Fans





1 Introduction

In modern dishwasher applications, there are two mandatory pump units used in the system: the circulation pump and the drain pump. The circulation pump is used for circulating the clean water while the drain pump drains out the waste water. Today, most dishwashers use high-voltage BLDC motors for these pumps due to their efficient operation and low audible noise performance.

This design is an alternative solution proposing the use of low-voltage (24 V) BLDC motors instead of high-voltage (above 300 V) motors.

The benefits of using low-voltage motors for power levels less than or equal to 100 W:

- Low-voltage motor driver ICs typically offer higher level of integration:
  - Low R_{DSON} Power MOSFETs + MOSFET drivers
  - Current sense amplifier, programmable current regulation, overcurrent protection, over temperature protection, auto restart, and so on
  -
- Reduced and easier routing efforts; low voltage reduces spacing requirements
- Cost reduction for manufacturing of *low-voltage low power motors* compared to *high-voltage low-power motors*
- Same motor and hard drive PCB can be used for 110-V or 220-V line voltage-based products as well as solar powered systems
- Reduced cost on bulk capacitor (low voltage versus 450 V)
- Overall reduced system level isolation requirements

The objective of this reference design is to provide a dual pump control unit. This design demonstrates the control unit in a small form factor (94 × 65 mm) operating from 24-V DC input (from output of the TIDA-00367) and delivers up to 130-W continuous power output to motor. The design also provides scalability for higher and lower current levels.

2 Key System Specifications

Table 1. Key System Specifications of Driver Unit—Circulation Pump

PARAMETER	SPECIFICATIONS
Input voltage	24-V DC (30 V max)
Current	4.5 A continuous (28 V max)
Power level	Thermal design for 100-W continuous operation
Control	120° trapezoidal with sensorless BEMF integration technique implemented in MSP430™
Speed range	2400 RPM max
Protection circuits	Overcurrent, lock detection, voltage surge protection, UVLO protection, thermal shutdown protection
Operating ambient	–10°C to 55°C
Cooling	Thermal pad MOSFETs with SON package and PCB layout for thermal management

Table 2. Key System Specifications of Driver Unit—Drain Pump

PARAMETER	SPECIFICATIONS
Input voltage	24-V DC (28 V max)
Current	1.5 A continuous
Power level	Thermal design for 30-W continuous operation
Control	Single chip, sensorless, completely integrated 180° sinusoidal control with power drive
Speed range	2400 RPM max
Protection circuits	Overcurrent, lock detection, voltage surge protection, UVLO protection, thermal shutdown protection
Operating ambient	–10°C to 55°C
Cooling	Thermally-enhanced 24-pin HTSSOP with PCB layout for thermal management

3 System Description

New generations of home appliances are targeting higher performance parameters such as better efficiency and lower acoustics. Brushless DC (BLDC) motors can achieve these requirements. This TI Design has two individual motor drive stages to drive BLDC motors. This feature can be used in home appliances to drive brushless motor-based water pumps in appliances like dishwashers.

The 100-W drive implementation enables the simplest 120-degree trapezoidal control of a BLDC motor. This implementation uses an MCU to run the InstaSPIN™ BEMF integration method software for BLDC motor commutation and features a rich three-phase MOSFET bridge driver and external MOSFETs. This implementation enables easy scaling up or down the power stage with minimal effort. This drive stage can be used for driving the water circulation pump in a dishwasher.

The 30-W drive is implemented using a totally integrated single-chip motor controller that can drive a sinusoidal BEMF motor or permanent magnet synchronous motor (PMSM) with a 180-degree continuous sine wave. This drive stage can be used for driving the drain pump in a dishwasher as it is a low power motor.

3.1 Brushless Permanent Magnet Motors

Permanent magnet synchronous motors can be classified based on BEMF profiles: the BLDC motor and the permanent magnet synchronous motor (PMSM). Both BLDC motors and PMSMs have permanent magnets on the rotor, but differ in the flux distributions and BEMF profiles. In a BLDC motor, the BEMF induced in the stator is trapezoidal, and in a PMSM the BEMF induced in the stator is sinusoidal. To obtain the maximum performance from each type of motor, an appropriate control strategy has to be implemented.

Table 3 shows the comparison between a BLDC motor and a PMSM.

Table 3. Comparison of BLDC Motors and PMSMs

BLDC	PMSM
Synchronous machine	Synchronous machine
Fed with direct currents	Fed with sinusoidal currents
Trapezoidal BEMF	Sinusoidal BEMF
Stator flux position commutation each 60 degrees	Continuous stator flux position variation
Only two phases ON at the same time	Possible to have three phases ON at the same time
Torque ripple at commutations	No torque ripple at commutations
Low order current harmonics in the audible range	Less harmonics due to sinusoidal excitation
Higher core losses due to harmonic content	Lower core loss
Less switching losses	Higher switching losses at the same switching frequency
Control algorithms are relatively simple	Control algorithms are mathematically intensive

3.1.1 BLDC Motor —Trapezoidal Control

The BLDC motor, or the trapezoidal BEMF motor, has the ampere conductor distribution of the stator ideally remains constant and fixed in space for a fixed interval known as the commutation interval. For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motor uses a two-phase ON control, where two phases of the motor will be energized at a time and the third winding will be open. There should be no torque production in the region of the BEMF zero crossings. The principle of the BLDC motor is, at all times, to energize the phase pair, which can produce the highest torque. The combination of a DC current with a trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase; as a consequence, the torque ripple is present at each 60° phase commutation. Figure 1 describes the electrical wave forms in the BLDC motor in the two-phase ON operation.

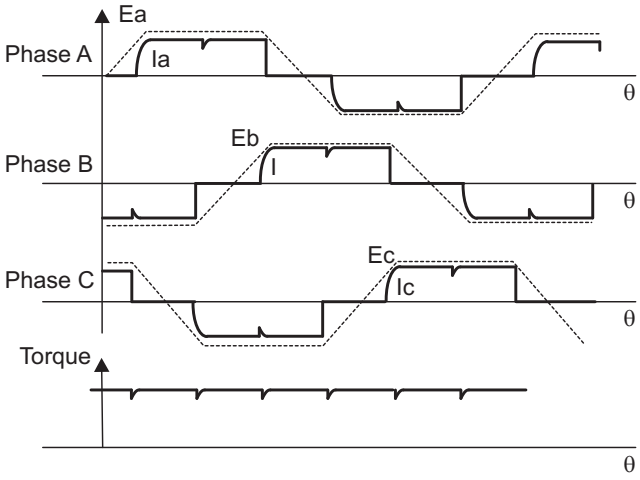


Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

Trapezoidal control has the following advantages:

- Only one current at a time needs to be controlled.
- Only one current sensor is necessary (or none in case of speed loop only).
- The positioning of the current sensor allows the use of low cost sensors as a shunt.

For more details about trapezoidal control, refer the application report SPRABQ7 on TI Web.

3.1.2 BLDC Motor —180° Sensorless Control

By continuously measuring the motor phase current and periodically measuring the supply voltage to the motor, one can achieve commutation control algorithm that provides continuous sinusoidal output voltages to the motor phases to enable ultra-quiet motor operation by keeping the electrically induced torque ripple small.

The DRV10983 implements the above mentioned control scheme with integrated power MOSFETs, which provide drive current capability up to 2 A continuous. The device is specifically designed for low noise, low external component count, 12- to 24-V motor drive applications. The device is configurable through a simple I^2C interface to accommodate different motor parameters and spin-up profiles for different customer applications.

4 Block Diagram

Figure 2 depicts the block diagram of the driver unit. The main parts of the driver unit consists of the three-phase MOSFET bridge using the CSD88539ND featuring a low R_{DSON}, the gate driver DRV8303, the three-phase sensorless motor driver DRV10983, the main controller MSP430, an ESD protection circuit, over temperature protection circuit, and sensing circuit for the input DC voltage, motor BEMF voltage, and current for the DC bus return.

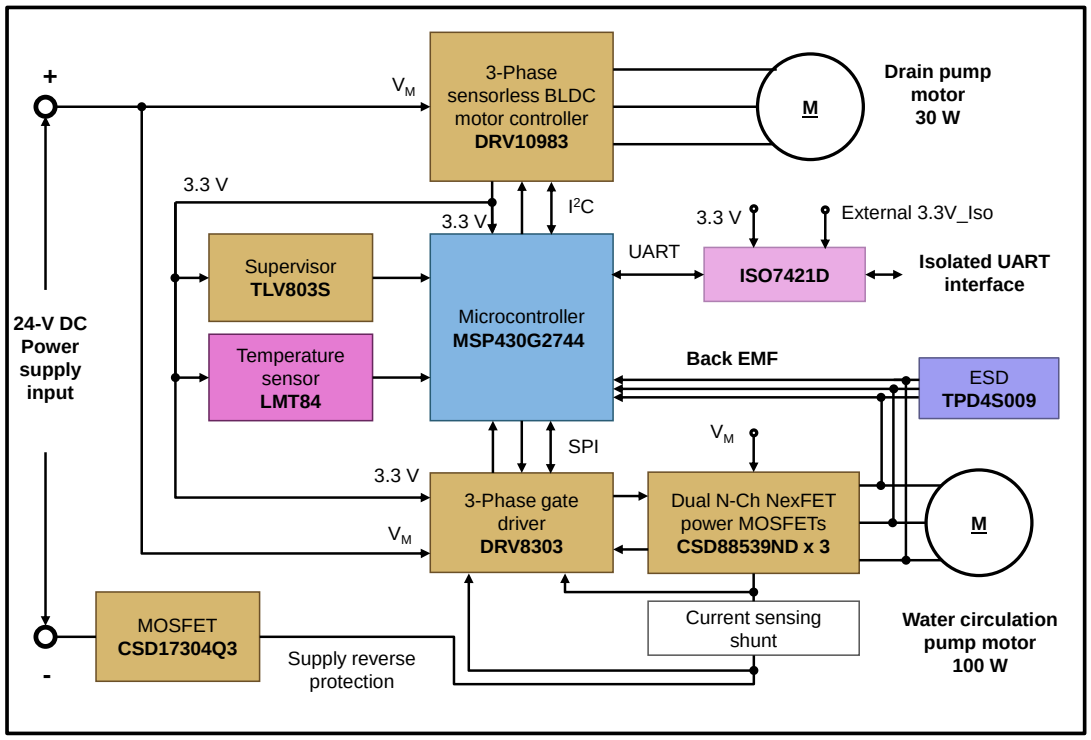


Figure 2. Block Diagram of Driver Unit

The drive unit is powered from a 24-V DC power supply, which can be derived from the AC mains using a suitable AC-DC power supply.

The water circulation pump motor is driven by the three-phase inverter consisting of the CSD88539ND, DRV8303, and MSP430G2744. The MCU MSP430G2744 configures the gate driver DRV8303 using SPI. The motor winding voltages and the inverter leg currents are sensed and fed to the MCU using appropriate signal conditioning circuits. Based on these feedbacks, the MCU executes the InstaSPIN-BLDC sensorless BLDC trapezoidal algorithm. The gate driver DRV8303 drives the three phase MOSFET bridge based on the PWM signals generated by the MCU. The DRV8303 includes two internal current shunt amplifiers, and of which is used to sense the DC return current of the three-phase bridge. The internal current shunt amplifier of the DRV8303 is used to sense the DC return current of the three-phase bridge. The voltage feedback signals are ESD protected by the transient voltage suppressor (TVS) diode array TPD4S009 before feeding to the MSP430 MCU. The temperature sensor LMT84 is used to sense the temperature of the MOSFET bridges.

The DRV10983 integrated motor driver is used to drive the water drain pump motor. The MSP430G2744 is used to configure the DRV10983 using an I^2C interface. The 3.3-V supply required for the MCU is generated by the built-in DC-DC converter of the DRV10983, which reduces the total BOM cost, by eliminating the extra power supply parts for 3.3 V. The DRV10983 provides configurable voltage surge, undervoltage, overcurrent, and motor lock protections.

The MOSFET CSD17304Q3 provides input voltage reverse polarity protection.

5 Highlighted Products

Key features of the highlighted devices can be taken from product datasheets. The following are the highlighted products used in the reference design.

5.1 DRV8303

The DRV8303 is a gate driver IC for three-phase motor drive applications. It provides three half-bridge drivers, each capable of driving two N-type MOSFETs (one for the high-side and one for the low side). It supports up to 2.3-A sink and 1.7-A source peak current capability and only needs a single power supply with a wide range from 6 to 60 V. The DRV8303 uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high-side FET or low-side FET is switching to prevent current shoot through. The V_{DS} of FETs is sensed to protect external power stage during overcurrent conditions. The DRV8303 includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3 V. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for current shunt amplifier and slew rate control of gate driver.

5.2 DRV10983

The DRV10983 is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive current capability up to 2 A continuous. The device is specifically designed for low-noise, low external component count, 12- to 24-V motor drive applications. The device is configurable through a simple I^2C interface to accommodate different motor parameters and spin-up profiles for different customer applications.

A 180° sensorless control scheme provides continuous sinusoidal output voltages to the motor phases to enable ultra-quiet motor operation by keeping the electrically induced torque ripple small. The DRV10983 features extensive protection and fault detect mechanisms to ensure reliable operation. Voltage surge protection prevents the input V_{CC} capacitor from overcharging, which is typical during motor deceleration.

The device provides overcurrent protection without the need for an external current sense resistor. Rotor lock detect is available through several methods. These methods can be configured with register settings to ensure reliable operation. The device provides additional protection for undervoltage lockout (UVLO) and for thermal shutdown.

5.3 MSP430G2744

The MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 1 µs.

The MSP430G2x44 series is an ultra-low-power mixed-signal microcontroller with two built-in 16-bit timers, a universal serial communication interface (USCI), 10-bit analog-to-digital converter (ADC) with integrated reference and data transfer controller (DTC), and 32 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone radio-frequency (RF) sensor front ends are another area of application.

5.4 CSD88539ND

The dual SO-8, 60-V, 23-mΩ NexFET™ power MOSFET is designed to serve as a half bridge in low-current motor control applications.

5.5 TPD4S009

The TPD4S009 provide system level electrostatic discharge (ESD) solution for high-speed differential lines. These devices offer four ESD clamp circuits for dual pair differential lines. The TPD4S009 offers an optional VCC supply pin, which can be connected to system supply plane. There is a blocking diode at the VCC pin to enable the I_{OFF} feature for the TPD4S009. The TPD4S009 can handle live signal at the D+, D– pins when the VCC pin is connected to zero volt. The VCC pin allows all the internal circuit nodes of the TPD4S009 to be at known potential during start up time. However, connecting the optional VCC pin to the board supply plane does not affect the system level ESD performance of the TPD4S009. The TPD4S009 is offered in DBV, DCK, DGS, and DRY packages. The TPD4S009 complies with IEC 61000-4-2 (Level 4) ESD. The TPD4S009 is characterized to operate over the ambient air temperature range of –40°C to 85°C.

5.6 TLV803S

The TLV803 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on, RESET asserts when the supply voltage (VDD) becomes greater than 2.93 V. Thereafter, the supervisory circuit monitors VDD and keeps RESET active as long as VDD remains below the threshold voltage VIT. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time (td(typ) = 200 ms) starts after VDD has risen above the threshold voltage, VIT. When the supply voltage drops below the VIT threshold voltage, the output becomes active (low) again. All the devices in this family have a fixed sense-threshold voltage (VIT) set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5, 3, 3.3, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV803 devices are characterized for operation over a temperature range of –40°C to 125°C.

5.7 CSD17304Q3

The NexFET power MOSFET minimizes losses in power conversion applications and optimized for 5-V gate drive applications with V_{DS} at 30 V and 15-A ID continuous drain current at T_A = 25°C (A).

5.8 LMT84

The LMT84 consists of precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. Its features make it suitable for many general temperature sensing C applications. It can operate down to a 1.5-V supply with 5.4-µA power consumption making it ideal for battery powered devices. Multiple package options including through-hole TO-92 and TO-126 packages also allow the LMT84 to be mounted on-board, off-board, to a heat sink, or on multiple unique locations in the same application. Class-AB output structures gives the LMT84 strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. This means it is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. It has an accuracy capability specified in the operating range of −50°C to 150°C. The accuracy, 3-lead package options, and other features also make the LMT84 an alternative to thermistors.

5.9 ISO7421D (Optional)

The ISO7420, ISO7420M, and ISO7421 provide galvanic isolation up to 2.5 kV_{RMS} for one minute per UL. These digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix M indicates wide temperature range (–40°C to 125°C).

6 System Design Theory

6.1 Main Power Input

The main power input section is shown in Figure 3. The input bulk aluminum electrolytic capacitors C21 and C28 provide the ripple current and its voltage rating is de-rated by 30% for better life and cost effectiveness. These capacitors are rated to carry high ripple current of 2.8 A. C29 and R26 are used as bypass capacitors to GND. D5 is the transient voltage suppressor having maximum breakdown voltage of 36.8 V and maximum peak pulse current of 8.3 A.

The MOSFET Q4 protects against input voltage reverse polarity. When the power supply is connected with the correct polarity, parasite diode of Q4 is turned on, R27 and R29 voltage dividers provide a proper V_{GS} to switch on the MOSFET to enable large current flow with a low conduction loss. D7 is a 16-V zener diode, provided to protect the MOSFET by limiting the V_{GS} of the MOSFET within the maximum ratings. When power supply is connected with reversed polarity, Q4 will not be turned on and no current can be drawn from the power supply; therefore, the system is protected.

When the AC-DC power supply is integrated in the same PCB, this reverse polarity protection MOSFET can be removed to make the design cost effective.

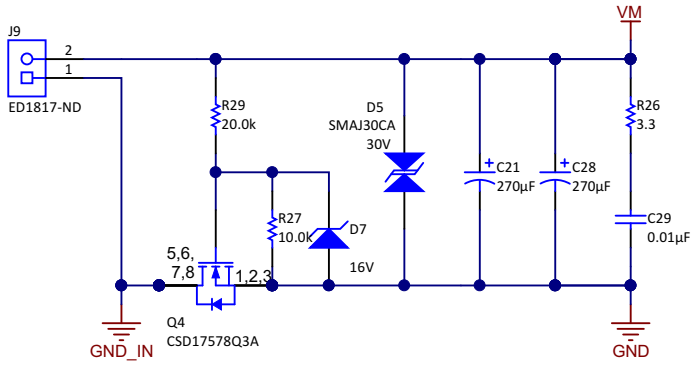


Figure 3. Main Power Input

6.2 Inverter Stage for the Circulation Pump Motor Drive

The power circuit is shown in Figure 4 consists of a three-leg MOSFET bridge. The DC return current is measured using single current sensor R24. The voltage drop across the current sensor R24 is amplified using the internal current shunt amplifier of DRV8303 and fed to the MCU MSP430G2744. A gate resistance of 3.9 Ω is used at the input of all MOSFET gates. C16, C17, and C18 are the decoupling capacitors connected across each inverter leg.

NOTE: These decoupling capacitors should be connected very near to the corresponding MOSFET legs for better decoupling (see Section 9.3). An improper lay out or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes and unintentional fault detection by the V_{DS} sensing overcurrent operation of the DRV8303.

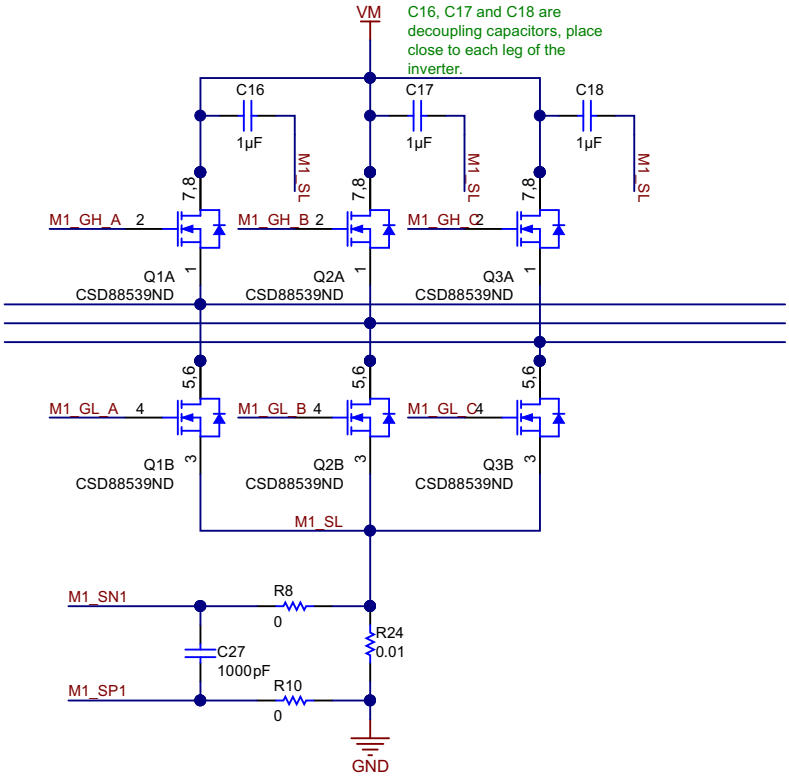


Figure 4. Three-Phase Inverter of Power Stage

6.2.1 MOSFET Selection

The board is designed to operate from 24-V DC power supply. Considering the safety factor and switching spikes, the MOSFET with a voltage rating of 1.5 times the maximum input voltage can be selected.

The current rating of the MOSFET depends on the peak winding current. The inverter bridge has to provide 4.2-A_{RMS} nominal current to the motor winding to achieve 100-W power output. In BLDC trapezoidal commutation, the peak winding current could be approximately 1.5 to 2 times the RMS current, and it depends on the motor parameters and applied voltage. Considering the worst condition, the peak winding current could be 2 × 4.2 A = 8.4 A. Considering an over loading of 120%, the peak winding current will be 10-A. Considering an overloading 120%, the peak winding current will be 7 A.

For better thermal performance, the MOSFETs with very low drain-to-source on resistance ($R_{DS(ON)}$) should be selected. In the reference design, the MOSFET CSD88539ND is selected, which is a dual-channel 60-V N-Channel NexFET power MOSFET with a low $R_{DS(ON)}$ of 23 mΩ and features very low total gate charge requirement. It has a continuous drain current capacity (package limited) of 15 and a peak current capacity of 46 A.

6.2.2 Sense Resistor Selection

Power dissipation in sense resistors and the input offset error voltage of the op-amps are important in selecting the sense resistance values. The nominal RMS winding current in motor is 4.2 A. Therefore, the sense resistors will be carrying a nominal RMS current of 4.2 A (approximately). A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8303 have DC offset error of 4 mV. The DRV8303 has the feature to do the DC offset calibration. However, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage, to reduce the effect of offset error.

Selecting a 10-mΩ resistor as the sense resistor, the power loss in the resistor at 4.2 A_{RMS} is given by Equation 1.

$$\text{Power loss in the resistor} = I_{RMS}^2 \times 0.01 = 0.18 \text{ W} \quad (1)$$

Therefore, a standard 2-W, 2512 package resistor can be used. For a current of 4.2 A, the sense voltage will be 42 mV, which is sufficiently larger than the offset error of the op-amp.

6.3 DRV8303—Three-Phase Gate Driver

The DRV8303 is used as the gate driver IC for the three-phase motor drive for the main motor. It provides three half-bridge drivers, each capable of driving two N-type MOSFETs, one for the high side and one for the low side. Figure 5 shows the schematic of the gate driver section.

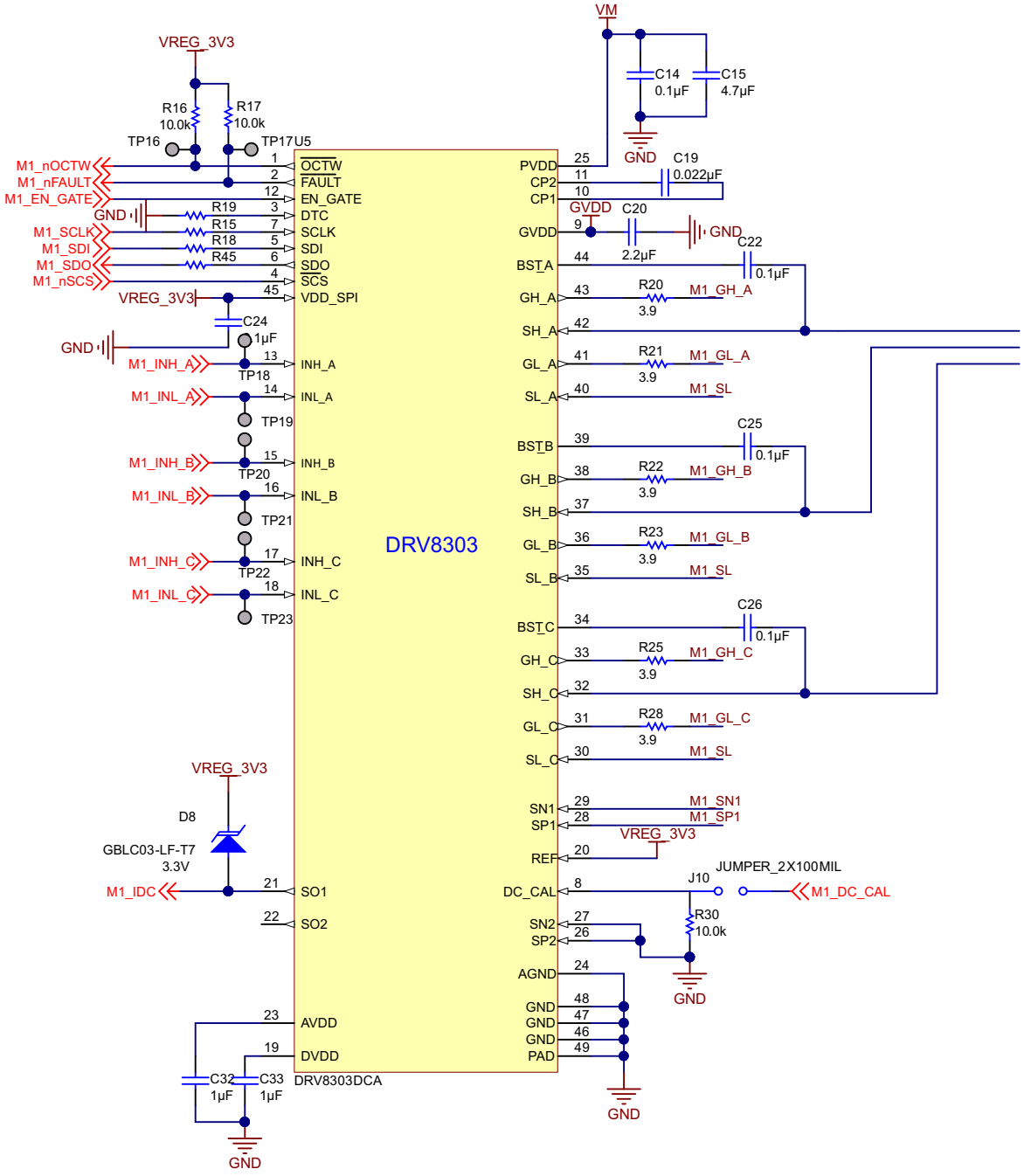


Figure 5. DRV8303 Schematic

The gate driver has following features:

- Internal handshake between high-side and low-side FETs during switching transition to prevent current shoot through
- Programmable slew rate or current driving capability through SPI
- Supports up to 200-kHz switching frequency with Qg(TOT) = 25 nC or total 30-mA gate drive average current
- Provide cycle-by-cycle (CBC) current limiting and latch overcurrent shut down of external FETs. Current is sensed through the FET V_{DS} and the overcurrent level is programmable through SPI. V_{DS} sensing range is programmable from 0.060 to 2.4 V with a 5-bit resolution
- High-side gate drive will survive negative output from half bridge up to –10 V for 10 ns
- During EN_GATE pin low and fault conditions, gate driver will keep external FETs in high impedance mode
- Programmable dead time through DTC pin. Dead time control range: 50 to 500 ns. Shorting DTC pin to ground will provide minimum dead time of 50 ns. External dead time will override internal dead time as long as the time is longer than the dead time setting
- Bootstraps circuits are used to drive high side FETs of three-phase inverter. Trickle charge circuitry is used to replenish current leakage from bootstrap cap and support 100% duty cycle operation.

In Figure 5, C14 and C15 are the PVDD decoupling capacitors. PVDD decoupling capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD; see Section 9.3 for more details). PVDD is the power supply pin for gate driver. The DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV). The PVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. C22, C25, and C26 are the bootstrap capacitors. The detailed design and features of the DRV8303 are explained in the following sections.

6.3.1 Internal Regulator Voltages of DRV8303

AVDD
The internal 6-V supply voltage. The AVDD capacitor should always be connected to AGND. This is an output, but not specified to drive external circuitry. In the schematic, C32 is used as the AVDD capacitor with a recommended value of 1 µF. Typical AVDD voltage is 6.5 V. The minimum specified value is 6 V with a maximum of 7 V.

DVDD
The internal 3.3-V supply voltage. The DVDD capacitor should connect to AGND. This is an output, but not specified to drive external circuitry. In the schematic, C33 is used as the DVDD capacitor with a recommended value of 1 µF. AVDD and DVDD capacitors should be placed close to their corresponding pins with a low impedance path to the AGND pin (see Section 9.3 for more details). It is preferable to make this connection on the same layer. AGND should be tied to the device GND (PowerPAD) through a low impedance trace/copper fill. Typical DVDD voltage is 3.3 V. The minimum specified value is 3 V with a maximum of 3.6 V. If DVDD goes to undervoltage, the external FETs go to high impedance state by means of the weak pulldown of all gate driver output. On recovering from undervoltage, the DRV8303 resets the SPI registers. The DVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin.

GVDD
The voltage output from internal gate driver voltage regulator. The capacitor C20 is connected at the GVDD pin. The GVDD capacitor should be connected to GND. Typically, a 2.2-µF ceramic capacitor is recommended as the GVDD capacitor. Place the GVDD capacitor close its corresponding pin with a low impedance path to device GND (PowerPAD; see Section 9.3 for more details). The GVDD pin is protected from undervoltage and overvoltage. The undervoltage protection limit of GVDD is 7.5 V and the overvoltage protection limit is 16 V. When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high impedance state. The GVDD undervoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register. The GVDD overvoltage fault is a latched fault and can only be reset through a transition on EN_GATE pin. The GVDD overvoltage will be reported through $\overline{\text{FAULT}}$ pin and SPI status register.

6.3.2 Current Shunt Amplifiers in DRV8303

The DRV8303 includes two high performance current shunt amplifiers for accurate current measurement. The current amplifiers provide output offset up to 3 V to support bi-directional current sensing. The current shunt amplifier has following features:

- Programmable gain: Four gain settings (10, 20, 40, and 80) are possible through SPI command
- Programmable output offset through reference pin (half of the V_{REF})
- Minimize DC offset and drift over temperature with DC calibration through SPI command or DC_CAL pin. When DC calibration is enabled, the device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at any time even when FET is switching since the load is disconnected. For best result, perform the DC calibrating during switching off period when no load is present to reduce the potential noise impact to the amplifier.

A simplified block diagram of the current shunt amplifiers are shown in Figure 6. The output of current shunt amplifier can be calculated using Equation 2.

$$V_O = \frac{V_{REF}}{2} - G \times \left(SN_X - SP_X\right) \quad (2)$$

Where V_{REF} is the reference voltage, G is the gain of the amplifier; SN_X and SP_X are the inputs of channel X. SP_X should connect to resistor ground for the best common mode rejection.

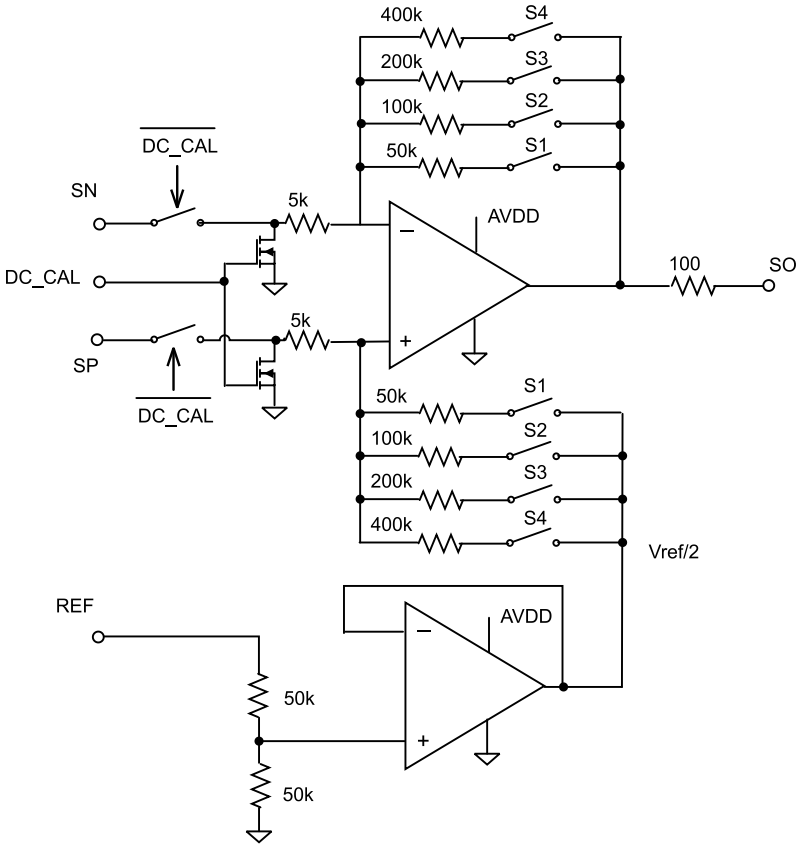


Figure 6. Current Shunt Amplifier in DRV8303 - Simplified Block Diagram

In the schematic, J10 is reserved for the MCU to be able to enable DC calibration. When not used, keep J10 open and DC_CAL signal is pulled down to GND through R30.

6.3.3 Protection Features in DRV8303

Overcurrent Protection and Reporting

To protect the power stage from damage due to high currents, a V_{DS} sensing circuitry is implemented in the DRV8303. Based on $R_{DS(ON)}$ of the power MOSFETs and the maximum allowed drain current, a voltage threshold can be calculated which, when exceeded, triggers the overcurrent protection feature. This voltage threshold level is programmable through SPI command. There are total four OC_MODE settings in SPI.

1. Current limit mode

   When current limit mode is enabled, the DRV8303 limits the MOSFET current instead of shutting down during an overcurrent event. The overcurrent event is reported through the $\overline{\text{OCTW}}$ pin. $\overline{\text{OCTW}}$ reporting will hold low during same PWM cycle or for a max 64-µs period (internal timer) so the external controller has enough time to sample the warning signal. If in the middle of reporting other FETs get overcurrent, then $\overline{\text{OCTW}}$ reporting will hold low and recount another 64 µs unless PWM cycles on both FETs are ended.

   There are two current control settings in current limit mode (selected by one bit in SPI and default is CBC mode).

   - Setting 1 (CBC mode): during an overcurrent event, the FET that detected overcurrent will turn off until next PWM cycle.
   - Setting 2 (off-time control mode):
     - During an overcurrent event, the FET that detected overcurrent will turn off for 64 µs as off time and back to normal after that (so same FET will be on again) if PWM signal is still holding high. Since all three phases or 6 FETs share a single timer, if more than one FET get overcurrent, the FETs will not be back to normal until the all FETs that have an overcurrent event pass 64 µs.
     - If PWM signal is toggled for this FET during timer running period, the device will resume normal operation for this toggled FET. So, the real off-time could be less than 64 µs in this case.
     - If two FETs get overcurrent and one FET's PWM signal gets toggled during timer running period, this FET will be back to normal, and the other FET will be off till timer end (unless its PWM is also toggled)

2. Overcurrent latch shutdown mode

   When overcurrent occurs, the device will turn off both high-side and low-side FETs in the same phase if any of the FETs in that phase has overcurrent.

3. Report only mode

   No protection action will be performance in this mode. Overcurrent detection will be reported through the $\overline{\text{OCTW}}$ pin and SPI status register. The external MCU should take actions based on its own control algorithm. A pulse stretching of 64 µs will be implemented on $\overline{\text{OCTW}}$ pin so the controller can have enough time to sense the overcurrent signal.

4. Overcurrent disable mode

   The device will ignore all the overcurrent detections and will not report them either.

Undervoltage Protection

To protect the power stage during undervoltage conditions, the DRV8303 provides power stage undervoltage protection by driving its outputs low whenever PVDD is below 6 V (PVDD_UV) or GVDD is below 7.5 V (GVDD_UV). When undervoltage protection is triggered, the DRV8303 outputs are driven low and the external MOSFETs will go to a high impedance state.

Overvoltage Protection (GVDD_OV)

The DRV8303 will shut down both the gate driver and charge pump if GVDD voltage exceeds 16 V to prevent potential issue related to GVDD or charge pump (for example, short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a transition on EN_GATE pin.

Over Temperature Protection

A two-level over temperature detection circuit is implemented in the DRV8303:

- Level 1: Over temperature warning. The warning is reported through the $\overline{\text{OCTW}}$ (overcurrent temperature warning) pin for default setting. $\overline{\text{OCTW}}$ can be set to report over temperature or overcurrent warnings only through SPI command.
- Level 2: Over temperature latched shut down of gate driver and charge pump (OTSD_GATE). The fault will be reported to $\overline{\text{FAULT}}$ pin. This is a latched shut down so the gate driver will not be recovered automatically; even an over temperature condition is not present anymore. An EN_GATE reset through pin or SPI (RESET_GATE) is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}. SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD is still within defined operation range.

Junction temperature for resetting over temperature warning (OTW_CLR) is 115°C. Junction temperature for over temperature warning and resetting the over temperature shutdown (OTW_SET/OTSD_CLR) is 130°C.

Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event (with shutdown) has occurred such as overcurrent, over temperature, overvoltage, or undervoltage. Note that $\overline{\text{FAULT}}$ is an open-drain signal. $\overline{\text{FAULT}}$ will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up. The $\overline{\text{OCTW}}$ pin indicates overcurrent event and over temperature event that not necessary related to shutting down. $\overline{\text{OCTW}}$ is an open-drain signal.

EN_GATE

EN_GATE low is used to put the gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low power consumption mode to save energy. SPI communication is not supported during this state. The device will put the MOSFET output stage to high impedance mode as long as PVDD is still present. When EN_GATE pin goes to high, it will go through a power up sequence, and enable the gate driver, current amplifiers, charge pump, internal regulator, and so on, and reset all latched faults related to gate driver block. The EN_GATE pin will also reset status registers in the SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present. When EN_GATE goes from high to low, it will shut down the gate driver block immediately, so the gate output can put external FETs in high impedance mode. It will then wait for 10 µs before completely shutting down the rest of the blocks. A quick fault reset mode can be done by toggling the EN_GATE pin for a very short period (less than 10 µs). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode. The other way to reset all the faults is to use SPI command (RESET_GATE), which will only reset the gate driver block and all the SPI status registers without shutting down other function blocks. One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset will not work with the GVDD_OV fault. A complete EN_GATE with a low-level holding longer than 10 µs is required to reset GVDD_OV fault. It is highly recommended to inspect the system and board when GVDD_OV occurs.

DTC

Dead time can be programmed through the DTC pin. A resistor should be connected from DTC to ground to control the dead time. Dead time control range is from 50 to 500 ns. Short the DTC pin to ground to provide the minimum dead time (50 ns). Resistor range is 0 to 150 kΩ. Dead time is linearly set over this resistor range. Current shoot through protection will be enabled in the device at all times independent of dead time and input mode settings.

In this reference design, a 1-Ω resistor is connected to the DTC pin.

6.3.4 SPI Communication

VDD_SPI
The power supply to power the SDO pin. It has to be connected to the same power supply (3.3 V or 5 V) that the MCU uses for its SPI operation. During power up or down transient, the VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at the SDO pin from any other devices in the system because it causes a parasitic diode in the DRV8303 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

DC_CAL
When DC_CAL is enabled, the device will short inputs of the shunt amplifier and disconnect from the load, so the external MCU can perform a DC offset calibration. DC offset calibration can be also done with SPI command. If using SPI exclusively for DC calibration, the DC_CAL pin can be connected to GND.

SPI Pins
The SDO pin has to be 3-state, so a data bus line can be connected to multiple SPI slave devices. SCS pin is active low. When SCS is high, SDO is at high impendence mode.

SPI
SPI is used to set device configuration, operating parameters and read out diagnostic information. The DRV8303 SPI Interface operates in the slave mode. The SPI input data (SDI) word consists of 16-bit word, with 11-bit data and 5-bit (MSB) command. The SPI output data (SDO) word consists of 16-bit word, with 11-bit register data and 4-bit MSB address data and 1 frame fault bit (active 1). When a frame is not valid, frame fault bit will set to 1, and rest of SDO bit will shift out zeroes.

A valid frame has to meet following conditions:

1. The clock must be low when /SCS goes low.
2. The user should have 16 full clock cycles.
3. The clock must be low when /SCS goes high.

Thus, the SCS pin cannot be left uncontrolled and pulled down to GND.

When SCS is asserted high, any signals at the SCLK and SDI pins are ignored, and SDO is forced into a high impedance state. When SCS transitions from HIGH to LOW, SDO is enabled and the SPI response word loads into the shift register based on 5-bit command in SPI at previous clock cycle. The SCLK pin must be low when SCS transitions low. While SCS is low at each rising edge of the clock, the response bit is serially shifted out on the SDO pin with MSB shifted out first.

While SCS is low, at each falling edge of the clock, the new control bit is sampled on the SDI pin. The SPI command bits are decoded to determine the register address and access type (read or write). The MSB will be shifted in first. If the word sent to SDI is less than or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in SDO (MSB) will report 1 at next 16-bit word cycle. After the 16th clock cycle or when SCS transitions from LOW to HIGH, in case of write access type, the SPI receive shift register data is transferred into the latch where address matches decoded SPI command address value. Any amount of time may pass between bits, as long as SCS stays active low. This allows two 8-bit words to be used.

For a read command (Nth cycle) in SPI, SP0 will send out data in the register with address in read command in next cycle (N+1). For a write command in SPI, SPO will send out data in the status register 0x00h in next 16-bit word cycle (N+1). For most of the time, this feature will maximize SPI communication efficiency when having a write command, but still get fault status values back without sending extra read command.

SPI Format

SPI input data control word is 16-bit long, consisting of:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

SPI output data response word is 16-bit long, and its content depends on the given SPI command (SPI Control Word) in the previous cycle. When a SPI Control Word is shifted in, the SPI Response Word (that is shifted out during the same transition time) is the response to the previous SPI Command (shift in SPI Control Word "N" and shift out SPI Response Word "N-1"). Therefore, each SPI Control / Response pair requires two full 16-bit shift cycles to complete. The definition of all SPI registers is given in the datasheet of the DRV8303.

6.4 Motor Winding Voltage Sensing

The voltage divider circuit shown in Figure 7 is used to measure the winding voltages. Voltage feedback is needed in the trapezoidal BEMF control algorithm firmware in the MSP430. In the firmware, phase voltages are measured directly from the motor phases instead of a software estimate. The firmware works on the BEMF integration technique. The algorithm derives the motor BEMF by sensing the winding voltages of the non-energized phase. The measured winding voltage will be overriding on the half of the DC bus voltage (VM/2) during the PWM ON time of the energized phases. Therefore, the BEMF is derived by subtracting VM/2 from the sensed winding voltages. The algorithm assumes same scaling in the winding voltage and DC bus voltage (VM) sensing network. Therefore, it is important to keep the exact same scaling configuration for BEMF voltage sensing circuits and VM sensing circuit.

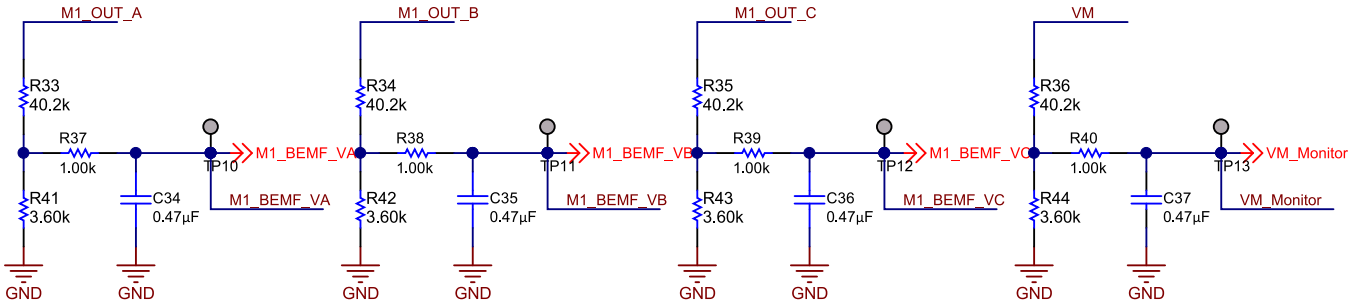


Figure 7. Motor Winding Voltage Sense Circuit

M1_OUT_A, M1_OUT_B, and M1_OUT_C are the phase voltages. These voltages are properly scaled and fed to the controller through M1_BEMF_A, M1_BEMF_A, and M1_BEMF_A. The ADC of the MSP430 is configured to use the internal 2.5-V reference for accurate measurement. Therefore, the maximum voltage measurable by the ADC (VADC_a(max) is 2.5 V.

Therefore, the maximum phase voltage or DC voltage ($V_{a(max)}$) measurable by the feedback network and MCU can be calculated using Equation 3.

$$V_{a(max)} = V_{ADC\_a(max)} \times \frac{(3.6\ k\Omega + 40.2\ k\Omega)}{3.6\ k\Omega} = 2.5 \times \frac{(3.6\ k\Omega + 40.2\ k\Omega)}{3.6\ k\Omega} = 30.4\ V \quad (3)$$

Thus, the rated max input voltage of the system (28 V) is within the appropriate measurement range.

6.5 Output Inductors for Circulation Pump Motor Drive

The inductors L5, L6, and L7 are provided for better EMI performance. These inductors also help reduce the short circuit current in low inductance motors and provide sufficient time for overcurrent protection to activate. Based on the final application motor, the user can consider eliminating this inductor. For more details about the inductor selection, see the DRV83x2 datasheet (SLES256).

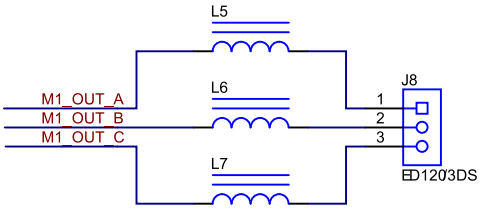


Figure 8. Output Inductor of DRV8303 for CBC Current Limit Protection

6.6 MOSFET Temperature Sensor

Figure 9 shows the temperature sensor circuit used to measure the temperature of the MOSFETs. The LMT84 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source. The average output sensor gain is –5.5 mV/°C.

Although the LMT84 is very linear, its response does have a slight umbrella parabolic shape. The output voltages at different temperatures are given in the LMT84 datasheet in tabular form. For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range using the two-point equation of a line. Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

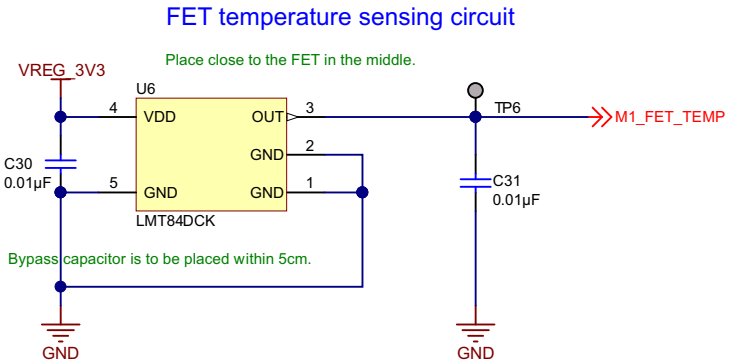


Figure 9. Heat Sink Temperature Sensor

6.7 Fault Indications

The DRV8303 fault indication outputs $\overline{\text{OCTW}}$ and $\overline{\text{FAULT}}$ are pulled up and connected input pins of MSP430. Table 4 shows the faults in the DRV8303 indicated through the two fault reporting output pins.

Table 4. Fault Events Reporting From DRV8303

REPORTING PIN	FAULT EVENTS
$\overline{\text{FAULT}}$	• PVDD undervoltage • DVDD undervoltage • GVDD undervoltage • GVDD overvoltage • OTSD_GATE: Gate driver latched shut down • External FET overload: Latch mode
$\overline{\text{OCTW}}$	• OTW: Over temperature • OTSD_GATE: Gate driver latched shut down • External FET overload: Current limit mode • External FET overload: Latch mode • External FET overload: Reporting only mode

6.8 DRV10983—Integrated Motor Driver for Drain Pump Motor Drive

The DRV10983 is the integrated motor driver for the secondary motor, which has a built-in 180° sensorless control scheme. In Figure 10, the bulk electrolytic capacitor C8 is placed next to VM near the IC DRV10983 for local ripple current capability.

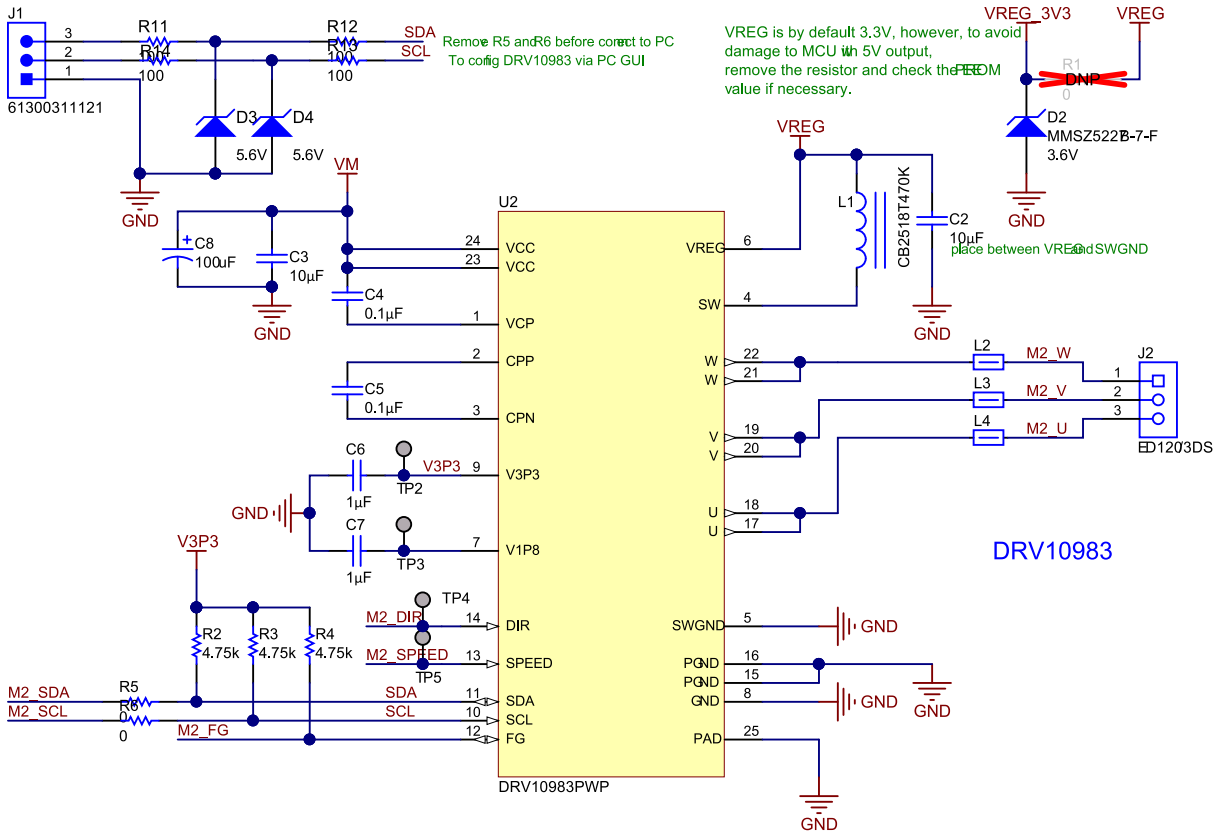


Figure 10. DRV10983 Circuit Schematic

6.8.1 Step-Down Voltage Regulator of DRV10983

The DRV10983 includes a step-down voltage regulator that can be operated as either a switching buck style regulator or as a linear regulator (see Figure 11). The regulator output voltage can be configured by register bit VregSel. When VregSel = 0, the regulator output voltage is 5 V, and when VregSel = 1, the regulator output voltage is 3.3 V with a 100-mA capacity. This reference design uses this as the power supply to the MCU. L1 and C2 are the output filter components for the buck regulator.

The voltage regulator can be configured for an output of 3.3 or 5 V through the internal EEPROM of the DRV10983. The MCU is powered using the 3.3 V generated by the DRV10983. An incorrect setting in the EEPROM for the 5-V output may damage the MCU rated for 3.3 V only. To avoid any such failures, it is recommended to leave R1 not populated when powering the board for the first time. After the properly checking the output of 3.3-V on V_{REG} of the DRV10983, R1 can be mounted. Also, the 3.3-V zener D2 is provided to protect the MCU from being damaged by the accidental 5-V output from the DRV10983.

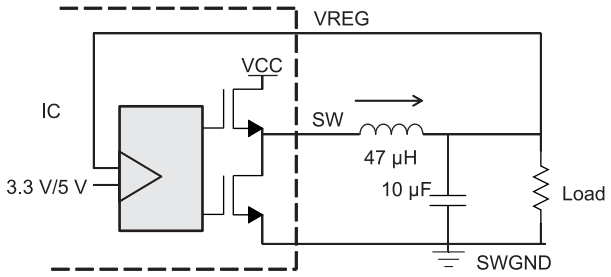


Figure 11. DRV10983 Step-Down Voltage Regulator

6.8.2 Protection Features in DRV10983

1. Thermal Shutdown

   The DRV10983 has a built-in thermal shutdown function, which shuts down the device when junction temperature is more than 150°C and recovers operating conditions when junction temperature falls to 140˚C. The OverTemp status bit (address 0x10 bit 7) is set during thermal shutdown.

2. UVLO

   The DRV10983 has a built-in UVLO function block. The hysteresis of UVLO threshold is 300 mV (typ.). The device is locked out when VCC is down to 7.1 V (typ.) and woke up at 7.4 V (typ.).

3. Current Protection

   The overcurrent shutdown function acts to protect the device if the current, as measured from the FETs, exceeds the 4-A (typ.) threshold. It protects the device in the short-circuit condition if by accident phase shorts to GND, or phase shorts to phase; the DRV10983 places the output drivers into a high-impedance state and maintains this condition until the overcurrent is no longer present. The OverCurr status bit (address 0x10 bit 5) is set.

   The DRV10983 also provides acceleration current limit and lock detection current limit functions to protect the device and motor.

4. Lock Protection

   When the motor is blocked or stopped by an external force, the lock protection is triggered, and the device stops driving the motor immediately. After the lock release time of five seconds, the DRV10983 resumes driving the motor again. If the lock condition is still present, it enters the next lock protection cycle until the lock condition is removed. With this lock protection, the motor and device does not get overheated or damaged due to the motor being locked. During lock condition, the MtrLck Status bit (address 0x10, bit 4) is set. To further diagnose, check the register FaultCode.

6.8.3 I²C Communication

The DRV10983 provides an I²C slave interface with slave address '101 0010'. TI recommends a pullup resistor 4.7 kΩ to 3.3 V for the I²C interface ports SCL and SDA. Four read/write registers (0x00:0x03) are used to set motor speed and control device registers and EEPROM.

Device operation status can be read back through 12 read-only registers (0x10:0x1E). Another 12 EEPROM registers (0x20:0x2B) can be accessed to program motor parameters and optimize the spin-up profile for the application.

7 Getting Started Firmware

This design includes a firmware that is based on the firmware of the TIDA-00274 with control function of the DRV10983 added. The circulation pump motor is driven by InstaSPIN-BLDC algorithm running on MSP430. InstaSPIN-BLDC is TI's one of the key flagship motor control technology targeted for cost sensitive sensorless BLDC applications. This sensorless technique uses traditional trapezoidal or 120° commutation and monitors motor flux by integrating BEMF of non-energized phase to determine the commutation instances. For certain market, such as fan, pumps, blowers, and so on, which do not require high accuracy speed control and fast dynamic torque response, InstaSPIN-BLDC implementation from TI's MSP430G2x value line of devices is right way to meet low cost requirements. Refer to the product page for more information about the firmware of the TIDA-00274.

Since a different MCU part number is used by the TIDA-00447, some pin mapping and configuration need to be modified from TIDA-00274 firmware. In TIDA-00447 firmware, communication with the DRV8303 through SPI is implemented to speed up development and evaluation of design with the DRV8303.

The control of the secondary pump using the DRV10983 features mainly the following functions:

- I^2C communication
- Setting motor parameters to the EEPROM of the DRV10983 from the MCU
- Control motor speed both by I^2C and by the PWM output from the MCU
- Reading the FG signal from the DRV10983

7.1 Modifying Hardware Configuration

The MSP430G2744 is used in this design. The control algorithm require only one timer output PWM channel at a given point of time. The same timer output for PWM is used by mapping it to different pins of the MCU at different times based on the commutation sequence. PWM output on TA1 is used in this design, and the pins used are marked as shown in Figure 12.

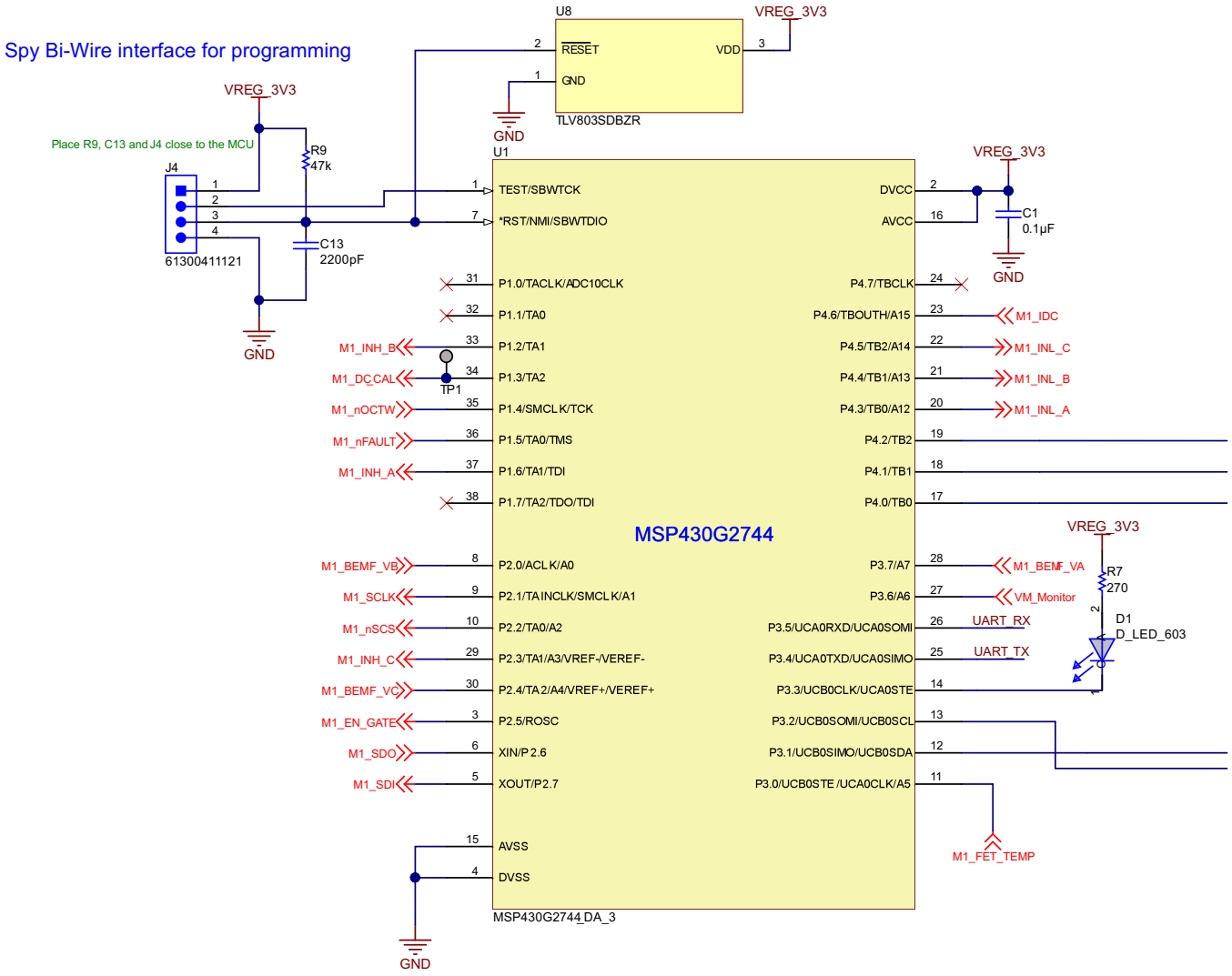


Figure 12. Pin Mapping for PWM Outputs on MSP430G2744

The firmware comes with a hardware configuration file "hardware_config.c". Change the content of the interfaces in the file according to the actual hardware configuration. Interfaces to be changed are:

```
void A_HIGH (void);
void A_LOW (void);
void A_PWM (void);
void A_Z(void);

void B_HIGH (void);
void B_LOW (void);
void B_PWM (void);
void B_Z(void);

void C_HIGH (void);
void C_LOW (void);
void C_PWM (void);
void C_Z(void);

void DRV_RESET_ENABLE(void);
void DRV_RESET_DISABLE(void);
uint8_t FAULT_STATE_PIN_FUNCTION(void);
volatile uint16_t * PWM_INITIALIZER(void);
uint16_t PWM_REGISTER_READ(void);

void High_Impedance(void);
```

Since the ADC channels may also be changed during the design, the following macro definitions might also be changed accordingly.

MEASURE_VDC
MEASURE_IDC
MEASURE_A
MEASURE_B
MEASURE_C

7.2 Configuring DRV8303 Registers

A GPIO-based SPI driver is provided in the firmware. The user can include the files of "drv_8303.c" and "drv_8303.h" into the project and use the simple interface of

```
uint16_t ReadRegister(uint8_t);
void WriteRegister(uint8_t, uint16_t);
```

to read and write the status and control registers of the DRV8303. Since the interfaces are using __delay_cycles() intrinsic, take care when calling these interfaces in time critical routines.

Register bits are provided as macro definitions for easy use in drv8303.h. They are:

```
/* Register 0x02 */
#define GATE_CURRENT_1P7         0x000
#define GATE_CURRENT_0P7         0x001
#define GATE_CURRENT_0P25        0x002
#define GATE_CURRENT_RSVD        0x003
#define GATE_RESET_NORMAL        (0x000 << 2)
#define GATE_RESET_LATCHED       (0x001 << 2)
#define PWM_MODE_INDEPENDENT     (0x000 << 3)
#define PWM_MODE_COMPLEMENTARY   (0x001 << 3)
#define OC_MODE_LIMIT            (0x000 << 4)
#define OC_MODE_SHUTDOWN         (0x001 << 4)
#define OC_MODE_REPORT_ONLY      (0x002 << 4)
#define OC_MODE_PROTECTION_DISABLED    (0x003 << 4)

#define OC_ADJ_SET        (0x00A << 6)/* user define according to RDSON */

/* Register 0x03 */
#define OCTW_SET_OTOC            (0x000)
#define OCTW_SET_OT              (0x001)
#define OCTW_SET_OC              (0x002)
#define OCTW_SET_RSVD            (0x003)
#define OPAMP_GAIN_10V           (0x000 << 2)
#define OPAMP_GAIN_20V           (0x001 << 2)
#define OPAMP_GAIN_40V           (0x002 << 2)
#define OPAMP_GAIN_80V           (0x003 << 2)
#define DC_CAL_CH1_LOAD          (0x000 << 4)
#define DC_CAL_CH1_SHORT         (0x001 << 4)
#define DC_CAL_CH2_LOAD          (0x000 << 5)
#define DC_CAL_CH2_SHORT         (0x001 << 5)
#define OC_TOFF_NORMAL           (0x000 << 6)
#define OC_TOFF_OFFTIME          (0x000 << 6)
```

The OC_ADJ_SET macro has to be set by the user according to the overcurrent threshold to be used in the system. In this project, 0.197 V is selected, thus OC_ADJ_SET is set to (0x007 << 6).

7.3 Configuring DRV10983 Registers

The DRV10983 internal registers and EEPROM can be configured through a standard I^2C communication interface, either from the MCU in the system or by an external calibration tool (for example, USB2ANY).

In this design, configuration from the MCU is provided as user can reference. Files of "drv_10983.c" and "drv_10983.h" provide necessary interface definitions for I^2C communication.

Refer to *Programming Guide for the DRV10983* (SLVUAA5) for more information.

To tune a user specified motor, refer to *DRV10983 and DRV10975 Tuning Guide*. The tuning procedure is demonstrated in Figure 13. Contact a local support team for more information about documentation and support.

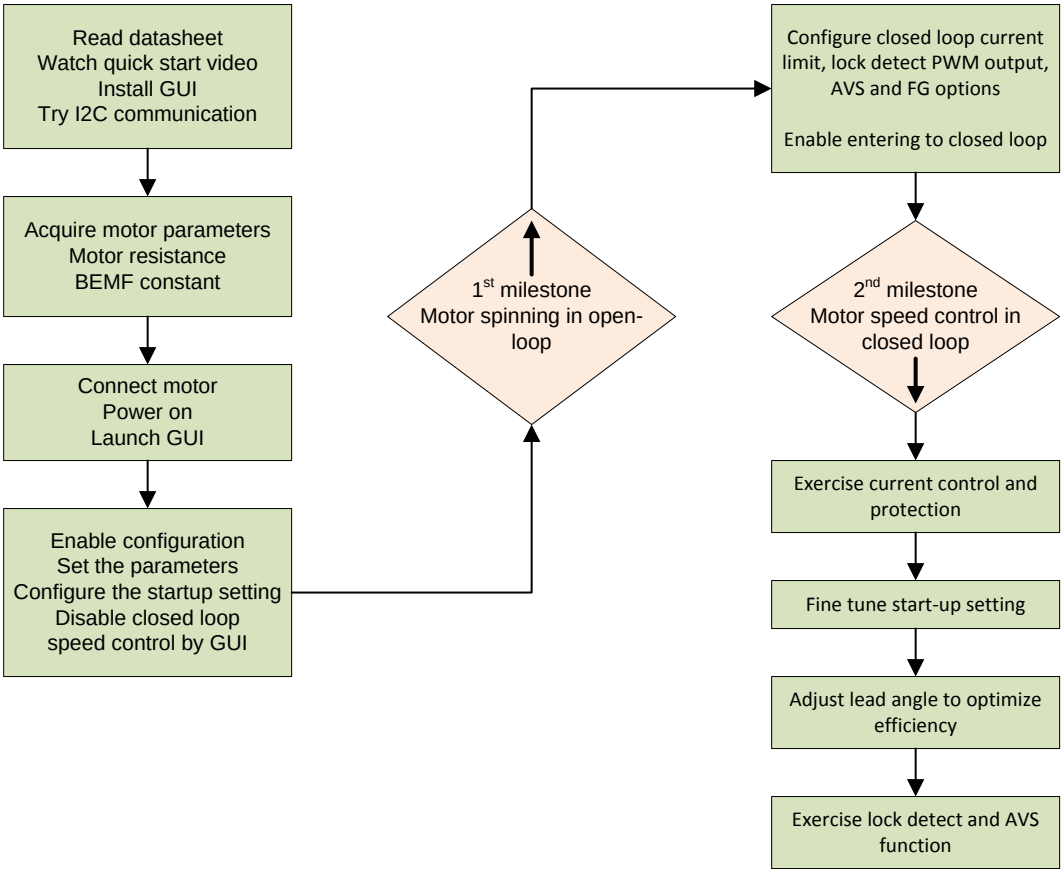


Figure 13. Events for Tuning Motor Parameters for DRV10983

7.4 Test Points

For easier performance test purposes, the hardware of the TIDA-00447 comes with a sufficient number of test points on the board. See Table 5 or the schematic for the test point to signal relationship.

Table 5. Test Point Descriptions

TEST POINT	SIGNAL NET	DESCRIPTION
TP1	M1_DC_CAL	DC offset calibration of DRV8303
TP2	V3P3	Internal 3.3-V supply voltage of DRV10983
TP3	V1P8	Internal 1.8-V digital core voltage of DRV10983
TP4	M2_DIR	Direction command of DRV10983
TP5	M2_SPEED	Speed command of DRV10983
TP6	M1_FET_TEMP	FET temperature from LMT84
TP7	GND	Ground
TP8	GND	Ground
TP9	GND	Ground
TP10	M1_BEMF_VA	BEMF on phase A to MCU ADC
TP11	M1_BEMF_VB	BEMF on phase B to MCU ADC
TP12	M1_BEMF_VC	BEMF on phase C to MCU ADC
TP13	VM_Monitor	VM sampling to MCU ADC
TP14	VREG	Regulator output of DRV10983
TP15	M2_FG	Speed feedback from DRV10983 to MCU
TP16	M1_nOCTW	nOCTW signal of DRV8303
TP17	M1_nFAULT	nFAULT signal of DRV8303
TP18	M1_INH_A	High-side input to DRV8303 on phase A from MCU
TP19	M1_INL_A	Low-side input to DRV8303 on phase A from MCU (PWM)
TP20	M1_INH_B	High-side input to DRV8303 on phase B from MCU
TP21	M1_INL_B	Low-side input to DRV8303 on phase B from MCU (PWM)
TP22	M1_INH_C	High-side input to DRV8303 on phase C from MCU
TP23	M1_INL_C	Low-side input to DRV8303 on phase C from MCU (PWM)

8 Test Results

Figure 14 and Figure 15 shows the top and bottom view of the assembled board. It can be noted that the complete assembly is with components only on the top of the board.

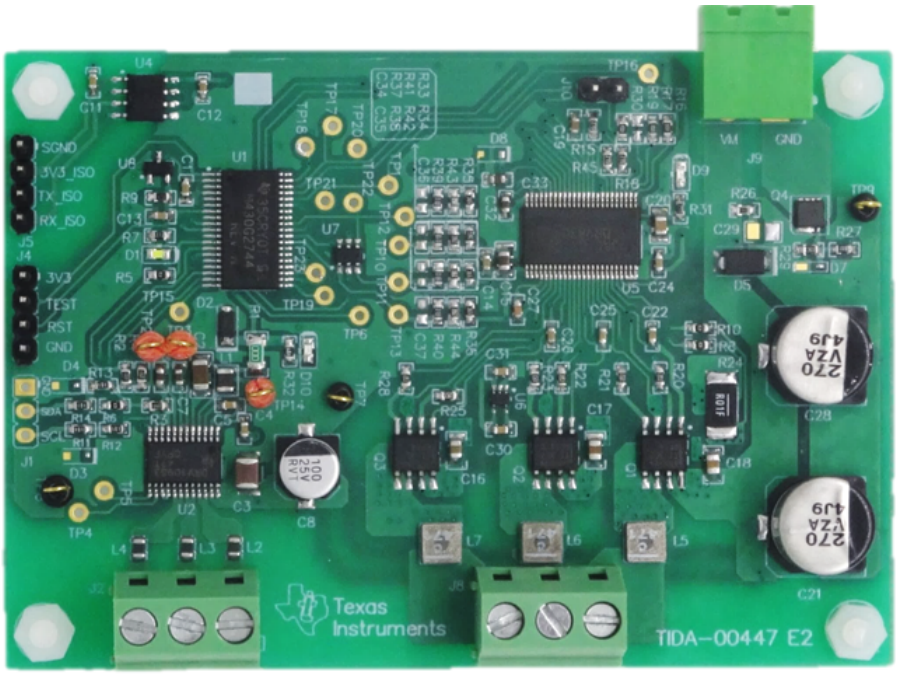


Figure 14. Assembled Control Unit—Top View

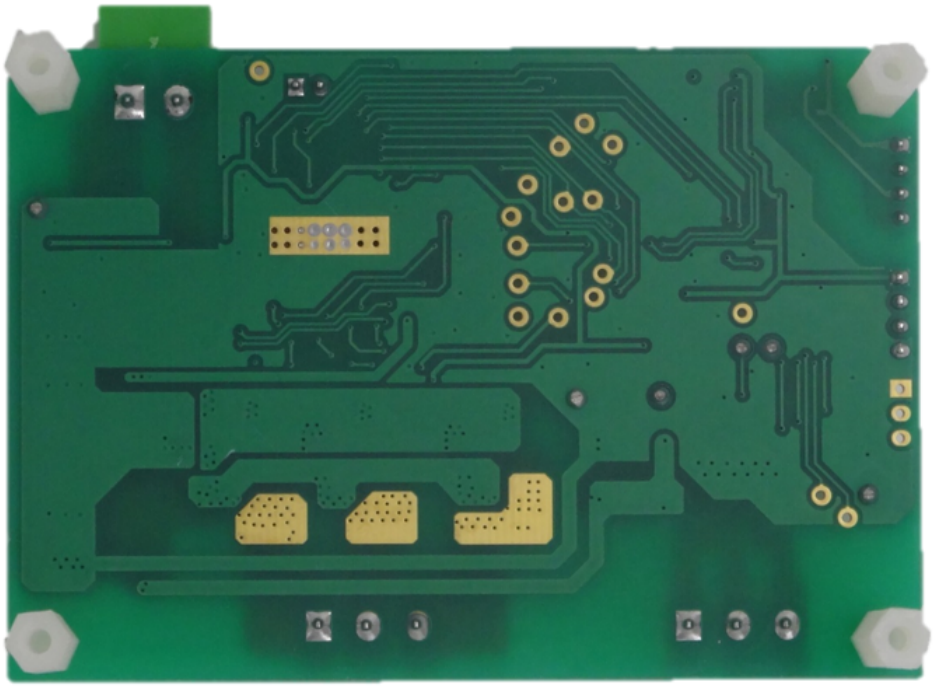


Figure 15. Assembled Control Unit—Bottom View

8.1 Functional Tests

Figure 16 shows the 3.3 V generated from the DRV10983 step-down regulator. The ripple in the 3.3-V rail is shown Figure 17.

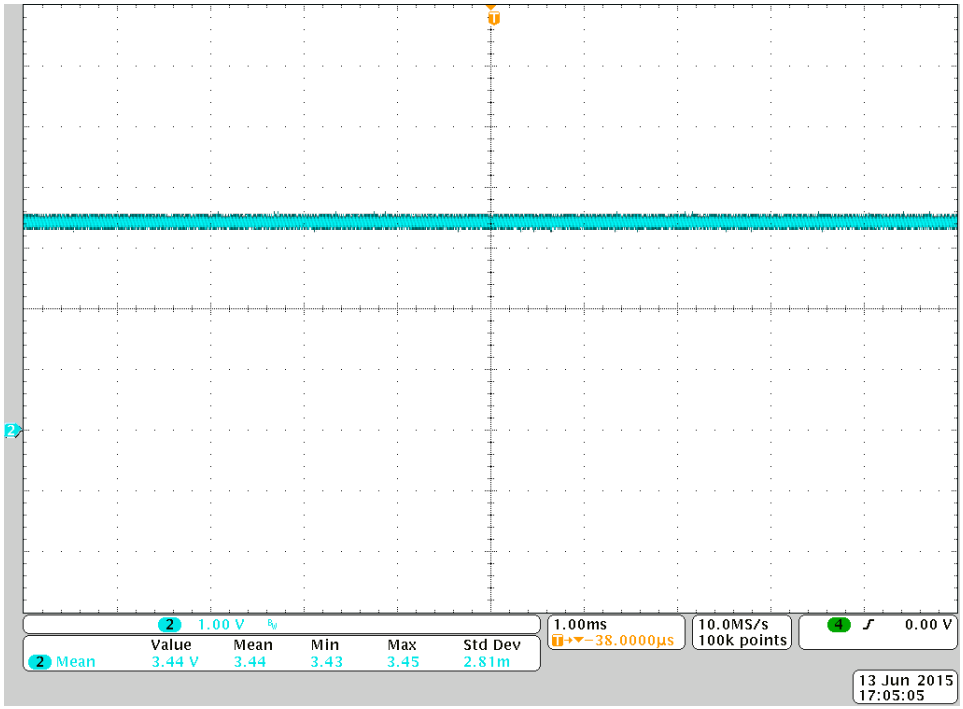


Figure 16. Output Voltage of 3.3 V From the Step-Down Regulator of DRV10983

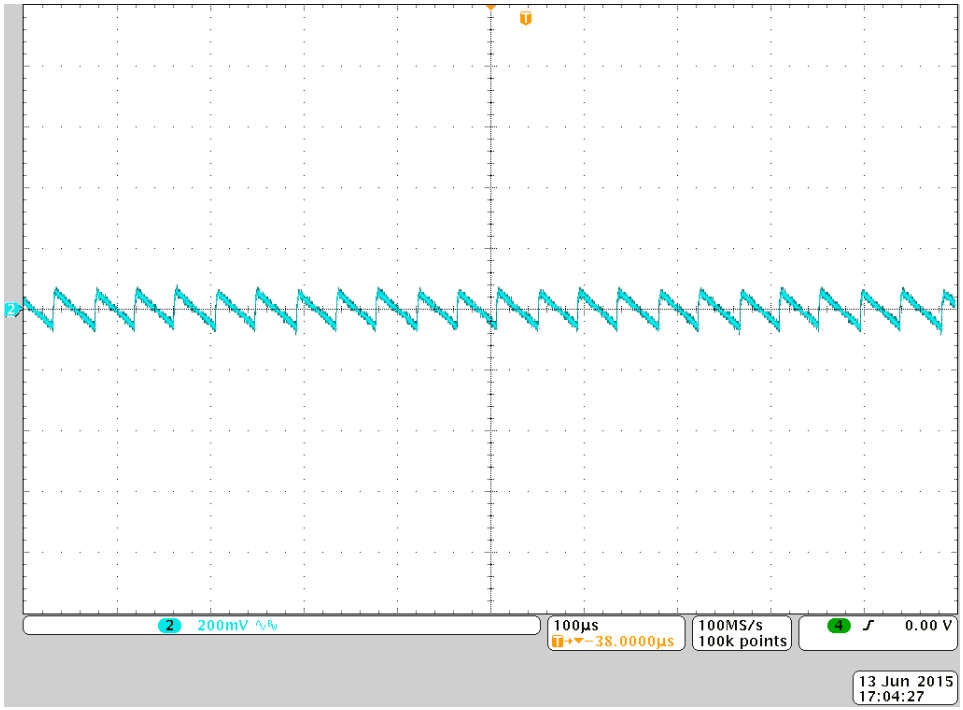


Figure 17. Ripple in 3.3-V Output From the Step-Down Regulator of DRV10983

Peak-to-peak ripple voltage of the 3.3-V output is around 140 mV.

The internal voltage regulator of the DRV8303 produces different regulated voltages. It includes GVDD, AVDD, and DVDD for the operation of the internal circuits of the DRV8303. Figure 18 shows the GVDD voltage of the DRV8303 and the voltage ripple in GVDD is shown in Figure 19. The mean voltage at the GVDD is observed to be 11 V, which is well above the undervoltage rating (7.5 V).

Testing the Circulation Pump Motor Drive

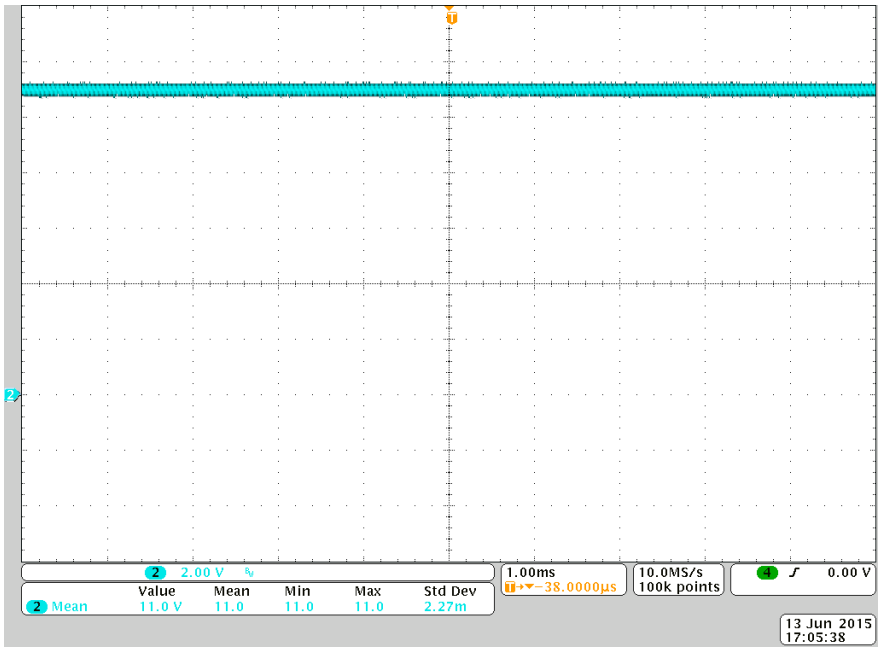


Figure 18. Voltage at GVDD Pin of DRV8303

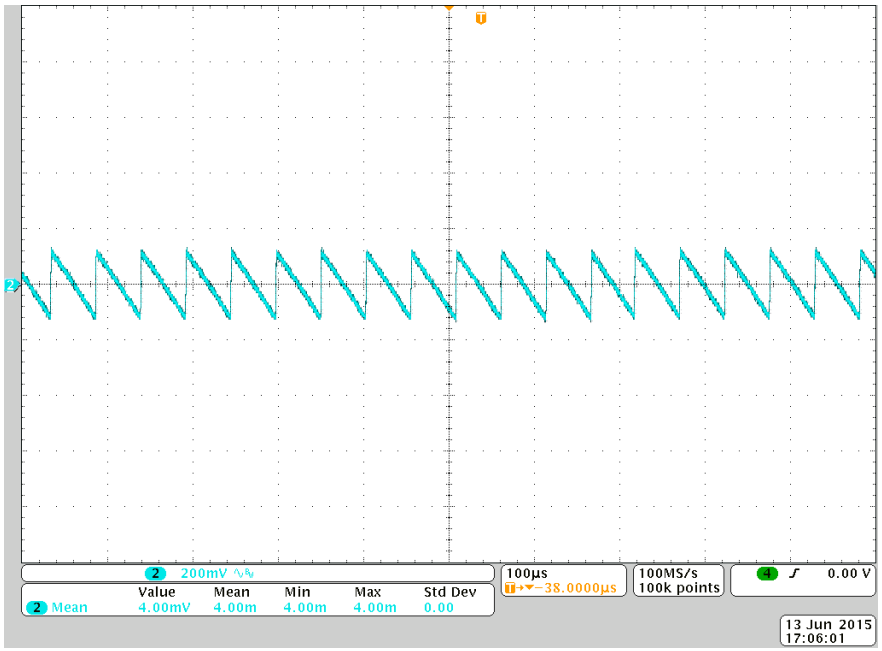


Figure 19. Ripple at GVDD Pin Voltage of DRV8303

Peak-to-peak ripple voltage on GVDD is around 240 mV.

Figure 20 shows the voltage output at the DVDD pin of the DRV8303 and the ripple in DVDD rail is shown in Figure 21.

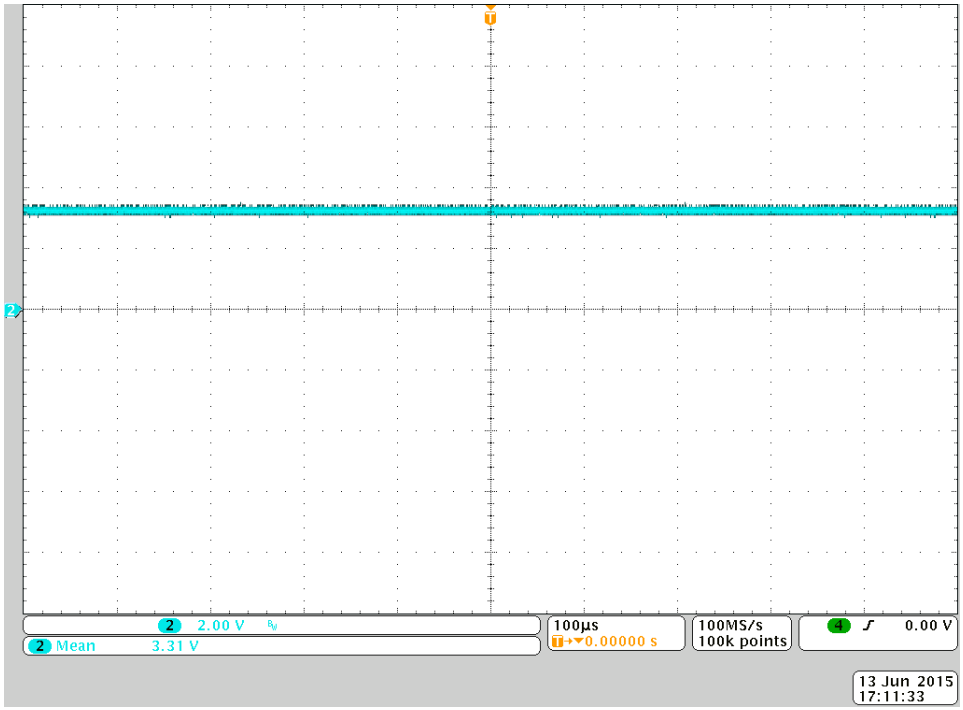


Figure 20. Voltage at DVDD Pin of DRV8303

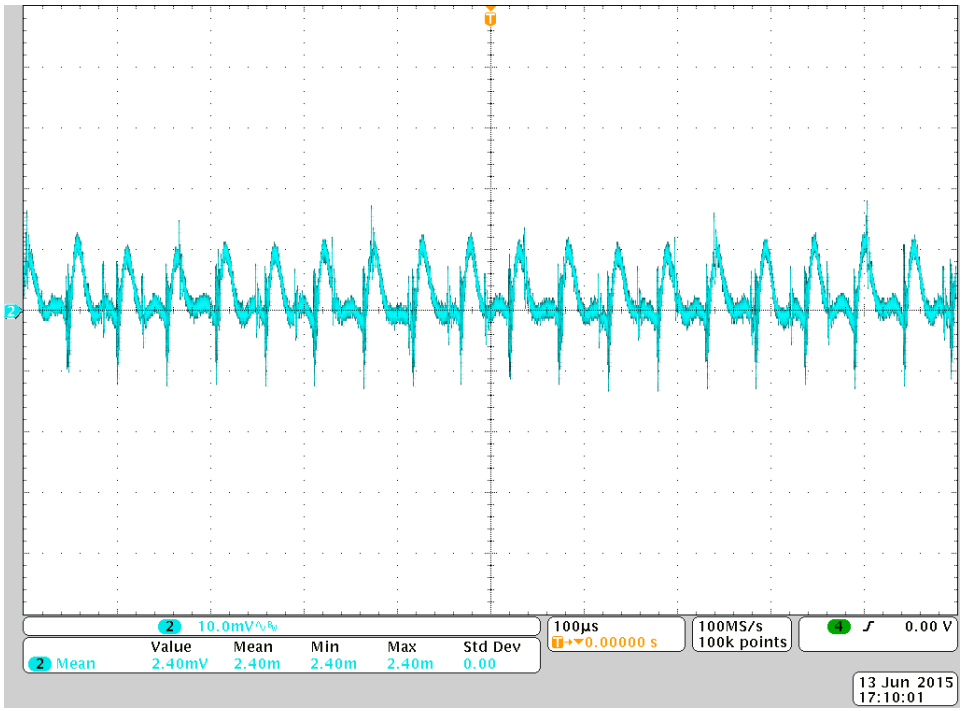


Figure 21. Ripple at DVDD Pin Voltage of DRV8303

Figure 22 shows the voltage output at the AVDD pin of the DRV8303, and Figure 23 shows the ripple in AVDD voltage rail. The mean voltage available at the AVDD pin is 6.64 V.

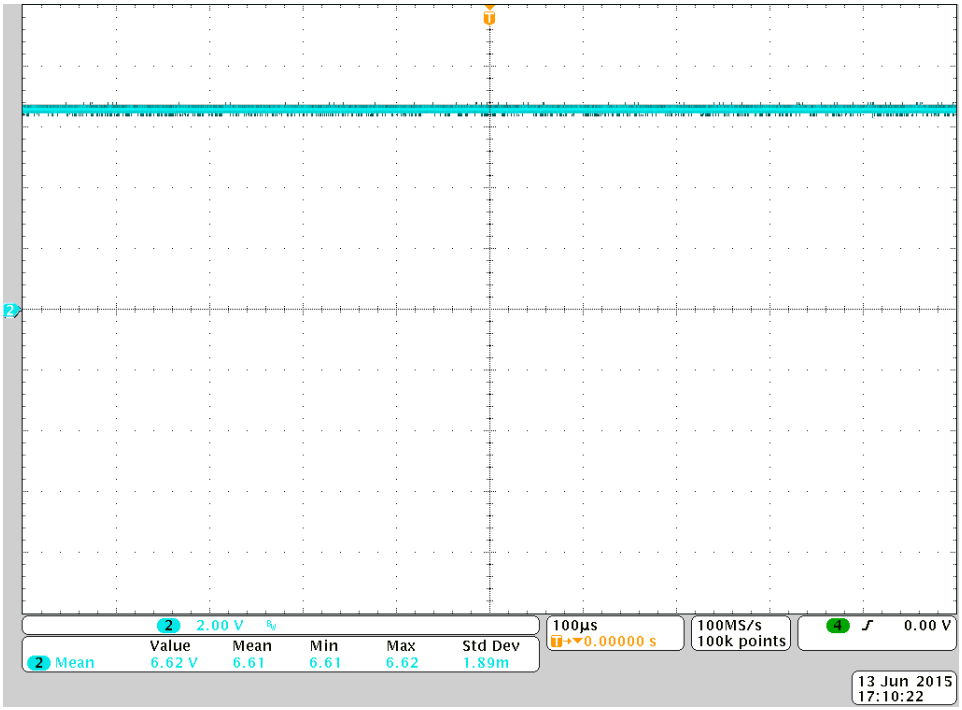


Figure 22. Voltage at AVDD Pin of DRV8303

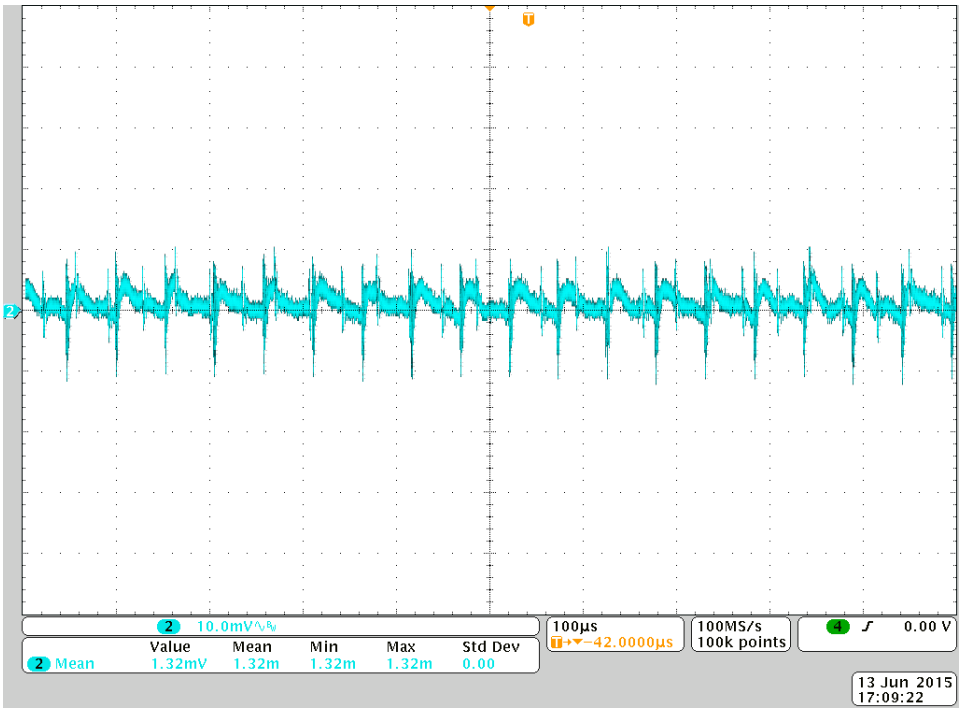


Figure 23. Ripple at AVDD Pin Voltage of DRV8303

The PWM signals are generated from the MSP430 controller is fed to the DRV8303 gate driver. A switching frequency of 20 kHz is used in the control unit inverter. Figure 24 shows the gate-to-ground voltage for one of the high-side MOSFET from the output of the DRV8303 and the corresponding input of the DRV8303 coming from the MCU.

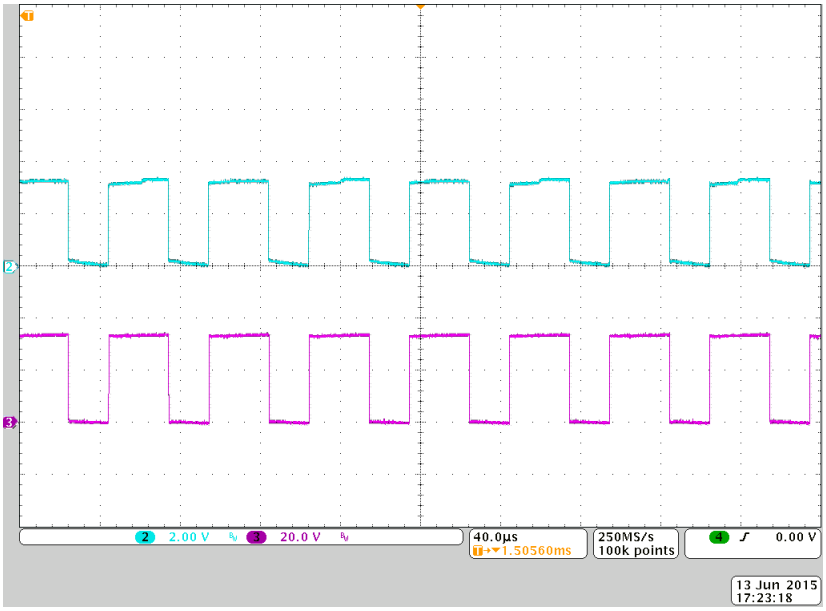


Figure 24. High-Side PWM Input and Output of DRV8303

Channel 2: PWM input to DRV8303; Channel 3: PWM output from DRV8303.

Figure 25 shows the two PWM gate signals from the DRV8303 for the upper and lower MOSFET of the same arm of the inverter. (Both the top-side and bottom-side waveforms are measured with the same ground reference.)

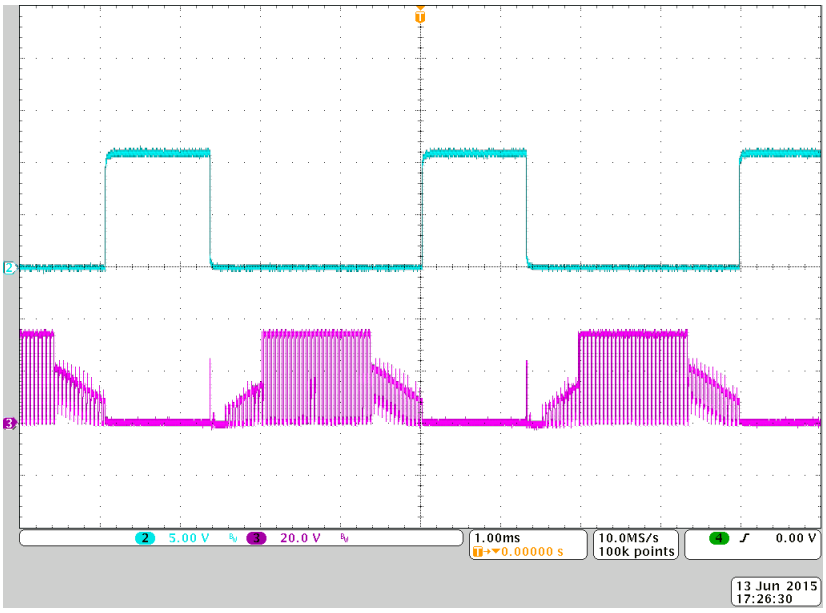


Figure 25. High-Side Gate-to-Ground versus Low-Side Gate-to-Source Signal From the DRV8303

Channel 2: Low-side gate-to-source signal of DRV8303; Channel 3: High-side gate-to-ground signal of DRV8303 on the same leg of the inverter.

Figure 26 shows the 3-phase BEMF voltage with single winding current at PWM duty of 50%. Figure 28 shows the motor line to line voltage filtered by the oscilloscope.

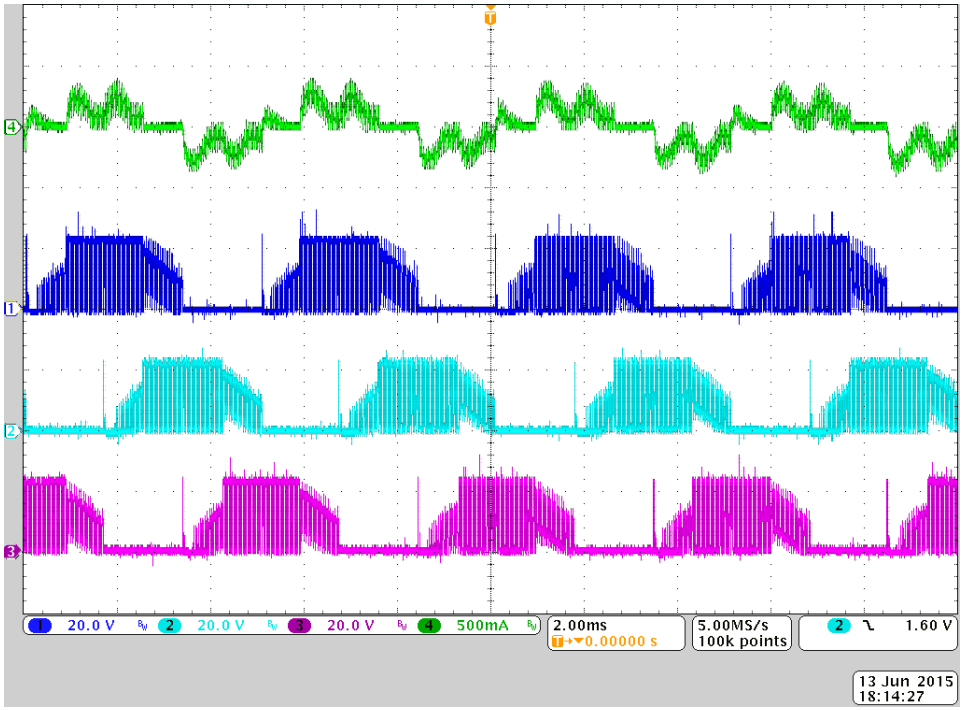


Figure 26. 3-Phase BEMF Voltage With Single Winding Current at PWM Duty of 50%

Channel 1: Winding A voltage with respect to negative DC bus; Channel 2: Winding B voltage with respect to negative DC bus; Channel 3: Winding C voltage with respect to negative DC bus; Channel 4: Winding A current.

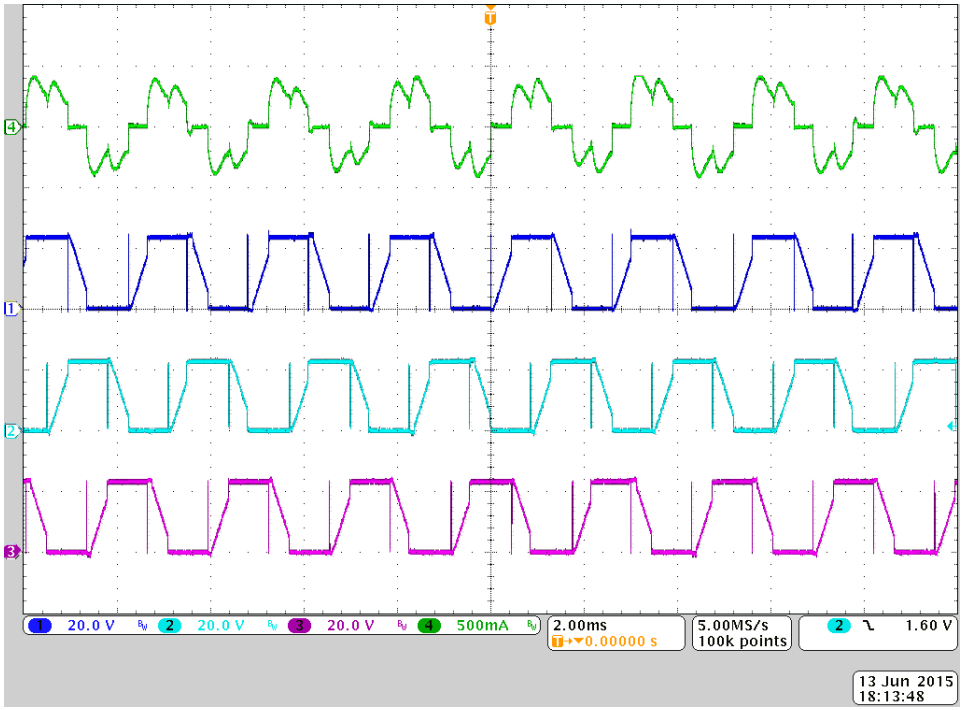


Figure 27. 3-Phase BEMF Voltage With Single Winding Current at PWM Duty of 100%

Channel 1: Winding A voltage with respect to negative DC bus; Channel 2: Winding B voltage with respect to negative DC bus; Channel 3: Winding C voltage with respect to negative DC bus; Channel 4: Winding A current.

Figure 28. MCU Output Signals to DRV8303 on the Same Leg of Inverter Circuit

Channel 2: Switching signal from MCU to DRV8303; Channel 3: PWM signal from MCU to DRV8303 on the same leg.

Testing the Drain Pump Motor Drive

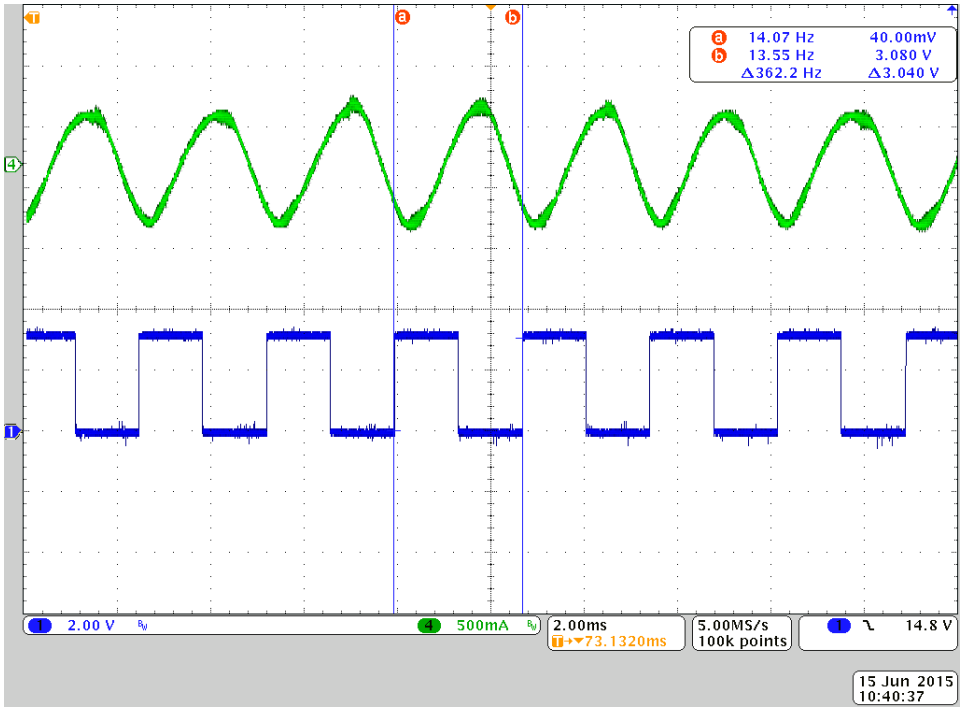


Figure 29. DRV10983 Speed Signal versus FG When FGcycle == 0x00

Channel 1: FG signal from DRV10983; Channel 3: Winding current.

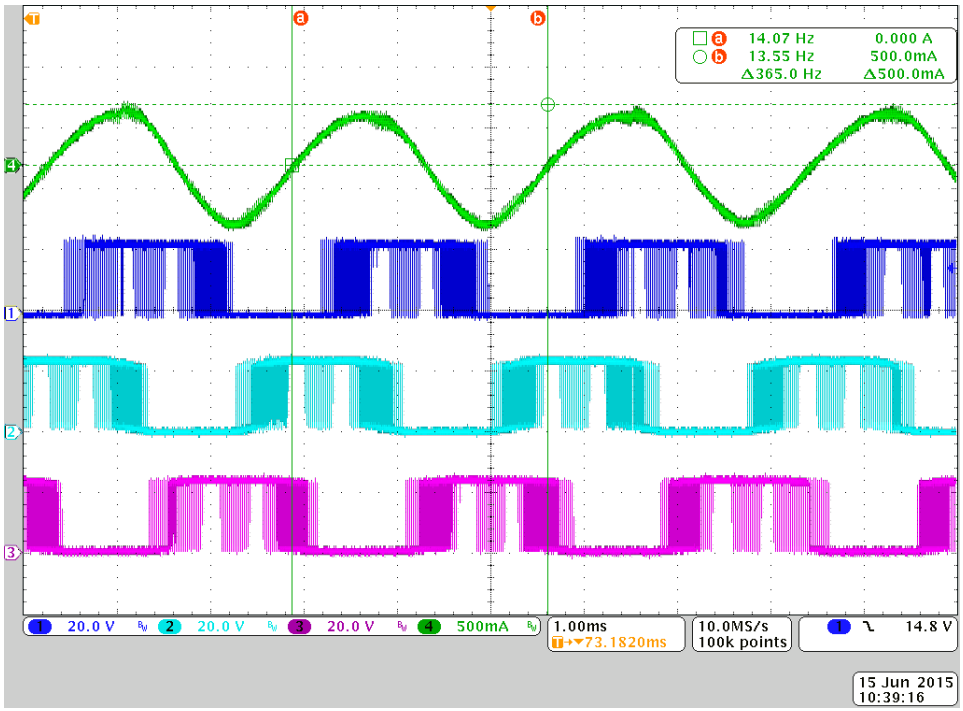


Figure 30. DRV10983 Single Winding Voltage versus Current

Channel 1: Winding A voltage with respect to negative DC bus; Channel 2: Winding B voltage with respect to negative DC bus; Channel 3: Winding C voltage with respect to negative DC bus; Channel 4: Winding A current.

8.2 Load Tests

The load test is done to determine the thermal characteristics and the current handling capability of the power stage. Figure 31 shows the block diagram of the test setup used for load testing.

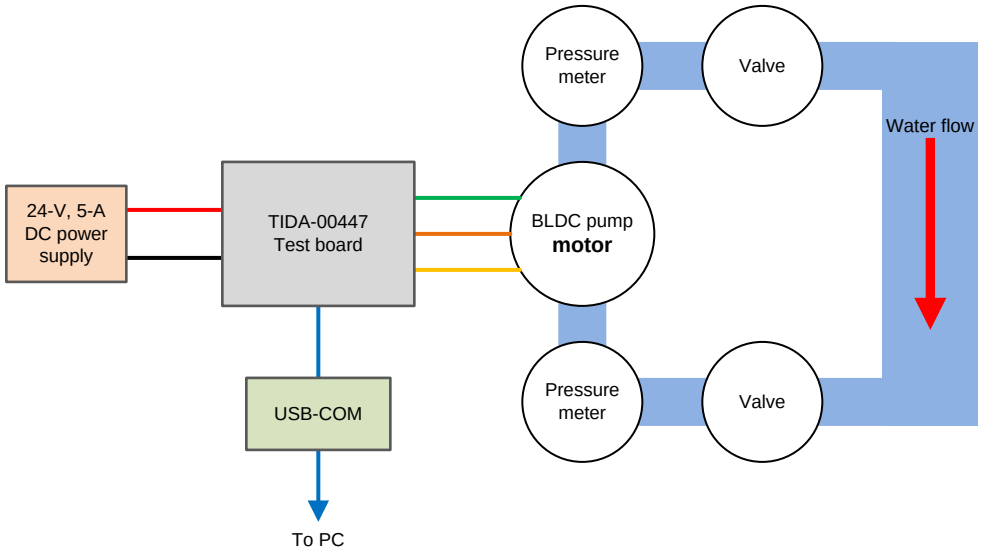


Figure 31. Block Diagram of Load Test Setup (Illustrated)

Simple-pump test equipment is used to perform the load test of the system. Figure 32 shows the test equipment built for the design. The system consists of a water tank, flow meter, pressure meter, and two valves.

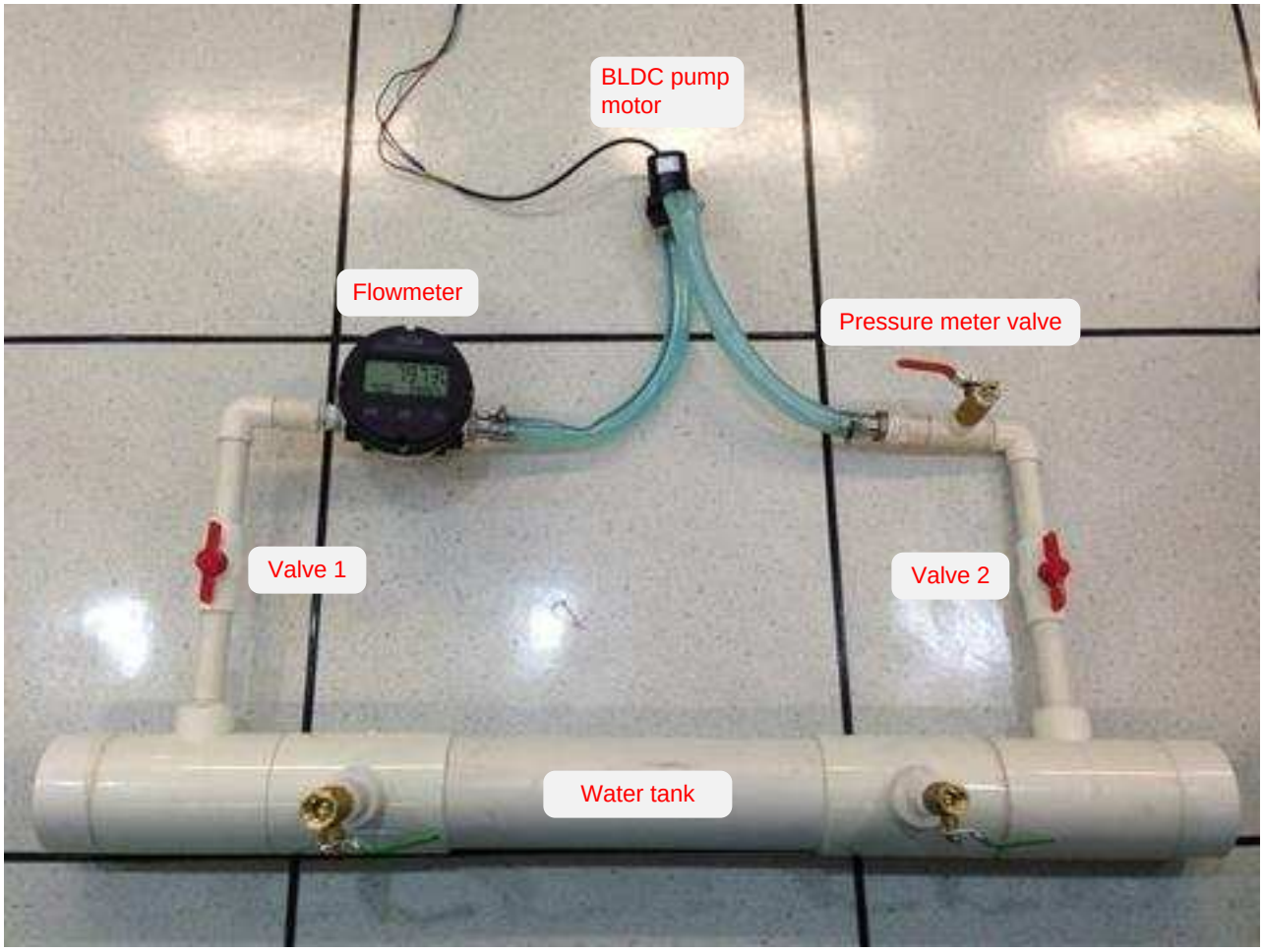


Figure 32. Block Diagram of Load Test Setup (Photo)

The motor under test is connected to the test equipment. A 2400-RPM/86.4-W (rated) motor is used for testing. The loading on the brushless motor is done by circulating the water in the test system. Water pressure of the system can be adjusted by closing or opening valve 1 and valve 2. The load testing was done by running the motor at a constant speed, the firmware on the MSP430 is running at velocity mode, which is a closed loop speed control. During testing, the speed of the 8-pole BLDC motor varied from 0 to 2400 RPM using the GUI. The measured values are motor speed, RMS and peak value of the motor winding current, pressure in the water passage, DC link voltage, and DC link current. The board temperature was measured using a thermal imager.

The main (circulation) pump and secondary (drain) pump are tested by the test equipment separately. The same pump motor load is used to test both drives in the board. Figure 33 shows the connection between the motor under test and the test board.

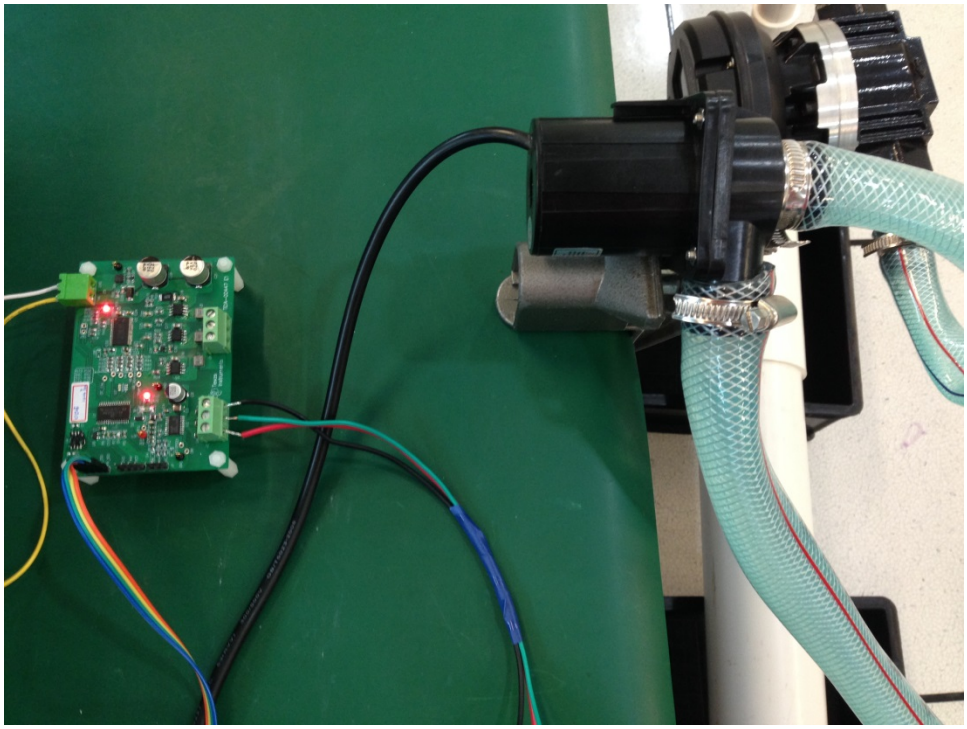


Figure 33. Assembled Control Board With Test System

8.2.1 Speed Control

Figure 34 shows the winding current of the motor driven by the DRV10983 at 2400 RPM and the winding voltage measured with respect to the negative DC bus.

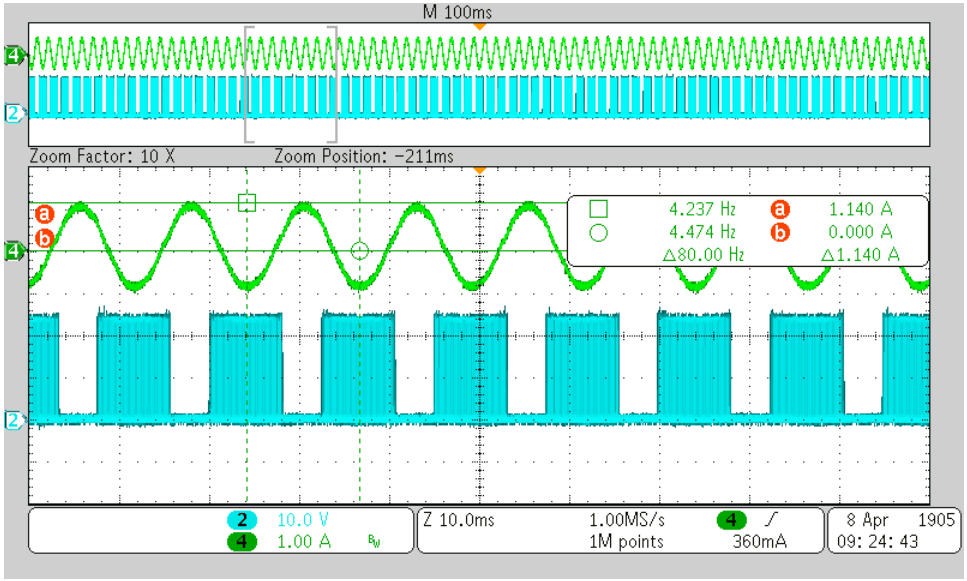


Figure 34. Load Test of DRV10983—Winding Current and Winding Voltage Measured With Respect to Negative DC Bus

Channel 2: Winding voltage measured with respect to negative DC bus; Channel 4: Winding current.

The duty cycle of the control PWM input to the DRV10983 against motor speed is shown in Figure 35:

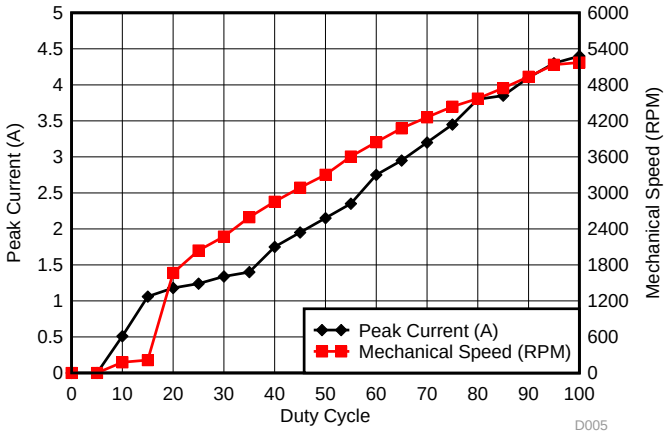


Figure 35. Speed Signal Duty versus Motor Speed

Figure 36 shows the winding current of the motor driven by the DRV8303 at 2400 RPM and the winding voltages measured with respect to the negative DC bus.

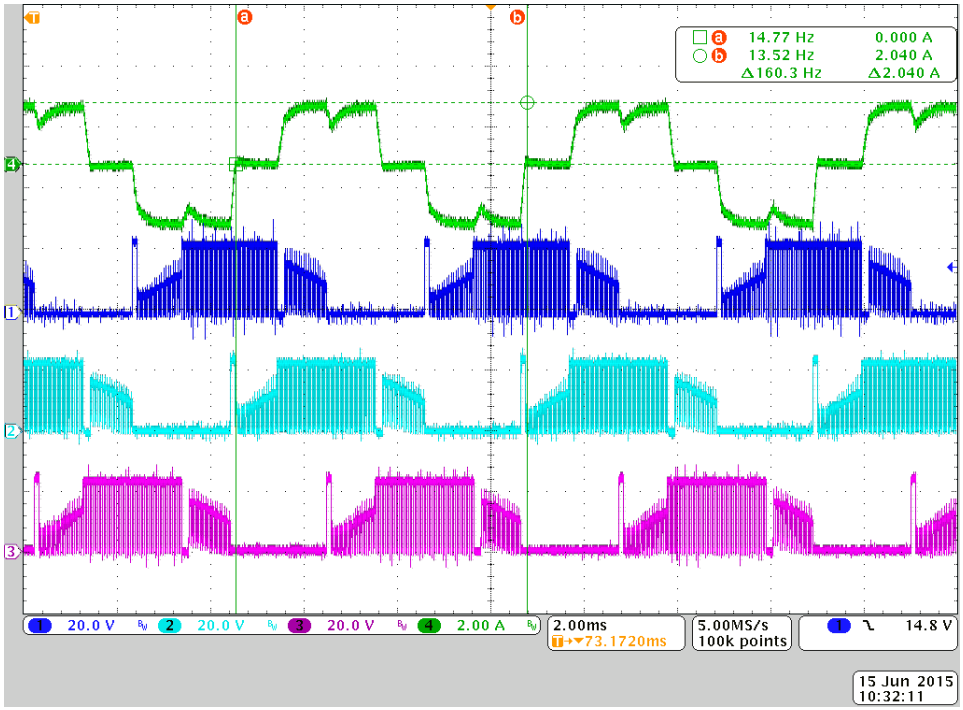


Figure 36. Phase Current Against 3-Phase Voltage With Load on DRV8303

Channel 1: Winding A voltage with respect to negative DC bus; Channel 2: Winding B voltage with respect to negative DC bus; Channel 3: Winding C voltage with respect to negative DC bus; Channel 4: Winding A current.

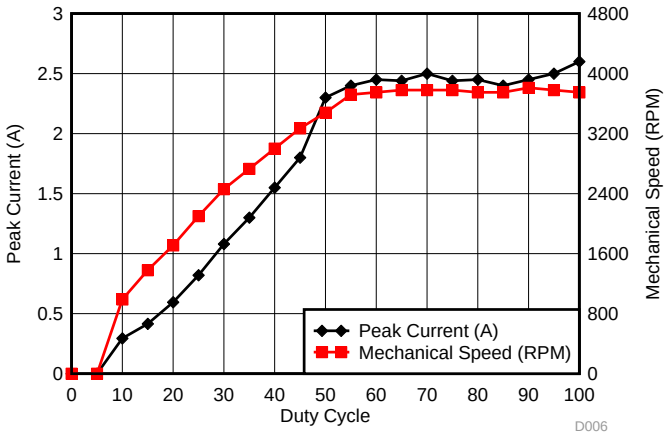


Figure 37. Duty Cycle Control versus Motor Speed

8.2.2 Thermal Condition Test

The TIDA-00447 board is supposed to operate in an open frame condition with no forced air flow so that the following test results are generated in a lab condition at an ambient temperature of 25°C without air flow.

Figure 38 shows a thermal image of the PCB assembly when the main (circulation) pump is running at its maximum output when V_{DC} = 24 V.

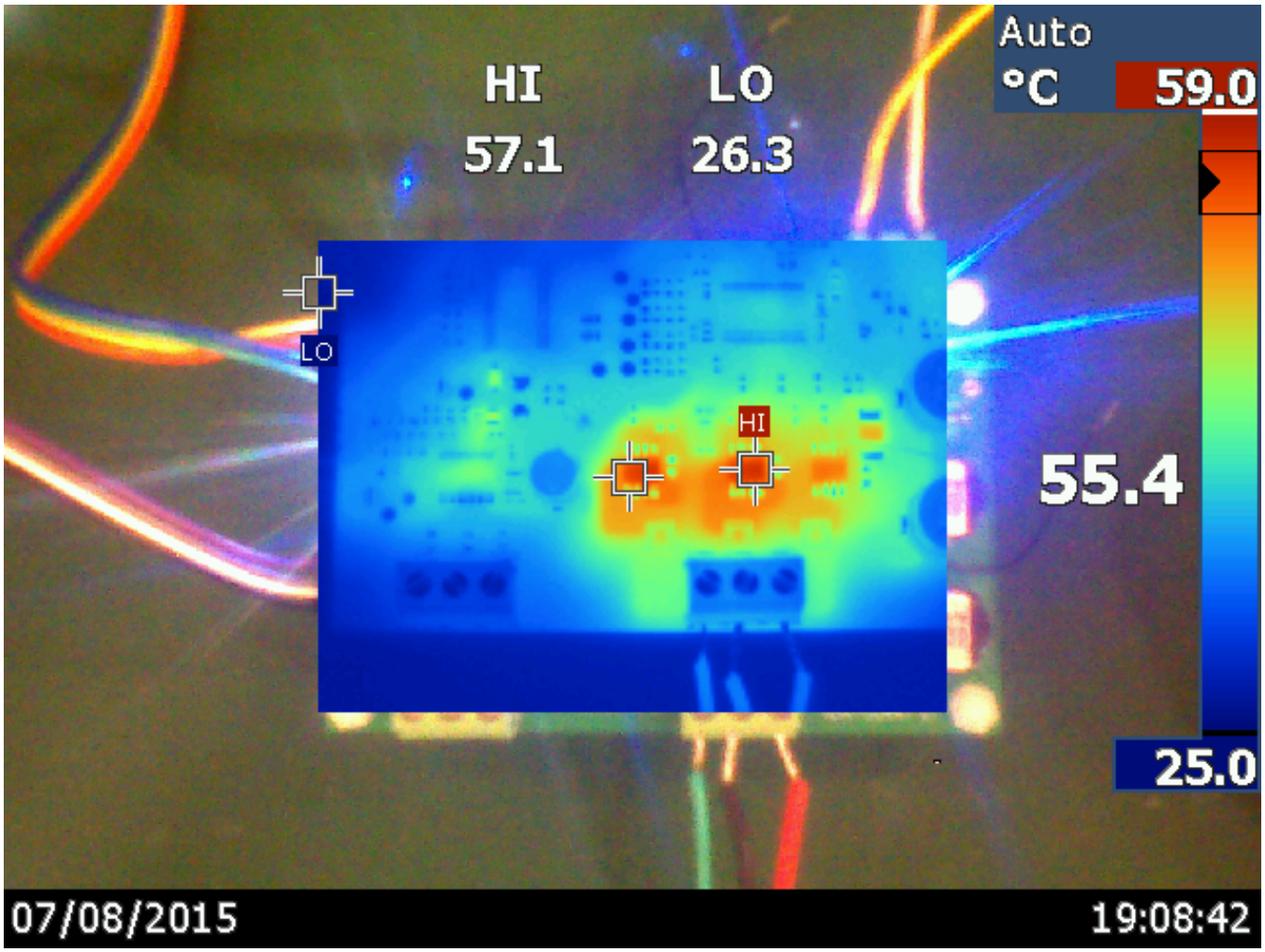


Figure 38. Load Test at 24 V—Thermal Image of Board at Winding Current of 4.7 A_{PEAK}

Table 6. Load Test Results at Input Voltage of 24 V and Winding Current of 4.7 A_{PEAK}

DC CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR ELECTRICAL FREQUENCY (Hz)	MECHANICAL SPEED (RPM)	TOP CASE TEMPERATURE OF DRV8303 (°C)	TOP CASE TEMPERATURE OF CSD88539ND (°C)
4	4.7	175	5250	41.1	57.1

Figure 39 shows a thermal image of the PCB assembly when the secondary (drain) pump is running at its rated output power of 30 W (1.77 A_{PEAK}) when V_{DC} = 24 V.

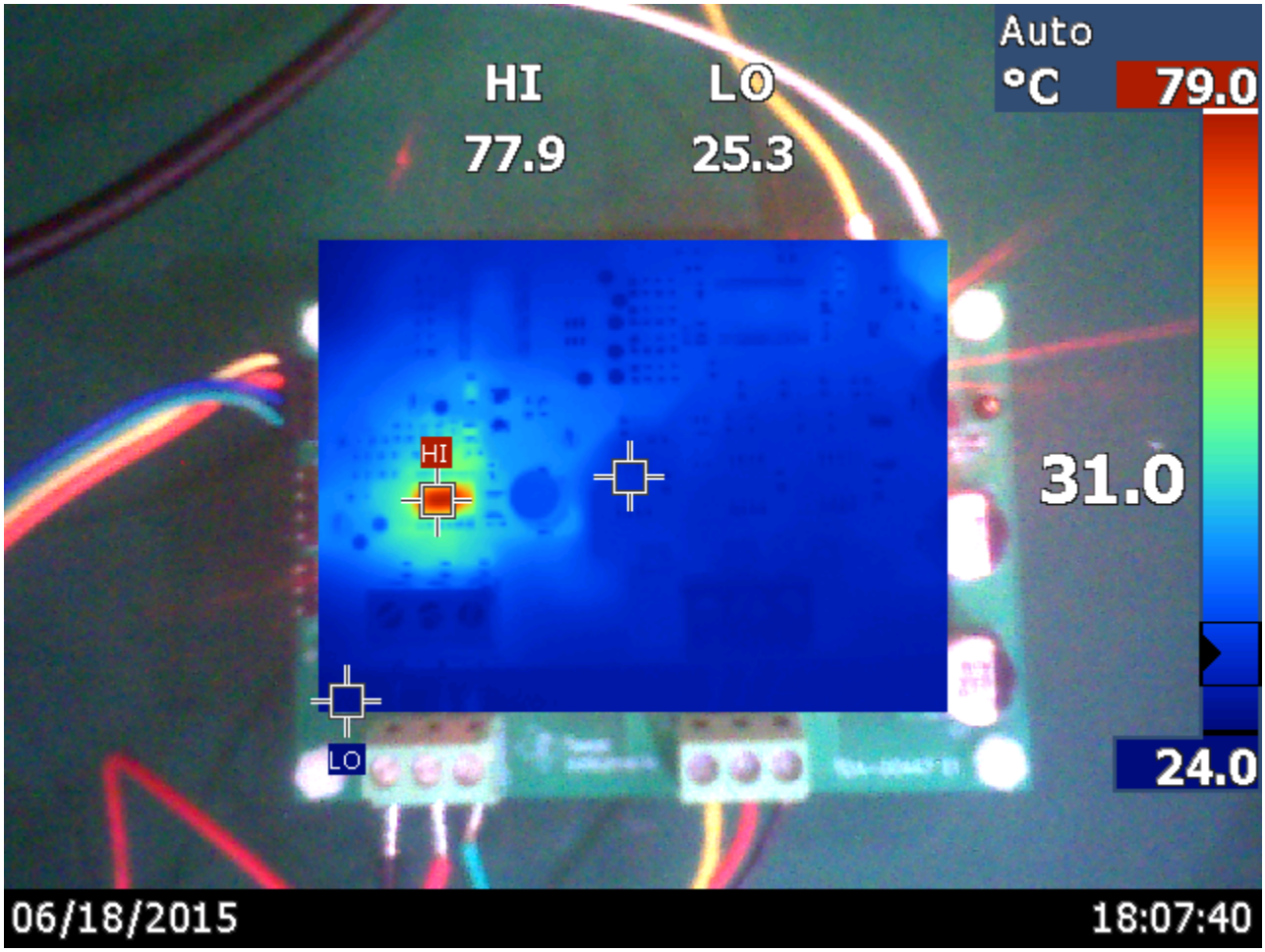


Figure 39. Load Test at 24 V—Thermal Image of Board at Winding Current of 1.77 A_{PEAK}

Table 7. Load Test Results at Input Voltage of 24 V and Winding Current of 1.77 A_{PEAK}

DC CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR ELECTRICAL FREQUENCY (Hz)	MECHANICAL SPEED (RPM)	TOP CASE TEMPERATURE OF DRV10983 (°C)
0.729	1.77	109	3270	77.9

Figure 40 shows the variation of the maximum temperature observed on the devices with the peak winding current when the main pump is driven.

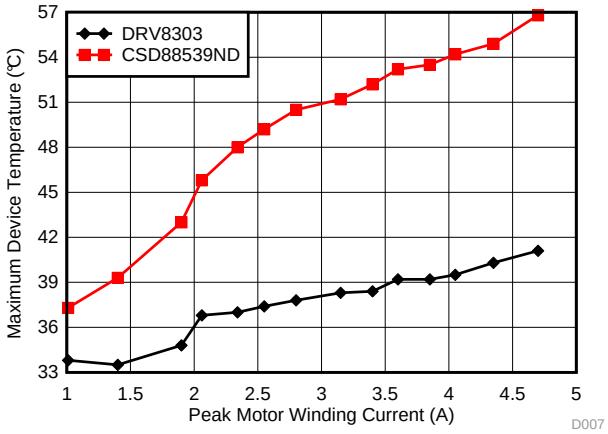


Figure 40. Peak Winding Current versus Maximum Temperature Observed on DRV8303 and CSD88539ND

Figure 41 shows the variation of the maximum temperature observed on the DRV10983 with the peak winding current when the second pump is driven.

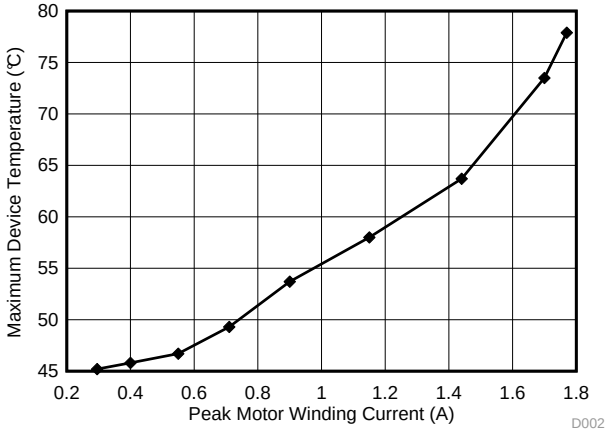


Figure 41. Peak Winding Current versus Maximum Temperature Observed on DRV10983

The complete load test result of the main pump driven by DRV8303 + CSD88539ND at 24 V is given in Table 8. The load test result of the second pump driven by the DRV10983 is tabulated in Table 9.

Table 8. Load Test Results at Input Voltage of 24-V DC for DRV8303 and CSD88539ND

DC CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR ELECTRICAL FREQUENCY (Hz)	MECHANICAL SPEED (RPM)	TOP CASE TEMPERATURE OF DRV8303 (°C)	TOP CASE TEMPERATURE OF CSD88539ND (°C)
0.44	1.01	82.24	2467	33.8	37.3
0.82	1.40	103.00	3090	33.5	39.3
1.36	1.90	122.00	3660	34.8	43.0
1.64	2.06	129.50	3885	36.8	45.8
1.88	2.34	137.40	4122	37.0	48.0
2.16	2.55	143.70	4311	37.4	49.2
2.40	2.80	151.50	4545	37.8	50.5
2.68	3.15	158.20	4746	38.3	51.2
3.00	3.40	165.60	4968	38.4	52.2
3.30	3.60	171.20	5136	39.2	53.2
3.40	3.85	177.30	5319	39.2	53.5
3.50	4.05	182.50	5475	39.5	54.2
3.70	4.35	188.00	5640	40.3	54.9
4.00	4.70	175.00	5250	41.1	56.8

Table 9. Load Test Results at Input Voltage of 24-V DC for DRV10983

DC CURRENT (A)	PEAK WINDING CURRENT (A)	MOTOR ELECTRICAL FREQUENCY (Hz)	MECHANICAL SPEED (RPM)	TOP CASE TEMPERATURE OF DRV10983 (°C)
0.152	0.295	33	990	45.2
0.164	0.400	46	1380	45.8
0.200	0.550	57	1710	46.7
0.243	0.710	70	2100	49.3
0.325	0.900	82	2460	53.7
0.428	1.150	91	2730	58.0
0.553	1.440	100	3000	63.7
0.729	1.700	109	3270	73.5
0.800	1.770	112	3360	77.9

8.3 Overcurrent Protection Test

The DRV8303 implements an overcurrent protection using the MOSFET V_{DS} sensing. The overcurrent condition is tested by a simple pump test equipment with the motor loaded. The overcurrent protection feature can be tested and monitored at different settings.

On detecting overcurrent, the DRV8303 pulls the $\overline{\text{OCTW}}$ pin low (with OCTW_SET == 0x0, 0x02 or 0x03). If the DRV8303 is set up to latch mode (OC_MODE == 0x01) on an overcurrent event, it will disable all the gate drive outputs until the DRV8303 is reset. In current limiting mode, the DRV8303 will release the pin from low state in the next PWM toggle or for a period of 64 µs.

The on-state V_{DS} of the MOSFET can be calculated by multiplying the drain current by the on-state resistance ($R_{DS(ON)}$) of the MOSFET. The $R_{DS(ON)}$ of the MOSFET is specified in the datasheet, and with CSD88539ND V_{DS} = 10 V, the $R_{DS(ON)}$ is 23 mΩ (typ.).

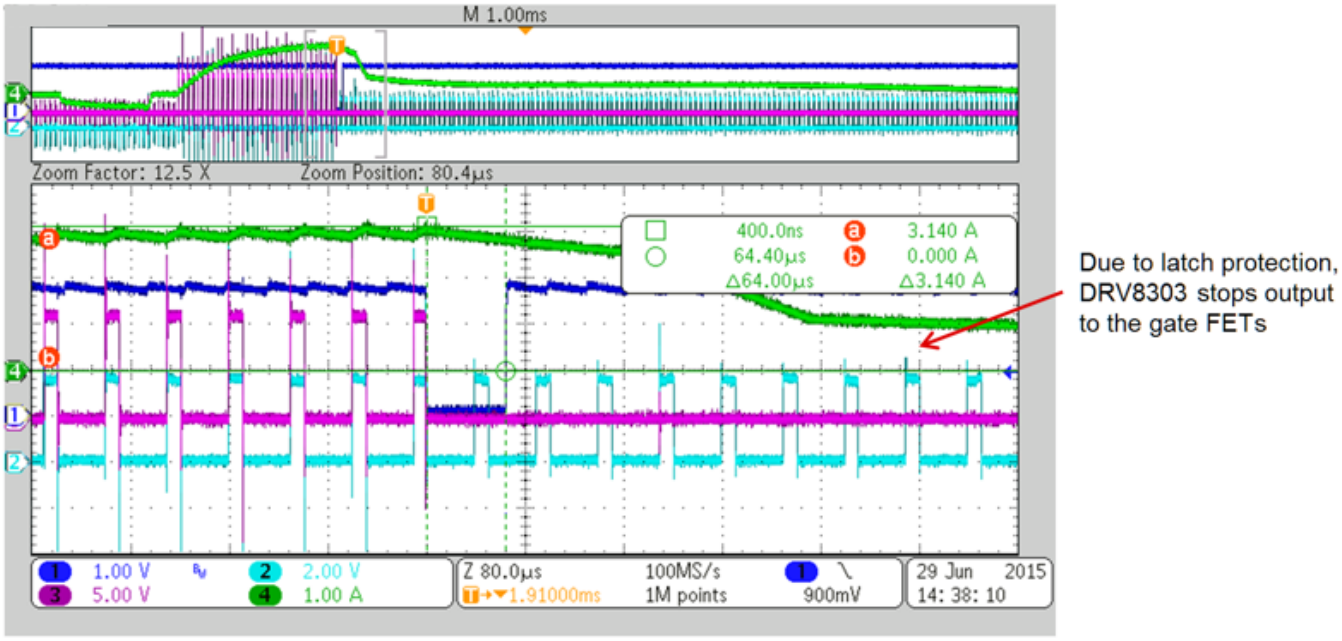


Figure 42. Overcurrent Protection Response by DRV8303 in Latch Mode

Channel 1: nOCTW; Channel 2: PWM output from MSP430; Channel 3: Gate driver signal from DRV8303; Channel 4: Winding current A.

For test purpose, the threshold value for V_{DS} sensing is set to 0.086 V (OC_ADJ_SET = 0x03). The $R_{DS(ON)}$ of the MOSFET specified in the datasheet is 23 mΩ at 25°C. The maximum value of $R_{DS(ON)}$ is 28 mΩ. The temperature of the MOSFET will cause increase in $R_{DS(ON)}$. The $R_{DS(ON)}$ of 28 mΩ corresponds to an overcurrent limit of 3.07 A (0.086 / 0.028 = 3.07). The signals monitored on the oscilloscope are $\overline{\text{OCTW}}$ from the DRV8303, and the high-side gate output signal from the DRV8303 and the MOSFET current.

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00447.

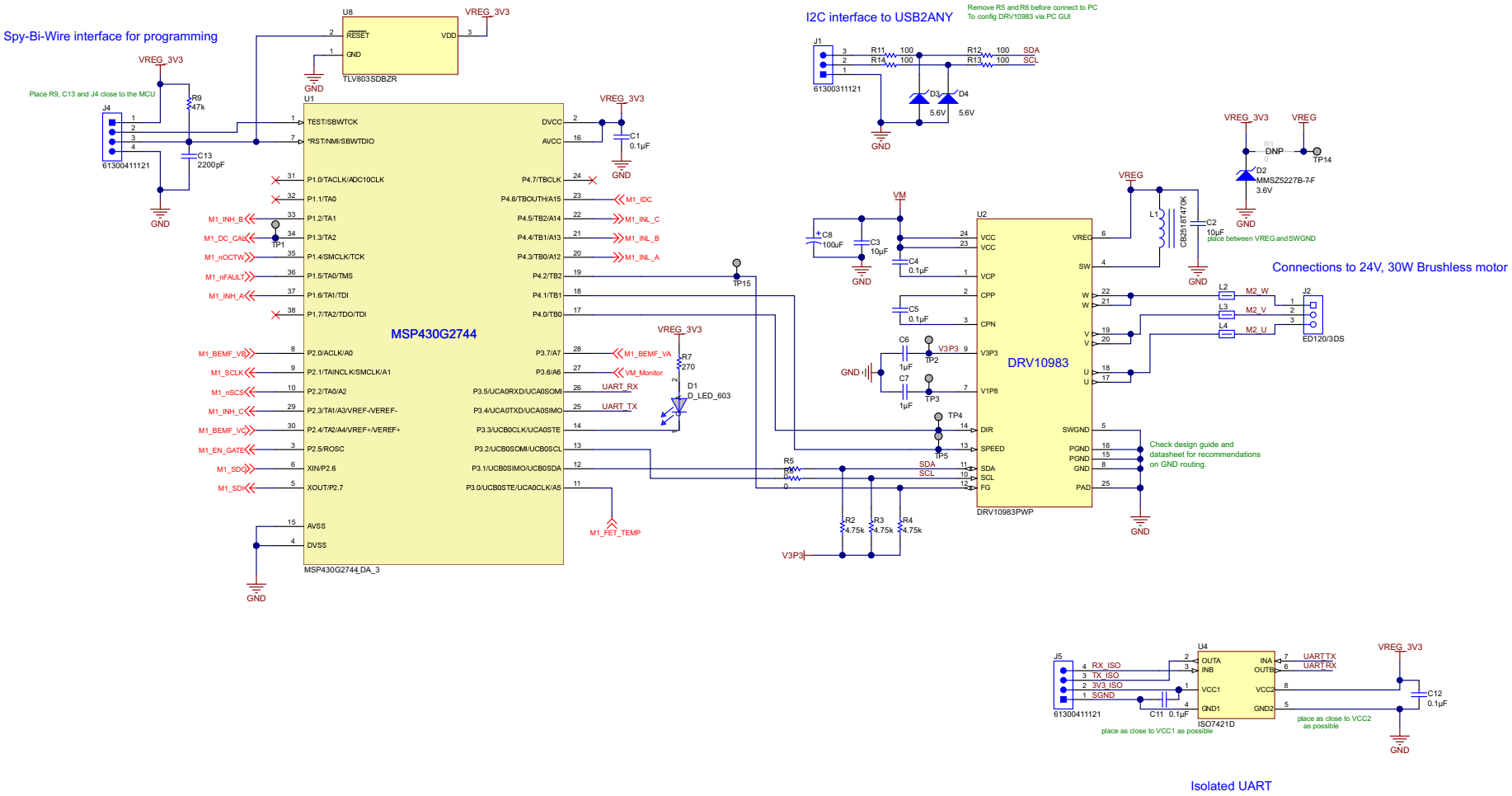


Figure 43. MCU + DRV10983 Schematic

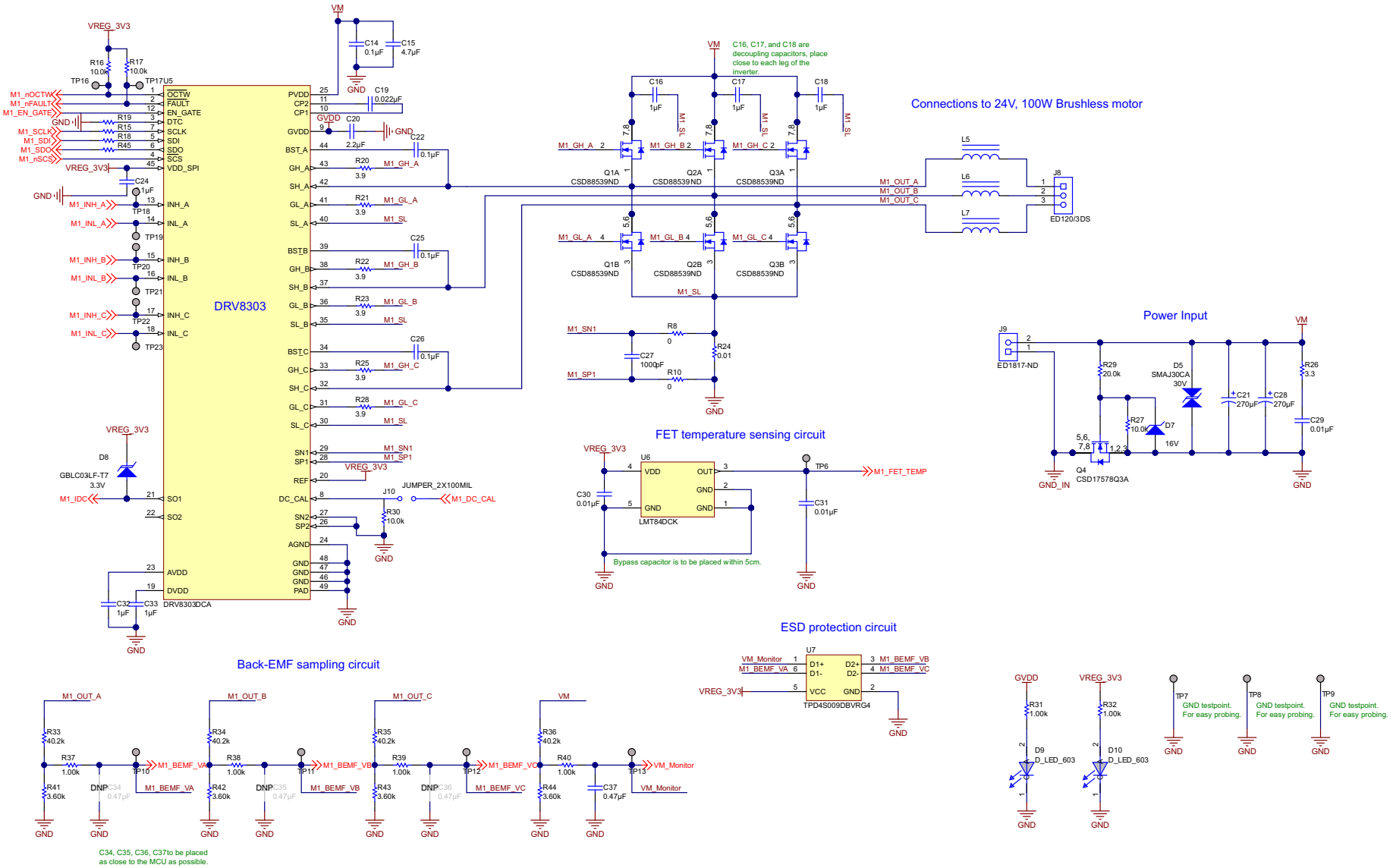


Figure 44. DRV8303 Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00447.

9.3 PCB Layout Recommendations

PCB Layout Recommendation for DRV10983

Consider the following points during the PCB layout design and PCB assembly:

1. The DRV10983 is provided with a thermally-efficient HTSSOP, 24-pin package with an exposed thermal pad. Be sure to connect the thermal pad of the DRV10983 properly to the PCB during soldering or assembly to achieve best thermal condition.
2. Keep the thermal pad connection area as large as possible, both on the bottom side and top side of the PCB. It should be one piece of copper without any cuts or gaps.
3. Place decoupling capacitors C3, C6, C7 close to their corresponding pins with a low impedance path to the device GND.
4. Place charge pump capacitors C4 and C5 as close to its corresponding pins as possible.
5. Apply the bulk capacitor (C8) to the power supply (VCC) of the device as well to supply the current ripple.
6. L2, L3, and L4 are applied to enhance EMI performance and to improve the hardware overcurrent detection. They are not mandatory.

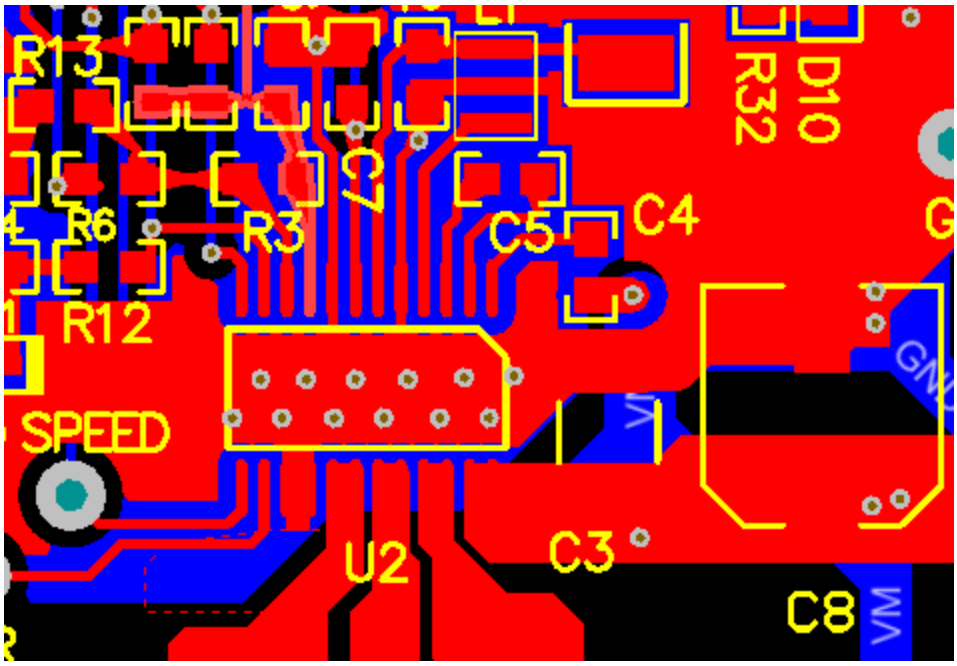


Figure 45. Layout Consideration for DRV10983

PCB Layout Recommendation for DRV8303 and CSD88539ND

Consider the following points during the PCB layout design and PCB assembly:

1. The DRV8303 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered (See PowerPAD application report [SLMA002]).
2. Place PVDD decoupling capacitors C14 and C15 close to their corresponding pins with a low impedance path to device GND (PowerPAD).
3. Place GVDD capacitor C20 close its corresponding pin with a low impedance path to device GND (PowerPAD). In this design and TIDA-00285, it is routed under the device itself to save space.
4. Place AVDD and DVDD capacitors C32 and C33 close to their corresponding pins with a low impedance path to the AGND pin. It is preferable to make this connection on the same layer.
5. Tie AGND to the device GND (PowerPAD) through a low impedance trace/copper fill.
6. Add stitching vias to reduce the impedance of the GND path from the top to bottom side. Make the vias larger to allow solder paste to avoid an unexpected short circuit between the PowerPAD and other pins when assembling the device.
   Refer to the TIDA-00285 design guide for more guidance on the layout design for the DRV8303.

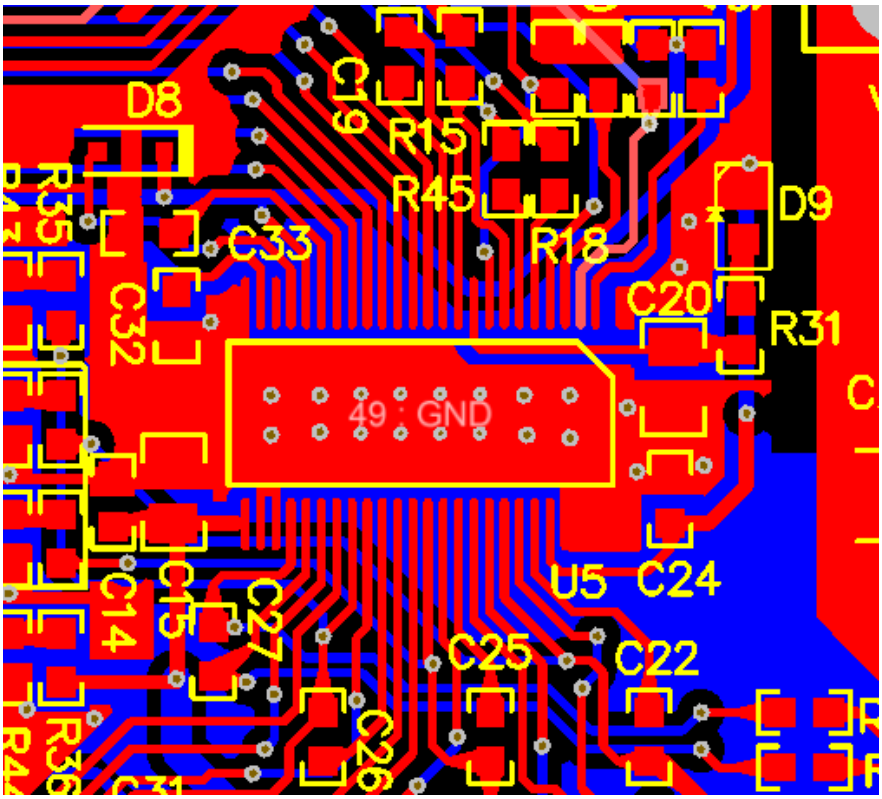


Figure 46. Layout Consideration for DRV8303

7. Make the motor current route as wide as possible with enough stitching vias applied to the bottom layer to help dissipate the heat generated by the CSD88539ND.
8. Create a wide route between pin 1 and pin 5 or pin 6 of the CSD88539ND because current will run through pin 1 (source) of the CSD88539ND.
9. Place decoupling capacitors C16, C17, and C18 as close to the device as possible with a short return path back to low side source of the circuit.
10. Enhance low side source (pin 3) connections. In this design, pin 3 of the CSD88539ND are connected to a large plain on the bottom layer through five stitching vias.

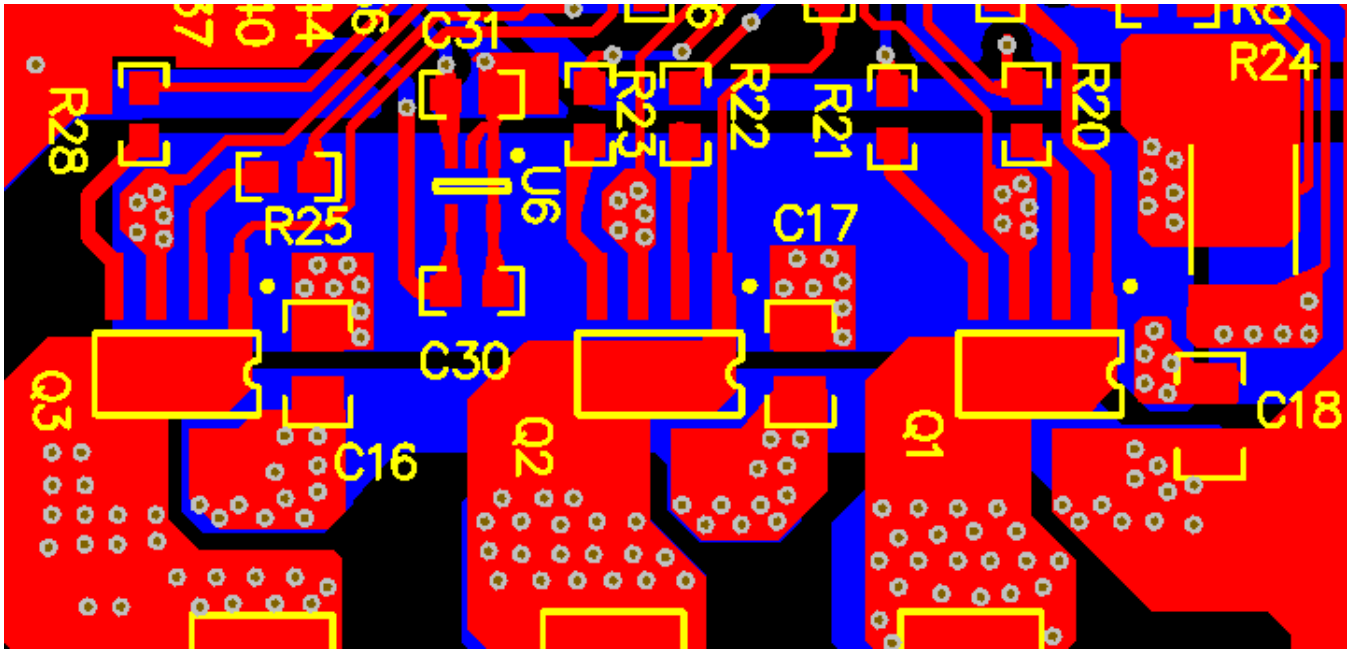


Figure 47. Layout Consideration for CSD88539ND

9.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00447.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00447.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00447.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00447.

10 References

1. Texas Instruments, *Three Phase Pre-driver with Dual Current Shunt Amplifiers*, DRV8303 Datasheet (SLOS846)
2. Texas Instruments, *DRV10983 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver*, DRV10983 Datasheet (SLVSCP6)
3. Texas Instruments, *CSD88539ND, Dual 60 V N-Channel NexFET™ Power MOSFETs*, CSD88539ND Datasheet (SLPS456)
4. Texas Instruments, *3-Pin Voltage Supervisors with Active-Low, Open-Drain Reset*, TLV803S Datasheet (SBVS157)
5. Texas Instruments, *LMT84/LMT84-Q1 1.5V, SC70/TO-92/TO-126 Analog Temperature Sensors with Class-AB Output*, LMT84 Datasheet (SNIS167)
6. Texas Instruments, *ISO742x Low-Power Dual-Channel Digital Isolators*, ISO7241D Datasheet (SLLS984)
7. Texas Instruments, *TPD4S009 4-Channel ESD Solution for High-Speed Differential Interface*, TPD4S009 Datasheet (SLVS817)
8. Texas Instruments, *Sensorless Trapezoidal Control of BLDC Motors* TMS320F2803x Application Report, (SPRABQ7)
9. Texas Instruments, *Programming Guide for the DRV10983*, DRV10983 Application Report (SLVUAA5)
10. Texas Instruments, *MSP430x2xx Family User's Guide*, MSP430G2744 User's Guide (SLAU144)
11. Texas Instruments, *MSP430G2x44 Mixed-Signal Microcontrollers*, MSP430G2744 Datasheet (SLAS892)
12. Texas Instruments, *Sensor-less 3-phase BLDC Drive*, TIDA-00274 Design Guide (TIDU439)
13. Texas Instruments, *DRV10983 and DRV10975 Evaluation Module*, DRV10983 and DRV10975 User's Guide (SLOU393)
14. Texas Instruments, *DRV10983 and DRV10975 Tuning Guide*, DRV10983 and DRV10975 User's Guide (SLOU395)
15. Texas Instruments, *Semiconductor and IC Package Thermal Metrics*, Application Report (SPRA953)
16. Texas Instruments, *The Effect of PCB Design on the Thermal Performance of SIMPLE SWITCHER® Power Modules*, Application Report (SNVA424)

11 Terminology

SPI— Serial peripheral interface

PWM— Pulse width modulation

BLDC— Brushless DC motor

PMSM— Permanent magnet synchronous motor

MCU— Microcontroller unit

FETs, MOSFETs—The metal–oxide–semiconductor field-effect transistor

ESD— Electrostatic discharge

TVS— Transient voltage suppressors

RPM— Rotation per minute

RMS— Root mean square

FOC— Field oriented control

12 About the Author

LEBO "RENTON" MA has joined TI's MCU SAE team in Shanghai and supported Hercules and the C2000 family since 2012. Renton came to TI from Renesas Electronics where he was a field application engineer and later a technical marketing for body applications in automotive market for MCUs for seven years. After joining the MCU SAE team, Renton designed firmware and core logic on modeling tools for automotive applications and residential air conditioning systems. He also leads the firmware architecture design and process management in some of the projects of SAE team. Renton has a bachelor's degree in electronic engineering and another in English from Dalian University of Technology.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (September 2015) to B Revision	Page
• Changed title	1

Revision A History

Changes from Original (June 2015) to A Revision	Page
• Changed from preview page	1

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