UCC24630 Secondary-Side Synchronous Rectifier Controller Diode Replacement Demonstration Board PMP11216

This test report demonstrates the efficiency improvements gained by synchronous rectification compared with diode rectification in 5V to 24V flyback output circuits. Results shown are for demonstration purposes only and thermal performance is not guaranteed. Maximum reverse blocking voltage, including spikes, must be less than 100V peak using the MOSFET specified. Higher voltage applications can be used if the MOSFET is replaced with a properly rated device. The illustration shown is for the existing diode anode connected to GND (refer to Figure 1). Use with any other diode connection arrangement would require a different IC bias arrangement.

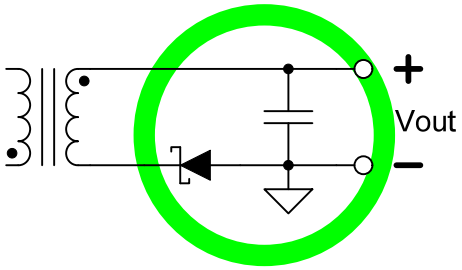

Figure 1. Diode that was replaced w located such that its anode is connected to GND; otherwise, additional circuitry would have been required.

To install the demonstration board on an existing design, the board was connected in parallel with the existing diode. This is recommended until proper SR timing is verified. Once correct SR operation is verified, the diode can be removed. Tthe VS pin of the board was connected to the anode pad of the host circuit, and the VD pin of the board was connected to the cathode pad of the host circuit. The VCC terminal was connected to the output, and the GND terminal was connected to the converter output ground with a short piece of wire. Connecting VCC and GND at a low noise connection, such as across a filter capacitor (refer to Figure 2) is recommended to reduce noise.

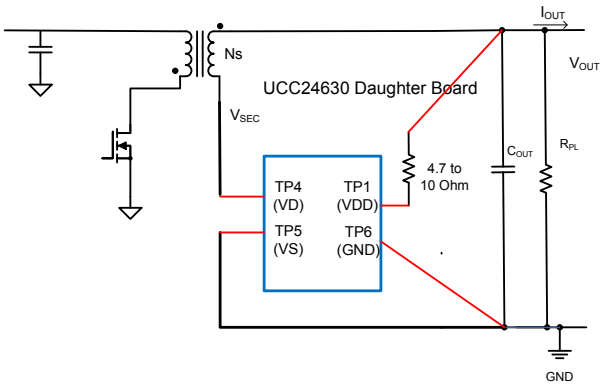

Figure 2. Demonstration card connection to existing circuit shown

PHOTO OF THE PROTOTYPE:

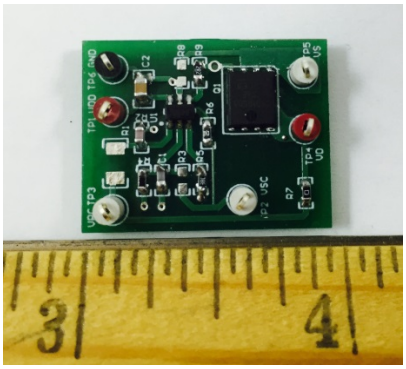

Figure 3. Front image of tested board

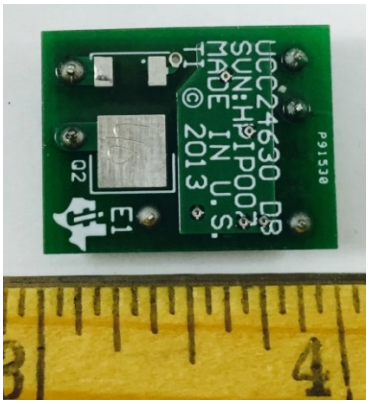

Figure 4. Back image of tested board

The reference design board allowed for an alternate D-Pak MOSFET package to be mounted on the back side to increase the thermal dissipation capability of the board for a higher-power applications. Forced airflow from a fan could also help extend the power level to be evaluated. The board was designed to test either the D-Pak (Q2) or SON package (Q1).

Detailed Component Selection

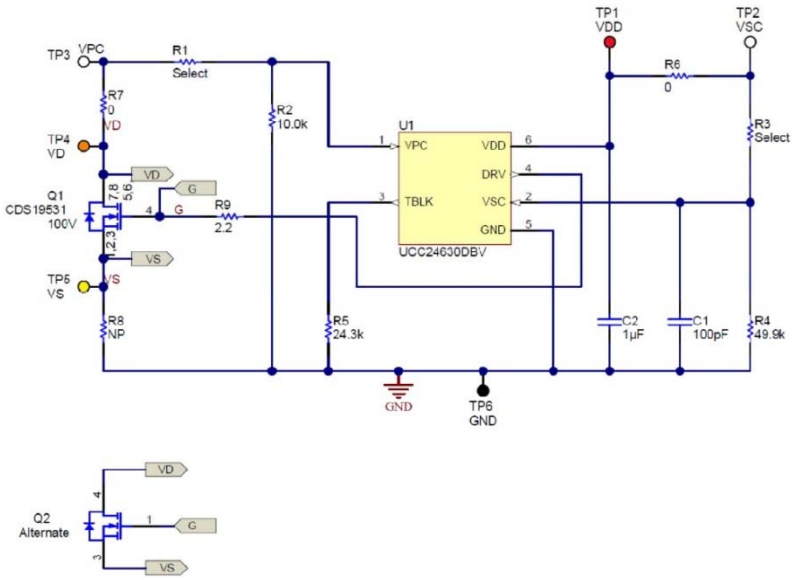

Figure 5 PMP11216 Schematic

The resistor dividers for the SR VDS sense and the Vout sense were determined for the application.
The resistor value of 24.3kΩ on the TBLK pin should be confirmed is correct for the application.
The SR Demonstration Board is pre-programmed for a VPC Blanking Time of 340ns with R5=24.3kΩ.
The blanking time was determined based on the converter minimum primary on time of 470ns.
The blanking time should be selected to be 120ns shorter than the minimum primary on time.

Determining the values for R1, R3, and R5 is a simple process.

Determine R1 value based on operating range of SR VDS voltage and Vout.

VPC divider: Calculate R1 Value. R2 is set at 10k Ohm.
*$V_{IN(min)}$ is bulk capacitor minimum
*$V_{OUT(min)}$) is output min operating voltage
*V_{VPC_EN} is 0.44V
*N_{PS} is transformer primary to secondary turns ratio.

$$R1 = \frac{\left[\left(\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right) - V_{VPC\_EN} \times 1.1\right] \times R2}{V_{VPC\_EN} \times 1.1}$$

Detailed Component Selection (continued)

VSC divider: Calculate R3 Value. R4 is set at 49.9K.

Calculated R3 value results in 10% margin SR on time for initial power up (early turn off).

*RatioVPC_VSC is 4.15

$$R3 = \left[\left(\frac{\frac{R1+R2}{R2}}{Ratio_{VPC\_VSC} \times 1.1} \right) - 1 \right] \times R4$$

TBLK resistor value: Confirm R5 value of 24.3K. Set tVPC_BLK to be ~100ns less than expected converter minimum primary on time.

$$R5 = \frac{t_{VPC-BLK} - 100ns}{18pF}$$

Use in CCM Operation

The UCC24630 SR controller is compatible with flyback converters operating in CCM with primary controllers that are fixed frequency at high load conditions. For the CCM dead time control reliable operation, the converter should be operating in fixed frequency mode at any line and load condition that results in CCM operation. Refer to typical primary controller control law below.

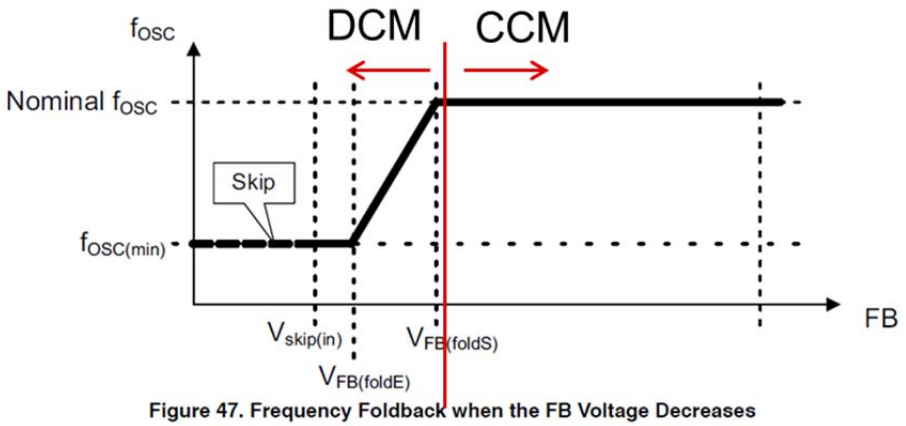

Figure 47. Frequency Foldback when the FB Voltage Decreases

Figure 6. Typical Fixed Frequency Controller Control Law

Efficiency Improvement: SR Compared to Diode Rectifier: 20V/65W

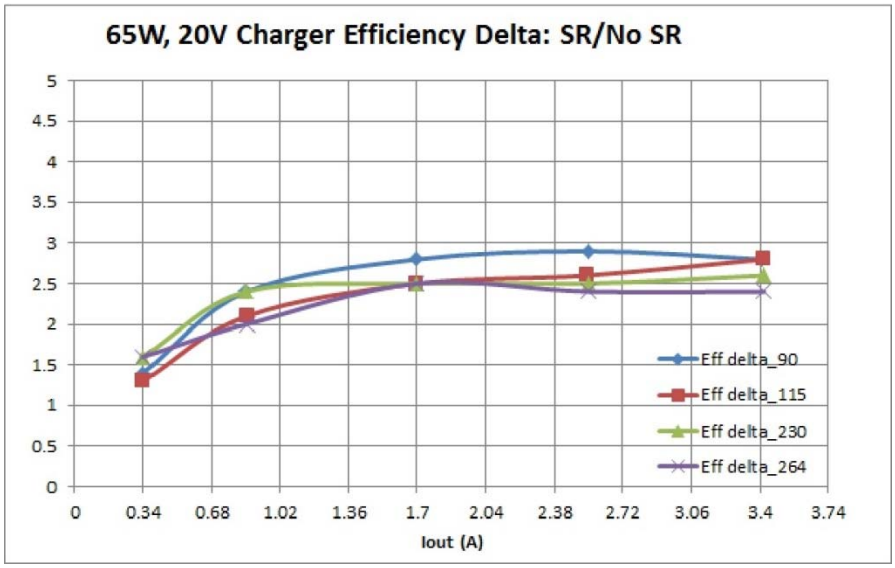

Figure 7. Efficiency improvement with SR over line and 10% to 100% load.

PMP11216 SR Daughter card with CSD19531 MOSFET Vs SSP5P10, schottky rectifier diode.

Efficiency Improvement: SR Compared to Diode Rectifier: 5V/15W

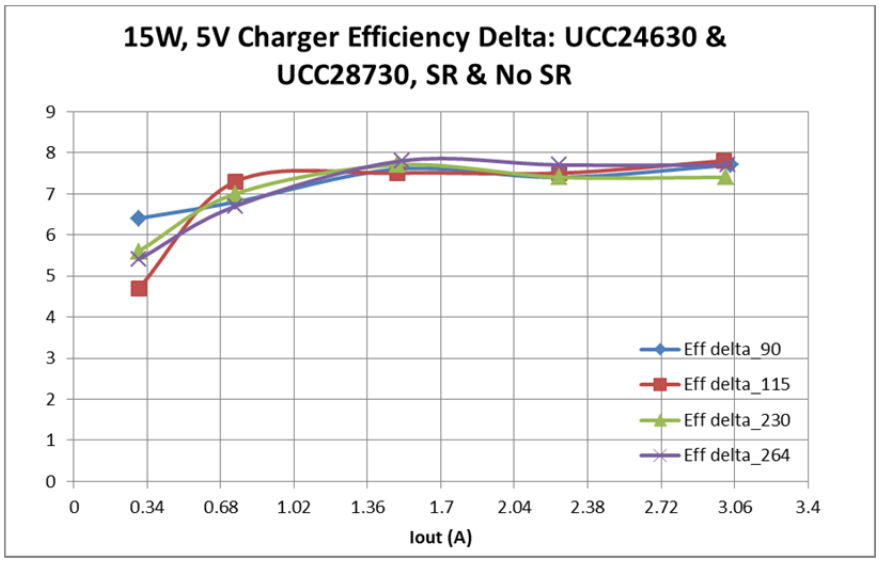

Figure 8. Efficiency improvement with SR over line and 10% to 100% load.

PMP11216 SR Daughter card with CSD18503 MOSFET Vs B540C-13 schottky rectifier diode.

Typical SR Timing in 20V/65W Converter at Full Load

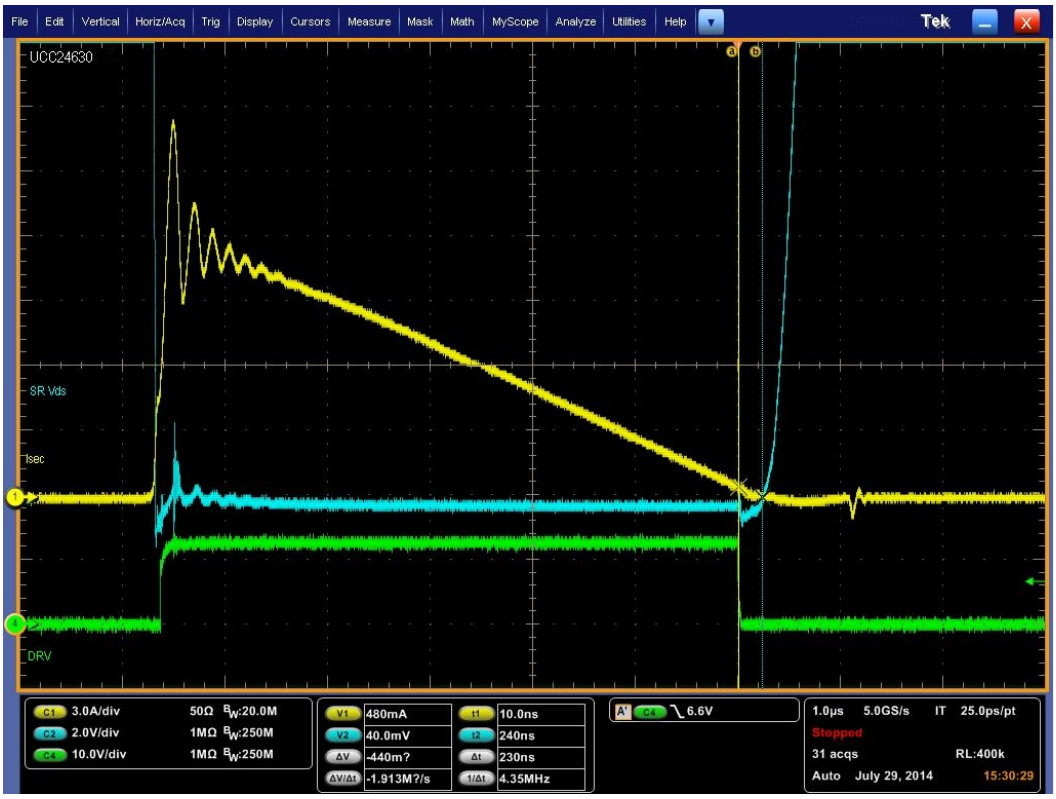

Figure 9. SR VDS, Isec, and SR Gate Drive at 115V, Full Load

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