TI reference design number: PMP9335 Rev B

Input: 12V

Output 1: 1V @ 10.6A VCCPINT

Output 2: 1V @ 3.7A MGTAVCC

Output 3: 1.8V@ 3.7A VCCPLL

DC–DC Converter Test Results

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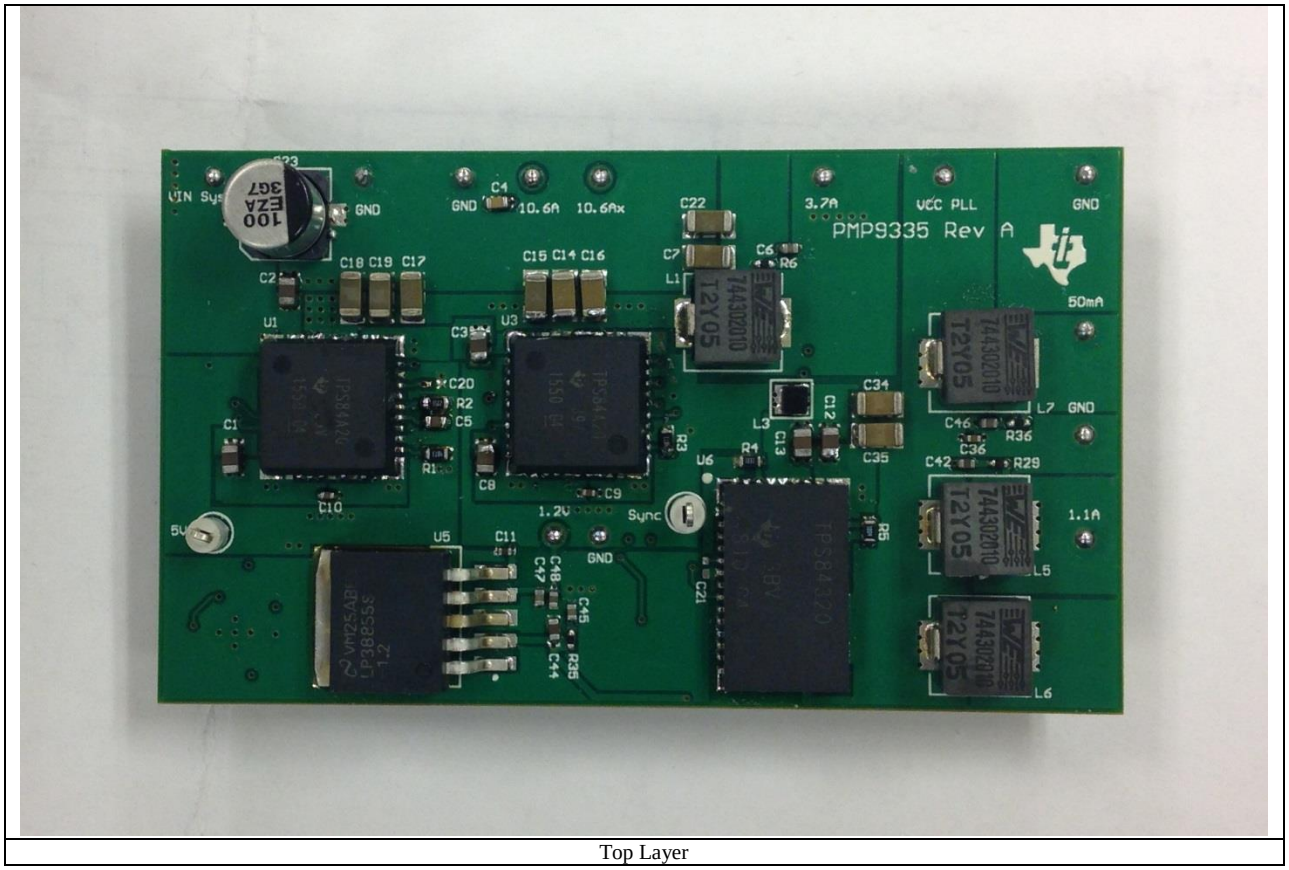
1. Circuit Description

PMP9335 is designed for Xilinx Zynq FPGA applications. PMP9335 utilizes the TPS84A20 and a TPS84320. This is a multi-output, multi-buck converter that operates at 12Vin and has multiple outputs for power rails. This design uses an external timer to synchronize the switching frequency to 300 kHz; it also employs a controlled power up and power down sequence. This design is configured for approximately 20W.

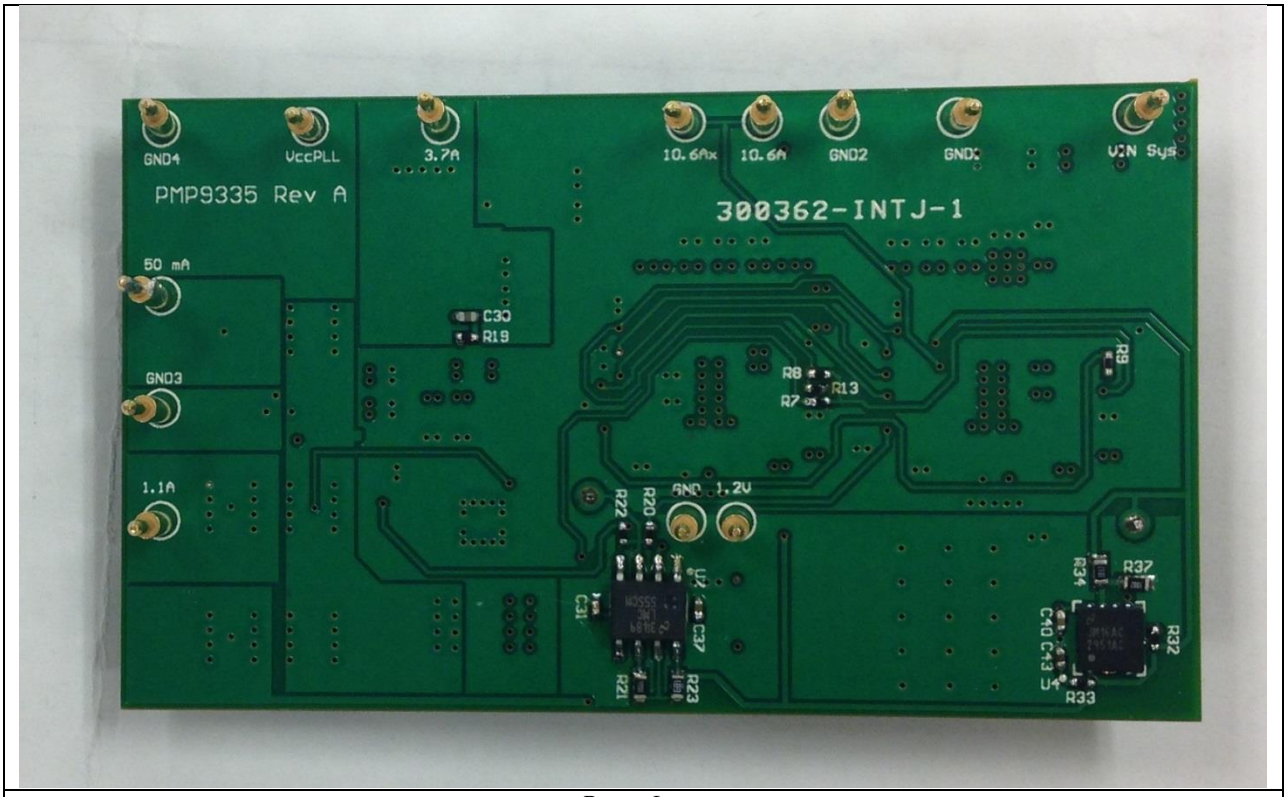
This board is intended to be used as a "plug in" module, the use of extra bulk capacitance on external pcb is assumed.

2. Fabrication

The PMP9335 is a four layer board with overall dimensions of 2.808" (71mm) x 1.633" (41mm). The copper weight is 1oz on the outer layers and 0.5oz the inner layers.

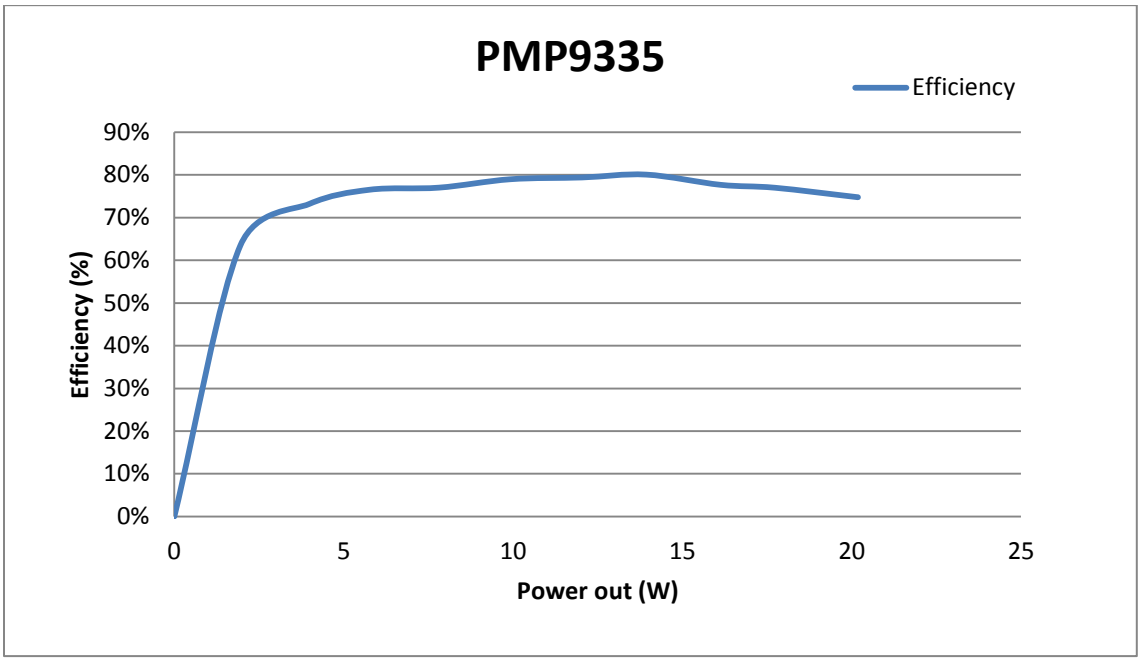


Top Layer

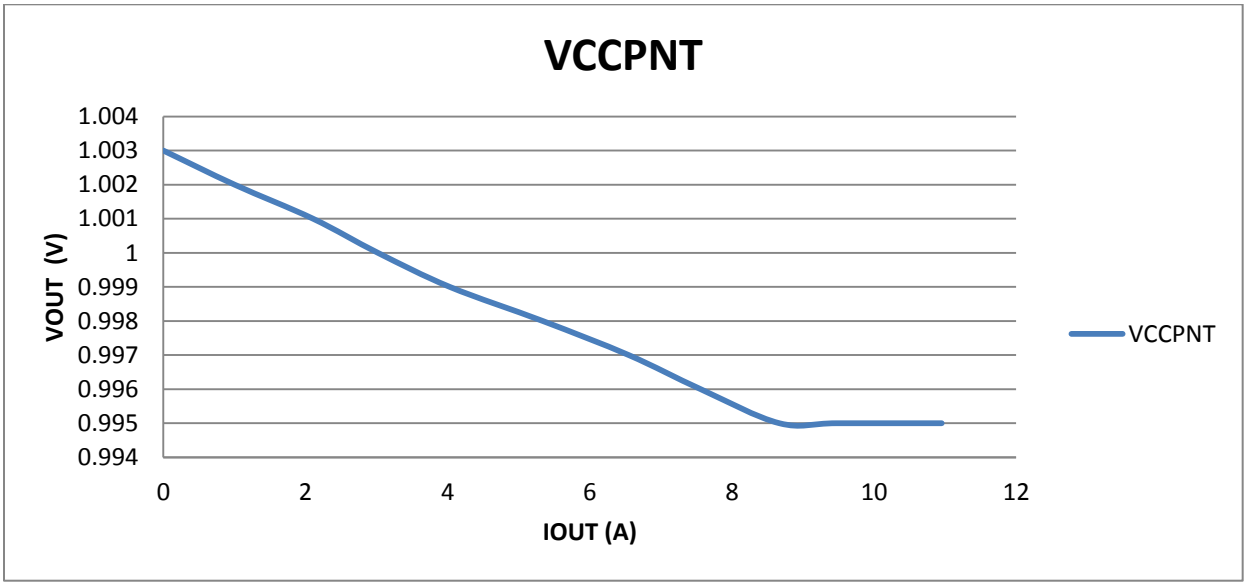


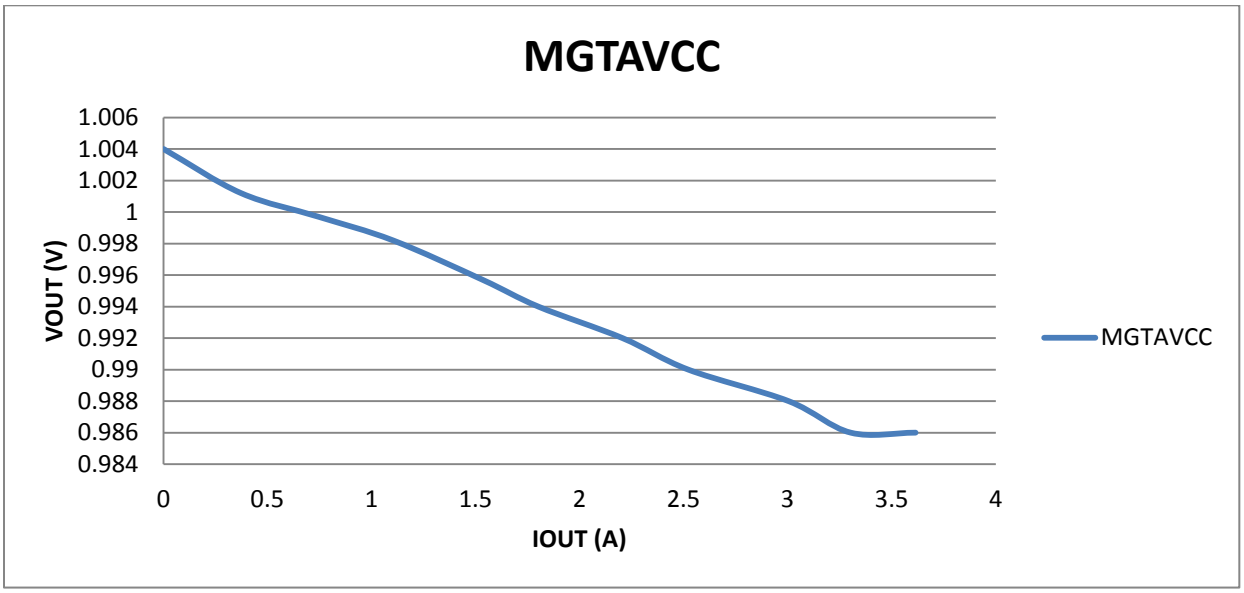
Bottom Layer

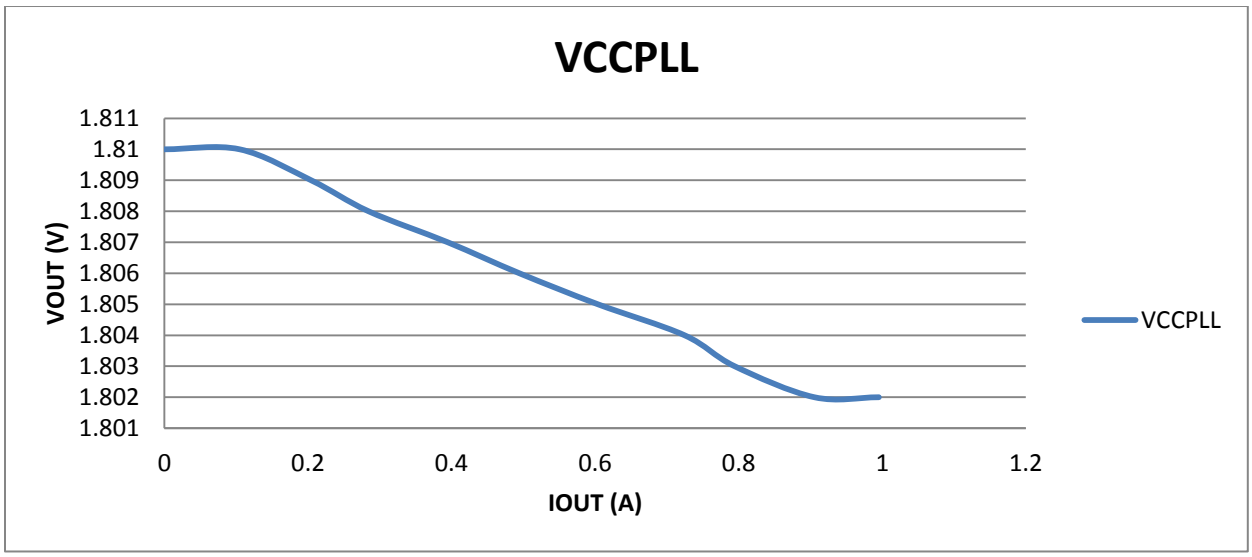
3. Efficiency

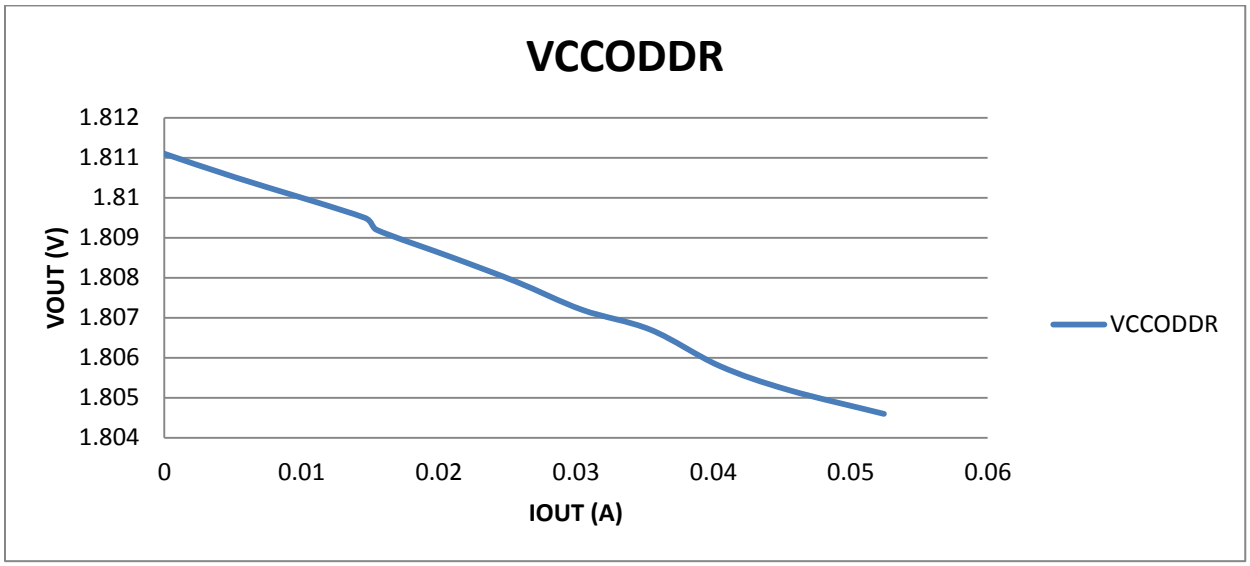


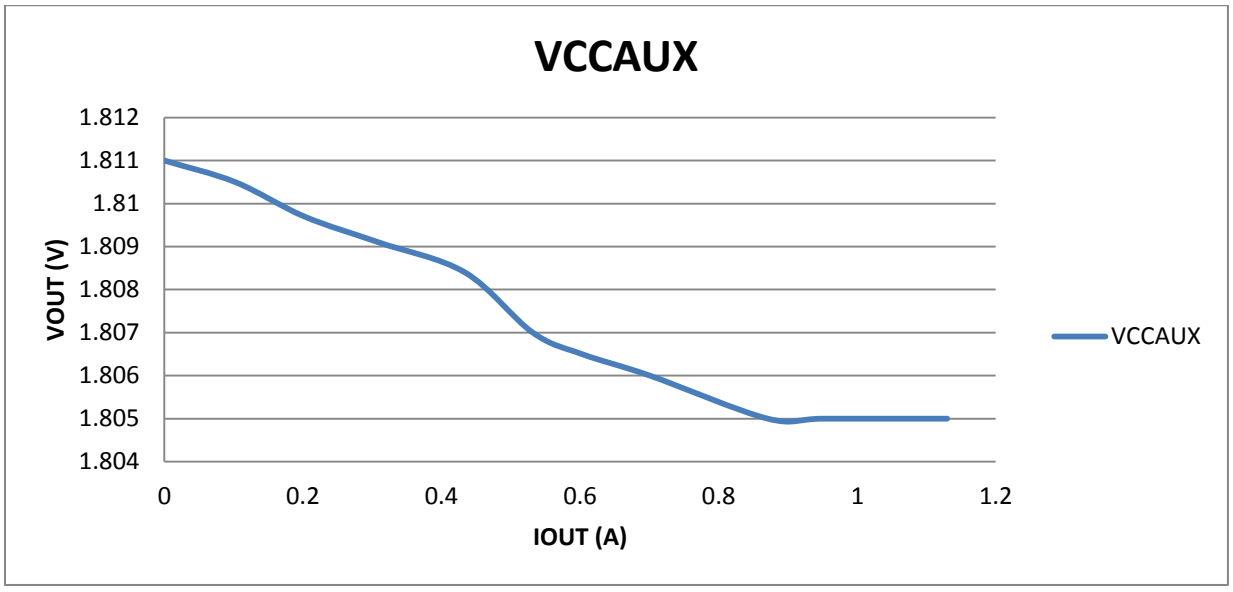
4. Load Regulation

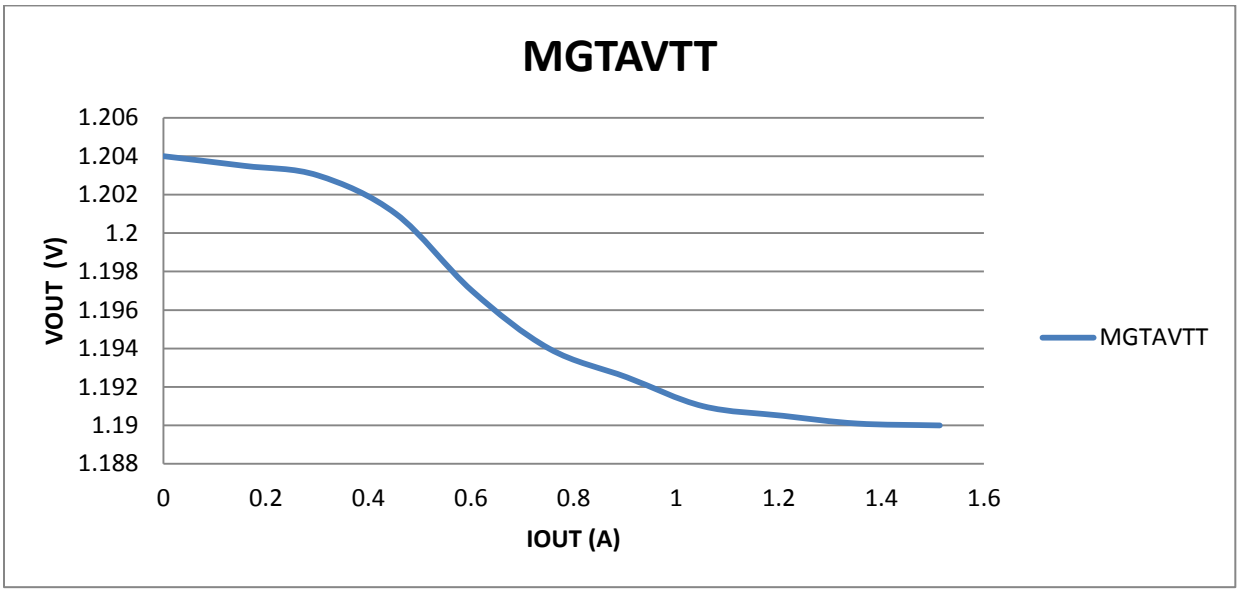



MGTAVCC
1.006
1.004
1.002
1
0.998
0.996
0.994
0.992
0.99
0.988
0.986
0.984
VOUT (V)
0
0.5
1
1.5
2
2.5
3
3.5
4
IOUT (A)
MGTAVCC


VCCPLL
1.811
1.81
1.809
1.808
1.807
1.806
1.805
1.804
1.803
1.802
1.801
VOUT (V)
0
0.2
0.4
0.6
0.8
1
1.2
IOUT (A)
VCCPLL

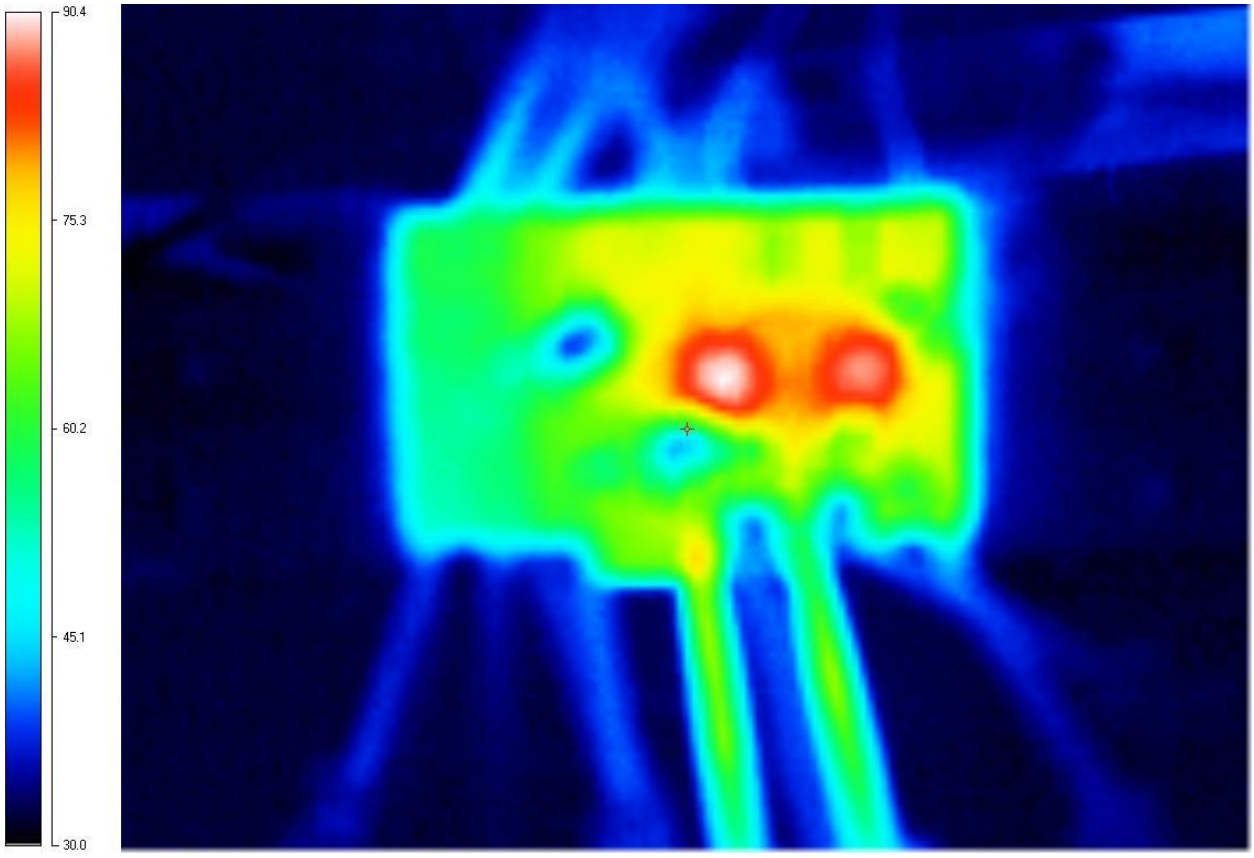

VCCODDR
1.812
1.811
1.81
1.809
1.808
1.807
1.806
1.805
1.804
VOUT (V)
0
0.01
0.02
0.03
0.04
0.05
0.06
IOUT (A)
VCCODDR


VCCAUX
1.812
1.811
1.81
1.809
1.808
1.807
1.806
1.805
1.804
VOUT (V)
0
0.2
0.4
0.6
0.8
1
1.2
IOUT (A)
VCCAUX


MGTAVTT
1.206
1.204
1.202
1.2
1.198
1.196
1.194
1.192
1.19
1.188
VOUT (V)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
IOUT (A)
MGTAVTT

5. Thermal

5.1 Steady State Temperature, 12Vin and 20W out.



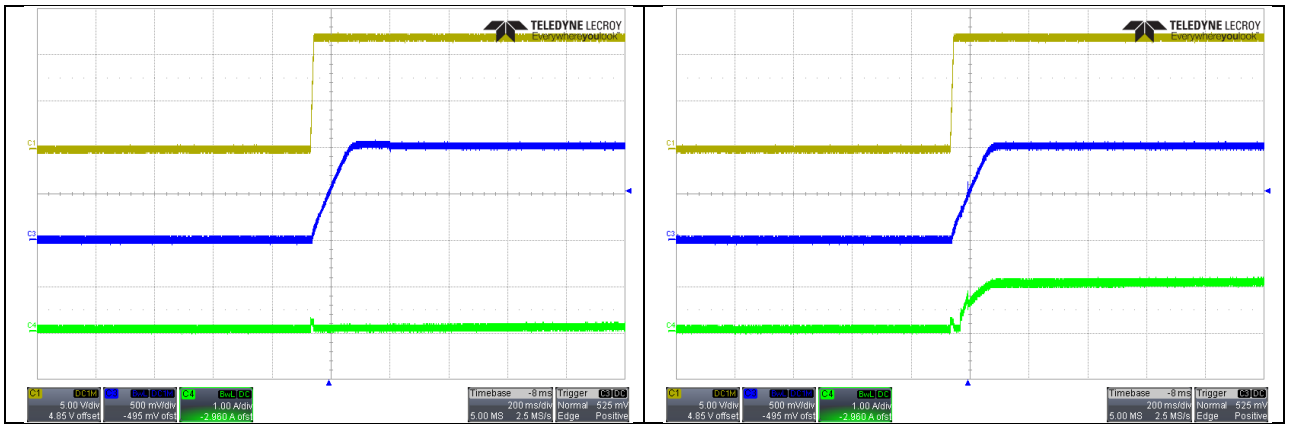
Top View

The warmest components are the paralleled combination of the TPS84A20. This image displays a 65°C temperature rise.

The temperature rise can be reduced by increasing the copper weight of the PCB.

6. Power Up VCCPINT

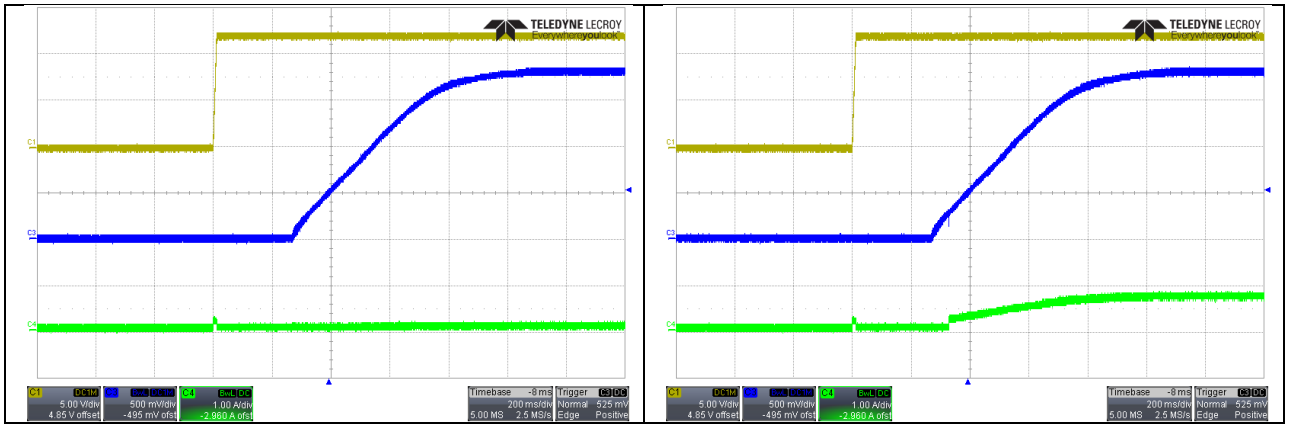
6.1 Power Up at 12V Input – No Load *Power Up at 12V Input –10.6A*



Channel 1 VIN
Channel 3 VOUT
Channel 4 IIN

6. Power Up VCCPLL

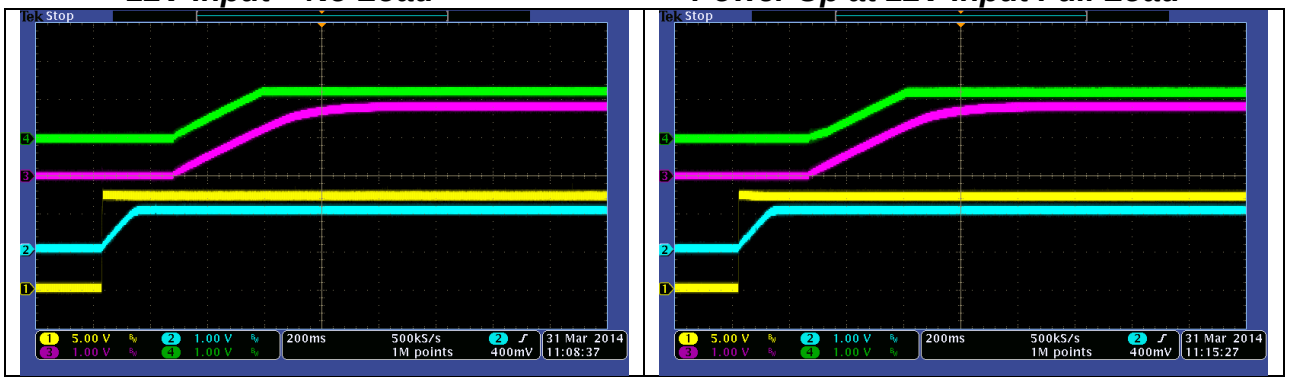
6.2 Power Up at 12V Input – No Load *Power Up at 12V Input –3.7A*



Channel 1 VIN
Channel 3 VOUT
Channel 4 IIN

6.3 Power Up Sequencing

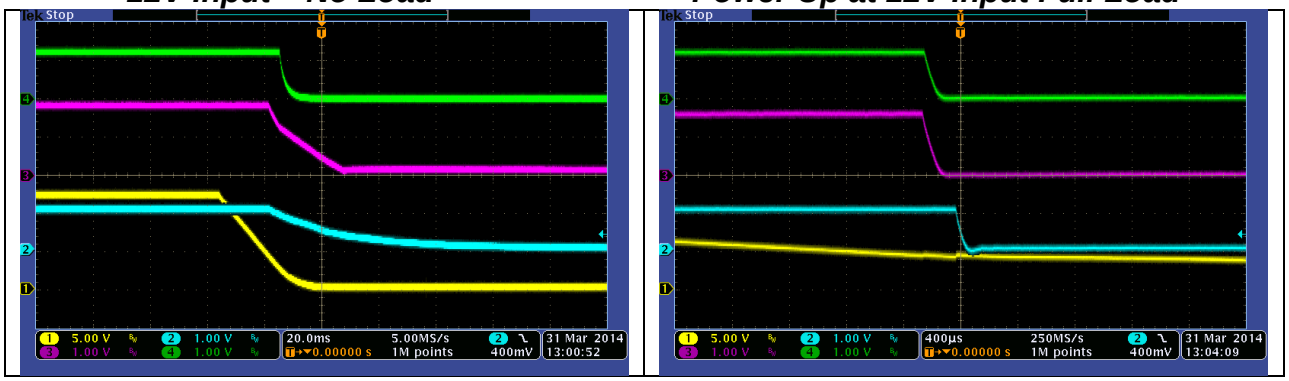
-12V Input – No Load ***Power Up at 12V Input Full Load***



Channel 1 VIN
Channel 2 VCCPINT
Channel 3VCCPLL
Channel 4 MGTAVTT

6.4 Power Down Sequencing

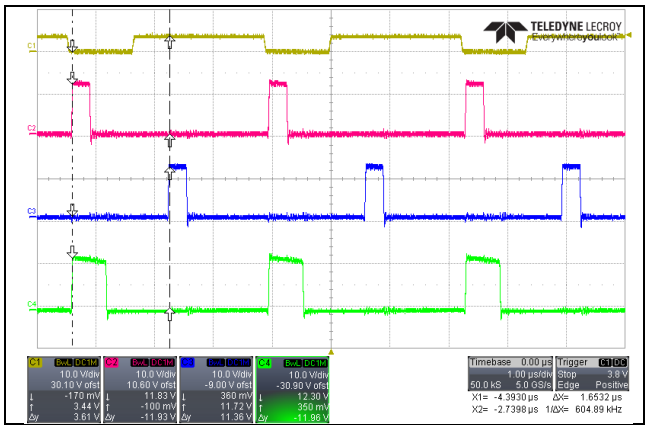
-12V Input – No Load ***Power Up at 12V Input Full Load***



Channel 1 VIN
Channel 2 VCCPINT
Channel 3VCCPLL
Channel

7. Clock Synchronization

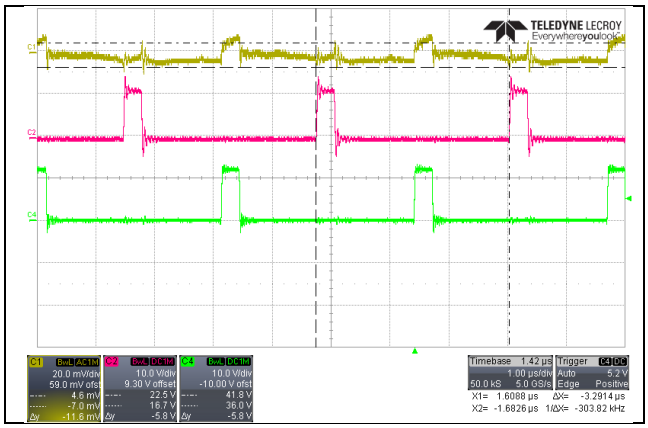
7.1 Clock and Phase



Channel 1 LMC555 Sync out
Channel 2 VCCPINT PH1
Channel 3 VCCPINT PH2
Channel 4 VCCPLL

8. Switching and Ripple

8.1 VCCPINT –10.6A

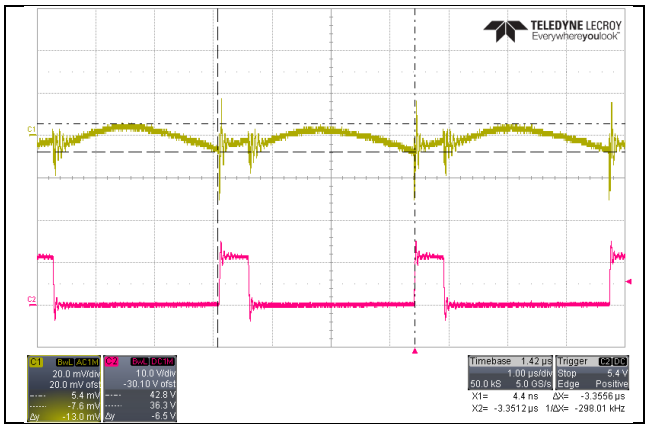


The cursors indicate 11mV ripple.

Channel 1 VOUT
Channel 3 VCCPINT PH1
Channel 4 VCCPINT PH2

9. Switching and Ripple

9.1 VCCPLL – 3.7A

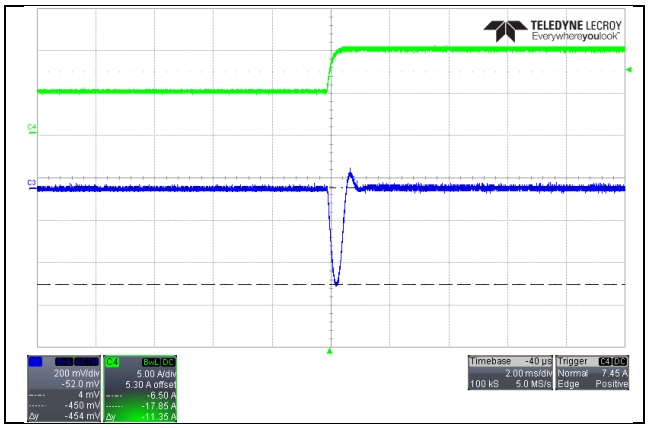


The cursors indicate less than 13mV ripple

Channel 1 VOUT
Channel 3 VCCPLL PH

10. Transient Response VCCPINT

10.1 12V Input – 5A to 10A Step, 100mA/µs, 30 Hz.



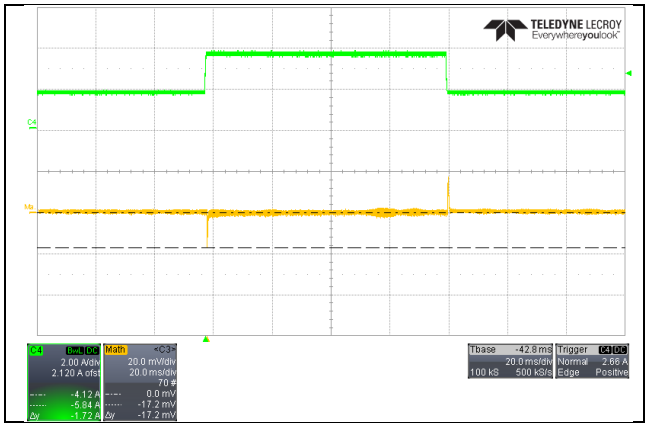
Cursors indicate ~0.45V deviation across output capacitor.

All testing was done with minimal output capacitance. Add additional output capacitance on motherboard to reduce deviation.

Channel 3 VOUT
Channel 4 IOUT

10. Transient Response VCCPLL

10.2 12V Input –1.8A to 3.7A Step, 100mA/µs, 30 Hz.



Cursors indicate ~17.2mV maximum deviation across output capacitor.

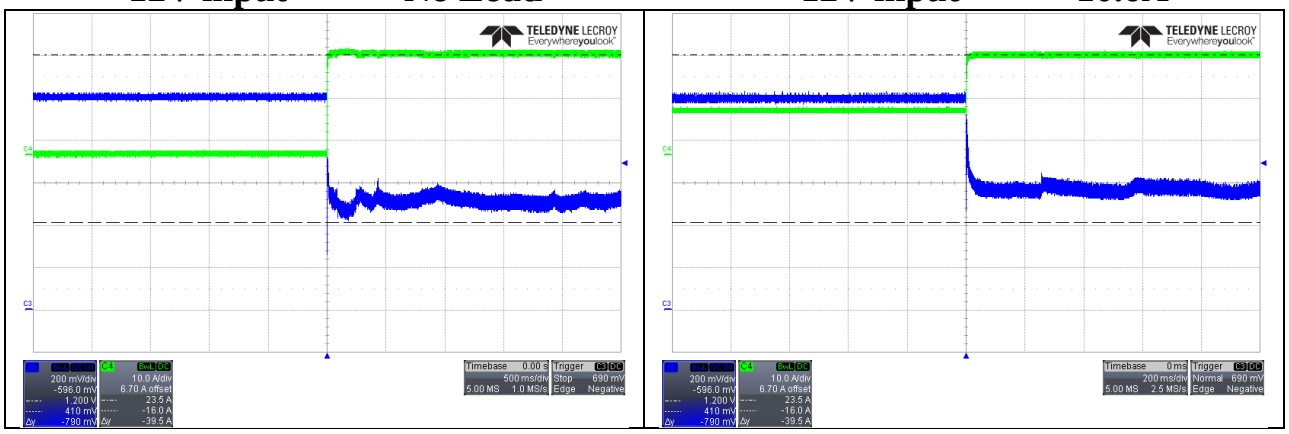
All testing was done with minimal output capacitance

Channel 1 VOUT
Channel 4 IOUT

11. Current Limit Tests

11.1 VCCPINT

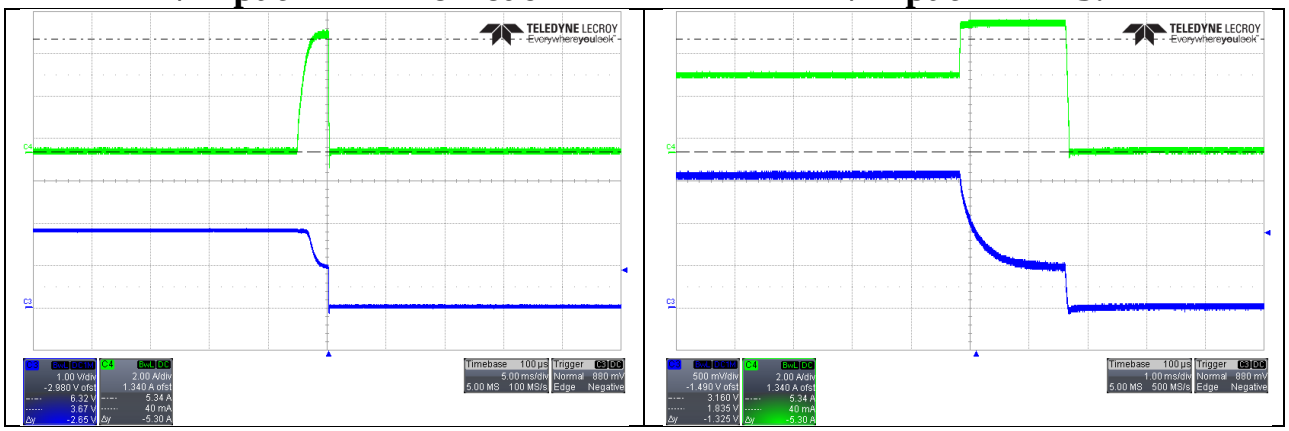
-12V input - No Load **-12V input - 10.6A**



Channel 3 VOUT
Channel 4 IOUT

11.2 VCCPLL

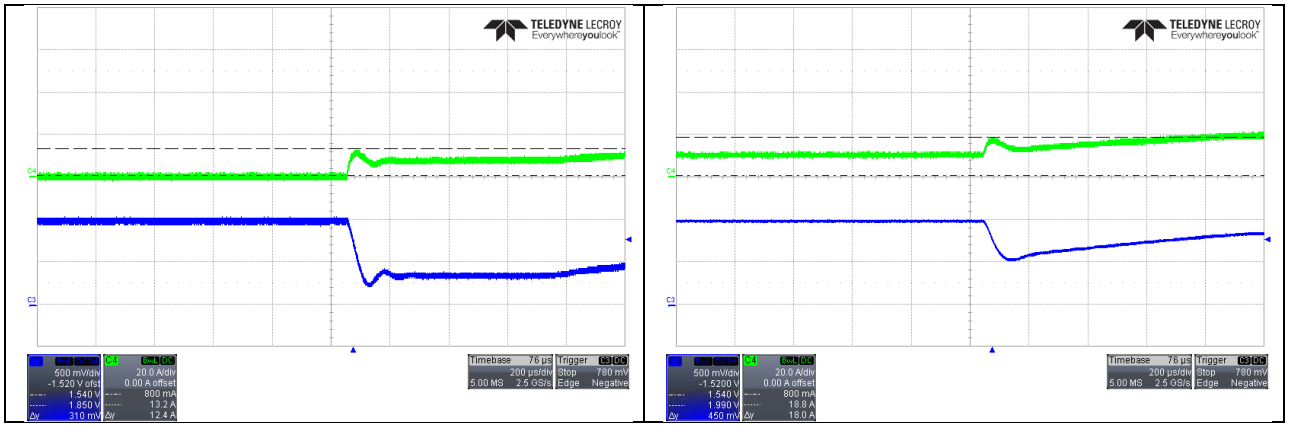
-12V input - No Load **-12V input - 3.7A**



Channel 3 VOUT
Channel 4 IOUT

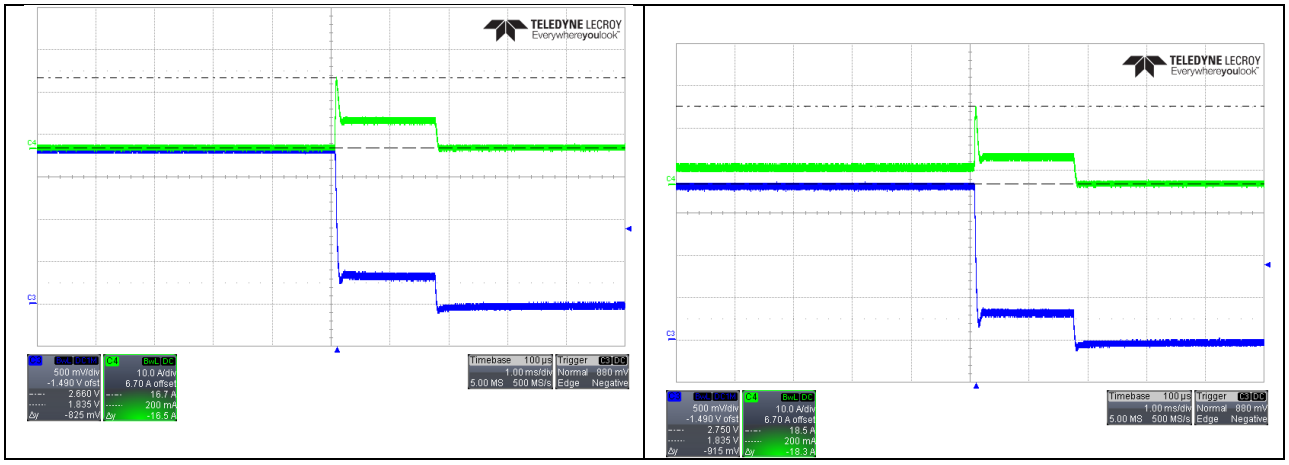
13. Short Circuit Tests

13.1 VCCPINT No Load VCCPINT 10.6A



Channel 3 VOUT
Channel 4 IOUT

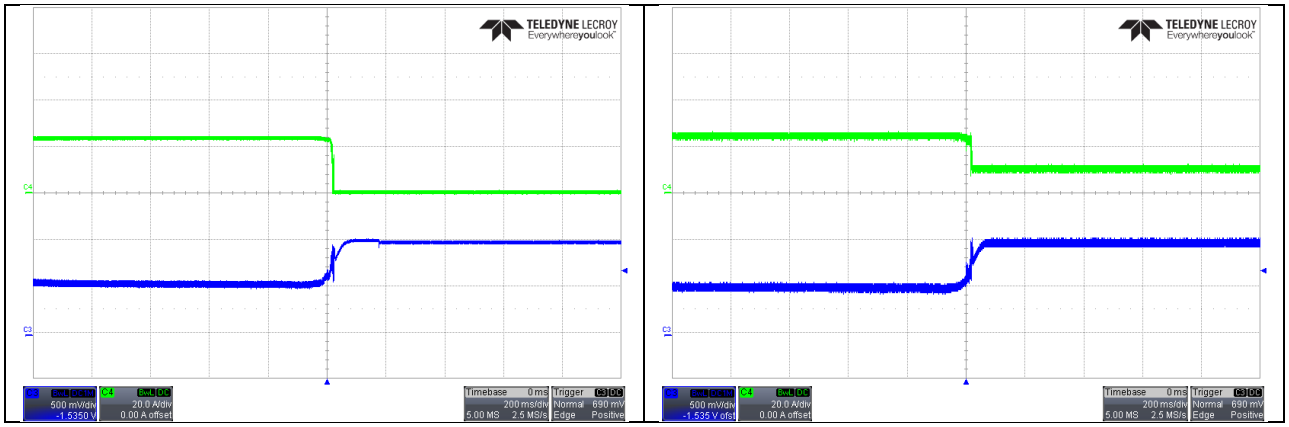
13.2 VCCPLL No Load VCCPLL 3.7A



Channel 3 VOUT
Channel 4 IOUT

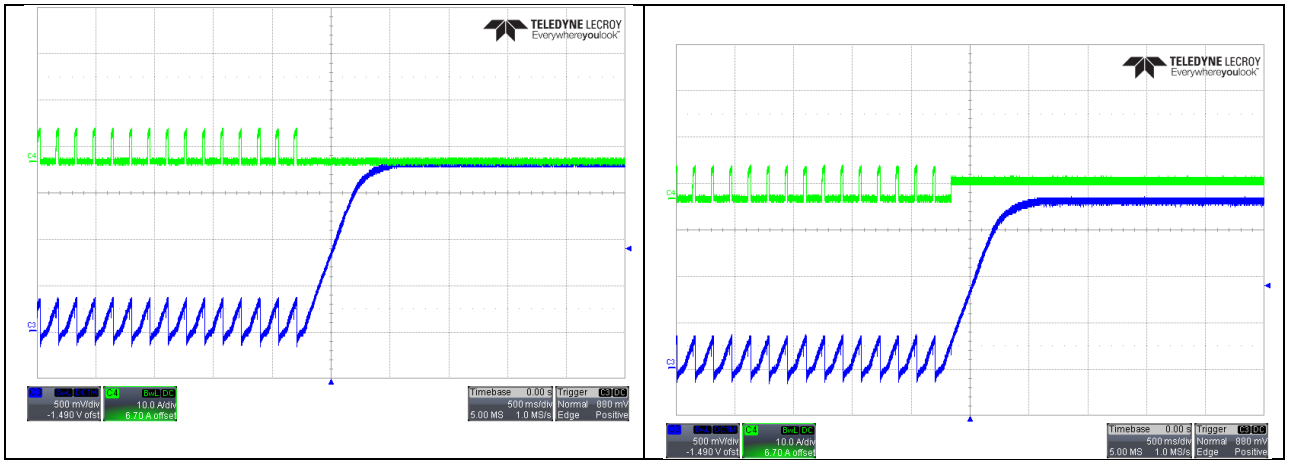
14. Short Circuit Recovery Tests

14.1 VCCPINT No Load VCCPINT 10.6A



Channel 3 VOUT
Channel 4 IOUT

14.2 VCCPLL No Load VCCPLL 3.7A



Channel 3 VOUT
Channel 4 IOUT

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