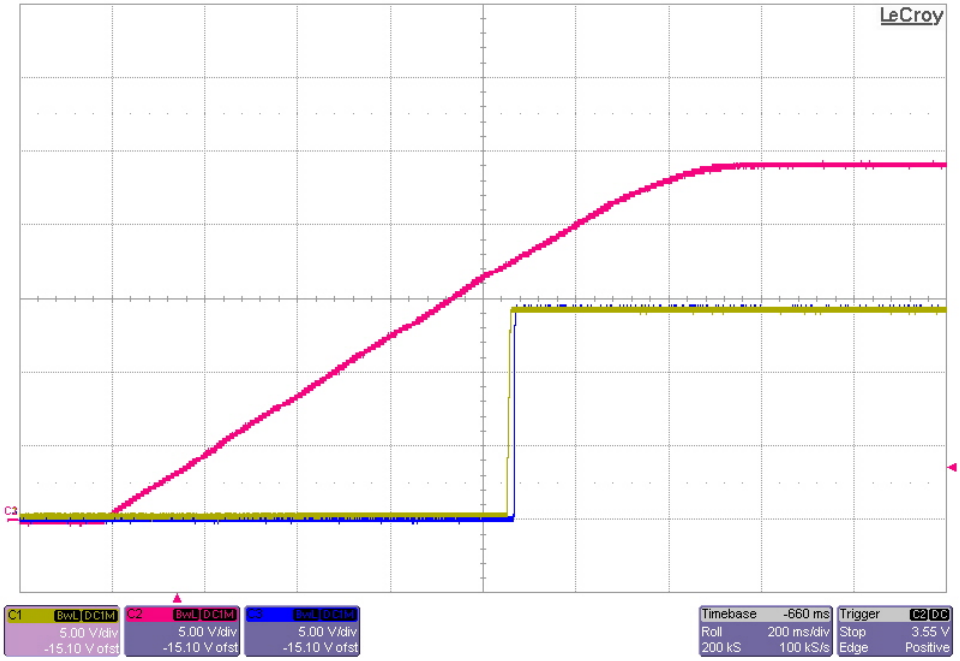
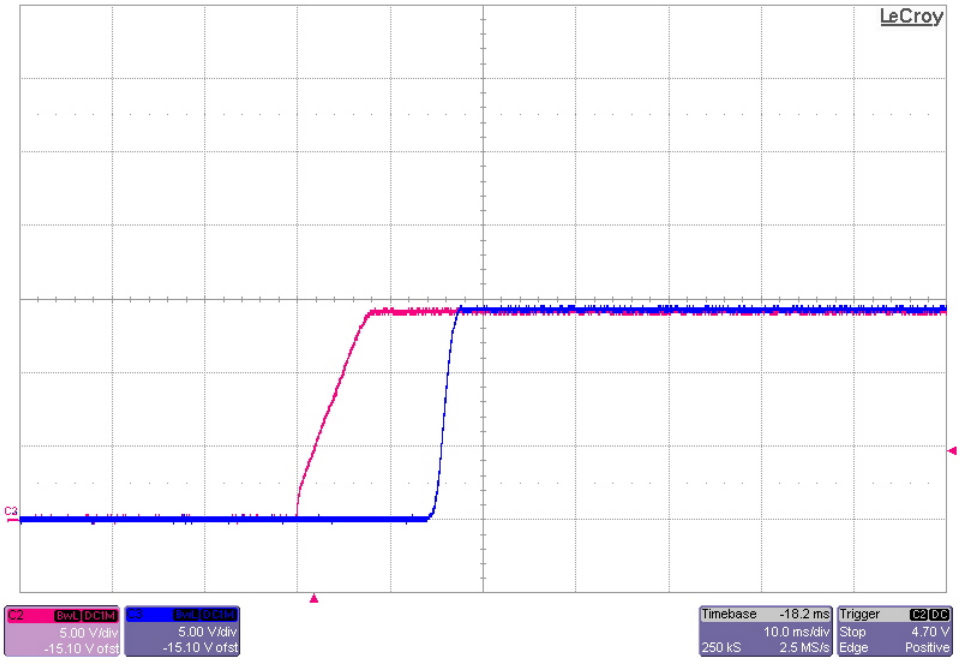
1 Startup

The photo below shows the output voltage startup waveform after the application of 24V in. The 14.4V output was loaded to 0A. RED is Vin, BLUE is Vout (TP19), and YELLOW is Vreg point (TP17) (5V/DIV, 200mS/DIV)

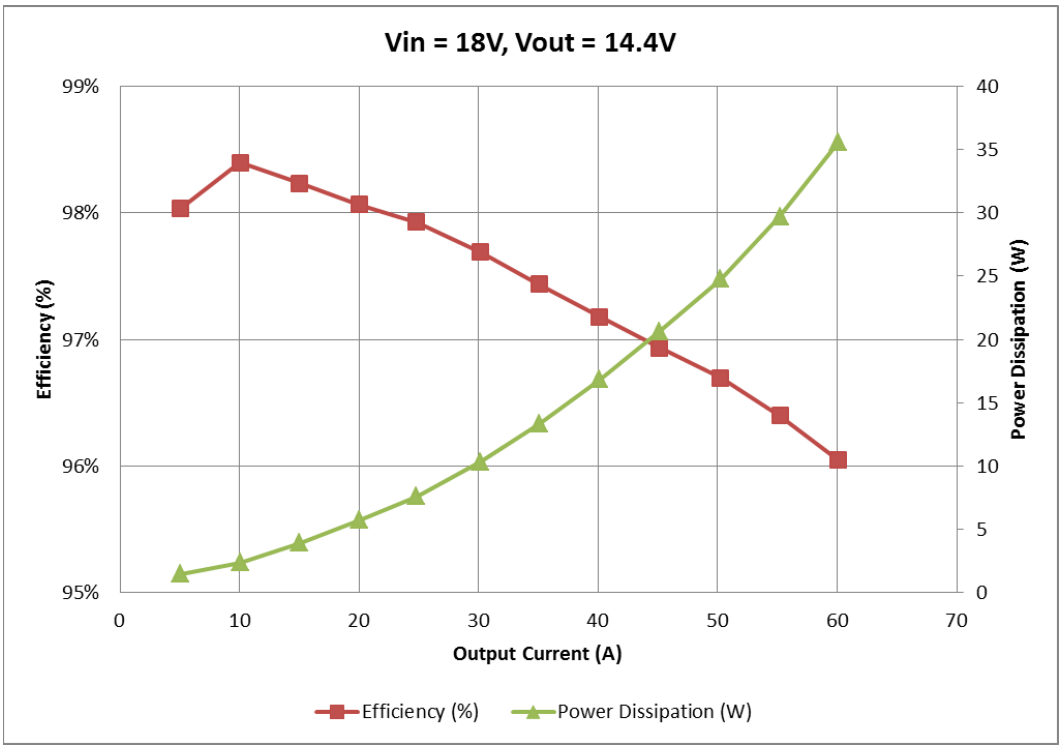


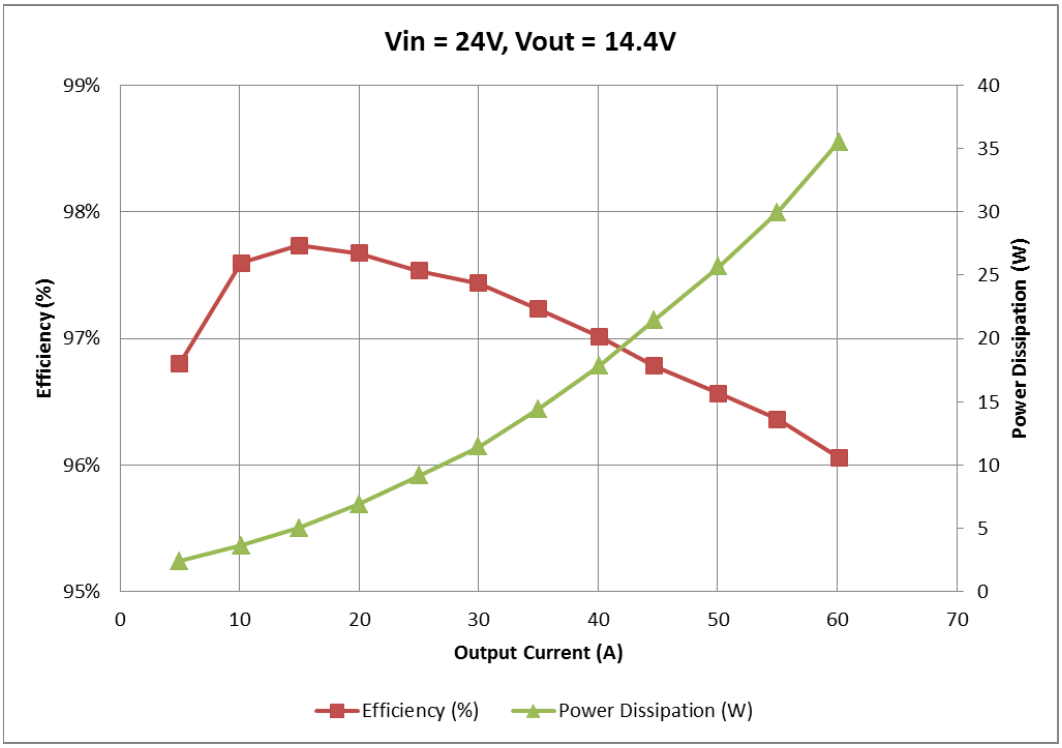
The photo below shows the output voltage startup waveform after the application of 24V in. The 14.4V output was loaded to 0A. RED is Vreg point (TP17), BLUE is Vout (TP19)
(5V/DIV, 200mS/DIV)

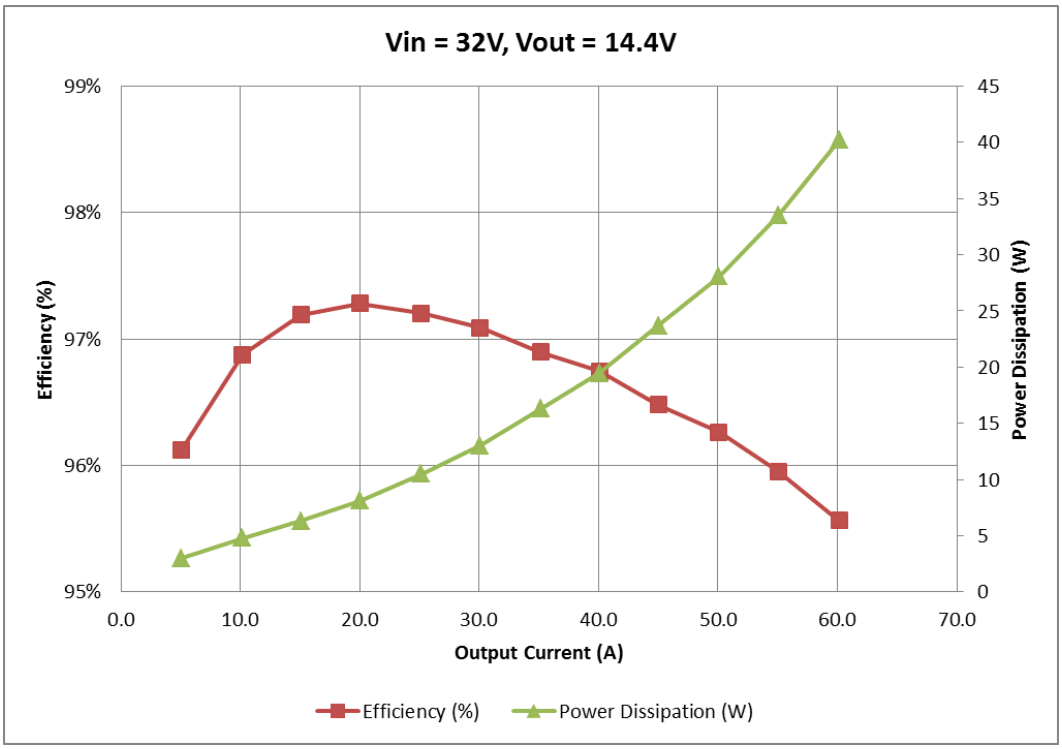


2 Efficiency

The converter efficiency is shown below for Vin = 18V, 24V, and 32V.

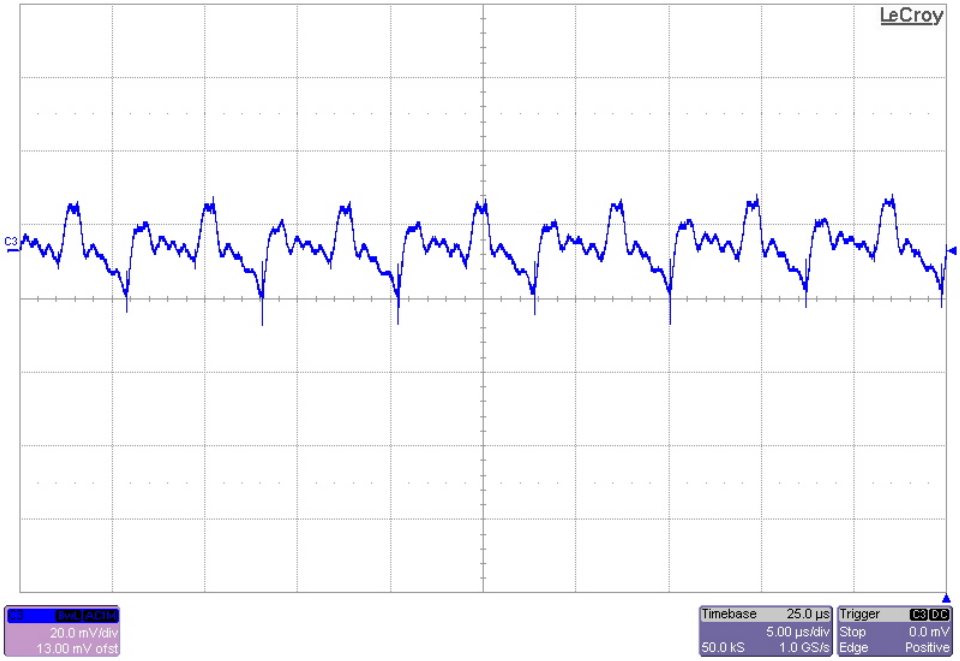




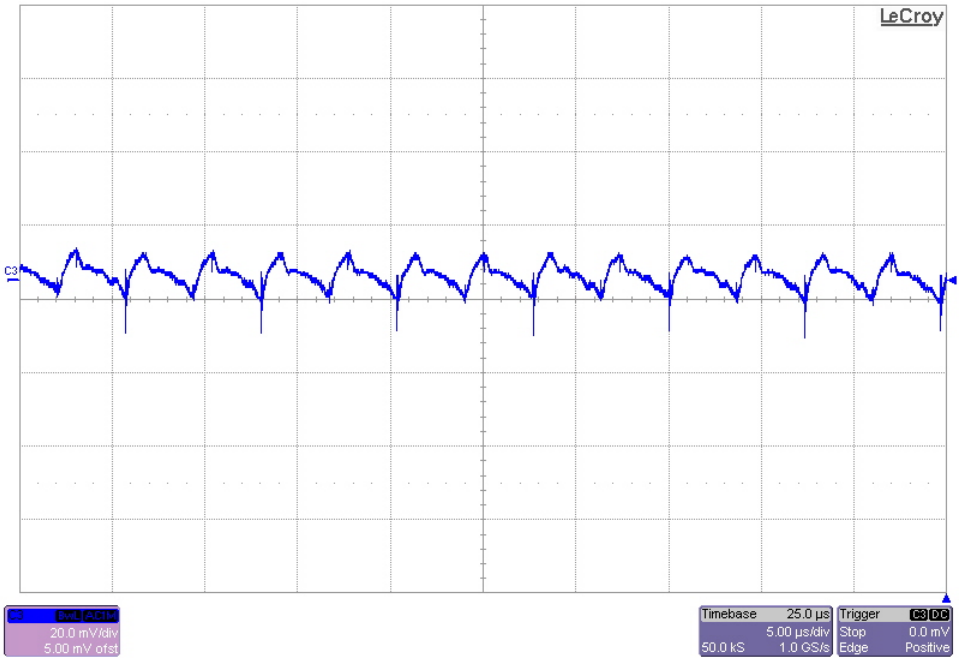

Vin = 32V, Vout = 14.4V
99%
98%
97%
96%
95%
Efficiency (%)
45
40
35
30
25
20
15
10
5
0
Power Dissipation (W)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
Output Current (A)
Efficiency (%)
Power Dissipation (W)

3 Output Ripple Voltage

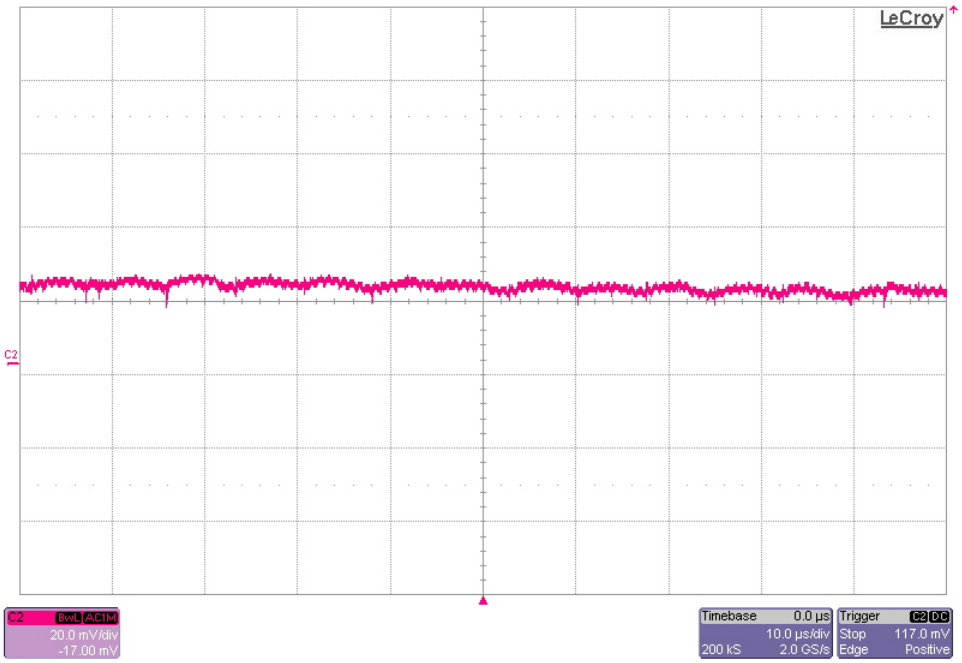
The 14.4V output ripple voltage (AC coupled) is shown in the figure below. The voltage is measured across C34 at TP17 which is before the hotswap on the output. The image was taken with the output loaded to 60A. The input voltage is set to 24V. (20mV/DIV, 5uS/DIV)



The 14.4V output ripple voltage (AC coupled) is shown in the figure below. The voltage is measured at the modules output terminals. The image was taken with the output loaded to 60A. The input voltage is set to 24V. (20mV/DIV, 5uS/DIV)

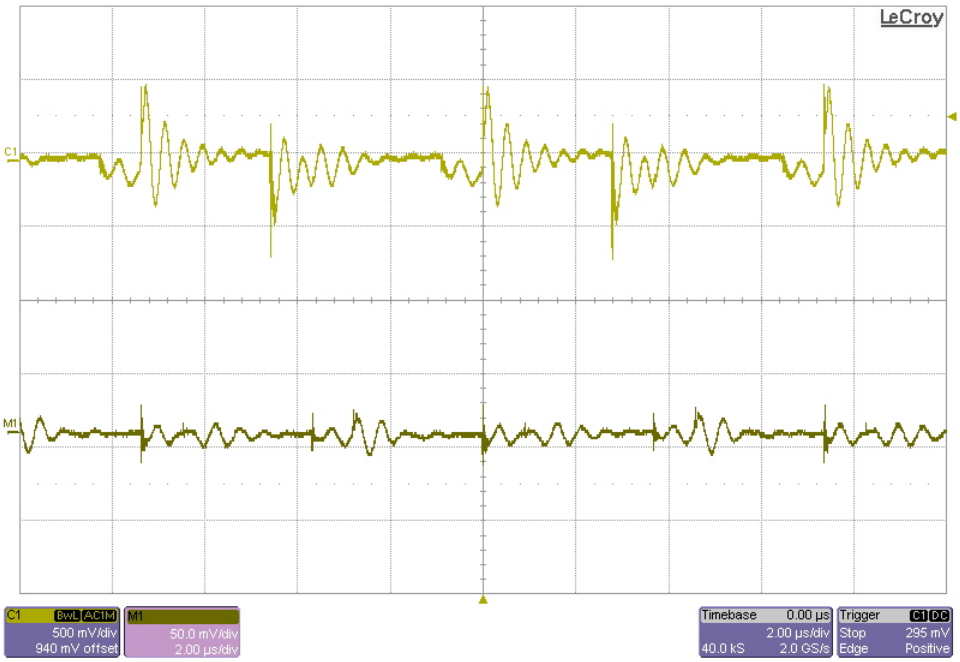


The photo below shows the TPS54060 5V bias supply output ripple voltage (AC coupled) for an input voltage of 32V and 0A external load. (20mV/DIV, 10uS/DIV)

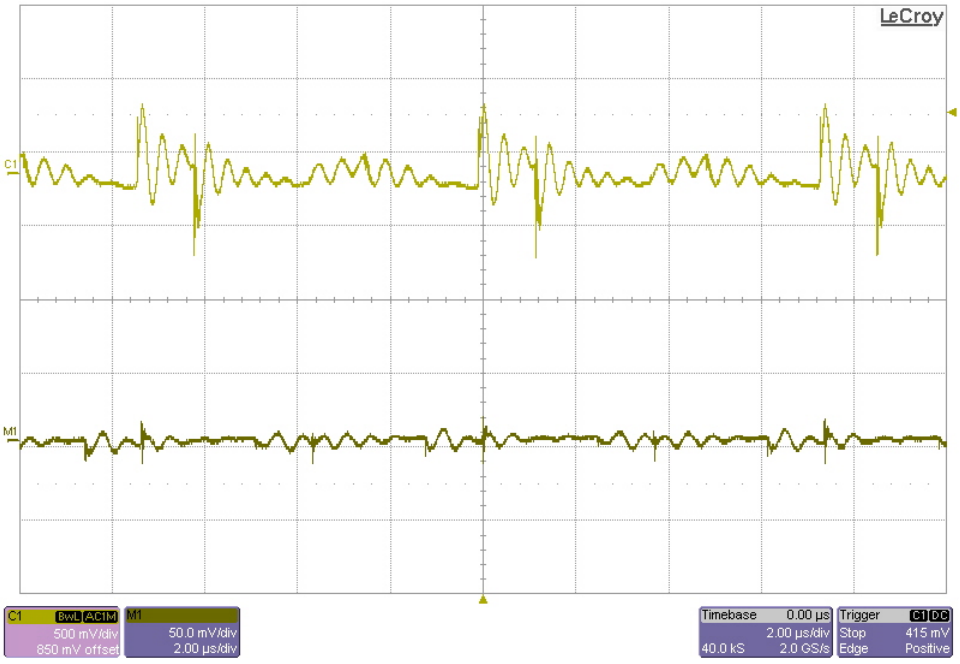


4 Input Ripple Voltage

The input ripple voltage (AC coupled) is shown in the figure below. The bottom waveform is measured at the modules input terminals while the top waveform is measured across C26 (after the EMI filter). The image was taken with the output loaded to 60A. The input voltage is set to 24V.
(top is 500mV/DIV, bot is 50mV/DIV, 2uS/DIV)

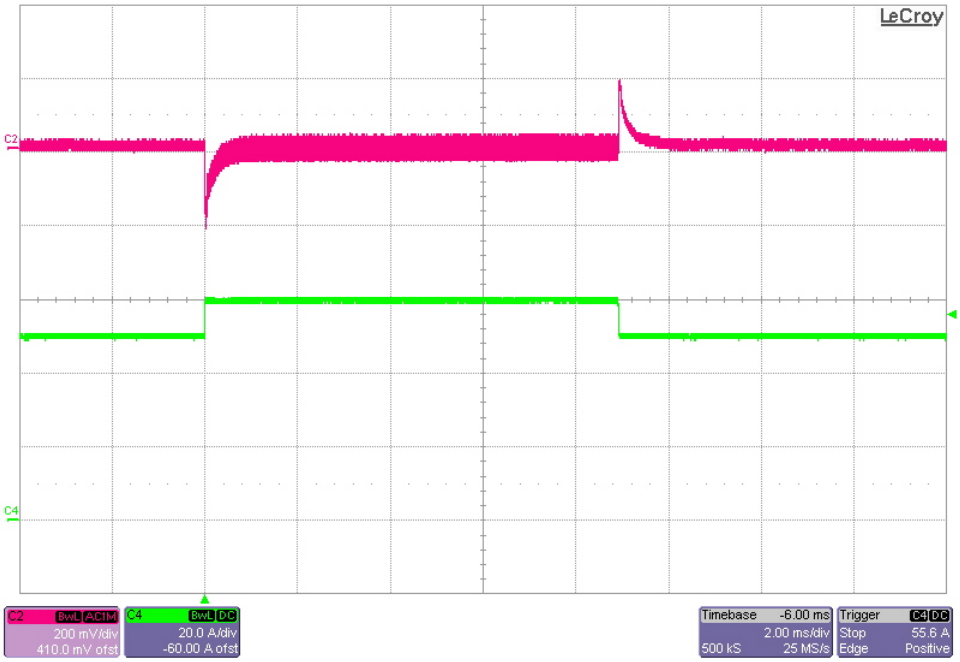


The input ripple voltage (AC coupled) is shown in the figure below. The bottom waveform is measured at the modules input terminals while the top waveform is measured across C26 (after the EMI filter). The image was taken with the output loaded to 60A. The input voltage is set to 18V.
(top is 500mV/DIV, bot is 50mV/DIV, 2uS/DIV)

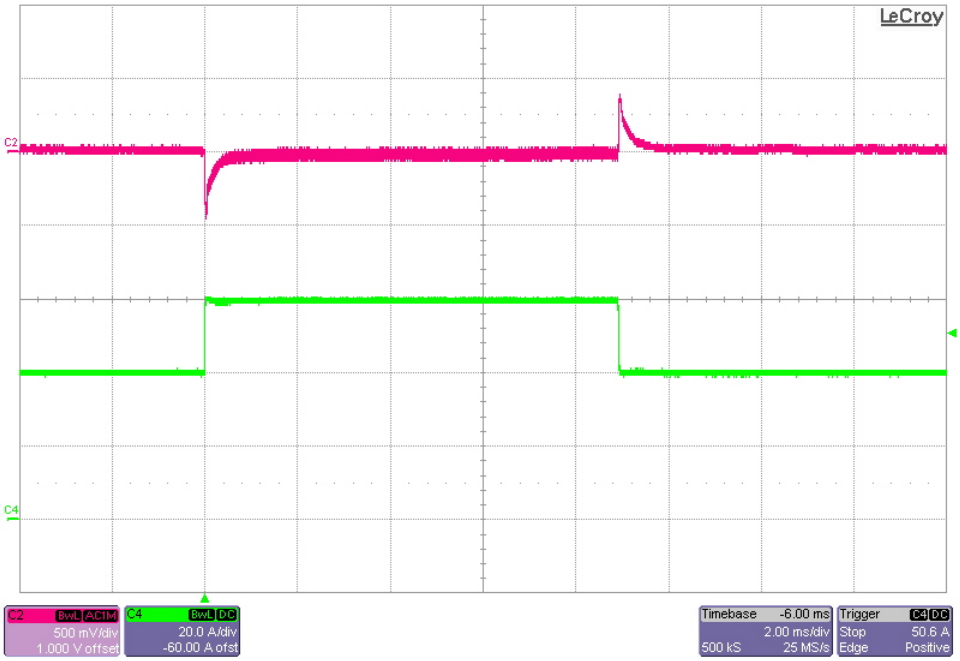


5 Load Transients

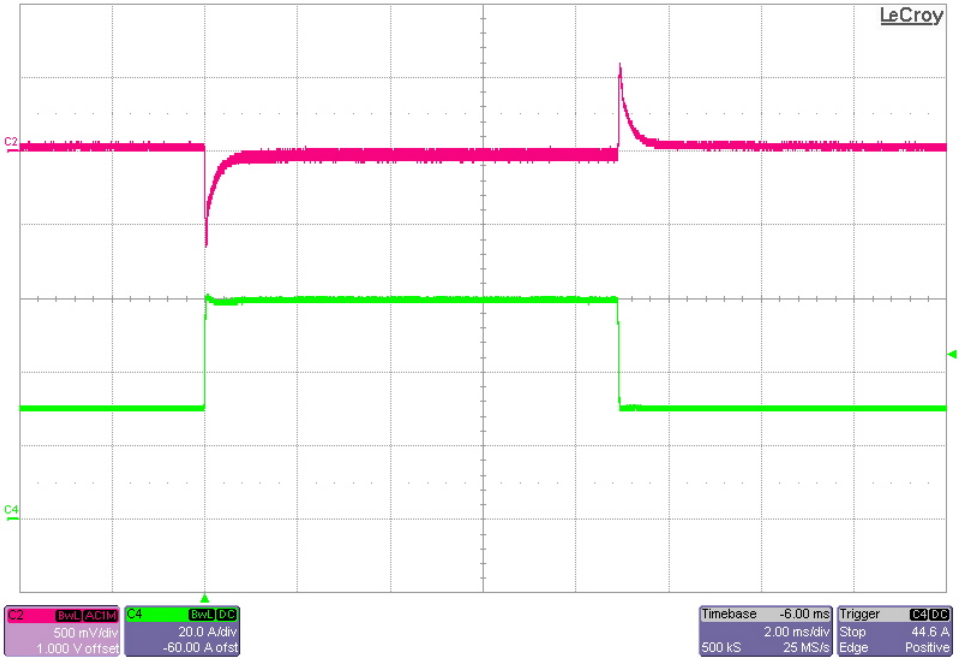
The photo below shows the 14.4V output voltage (ac coupled) when the load current is stepped between 50A and 60A. Vin = 24V. (200mV/DIV, 20A/DIV, 2mS/DIV)



The photo below shows the 14.4V output voltage (ac coupled) when the load current is stepped between 40A and 60A. Vin = 24V. (500mV/DIV, 20A/DIV, 2mS/DIV)

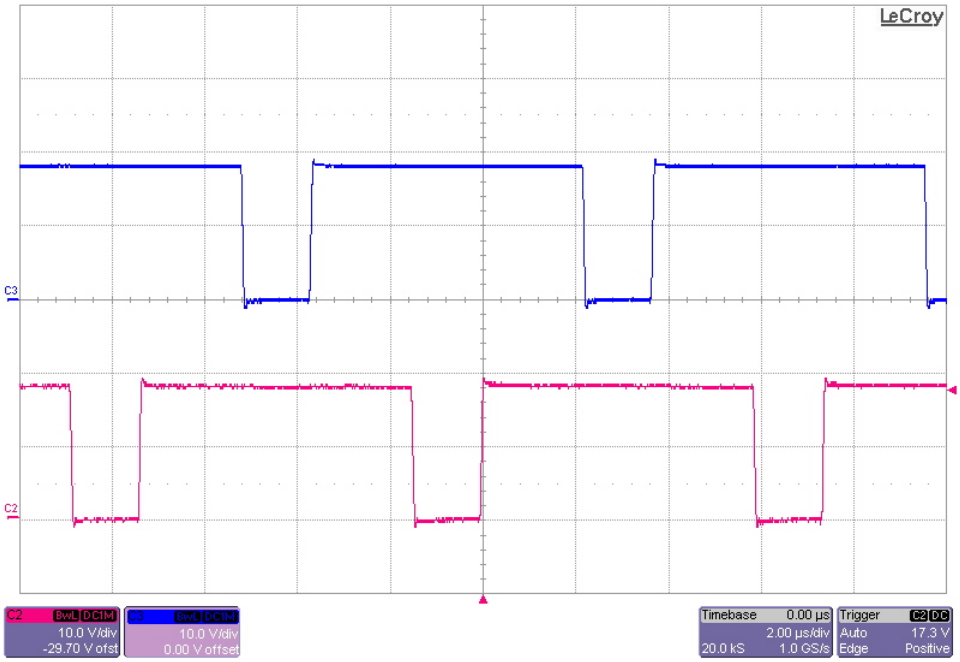


The photo below shows the 14.4V output voltage (ac coupled) when the load current is stepped between 30A and 60A. Vin = 24V. (500mV/DIV, 20A/DIV, 2mS/DIV)

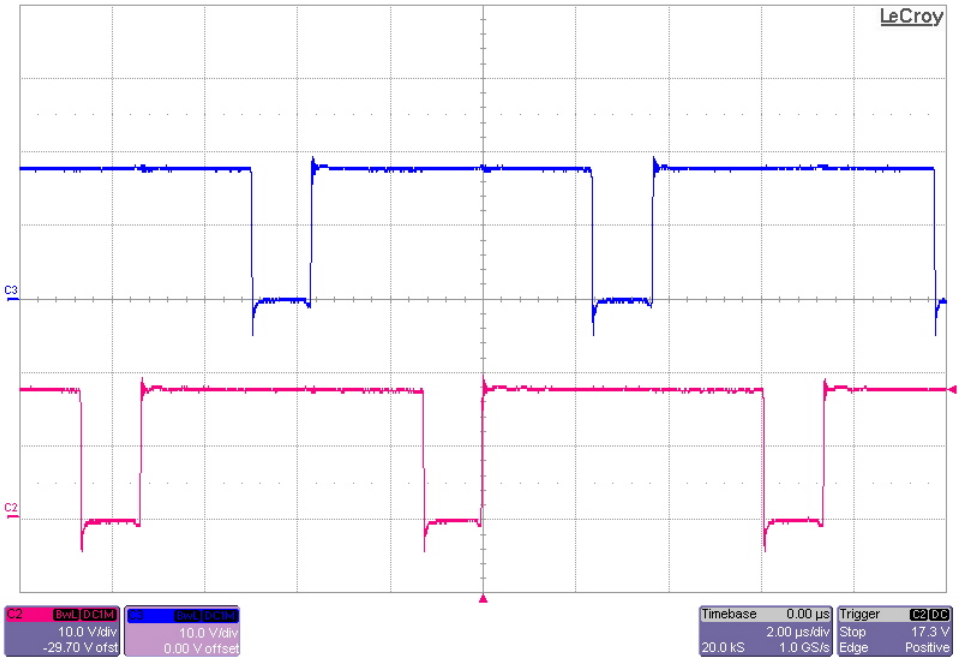


6 Switch Node Waveforms

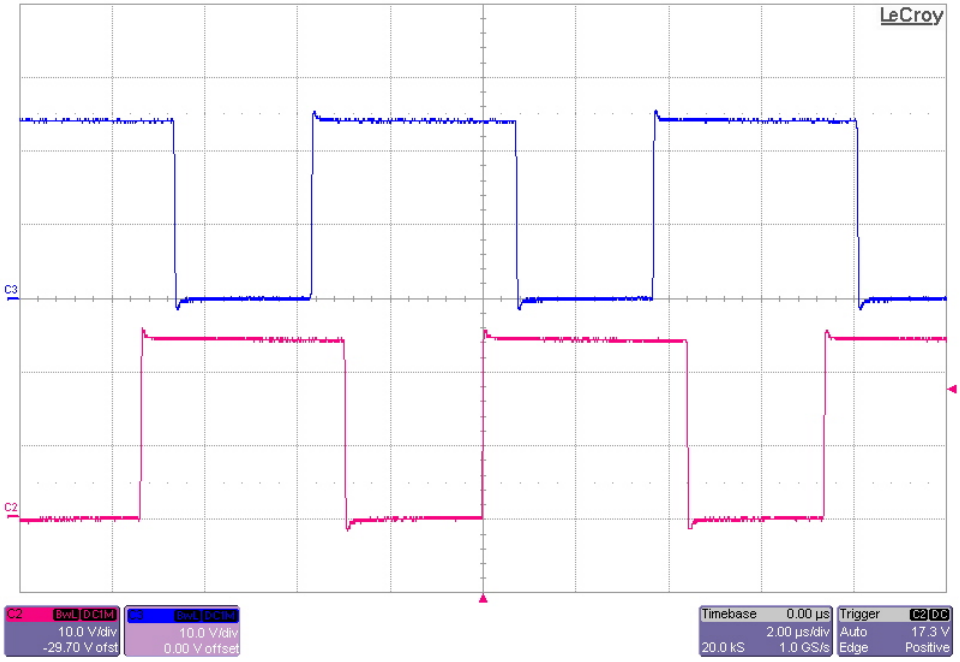
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 18V and a 0A load. (10V/DIV, 2uS/DIV)



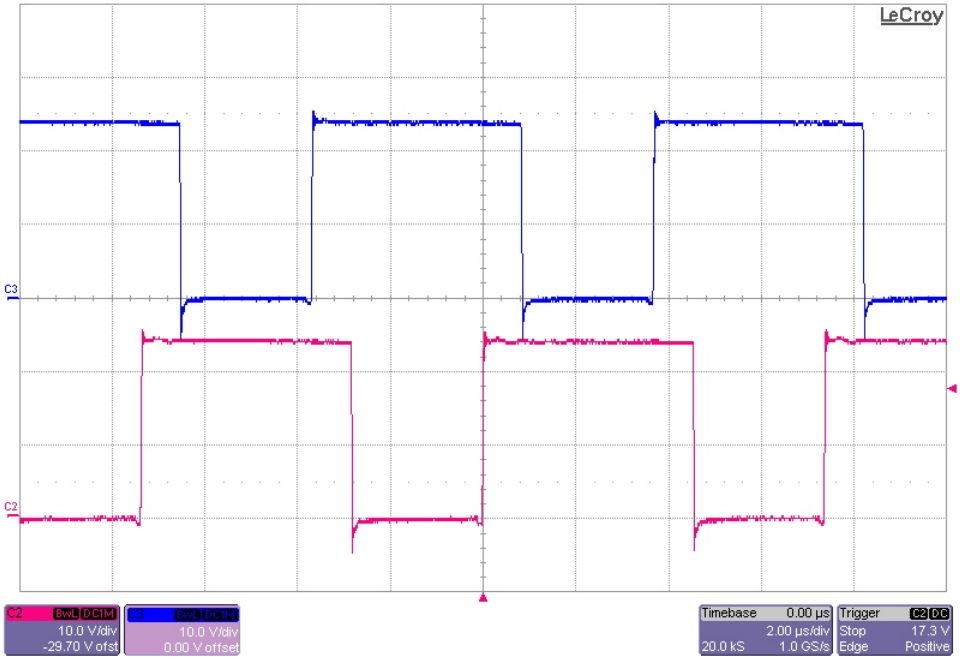
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 18V and a 60A load. (10V/DIV, 2uS/DIV)



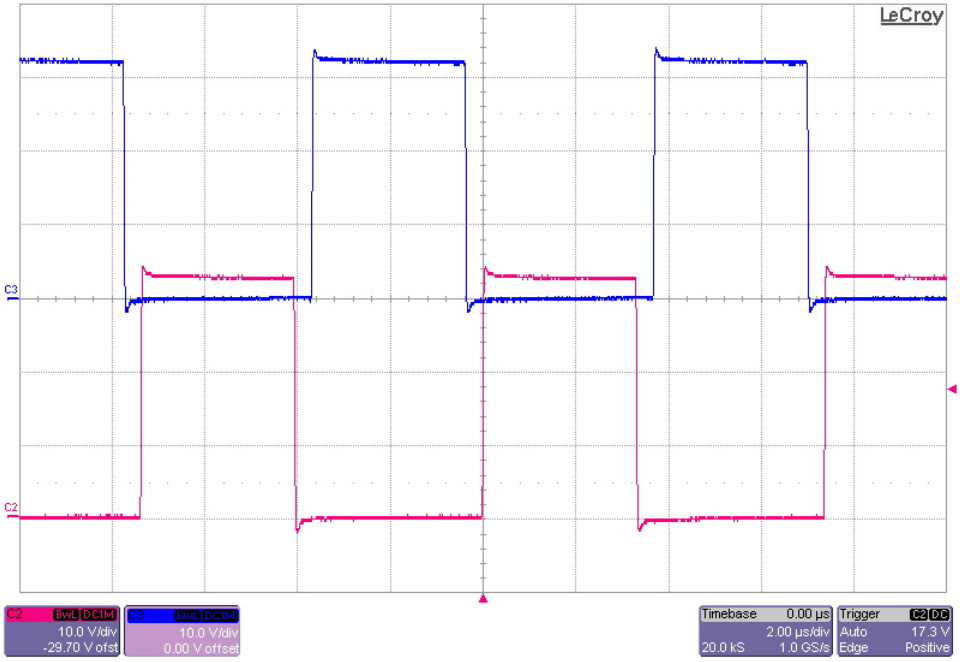
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 24V and a 0A load. (10V/DIV, 2uS/DIV)



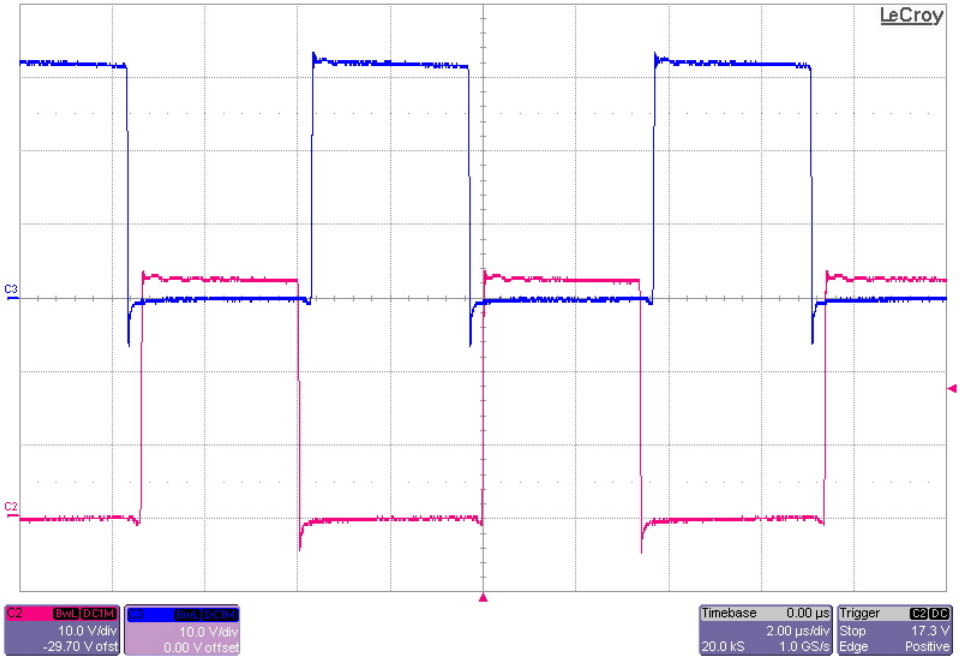
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 24V and a 60A load. (10V/DIV, 2uS/DIV)



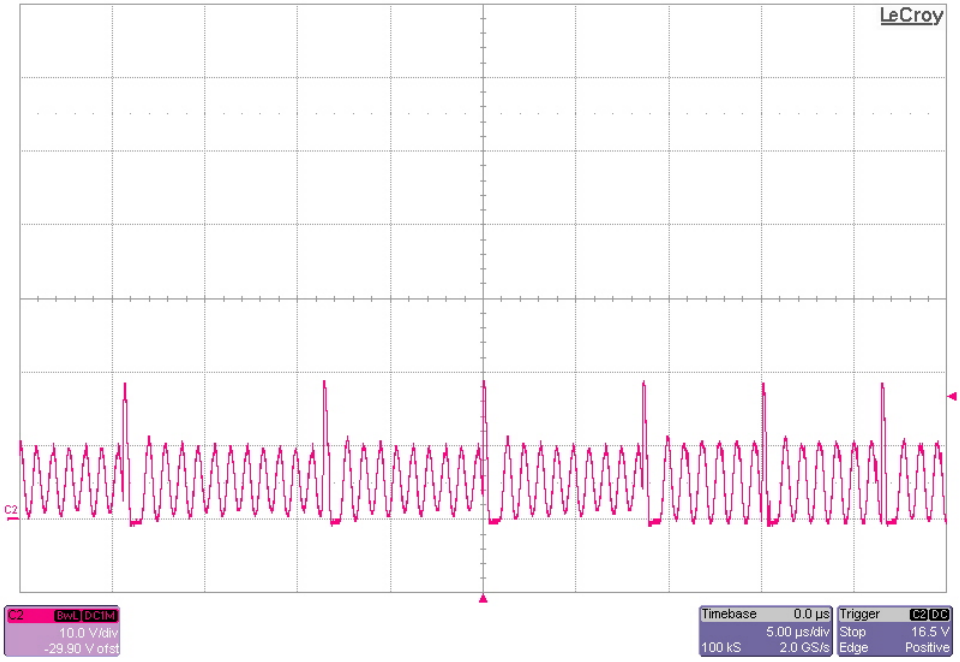
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 32V and a 0A load. (10V/DIV, 2uS/DIV)



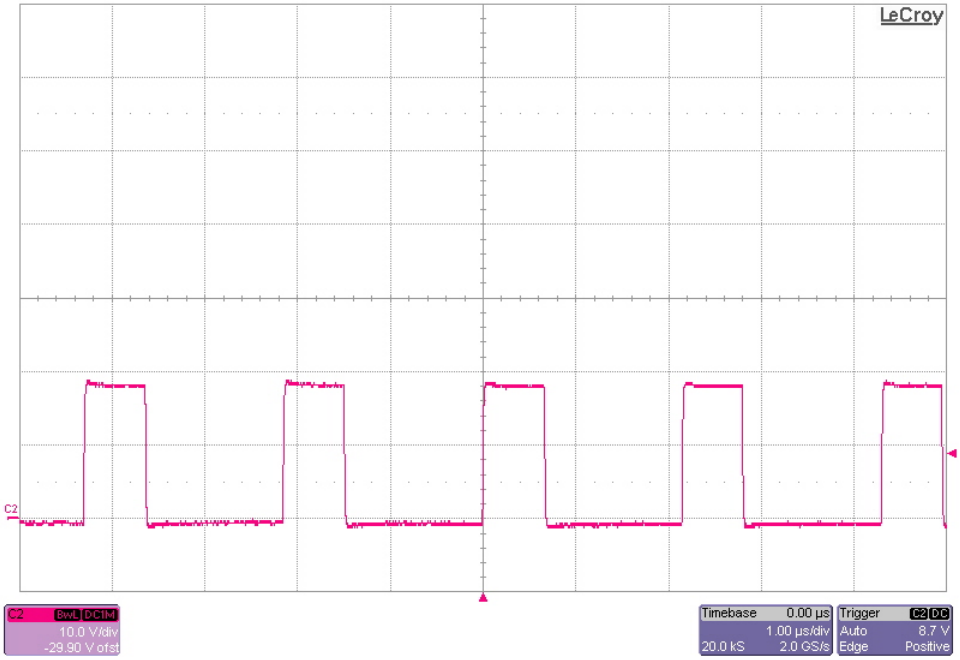
The photo below shows the FET switching voltages (TP15 and TP16) for an input voltage of 32V and a 60A load. (10V/DIV, 2uS/DIV)



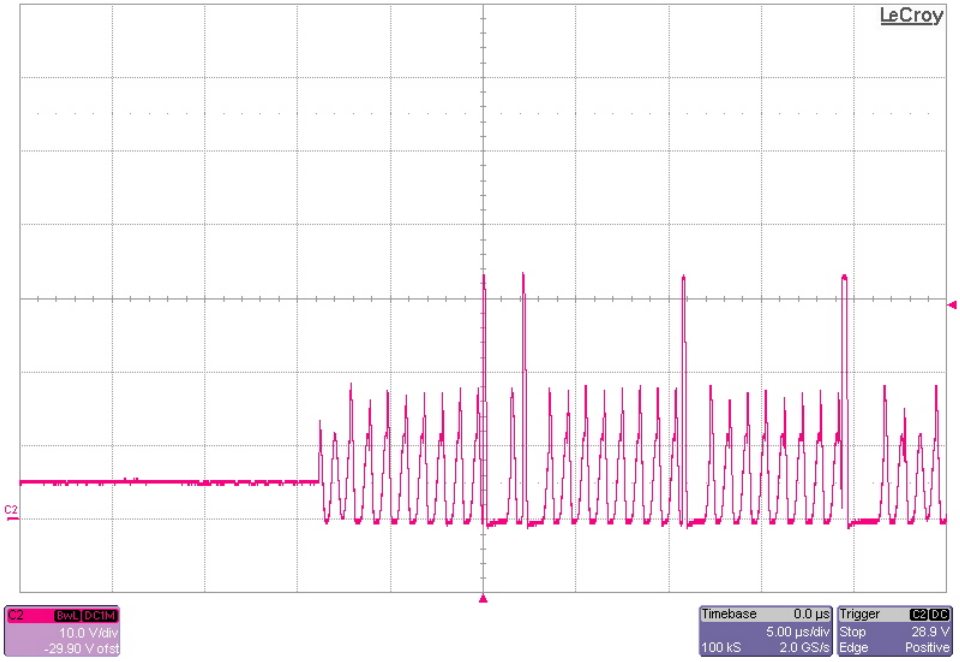
The photo below shows the TPS54060 5V bias supply FET switching voltages (TP5) for an input voltage of 18V and 0A load. (10V/DIV, 5uS/DIV)



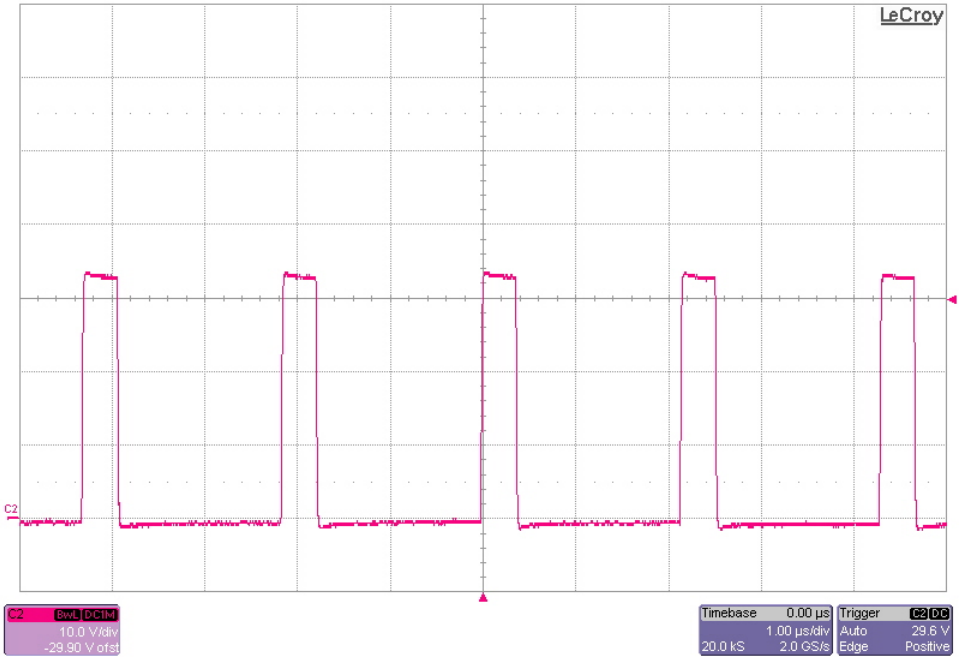
The photo below shows the TPS54060 5V bias supply FET switching voltages (TP5) for an input voltage of 18V and with a 0.5A external load. (10V/DIV, 1uS/DIV)



The photo below shows the TPS54060 5V bias supply FET switching voltages (TP5) for an input voltage of 32V and 0A load. (10V/DIV, 5uS/DIV)



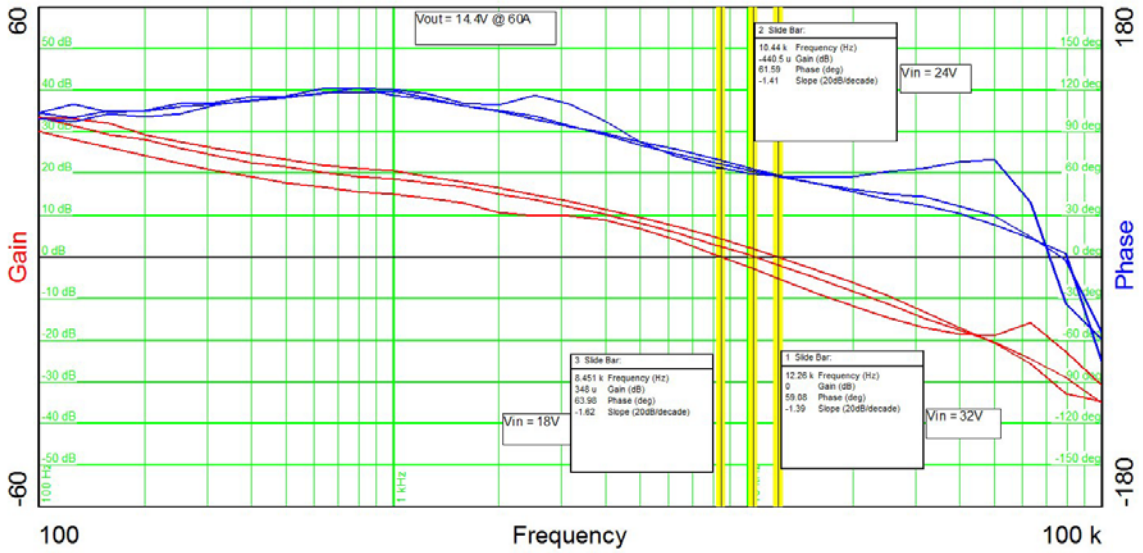
The photo below shows the TPS54060 5V bias supply FET switching voltages (TP5) for an input voltage of 32V and with a 0.5A external load. (10V/DIV, 1uS/DIV)



7 Loop Gain

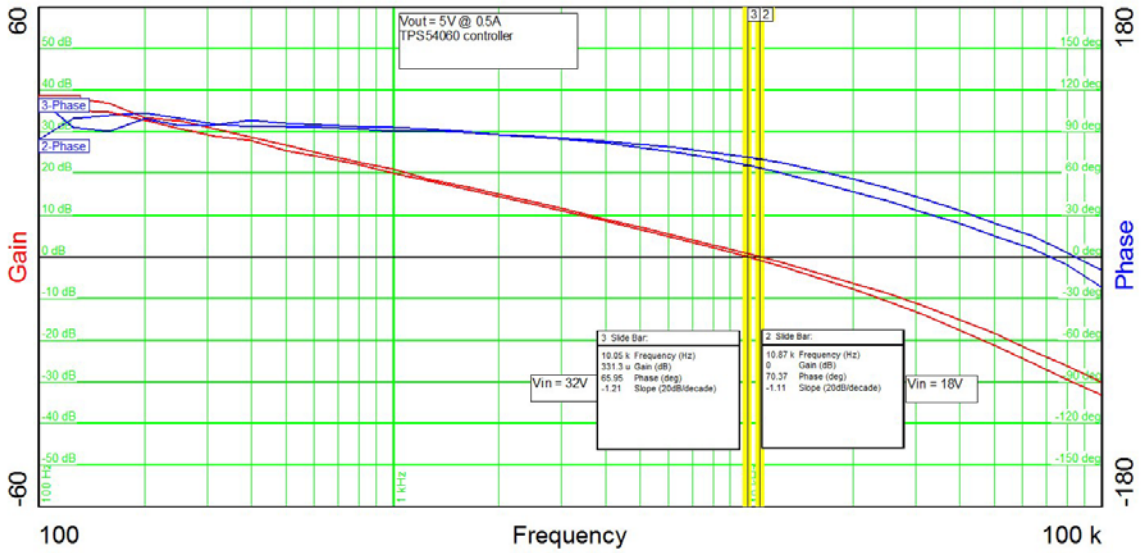
The plot below shows the LM5119 loop gain for input voltage of 32V, 24V and 18V. The output was set to 14.4V at 60A.

Loop Gain (Vin = 32V)	BW: 12.26KHz	PM: 59 degrees
Loop Gain (Vin = 24V)	BW: 10.44KHz	PM: 62 degrees
Loop Gain (Vin = 18V)	BW: 8.45KHz	PM: 64 degrees



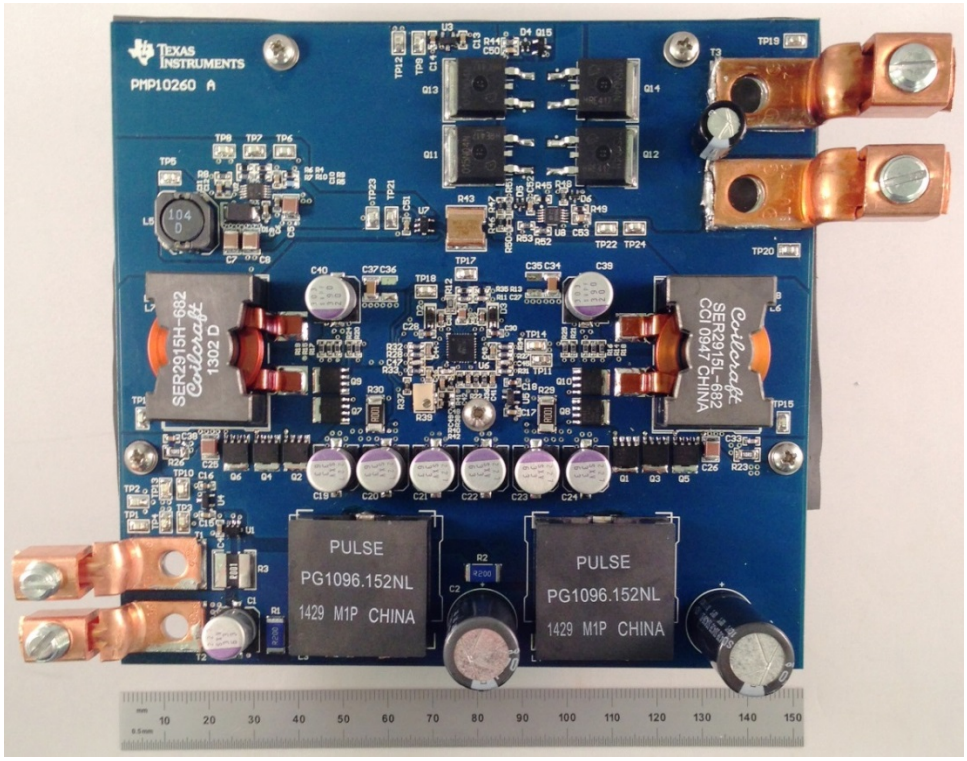
The plot below shows the TPS54060 5V bias supply loop gain for input voltage of 18V and 32V. The output was loaded to 0.5A.

Loop Gain (Vin = 32V)	BW: 10.05KHz	PM: 66 degrees
Loop Gain (Vin = 18V)	BW: 10.87KHz	PM: 70 degrees



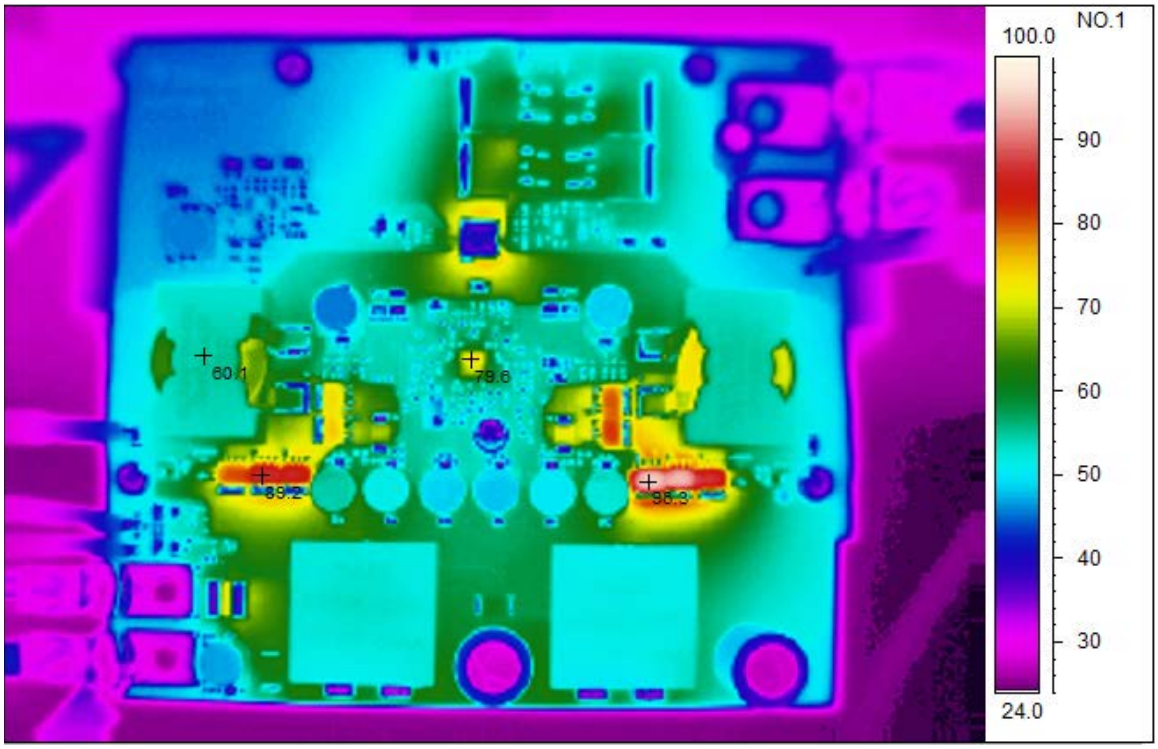
8 Photo

The photo below shows the PMP10260 REVB assy.

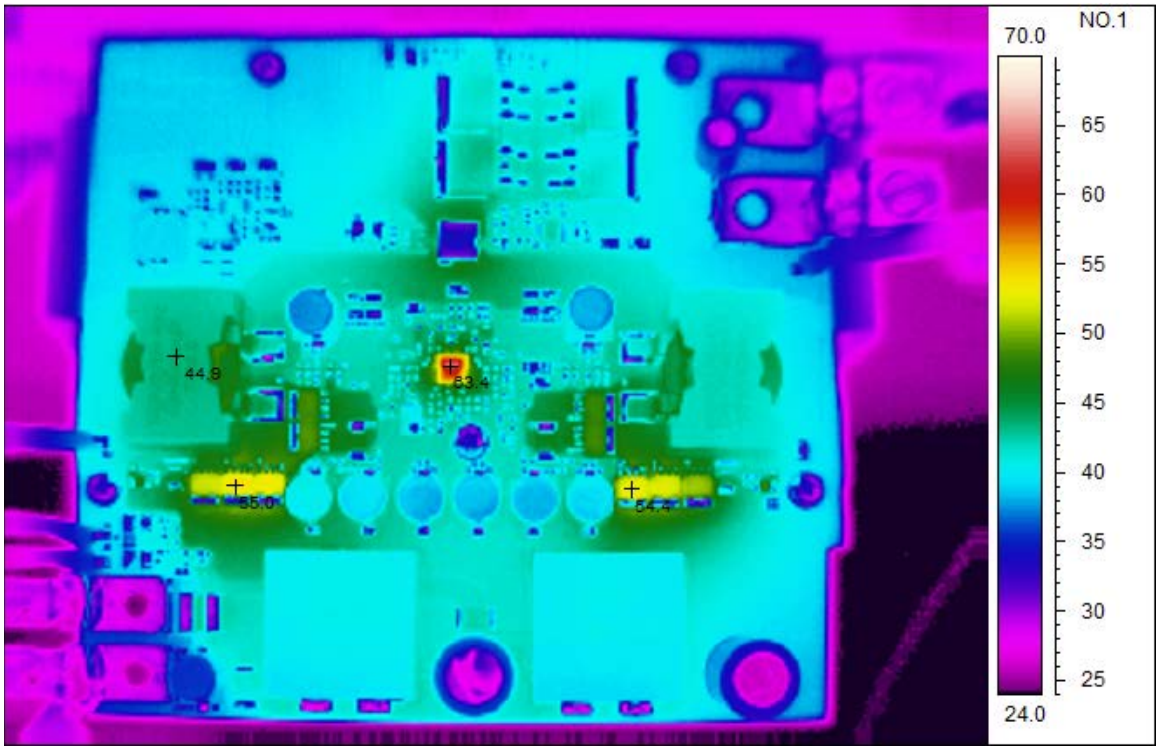


9 Thermal Image

A thermal image is shown below operating at 24V input and 14.4V@60A output (room temp, no airflow).



A thermal image is shown below operating at 24V input and 14.4V@30A output (room temp, no airflow).



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