TI Designs

Getting Power from Earphone Jack

Design Overview

This circuit is designed to power a small system attached to smartphone audio jack. The audio jack is power-limited and can output square or sine signal. The reference design includes a charge pump and a boost converter. The charge pump is used to filter AC output of one audio channel into a DC voltage and the ultra-low quiescent current boost converter TPS610981 is used to generate a regulated 3.3V. This reference design can work at a minimum 0.4V (peak) audio output sine (or square) signal and 2.2V biased voltage for micro-phone. The whole solution size is only 2.3 cm^2.

Design Features

- 0.4V to 2.2Vac (peak) input voltage range
- 3.3V and more than 1mA output current capability with 0.4Vac (peak) input
- Small solution size
- Smartphone remote control
- E-bank
- Mobile payment
- Sensor

Design Resources

Design Page	All Design files
TPS610981	Datasheet
LMV7271	Datasheet
CSD17483F4	Datasheet

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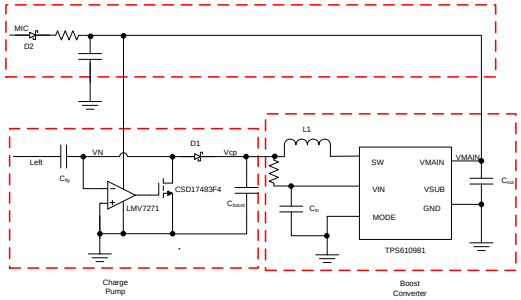

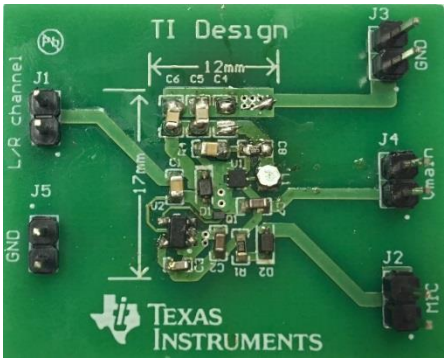

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1 Key System Specifications

Table 1: System Specification

Specification	Test condition	Value
Input Voltage range	-40 ~85°C	0.4V-2.2Vac (peak)
Output voltage range	-40 ~85°C	3.2V-4.4V
Output Current	-40 ~85°C	>1mA

2 System Description

The audio earphone jack is a common interface port in smartphone. Some smartphone APPs can work with hardware accessories through the earphone jack. The accessories can be e-bank, mobile payment, remote control and sensor. The reference design implements a power supply solution using the audio signal from the earphone jack for an accessory attached.
The standard 3.5mm audio plug contains 4 traces as shown in figure 1:

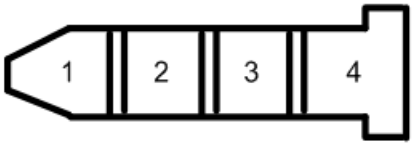

Figure 1: Audio Plug

Where

1. Left earphone (output)
2. Right earphone (output)
3. Common ground
4. Microphone (input)

Figure 2 is a typical application block diagram of a low power accessory attached to the earphone jack. The right channel functions as the communication line. Signal from smartphone is transmitted to the sub-system. The left channel provides power for the whole system. The microphone receives information from sub-system. A typical sub-system consists of low power MCU and sensors.

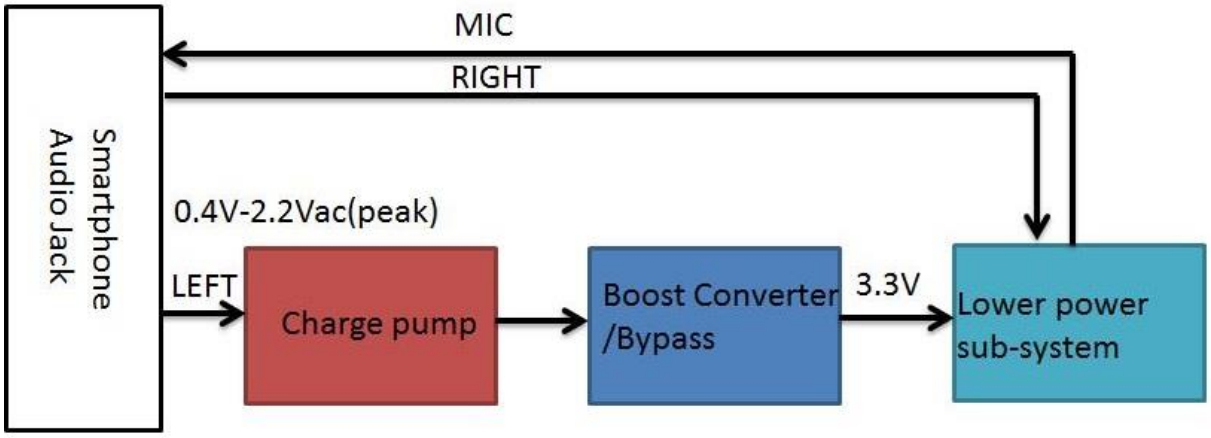

Figure 2: Application Block Diagram

The earphone jack power supply reference design is realized with the ultra-low power boost converter TPS610981 and a charge pump as shown in Figure 3. To improve the efficiency of the charge pump, a low threshold voltage NMOS FET is used to replace the traditional diode, controlled by a low power comparator LMV7271.
The minimum startup voltage of TPS610981 is 0.7V. After the startup phase is finished, the input voltage can be as low as 0.4V. The quiescent current of the TPS610981 is 300nA under no load condition.

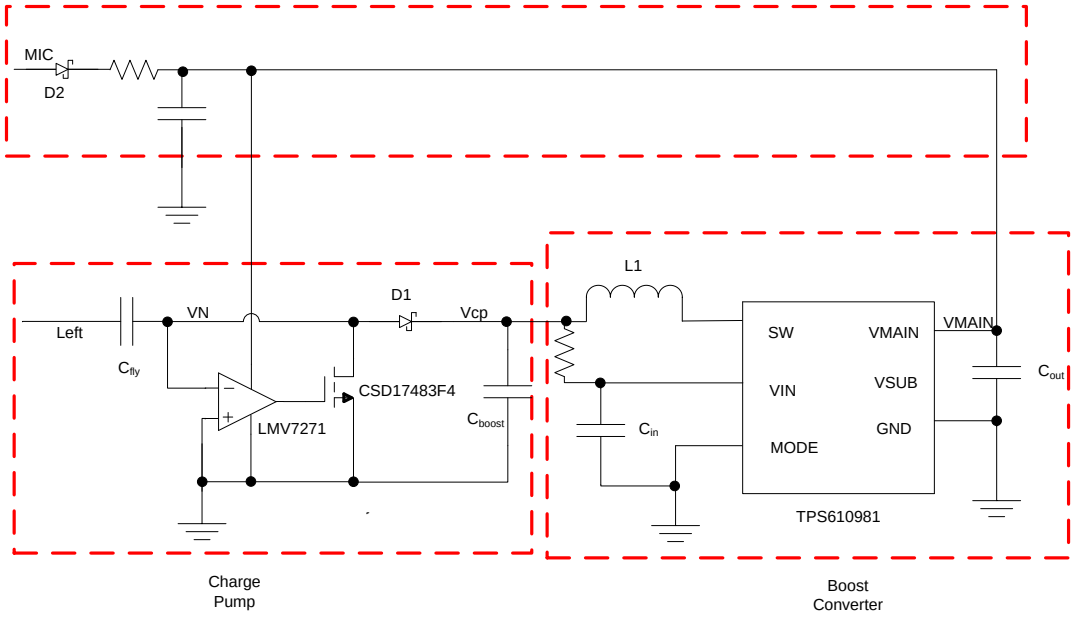

Figure 3: System Implementation

2.1 LMV7271

The LMV7271 is a rail-to-rail input low power comparator. It consumes only 9-µA supply current while achieving 800-ns propagation delay.
The LMV7271 is available in SC70 and SOT-23 packages. With this tiny package, the PCB area can be significantly reduced. It is ideal for low voltage, low power, and space-critical designs.
The LMV7271 features a push-pull output stage which allows operation with minimum power consumption when driving a load.

2.2 TPS610981

The TPS610981 is an ultra-low power solution for products powered by coin battery, one-cell Li-Ion battery, or Li-polymer battery. It integrates a low-dropout linear regulator (LDO) with a boost converter and provides two output rails. The boost output VMAIN is designed as an always-on supply for a main system, and the LDO output VSUB is to power peripheral devices.
The TPS610981 has two modes controlled by the MODE pin: active mode and low power mode. In active mode, both outputs are enabled with enhanced response performance. In low power mode, the LDO is disabled to disconnect peripherals. The TPS610981 consumes only 300nA quiescent current.
The TPS610981 supports automatic pass-through function. When input voltage is higher than a pass-through threshold, the boost converter stops switching and passes the input voltage to VMAIN rail; when input voltage is lower than the threshold, the boost works in boost mode and regulates output at the target value.
The TPS610981 can provide up to 50 mA total output current at 0.7 V input to 3.3 V output conversion. The boost is based on a hysteretic controller topology using synchronous rectifier to obtain maximum efficiency at minimal quiescent current.
The TPS610981 is available in 1.5 mm × 1.5 mm WSON package to enable small circuit layout size.

2.3 CSD17483F4

The CSD17483F4 N-Channel MOSFET is a tiny footprint NMOS. The maximum $V_{GS(th)}$ is 1.1V and the drain-source voltage limit is 30V. CSD17483F4 is very good for this application with 0.21ohm typical on resistance at VGS=3.3V.

3 System Design Theory

3.1 Charge pump

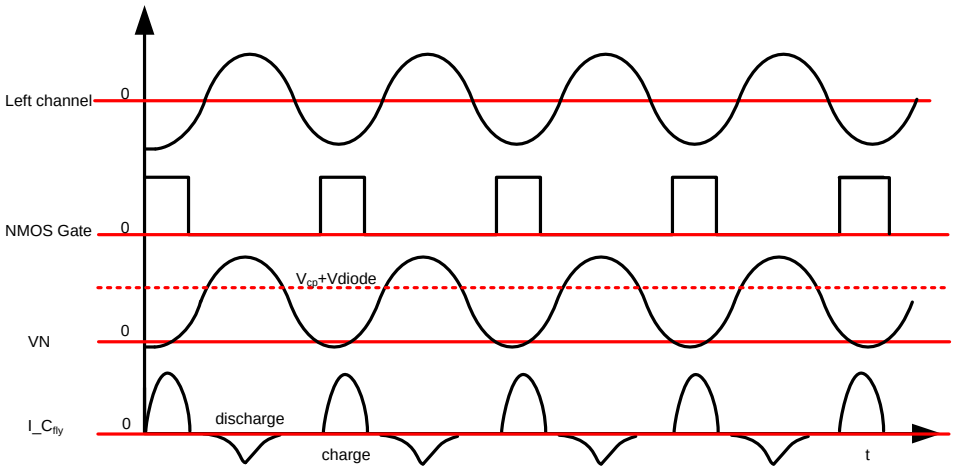

Figure 4: Typical Waveforms of the Charge Pump

The charge pump is used to filter AC input from the left channel to DC voltage. Typical waveforms are shown in figure 4. Three phases are included: charge phase, discharge phase and hold phase.

3.1.1 Operating Principle

Phase 1—Charge phase

After the hold phase, the left channel goes down. VN will follow down and once VN goes below zero, the comparator LMV7271 will be triggered and output high voltage to turn on the NMOS FET. Charge will be stored on the C_{fly}, the voltage across the capacitor V_{fly} will ramp up. The simplified circuit is shown in figure 5. When VN goes higher than zero, LMV7271 will turn off the NMOS FET and the charge phase finished.

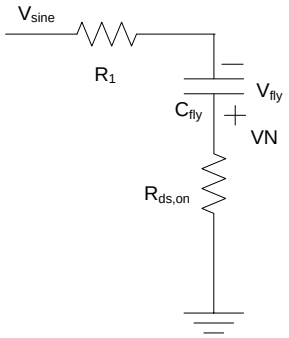

Figure 5: NMOS ON

Phase 2—Discharge phase

After the charge phase, V_{fly} is constant, VN will follow up with the input—V_{sine}. Once VN reaches V_{cp} plus Vdiode (the diode forward voltage), energy stored in the C_{fly} will be delivered to the output cap C_{boost} and the following boost converter. The simplified circuit is shown in figure 6. When VN is lower than V_{cp} plus Vdiode, D1 will block the path from V_{cp} to VN, discharge phase finished.

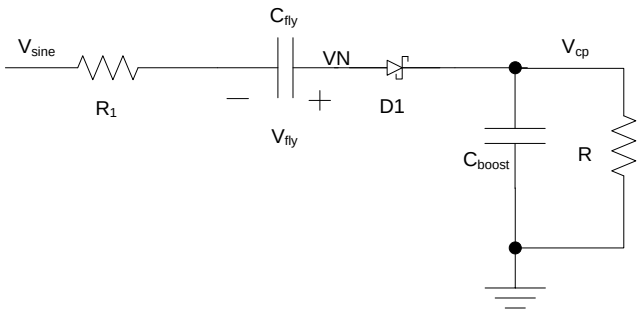

Figure 6: NMOS OFF

Phase 3—Hold phase

The period between the charge phase and discharge phase is the hold phase. During this period, both the NMOS and schottky diode are off, V_{fly} is constant. The capacitor C_{boost} will deliver the energy to the following boost converter.

3.2 Boost Converter

Figure.3 shows the boost converter to power the sub-system based on the TPS610981. The MODE pin is grounded, then VMAIN will be regulated at 3.3V and the ultra-low power mode is enabled. When input voltage is higher than VMAIN, TPS610981 will automatically switch to bypass mode. The detail operating principle can be found in the datasheet (SLVS873B).

For this application, the input voltage can go as low as 0.4V after the startup phase. With a chosen minimum input voltage of 0.4V, output current of 1mA and efficiency of 60%, the input current is 13.75mA.TPS610981 has the peak current at 350mA (minimum) which is enough to cover the worst case. This application operates in burst mode. A 4.7uH inductor with small package size 1608 or 2016 is preferred.

A 10uF 6.3V ceramic capacitor is selected as the output capacitor.

3.3 Auxiliary Power Supply Circuit

The simplified circuit of the auxiliary power supply circuit is shown in figure 7. This part can be removed if the input sine peak voltage is higher than 0.65V. Before the input voltage of TPS610981 ramps up, current will directly flow through the schottky diode D2 to VMAIN from the MIC input. VMAIN should be charged to 1.8V to start the comparator and TPS610981.The current path will be blocked when the TPS610981 enters normal operation and VMAIN outputs 3.3V. The resistor R_{mic} of 100 ohm is reasonable if the MIC bias voltage is 2.2V.

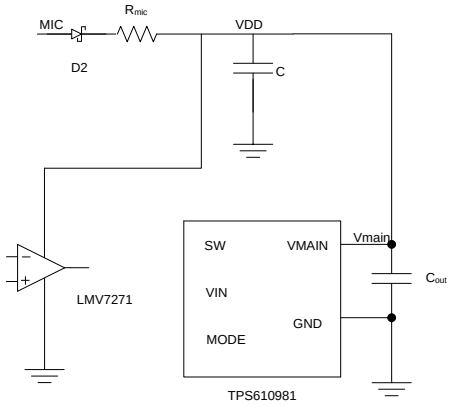

Figure 7: Auxiliary Circuit

4 Getting Started Hardware

4.1 Schematic

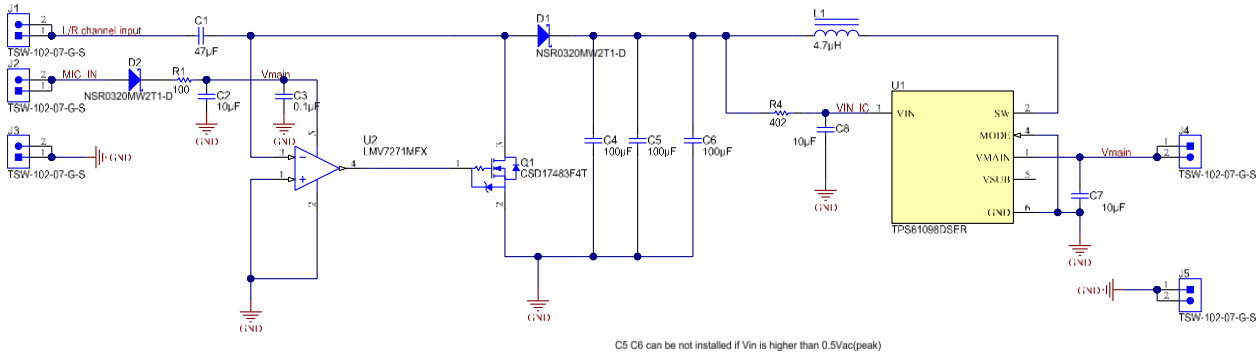

Figure 8: Schematic of the Reference Design

The schematic of the whole power supply system is shown in Figure.8. Attentions should be paid on if the peak value of the input sine signal is less than 0.5V.

1. At least one of C5 and C6 must be installed.
2. The diodes D_1 and D_2 should have a low forward voltage(<=0.25V at TA=25°C,I_D=10mA)

4.2 Bill of Materials

Table 2: Bill of Materials

Designator	Quantity	Value	Description	Package	PartNumber	Manufacturer
C1	1	47uF	CAP, CERM, 47 µF, 6.3 V, +/- 20%, X5R, 0603	0603	GRM188R60J476M	Murata
C2, C7, C8	3	10uF	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	0603	C0603C106M9PACTU	Kemet
C3	1	0.1uF	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X5R, 0402	0402	GRM155R60J104KA01D	Murata
C4, C5, C6	3	100uF	CAP, CERM, 100 µF, 4 V, +/- 20%, X5R, 0805	0805_HV	GRM21BR60G107ME15L	Murata
D1, D2	2		Diode, Schottky, 20 V, 1 A, SOD-323	sod-323	NSR0320MW2T1-D	ON Semi
J1, J2, J3, J4, J5	5		Header, 100mil, 2x1, Gold, TH	TSW-102-07-G-S	TSW-102-07-G-S	Samtec
L1	1	4.7uH	Inductor, Wire wound, 4.7 µH, 0.95 A, 0.38 ohm, SMD	MAKK2016	MAKK2016T4R7M	Taiyo Yuden
Q1	1		MOSFET, N/P-CH, 30 V, 1.5 A, 1.0x0.35x0.6mm	YJC0003A	CSD17483F4T	TI
R1	1	100	RES, 100, 1%, 0.1 W, 0603	0603	CRCW0603100RFKEA	Vishay
R4	1	402	RES, 402, 1%, 0.1 W, 0603	0603	CRCW0603402RFKEA	Vishay
U1	1		Low Input Voltage Synchronous Boost with ultra-Low Quiescent Current and Integrated LDO/Load Switch, DSE0006A	WSON	TPS610981DSE	TI
U2	1		Single 1.8V Low Power Comparators with Rail-to-Rail Input	SOT23	LMV7271MFX	TI

5 Test Data

Typical values are at Vsine = 0.4V (peak), Ta=25°C, unless otherwise noted.

5.1 Output Capability

Table 3: Max Output Capability with Different Audio Waveforms

All done with C_{boost}=200uF, C_{fly}=47uF,Ta=-40°C

Peak value of input voltage (V)	Load capability for Sine (mW)	Load capability for Square with 50% duty (mW)
0.4	8.8	13
0.45	17	21
0.5	25	28
0.55	35.5	38
0.6	48.5	51
0.7	75	82

5.2 Startup Waveform

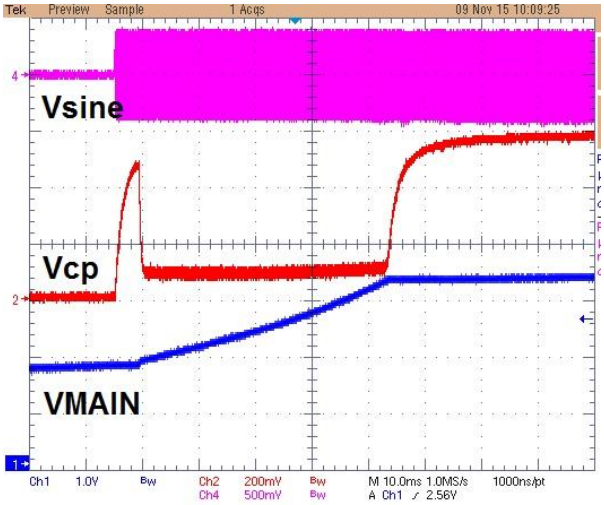

Figure 9: No Load Startup with VMAIN Pre-biased by MIC Voltage

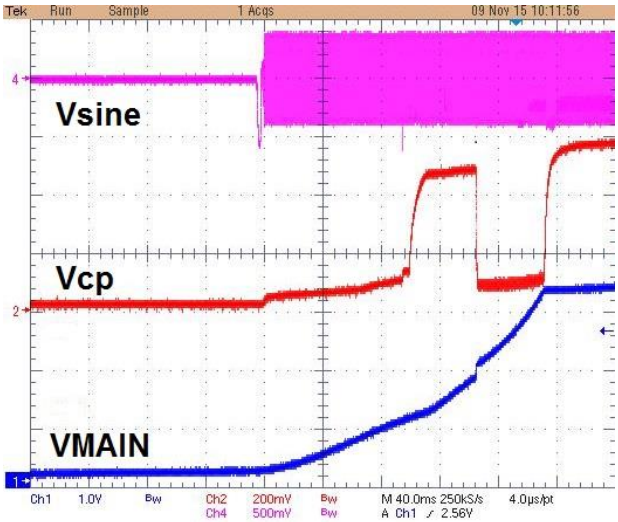

Figure 10: No Load Startup

5.3 Switching waveform

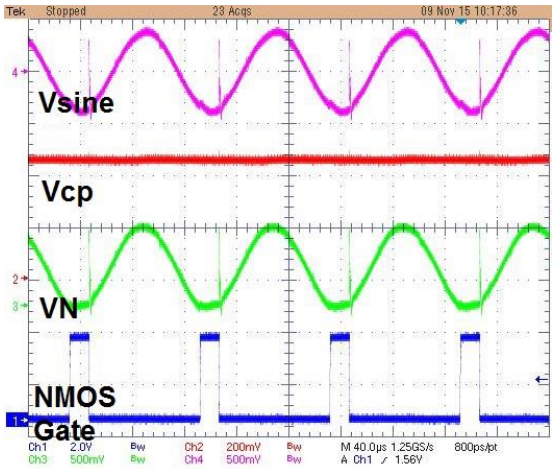

Figure 11: Rload=3.3K Ohm, Charge Pump Switching

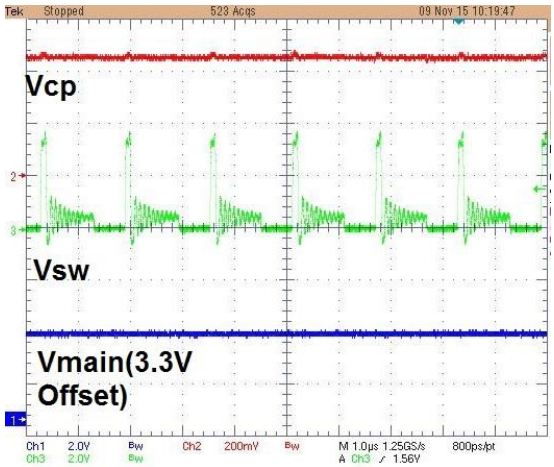

Figure 12: Rload=3.3K Ohm, Boost Converter Switching

5.4 Load Transient

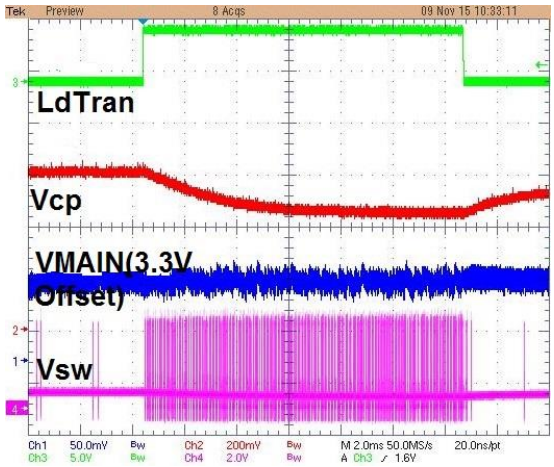

Figure 13: Iout=0-1mA-0

6 Design Files

6.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/PMP9777

6.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/PMP9777

6.3 PCB Layout Recommendations

6.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/PMP9777

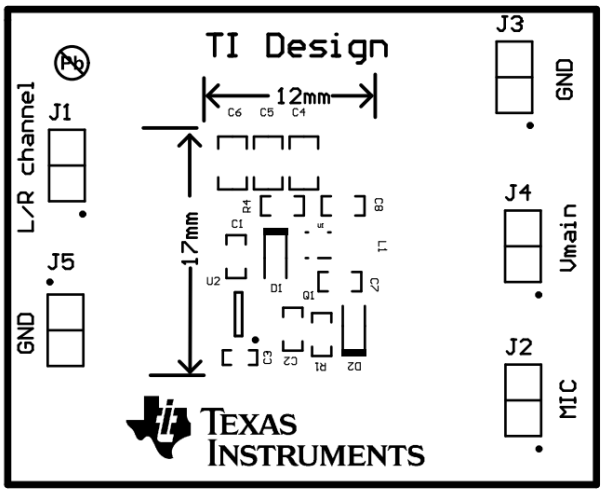

Figure 14: PMP9777 Top Overlay

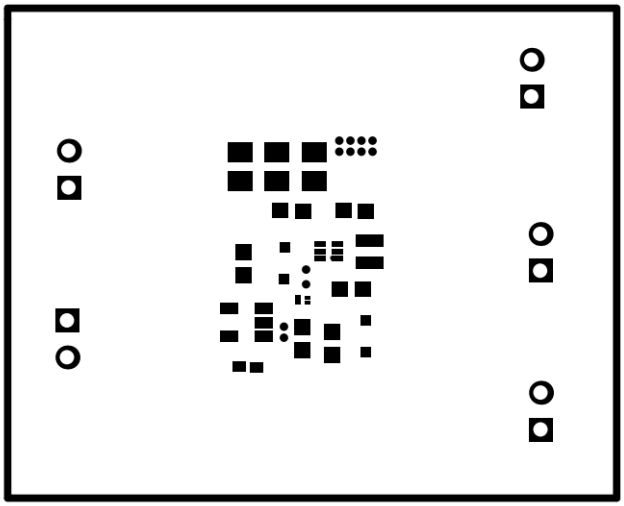

Figure 15: PMP9777 Top Solder Mask

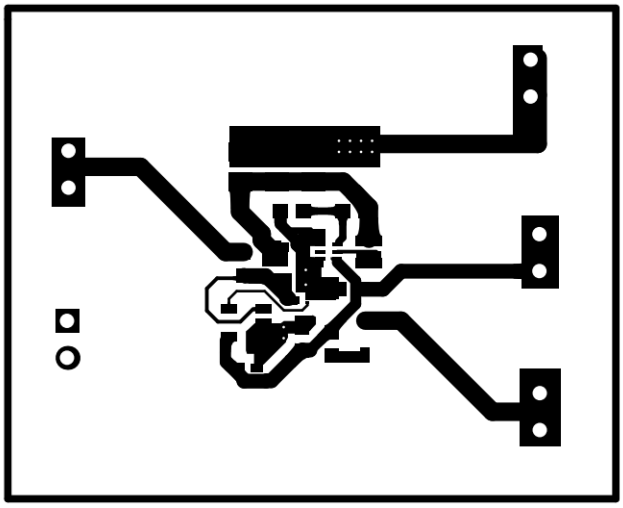

Figure 16: PMP9777 Top Layer

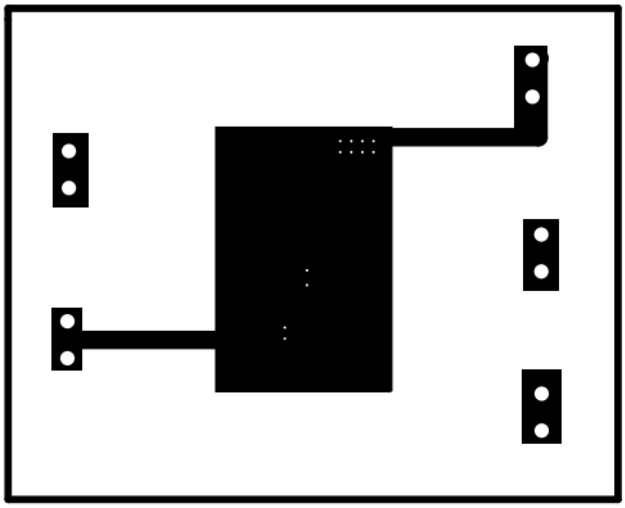

Figure 17: PMP9777 Bottom Layer

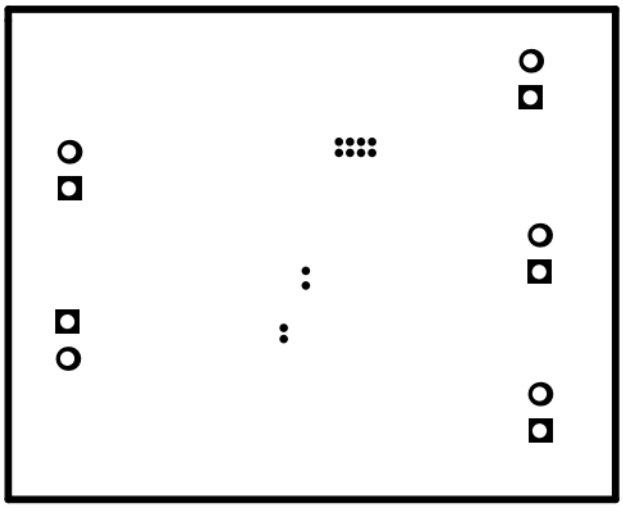

Figure 18: PMP9777 Bottom Solder Mask

6.4 Altium Project

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6.5 Gerber files

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6.6 Assembly Drawings

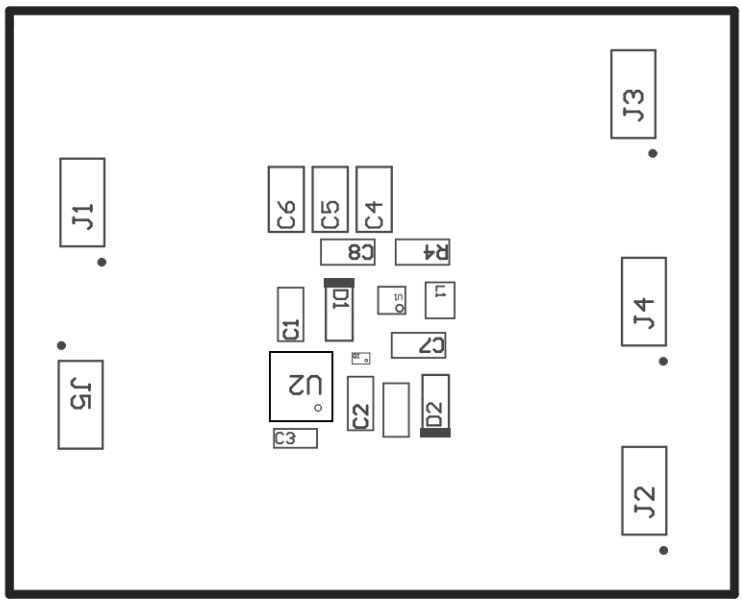

Figure 19: PMP9777 Assembly Drawing

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