

Testing performed with 48V input, maximum loads and 20MHz bandwidth unless noted.

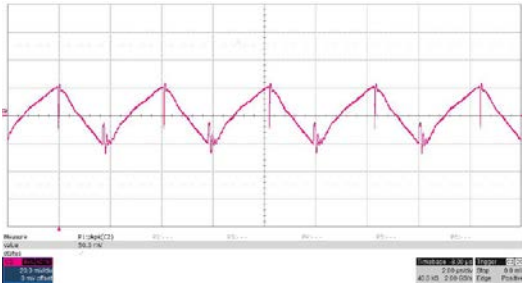
Efficiency and Regulation

The efficiency and regulation is shown below:

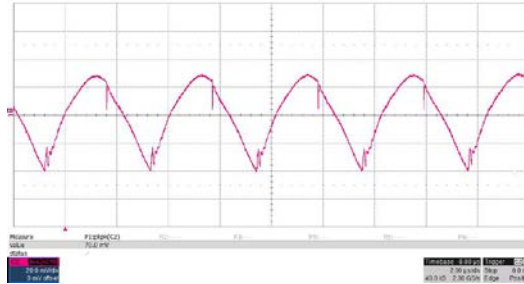
3.3V	3.3V	5V	5V	J1	J1	J1	%
Iout	Vout	Iout	Vout	Iin	Vin	Eff	Load
0.00	3.314	0.00	5.010	0.035	48.00	0.0%	0%
0.25	3.314	0.25	5.012	0.077	48.00	56.3%	~10%
0.50	3.314	0.50	5.014	0.121	48.00	71.7%	~20%
0.75	3.313	0.75	5.015	0.164	48.00	79.3%	~30%
1.00	3.313	1.00	5.017	0.208	48.00	83.4%	~40%
1.25	3.313	1.25	5.020	0.252	48.00	86.1%	~50%
1.50	3.312	1.50	5.022	0.297	48.00	87.7%	~60%
1.75	3.312	1.75	5.024	0.342	48.00	88.9%	~70%
2.00	3.312	2.00	5.026	0.388	48.00	89.5%	~80%
2.25	3.312	2.25	5.028	0.434	48.00	90.1%	~90%
2.50	3.312	2.80	5.020	0.514	48.00	90.5%	100%
2.50	3.312	0.00	5.117	0.210	48.00	82.1%	Max/Min
0.00	3.314	2.80	4.913	0.326	48.00	87.9%	Min/Max

Ripple and Noise

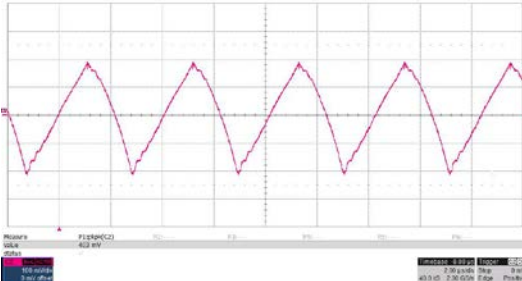
3.3V Ripple (C23)
 20mV/div, 2usec/div
 Measured 50mVpp:



5V Ripple (C13)
 20mV/div, 2usec/div
 Measured 70mVpp:



Input Ripple (C4)
 100mV/div, 2usec/div
 Measured 403mVpp:

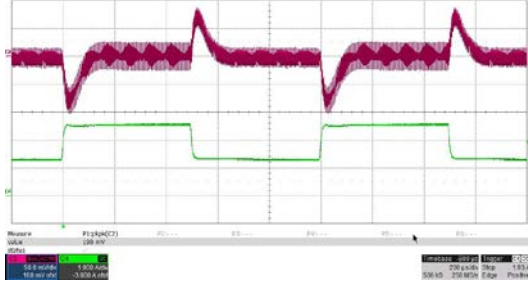


Input Ripple (J1)
 20mV/div, 2usec/div
 Measured 19.3mVpp:



Dynamic Loading

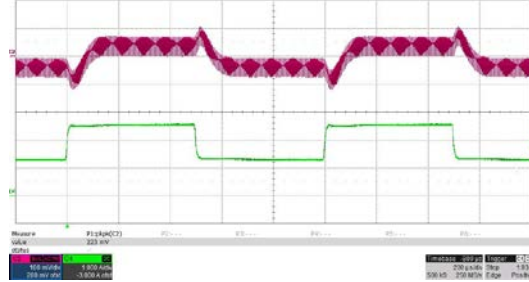
3.3V load step, 3.3V response
1.25A to 2.5A load step
50mV/div, 1A/div, 200usec/div
Slew Rate = 200mA/usec
Measured 190mVpp across C13:



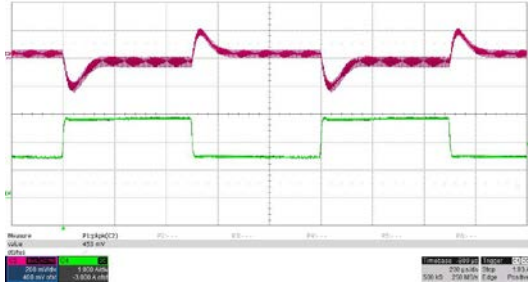
3.3V load step, 5V response

100mV/div

Measured 223mVpp across C23:



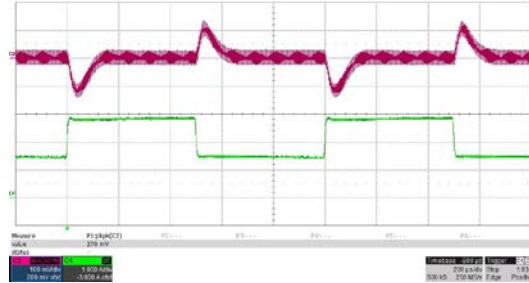
5V load step, 5V response
1.4A to 2.8A load step
200mV/div, 1A/div, 200usec/div
Slew Rate = 200mA/usec
Measured 453mVpp across C23:



5V load step, 3.3V response

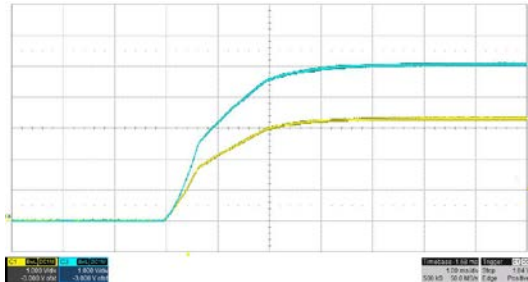
100mV/div

Measured 270mVpp across C13:

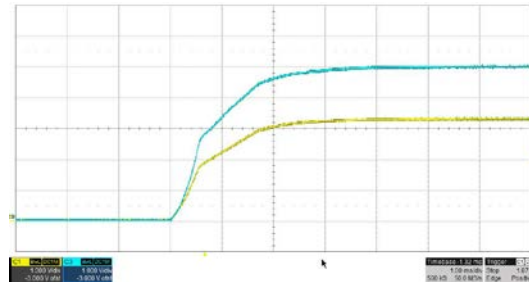


Turn On Response

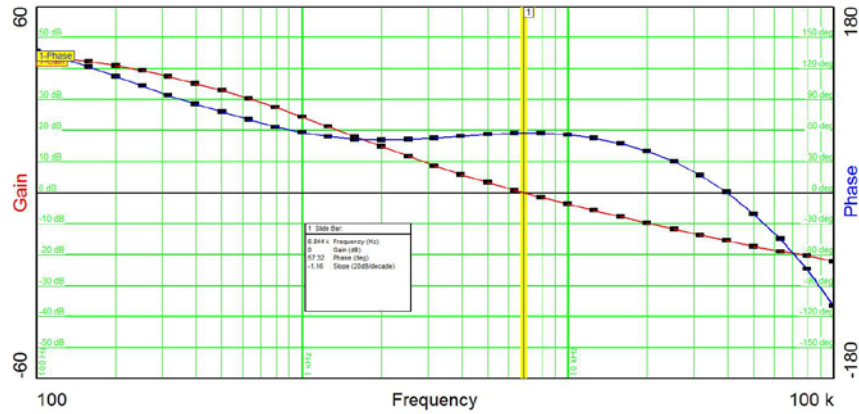
Max Loads, 1msec/div, 1V/div:



0A Loads, 1msec/div, 1V/div:



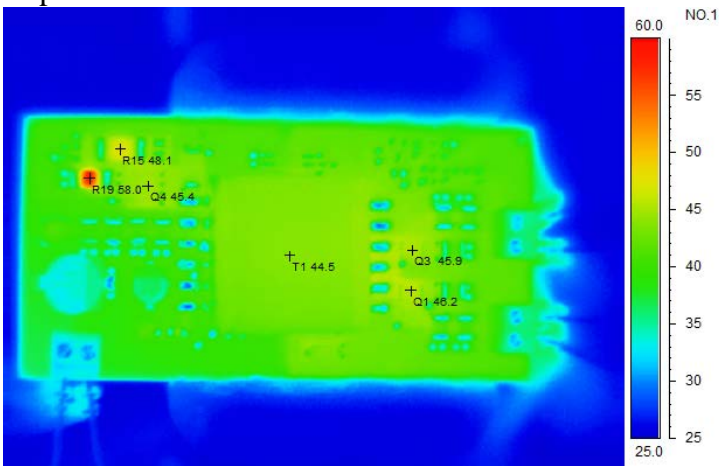
Loop Stability



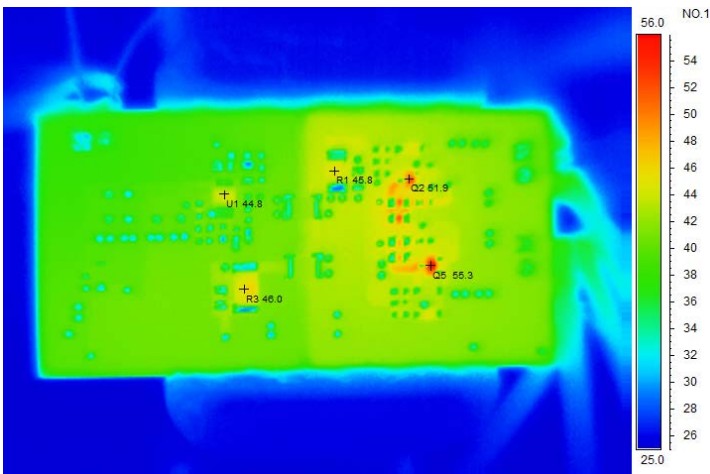
Bandwidth= 6.8 kHz Phase Margin=57 degrees Gain Margin=15dB

Thermal Plots

Top:

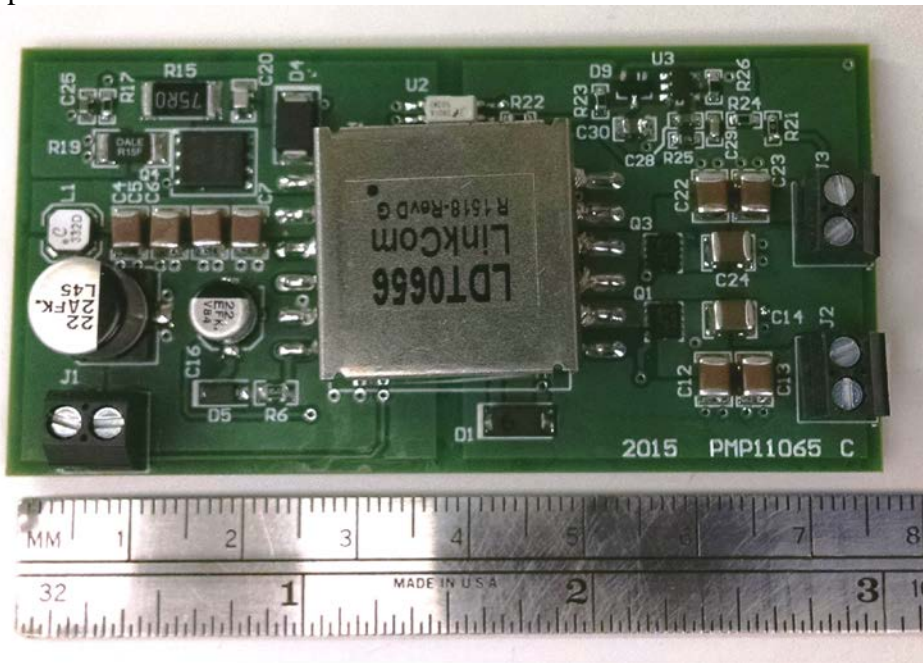


Bottom:

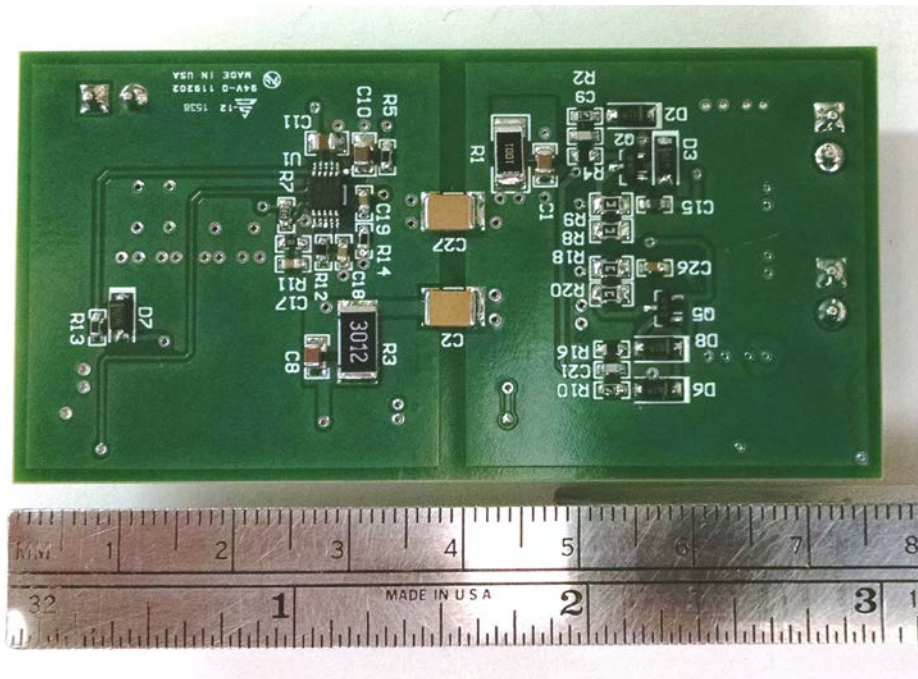


Photo

Top:



Bottom:



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