TI Designs

TIDA-00845: Reference Design of Two-Port Automotive USB 2.0 Hub with Short-to-Battery Protection

0.1 Design Overview

TIDA-00845 is comprised of the TUSB4020BI-Q1, a two-port USB 2.0 hub, with short-to-battery (STB), and short-circuit protection on both downstream ports provided by the TPD3S714-Q1. Downstream Port 1 (DP1) includes a STB tester for applying 18-V DC, using two TPD3S714-Q1s to protect both the hub and a peripheral, for easily demonstrating pre-test and post-test functionality. Downstream Port 2 (DP2) represents a best practice design.

0.2 Design Resources

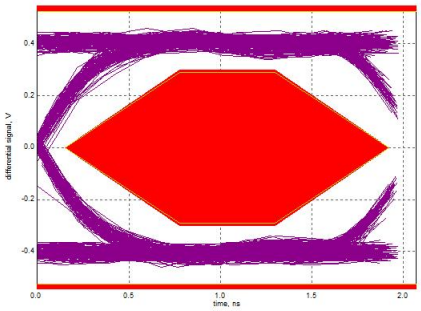
TIDA-00845	Design Folder
TPD3S714-Q1	Product Folder
TUSB4020BI	Product Folder
TPS7A4533	Product Folder
TPS74801	Product Folder
LMR14030	Product Folder

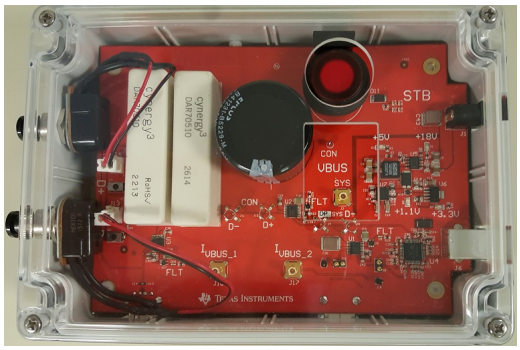
0.3 Design Features

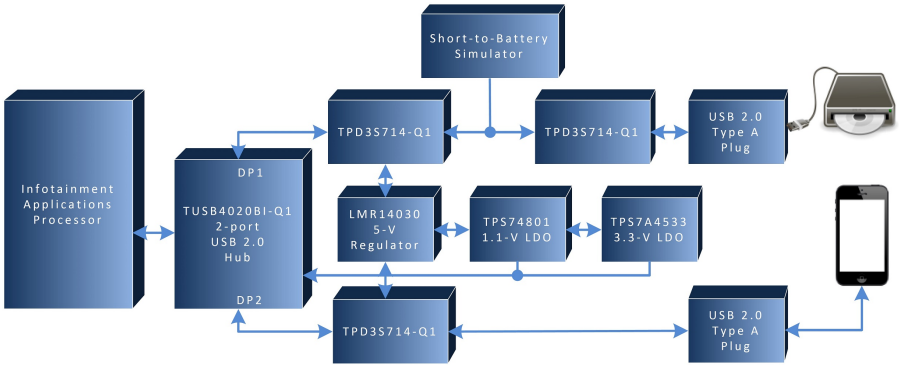
- Fully Functional USB Hub With Built-In Short-to-Battery Test Simulator on Downstream Port 1
- Supports USB 2.0 High-Speed Data Rates
- Short-to-Battery Protection (up to 18 V) on V_{BUS_CON}, VD+, VD-
- Short-to-Ground Protection on V_{BUS_CON} for Downstream Port 2
- Over-Current Protection Current Limit: 550 mA (min)
- IEC 61000-4-2 (Level 4) System Level ESD Protection at V_{BUS_CON}, VD+, VD-

0.4 Featured Applications

- Remote USB ports where short to battery is a concern such as Media Connection modules and Head Units with remote USB ports







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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
STB Response Time	TPD3S714-Q1 shuts off in 2 µs to protect the system from up to 18-V STB	See Section 3.1
ESD Protection	±8-kV contact and ±15-kV air-gap per IEC 61000-4-2	See Section 3.1
Built-in STB Tester	Built-in demonstration of the STB protection on DP1	See Section 4.1.3
Over-Current Protection	TPD3S714-Q1 limits current on V_{BUS} to 550 mA	See Section 3.1

2 Automotive USB 2.0 Hub with Short-to-Battery and Short-Circuit Protection

This automotive USB 2.0 hub has short-to-battery (STB), short-circuit, IEC 61000-4-2 ESD Level 4, and over-current protection. The USB 2.0 hub is the TUSB4020BI-Q1. The downstream ports (DP) are protected by the TPD3S714-Q1. DP1 includes a STB tester for demonstrating the protection from shorting the USB lines to 18-V DC. DP2 represents a best practice design for protecting a USB 2.0 hub with the TPD3S714-Q1. The upstream port (UP) has IEC 61000-4-2 Level 4 ESD protection provided by the TPD1E05U06.

2.1 TPD3S714-Q1

The TPD3S714-Q1 is a single-chip solution for automotive STB, short-circuit, IEC 61000-4-2 ESD, and over-current protection for USB 2.0 interfaces. The integrated data switches provide best-in-industry bandwidth for minimal signal degradation in USB 2.0 STB applications.

The STB protection protects against shorts up to 18 V, in both hot-plug and DC events. The over-voltage protection reacts very quickly, shutting off the switches and protecting the upstream transceiver from harmful voltage and current spikes. The integrated ESD protection provides system-level IEC 61000-4-2 Level 4 protection. The over-current protection automatically limits current to 550 mA, preventing the voltage from drooping below specification of the upstream V_{BUS} rail.

2.2 TUSB4020BI-Q1

The TUSB4020BI-Q1 is a two-port USB 2.0 hub. It provides USB high-speed/full-speed connections on the UP, and provides high-speed, full-speed, or low-speed connections on the two DPs. When the UP is connected to an electrical environment that supports high-speed and full-speed/low-speed connections, high-speed and full-speed/low-speed USB connectivity is enabled on the DPs. When the UP is connected to an electrical environment that only supports full-speed/low-speed connections, high-speed connectivity is disabled on the DPs.

2.3 LMR14030-Q1

The LMR14030-Q1 is a 40-V, 3.5-A step down regulator with an integrated high-side MOSFET. Featuring a wide input range from 4 V to 40 V, the LMR14030-Q1 is suitable for various applications from industrial to automotive, for power conditioning from unregulated sources. The regulator's quiescent current is 40 µA in sleep-mode, suitable for battery-powered systems. An ultra-low 1-µA current, while in shutdown mode, can further prolong battery life. A wide adjustable switching-frequency range allows either efficiency or external component size to be optimized. Internal loop compensation means the user is free from the tedious task of loop-compensation design. This feature also minimizes the external components of the device. A precision-enable input allows simplification of regulator control and system-power sequencing. The device also has built-in protection features such as cycle-by-cycle current limit, thermal sensing and shutdown due to excessive power dissipation, and output over-voltage protection.

2.4 TPS7A4533

The TPS7A4533 device is a low-dropout (LDO) regulator optimized for a fast transient response. The device can supply 1.5 A of output current with a dropout voltage of 300 mV. Operating quiescent current is 1 mA, dropping to less than 1 µA in shutdown mode. Quiescent current is well controlled; it does not rise in dropout as with many other regulators. In addition to fast transient response, the TPS7A45xx regulators have very low-output noise, making them ideal for sensitive RF supply applications.

The output voltage is 3.3 V. The TPS7A4533 regulator is stable with an output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal-protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection.

2.5 TPS74801-Q1

The TPS74801-Q1 LDO linear regulator provides an easy-to-use, robust, power-management solution for a wide variety of applications. The user-programmable soft-start minimizes stress on the input-power source by reducing the capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and an error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2 µF, and is fully specified from –40°C to 105°C for the DRC package, and from –40°C to 125°C for the RGW package. The TPS74801-Q1 is offered in a small 3-mm × 3-mm SON-10 package, yielding a highly compact, total solution size. It is also available in a 5 × 5 QFN-20 for compatibility with the TPS74401.

2.6 TPD1E05U06

The TPD1E05U06 is a unidirectional transient voltage suppressor (TVS) based ESD protection diode with ultra-low capacitance. The TPD1E05U06 can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 Level 4 international standard. The TPD1E05U06's ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

3 Block Diagram

This automotive USB 2.0 hub with STB protection has two DPs. DP1 has two TPD3S714-Q1s arranged so that when the STB simulator is engaged, applying 18 V to either V_{BUS} or the data lines, both the upstream hub and downstream peripheral are protected from the over-voltage. To accomplish this, the TPD3S714-Q1 protecting the peripheral attached to the USB 2.0 Type-A plug has the connector-side pins facing the hub, and the system-side data line pins facing the connector. The system-side data pins are not rated for IEC 61000-4-2 ESD, but for AEC-Q100 Classification H3 HBM of ±4 kV. To maintain IEC 61000-4-2 Level 4 ESD protection on the DP1, additional ESD protection has been added in the form of the TPD1E05U06, an IEC 61000-4-2 Level 4 rated ESD protection device. Despite the additional TPD3S714-Q1 and TPD1E05U06 on the DP1, the device is still capable of high-speed communication at 480 Mbps.

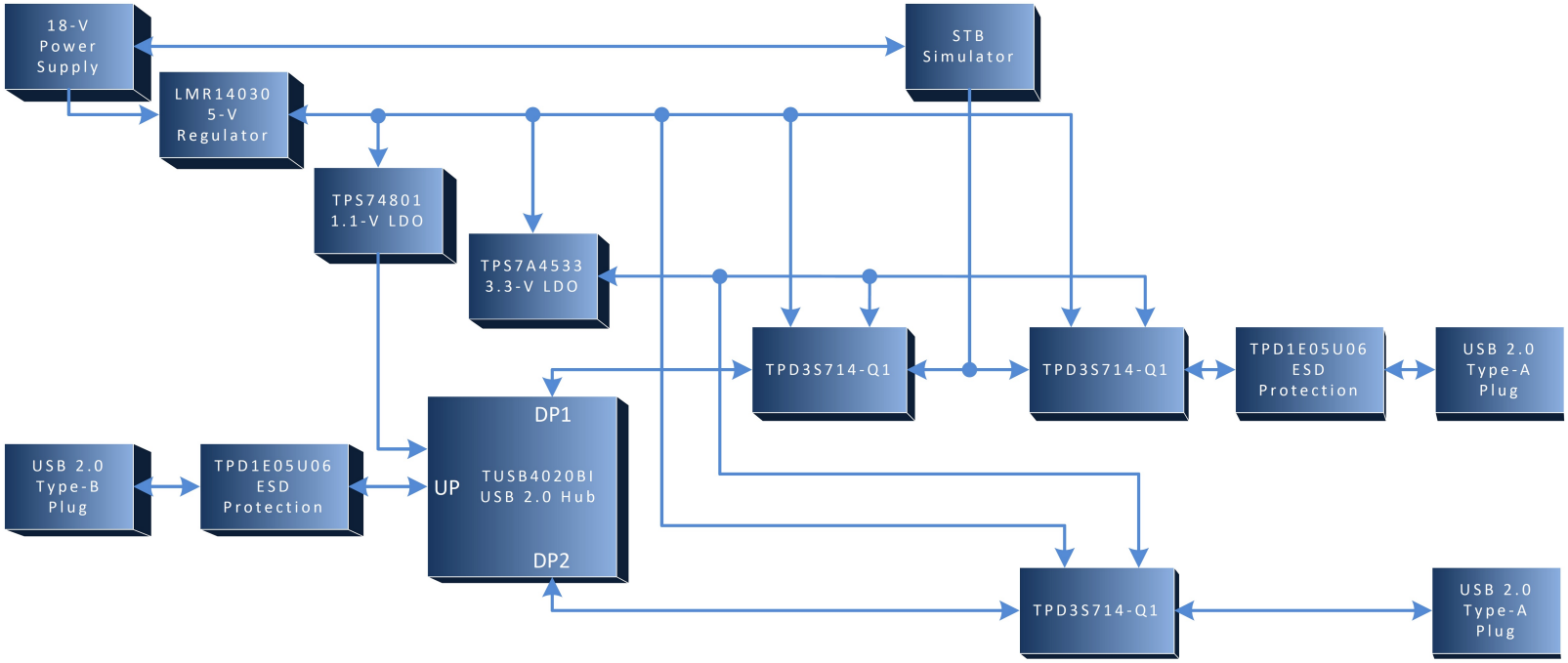

Figure 1. TIDA-00845 Functional Block Diagram

A single TPD3S714-Q1 protects the DP2, providing STB, short-to-ground, ESD, and over-current protection for the TUSB4020BI-Q1 USB 2.0 two-port hub. DP2 represents the reference design for a TPD3S714-Q1 protecting a USB 2.0 hub.

An external 18-V DC power supply provides power to the STB circuit and USB 2.0 hub circuitry. A step-down (Buck) regulator, LMR14030-Q1, steps down the 18 V to provide a 5-V rail for the two LDOs and V_{BUS} for the two DPs. The LDO TPS7A4533 provides the 3.3-V rail, and the LDO TPS74801-Q1 provides the 1.1-V rail.

3.1 TPD3S714-Q1

- AEC-Q100 Qualified (Grade 1)
  - –40°C to 125°C Operating Temperature Range
- STB Protection, up to 18 V, on V_{BUS_CON}, VD+, VD–
- Short-to-Ground Protection on V_{BUS_CON}
- Short-to-Bus Protection on VD+, VD–
- ESD Protection on V_{BUS_CON}, VD+, VD–
  - ±8 kV Contact Discharge (IEC 61000-4-2)
  - ±15 kV Air-Gap Discharge (IEC 61000-4-2)
- Low R_{ON} nFET V_{BUS} Switch
- High-Speed Data Switches
- Hiccup Current Limit
  - 550 mA Over-Current Limit (minimum)
- Integrated Input Enable for V_{BUS} and Data Lines
- Fault Output Signal
- Thermal Shutdown Feature
- 16-Pin DBQ Package (3.9 mm × 4.94 mm)
- STB Response Time of 2 µs (Typ) for V_{BUS}, and 200 ns for the Data Path

3.2 TUSB4020BI-Q1

- Two-Port USB 2.0 Hub
- USB 2.0 Hub Features:
  - Multi-Transaction Translator (MTT) Hub: Two Transaction Translators
  - Four Asynchronous Endpoint Buffers per Transaction Translator
- Per Port or Ganged Power Switching, and Over-Current Notification Inputs
- OTP ROM, Serial EEPROM, or I^2C or SMBus Slave Interface for Custom Configurations:
  - VID and PID
  - Port Customization
  - Manufacturer and Product Strings (not by OTP ROM)
  - Serial Number (not by OTP ROM)
- Application Feature Selection Using Terminal Selection, EEPROM/ or I^2C or SMBus Slave Interface
- Provides 128-Bit Universally Unique Identifier (UUID)
- Supports On-Board and In-System OTP or EEPROM Programming Through the USB 2.0 UP
- Single Clock Input, 24-MHz Crystal or Oscillator
- No Special Driver Requirements; Works Seamlessly on any Operating System With USB Stack Support
- 48-Pin HTQFP Package (PHP)

3.3 LMR14030-Q1

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C4A
- 4-V to 40-V Input Range
- 3.5-A Continuous Output Current
- Ultra-low 40-µA Operating Quiescent Current
- 90-mΩ High-side MOSFET
- Minimum Switch-On Time: 75 ns
- Adjustable Switching Frequency from 200 kHz to 2.5 MHz
- Frequency Synchronization to the External Clock
- Spread-Spectrum Option for Reduced EMI
- Internal Compensation for Ease of Use
- High-Duty Cycle Operation Supported
- Precision-Enable Input
- 1-µA Shutdown Current
- External Soft-Start
- Thermal, Over-voltage, and Short Protection
- 8-Pin HSOIC with PowerPAD™ Package

3.4 TPS7A4533

- Optimized for Fast Transient Response
- Output Current: 1.5 A
- High Output Voltage Accuracy: 1% at 25°C
- Dropout Voltage: 300 mV
- Low Noise: 35 μV_{RMS} (10 Hz to 100 kHz)
- High Ripple Rejection: 68 dB at 1 kHz
- 1-mA Quiescent Current
- Controlled Quiescent Current in Dropout
- Less Than 1-µA Quiescent Current in Shutdown
- Stable With 10-µF Ceramic Output Capacitor
- Reverse-Battery Protection
- Reverse-Current Protection

3.5 TPS74801-Q1

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device HBM ESD Classification Level C4B
- V_{OUT} Range: 0.8 V to 3.6 V
- Ultra-low V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range 2.7 V to 5.5 V
- Low Dropout: 60-mV typ at 1.5 A, V_{BIAS} = 5 V
- 2% Accuracy Over Line, Load, and Temperature

- Programmable Soft-Start Provides Linear-Voltage Startup
- V_{BIAS} Permits Low V_{IN} Operation with Good Transient Response
- Stable with Any Output Capacitor ≥ 2.2 µF
- Available in Small 3-mm × 3-mm × 1-mm SON-10, and 5 × 5 QFN-20 Packages

3.6 TPD1E05U06

- IEC 61000-4-2 Level 4 ESD Protection
  - ±12-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- IO Capacitance of 0.42 pF (Typ)
- DC Breakdown Voltage 6.5 V (minimum)
- Ultra-low Leakage Current of 10 nA (maximum) and 0.1 nA (typ)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to +125°C
- Easy Routing Package

4 System Design Theory

The TIDA-00845 two-port automotive USB 2.0 hub with STB and short-circuit protection highlights the TPD3S714-Q1, providing USB 2.0 DP protection against STB, short-circuit, IEC 61000-4-2 ESD Level 4, and over-current. To facilitate easy demonstration of the protection by the TPD3S714-Q1, a built-in STB tester can be used for live demonstrations of the STB on the DP1. By pressing either the S1, S2, or S3 switch, all together or individually, while the hub is attached to a personal computer with a peripheral (such as a webcam) and operating on the DP1, the functionality maintained after 18 V is applied to V_{BUS}, and-or the data lines demonstrate the capabilities of the TPD3S714-Q1. Equipment, such as an oscilloscope, can be optionally attached to record the STB event.

4.1 Downstream Port 1 (DP1)

4.1.1 TPD3S714-Q1 Upstream from Short-To-Battery Test

Figure 2 shows the TPD3S714-Q1 (U2) connected to the TUSB4020BI-Q1, following the data sheet guidelines of the TPD3S714-Q1. Additionally, test points for measuring system-side voltages on V_{BUS}, and the data lines during STB tests are provided by the SMB (J2) and high-impedance probe (J3 and J4) connectors. The SN74LVC1G125 (U8, see Figure 27) single-bus buffer gate compares the $\overline{FLT}$ pin logic of the TPD3S714-Q1 to the 3.3-V rail, and indicates a fault by illuminating the LED (D8).

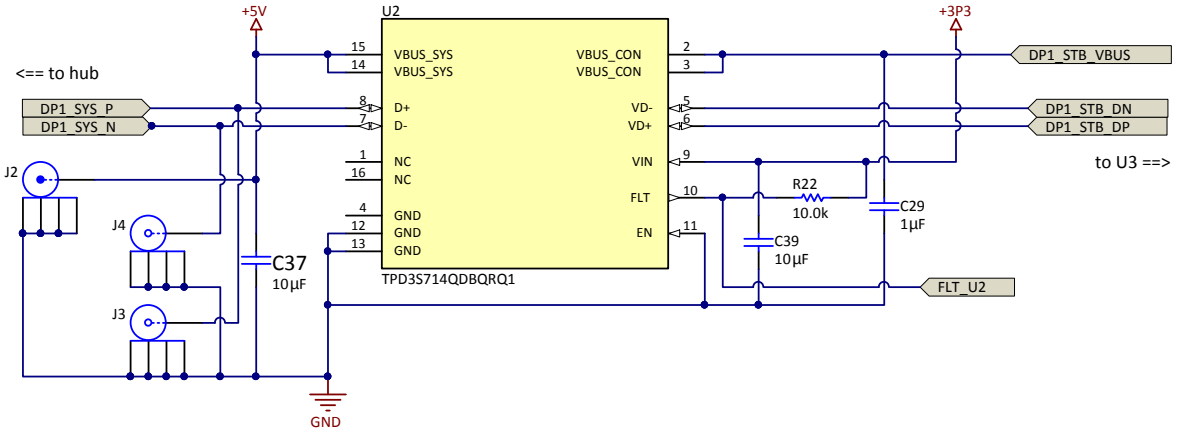

Figure 2. TPD3S714-Q1 Protecting Hub from STB on DP1

4.1.2 TPD3S714-Q1 Downstream from Short-to-Battery Test

Figure 3 shows downstream from U2 (previously discussed), another TPD3S714-Q1 (U3) for protecting any peripheral attached to the DP1 USB port during the STB demonstrations. Because, for demonstration purposes, the system-side data lines of U3 connect to the USB port, the TPD1E05U06 (U13 and U14) adds additional ESD protection to the data lines. The V_{BUS} line follows the data sheet in that the VBUS_CON pin connects to the USB port and the VBUS_SYS pin connects to the 5-V rail supplied by the LMR14030 (U5 not shown here, see Section 4.4). The V_{BUS} line passes through a hall-effect current sensor (U11 not shown here, see Figure 26) for easily observing the current during tests. The SN74LVC1G125 (U17, see Figure 27) single-bus buffer gate compares the $\overline{FLT}$ pin logic of the TPD3S714-Q1 to the 3.3-V rail, and indicates a fault by illuminating the LED (D15).

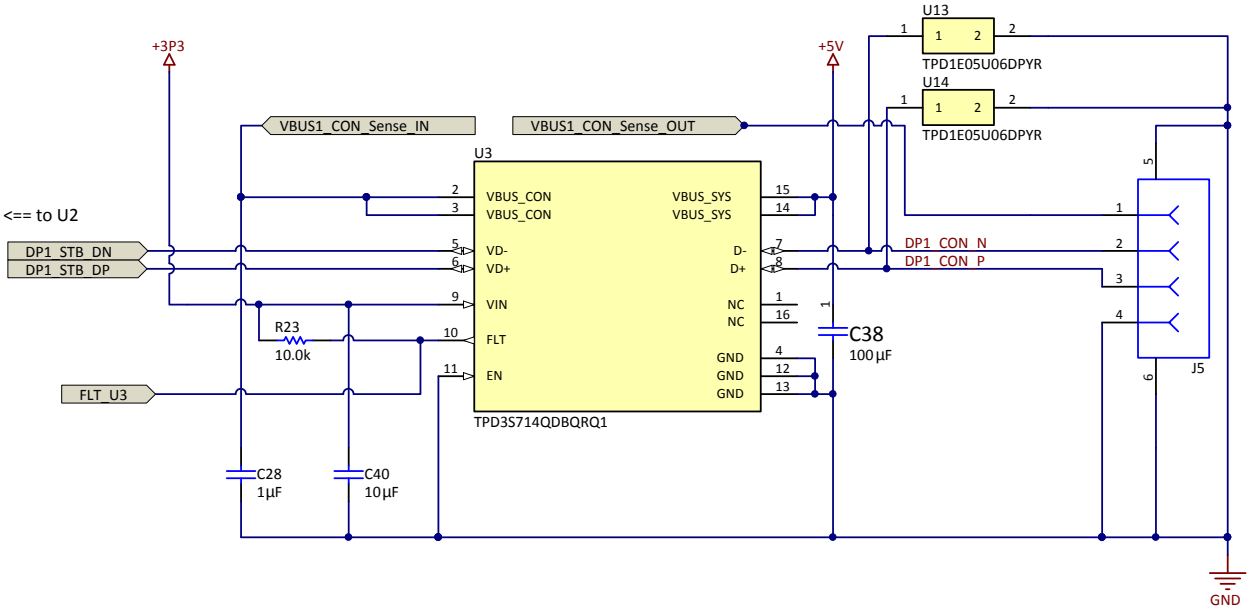

Figure 3. TPD3S714-Q1 Protecting Peripheral from STB on DP1

4.1.3 Short-To-Battery Tester

Figure 4 shows a built-in STB tester implemented to facilitate on-board STB tests. Using a high-current switch (S1), 18 V can be applied to the V_{BUS} rail protected by the TPD3S714-Q1 (U2). The 18 V is stored in a large electrolytic, low-ESR capacitor (C1). Users can observe the over-voltage by connecting a high-impedance probe of an oscilloscope to the test-point (TP1). Four LEDs (D10, D12, D13, and D14) indicate when S1 completes the circuit, and applies 18 V to V_{BUS}.

Using switch S2 or S3, either of the high-voltage low-capacitance relays (K2 and K3) can apply, respectively, 18-V STB to either DP1- or DP1+. Two-pin headers (J13 and J14) are placed parallel with S2 and S3 for attaching external switches to operate K2 or K3, respectively.

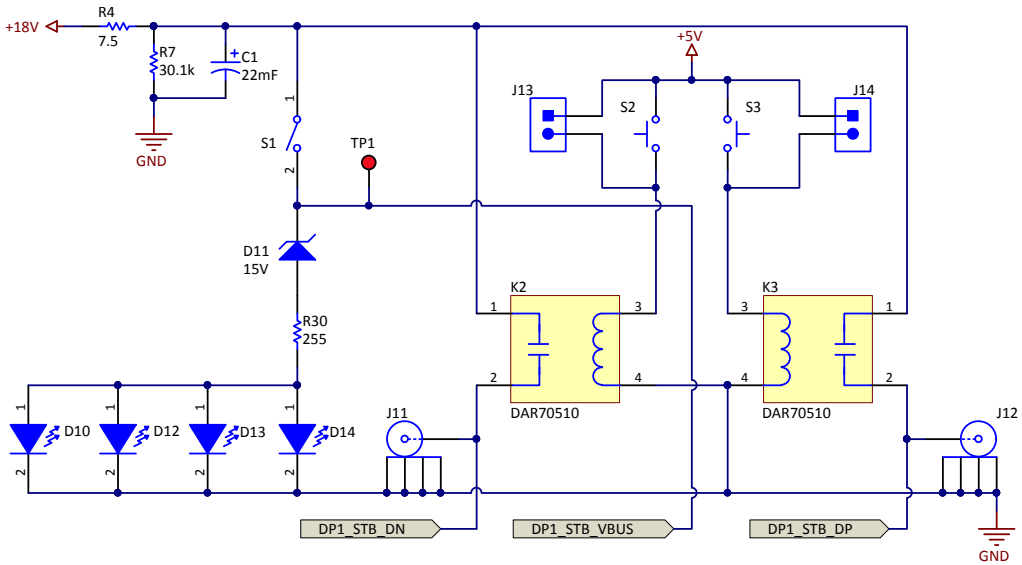

Figure 4. STB Test Circuit

By design, any peripheral attached to the DP1 USB port is also protected during STB tests. This feature makes it simple to install the USB 2.0 hub to a computer, and demonstrate the USB 2.0 hub and peripheral functionality before and after a STB demonstration.

4.2 Downstream Port 2

Figure 5 shows the TPD3S714-Q1 (U4) connected to the TUSB4020BI-Q1, following the data sheet guidelines of the TPD3S714-Q1. Additionally, test points (J8 and J10) for measuring ESD clamping voltages are included with the ground pins J15 and J18.

The SN74LVC1G125 (U9, see Figure 27) single-bus buffer gate compares the $\overline{\text{FLT}}$ pin logic of the TPD3S714-Q1 to the 3.3-V rail, and indicates a fault by illuminating the LED (D9).

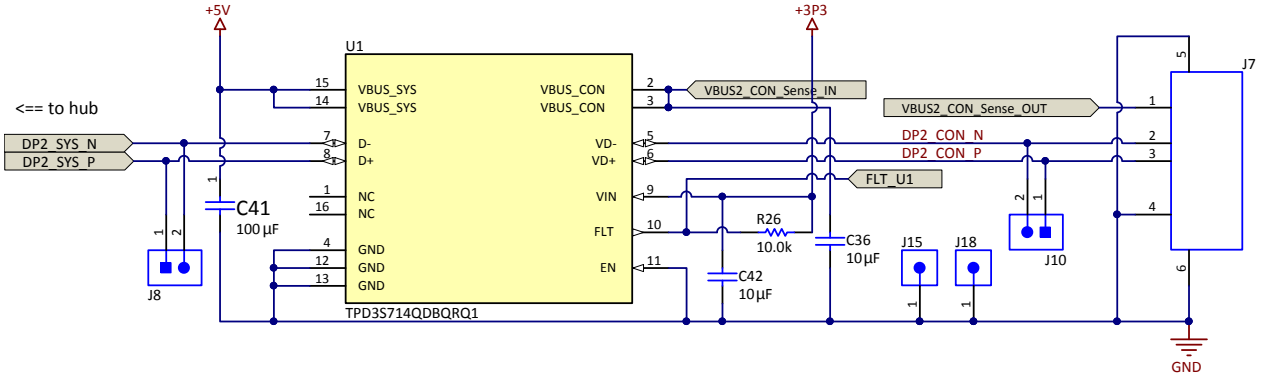

Figure 5. TPD3S714-Q1 in DP2

4.3 TUSB4020BI-Q1

The TUSB4020BI-Q1 is a two port USB 2.0-compliant hub device. It provides high-speed and full-speed connections on the UP. The TUSB4020BI-Q1 also supports high, full, or low-speed connections on the DPs. When the UP connects to an environment that supports only full and low-speed connections, high-speed is disabled on the DPs. The hub's individual port power switching is not used due to the TPD3S714-Q1 over-current limiter, providing the two-port protection scheme. The USB 2.0 hub is configured with the de-assertion of RESET.

Figure 6, shows the TUSB4020BI-Q1 (U4) configured. Only connected pins are shown.

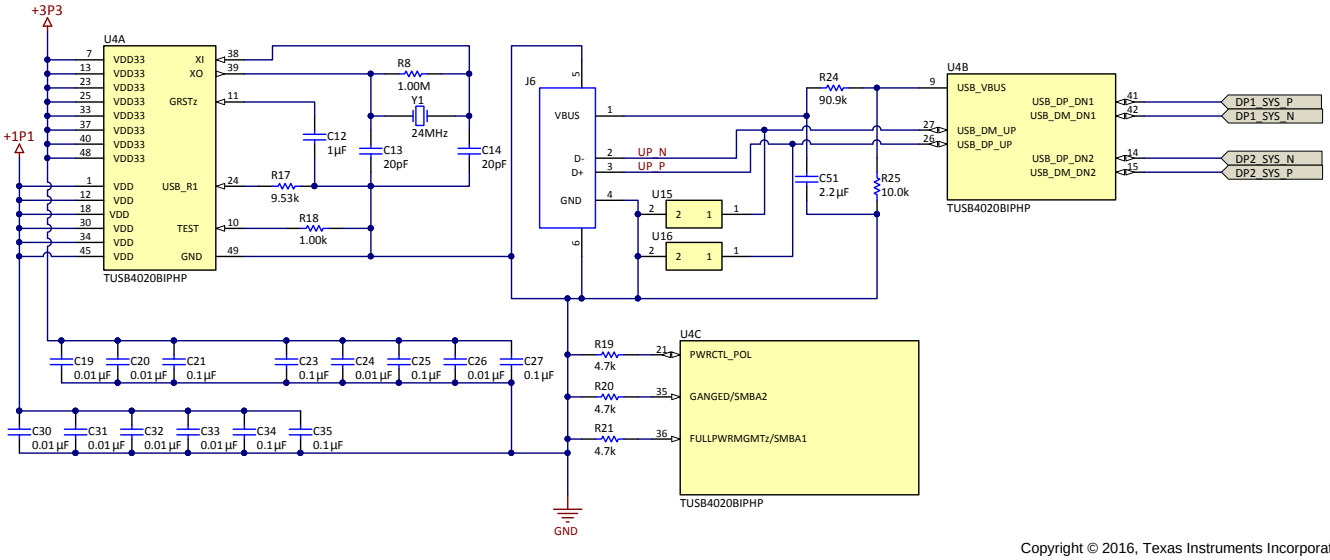

Figure 6. TUSB4020BI-Q1 Schematic

4.4 LMR14030-Q1

Figure 7 shows the LMR14030-Q1 (U5) configured for a 5-V output capable of 3.5 A. An 18-V external AC-DC converter supplies the input power. The 5-V output rail supplies the 3.3-V LDO TPS7A4533 and 1.1-V LDO TPS74801. An LED diode (D3) indicates when the power rail becomes active.

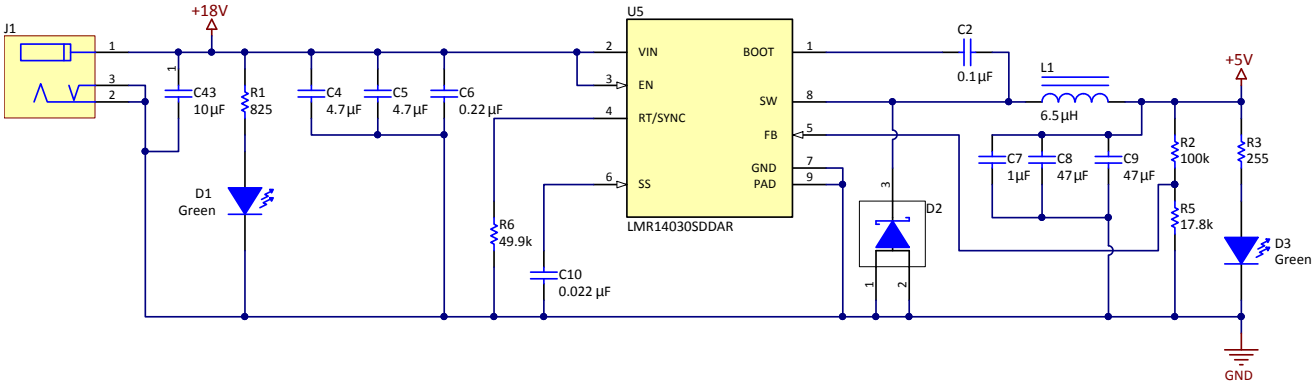

Figure 7. LMR14030 Step Down (Buck) Regulator Schematic

4.4.1 Output Voltage Selection

The internal voltage reference produces a precise 0.75-V (typical) voltage reference over the operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. It is recommended to use divider resistors with 1% tolerance or better, and a temperature coefficient of 100 ppm or less. Select the high-side resistor R_{FBT} (R2) for the desired divider current, and use Equation 1 to calculate low-side R_{FBB} (R5). Larger value divider resistors are good for efficiency at light load. However, if the values are too high the regulator is more susceptible to noise, and voltage errors from the FB input current may become noticeable. R_{FBB} in the range from 10 kΩ to 100 kΩ are recommended for most applications.

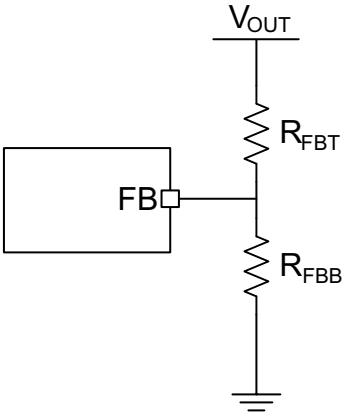

Figure 8. Output Voltage Setting

$$R_{FBB} = 0.75 / V_{OUT} – .75 \times R_{FBT} \quad (1)$$

Choosing R_{FBT} = 100 kΩ and V_{OUT} = 5 V, gets R_{FBB} = 17,647Ω. Choose a standard value of 17.8 kΩ.

4.4.2 Switching Frequency

For a desired frequency, use Equation 2 to calculate the required value for R_T (R6).

$$R_T(K\Omega) = 42904 \times f_{sw}(kHZ)^{-1.088} \quad (2)$$

This design uses a switching frequency of 500 kHz. For 500 kHz, the calculated R_T is 49.66 kΩ, and a standard value of 49.9 kΩ can be used to set the switching frequency at 500 kHz.

4.4.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance, L_{MIN}. Use Equation 4 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} should be 20%-40%. During an instantaneous short or over-current operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than the current limit.

$$\Delta i_L = V_{OUT} \times (V_{IN\_MAX} - V_{OUT}) / V_{IN\_MAX} \times L \times f_{SW} \quad (3)$$

$$L_{MIN} = V_{IN\_MAX} - V_{OUT} / I_{OUT} \times K_{IND} \times V_{OUT} / V_{IN\_MAX} \times f_{SW} \quad (4)$$

In general, it is preferable to choose lower inductance when switching power supplies, because it usually corresponds to a faster transient response, smaller DCR, and reduced size for more compact designs. However, too low of an inductance can generate too large of an inductor current ripple, to where over-current protection at the full load could be falsely triggered. Lower inductance also generates more conduction loss since the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal-to-noise ratio. For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 6.12 µH, and the nearest standard value above that is chosen 6.5 µH. Use a standard 6.5-µH ferrite inductor (L1) with a capability of 5-A RMS current and 7-A saturation current.

4.4.4 Output Capacitor Selection

The output capacitor(s), C_{OUT} (C7, C8, C9), should be carefully chosen since it directly affects the steady-state output voltage ripple, loop stability, and the voltage overshoot and undershoot during load current transients. The output ripple is essentially composed of two parts. One part is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (5)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$V_{OUT\_C} = \Delta i_L / 8 \times f_{SW} \times C_{OUT} = K_{IND} \times I_{OUT} / 8 \times f_{SW} \times C_{OUT} \quad (6)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks. Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with the presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for the three clock cycles to maintain the output voltage within the specified range.

Equation 7 shows the minimum output capacitance needed for a specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode can't sink current so the energy stored in the inductor results in an output voltage overshoot. Equation 8 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > 3 \times (I_{OH} - I_{OL}) / (f_{SW} \times V_{US} \quad (7)$$

$$C_{OUT} > I^2_{OH} - I^2_{OL} / (V_{OUT} - V_{OS})^2 - V^2\_{OUT} \quad (8)$$

where:

- K_{IND} = ripple ratio of the inductor ripple current (ΔiL / IOUT)
- I_{OL} = low-level output current during load transient
- I_{OH} = high-level output current during load transient
- V_{US} = target output-voltage undershoot
- V_{OS} = target output-voltage overshoot

For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50-mV, and chose K_{IND} = 0.4. Equation 5 yields ESR no larger than 35.7 mΩ and Equation 6 yields C_{OUT} no smaller than 7 µF. For the target over and undershoot range of this design, $V_{US} = V_{OS}$ = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 75.6 µF and 30.8 µF by Equation 7 and Equation 8 respectively. In summary, the most stringent criteria for the output capacitor is 75.6 µF. Two 47-µF, 16-V, X7R ceramic capacitors (C8 and C9) with 5-mΩ ESR are used in parallel. A 1-µF, X7R, capacitor (C7) is also used for high-frequency filtering, placed as close as possible to the device pins.

4.4.5 Schottky Diode Selection

The preferred breakdown voltage rating of the diode is 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for the best reliability in most applications. In cases where the input voltage is much greater than the output voltage, the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-*D*) × I_{OUT}, however the peak current rating should be higher than the maximum load current. A 4-A to 5-A rated diode is a good starting point. For this design example, a 5-A 60-V Schottky diode (D2) was chosen.

4.4.6 Input Capacitor Selection

The LMR14030-Q1 device requires high-frequency input decoupling capacitor(s) and a bulk-input capacitor, depending on the application. The typical recommended value for the high-frequency decoupling capacitor is from 4.7 µF to 10 µF. A high-quality ceramic capacitor, type X5R or X7R, with a sufficient voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LMR14030-Q1 circuit is not located within approximately 5-cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 4.7-µF, X7R ceramic capacitors, rated for 50 V, are used. A 0.22-µF, X7R ceramic capacitor (C6), rated for 50 V, is also used for high-frequency filtering, placed as close as possible to the device pins.

4.4.7 Bootstrap Capacitor Selection

Every LMR14030-Q1 design requires a bootstrap capacitor, CBOOT (C2). The recommended capacitor is 0.1 µF and rated 16 V or higher, the values used in this design. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type, with an X7R or X5R grade dielectric for temperature stability. This design uses X7R.

4.5 TPS7A4533

Figure 9 shows the TPS7A4533 (U6) configured in this design. The LMR14030-Q1 supplies the V_{IN}. V_{OUT} is the VDD33 supply rail for the USB 2.0 hub TUSB4020BI-Q1 and the TPD3S714-Q1. An LED diode (D7) indicates when the power rail becomes active.

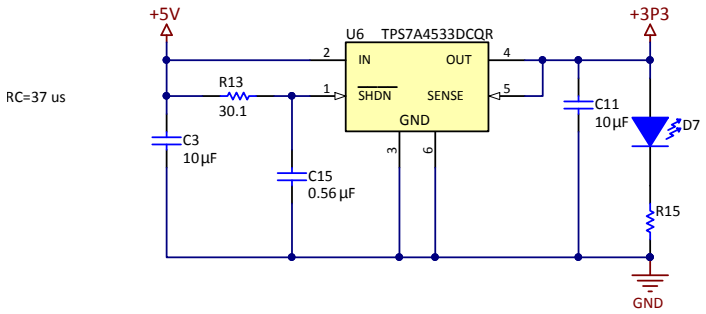

Figure 9. TPS7A4533 3.3-V Low Dropout Regulator Schematic

4.5.1 Start-up Timing

The USB 2.0 hub TUSB4020BI-Q1 requires that the VDD33 supply (TPS704533 in this design) be stable before at least 10-µs before the VDD supply (TPS74801-Q1 in this design) powers on. To accomplish this, an RC circuit (R13 and C15) adds a 37-µs startup delay to the $\overline{\text{SHDN}}$ pin with the VDD33 supply, and a 66-µs startup delay for the VDD supply. The difference of 29 µs meets this requirement.

4.5.2 Output Capacitor Selection

Extra consideration must be given for the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behaviors over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10-µF Y5V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. This design uses a 10-µF capacitor (C11) with an X5R rating.

4.6 TPS78401-Q1

Figure 10 shows the TPS78401-Q1 (U7) configured in this design. The LMR14030-Q1 supplies the IN voltage-supply pin. The OUT pin is the VDD supply rail for the USB 2.0 hub TUSB4020BI-Q1.

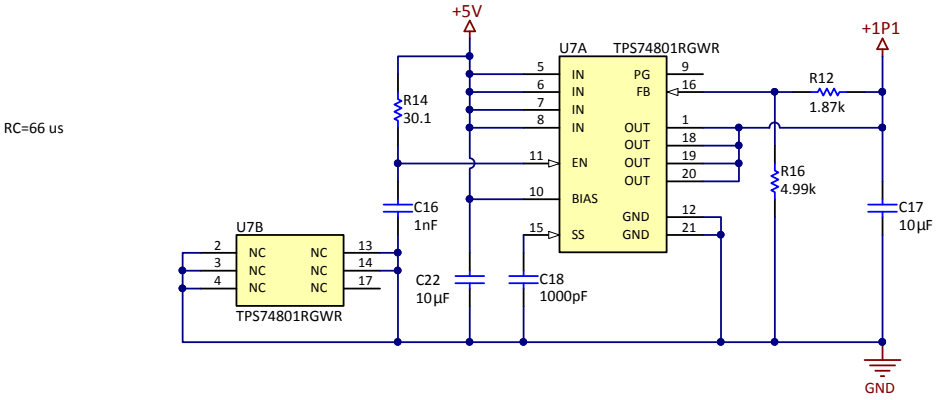

Figure 10. TPS78401-Q1 1.1-V Low Dropout Regulator Schematic

4.6.1 Output Voltage Selection

For an output voltage of 1.1 V, the resistor divider (R12 and R16) on the FB pin was set by Equation 9 where R16 should be ≤ 4.99 kΩ. A value for R16 of 4.99 kΩ was chosen to minimize the FB pin input current. This yields a value of 1.87 kΩ for R12.

$$V_{OUT} = 0.8 \times (1 + R_{12} / R_{16}) \quad (9)$$

4.6.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low ESR capacitors should be used on the input, ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close to the pins as possible for optimum performance. For this design, C_{OUT} (C17) is a 10-µF capacitor with an X5R rating. Since the IN and BIAS pins are connected to the same supply, C_{IN} (C22) is a 22-µF capacitor with an X5R rating.

4.6.3 Programmable Soft-Start

The TPS74801-Q1 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (CSS or C18). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus. To achieve a linear and monotonic soft-start, the TPS74801-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (ISS), soft-start capacitance (CSS), and the internal reference voltage (VREF), and can be calculated using Equation 10:

$$t_{SS} = (V_{REF} \times C_{SS}) / I_{SS} \quad (10)$$

where:

- V_{REF} = 0.8 V
- I_{SS} = 440 nA

This design uses a C_{SS} (C18) of 1000 pF for t_{SS} = 1.82 ms. This measure, along with the 66-µs RC (R14 and C16) circuit on the EN pin, ensures the VDD stabilizes after VDD33 for the TUSB4020BI-Q1 timing requirement.

5 Test Data

5.1 Short-to-Battery

Once a voltage above the V_{OVP} threshold is detected by the device, the TPD3S714-Q1 shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. When the excessive voltage is removed, the device automatically re-enables and the $\overline{FLT}$ de-asserts.

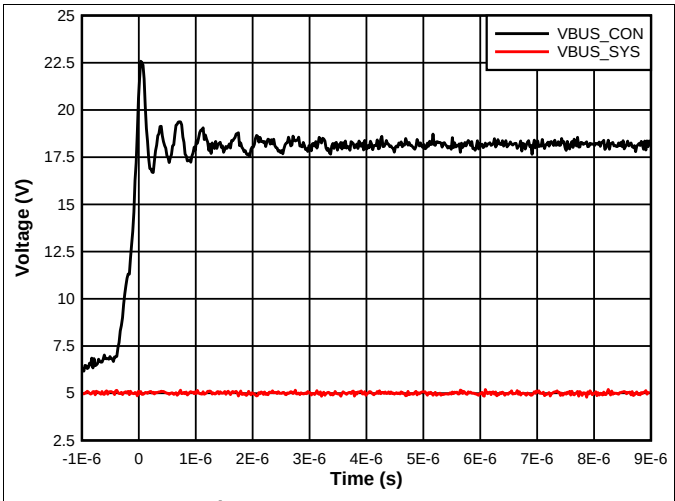

Figure 11. 18-V STB to DP1 V_{BUS}

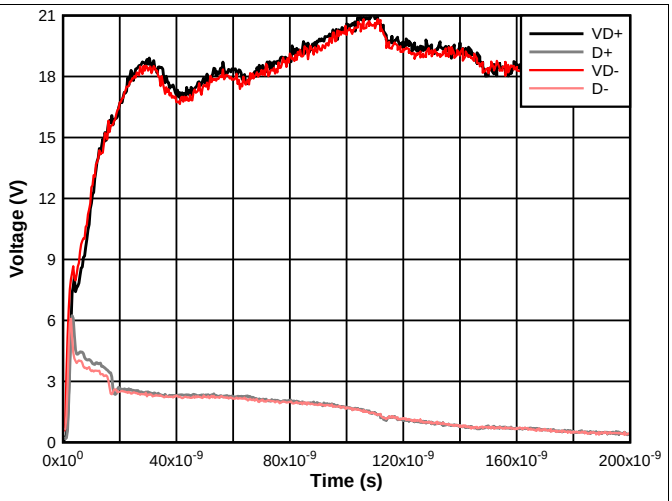

Figure 12. 18-V STB to DP1 USB Data Lines

5.2 IEC 61000-4-2 ±8-kV Clamping Waveforms on USB Data Lines

The protected pins (VBUS_CON, VD+, VD-) are tested to pass the IEC 61000-4-2 ESD standard up to Level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330-pF and 330-Ω equivalent network. This guarantees passing of at least ±8-kV contact discharge, and ±15-kV air-gap discharge according to both standards.

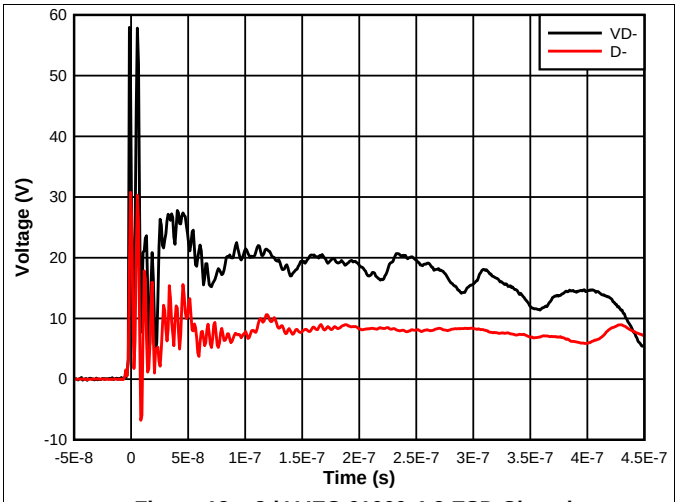

Figure 13. +8-kV IEC 61000-4-2 ESD Clamping

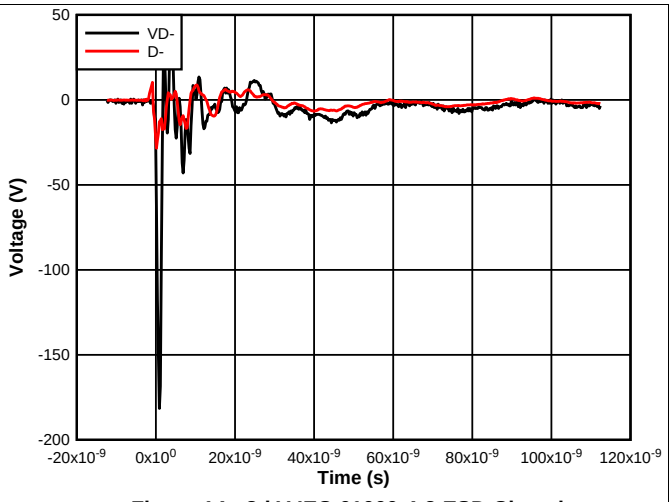

Figure 14. -8-kV IEC 61000-4-2 ESD Clamping

5.3 Short to Ground

When a voltage on VBUS_CON is detected as too low (below the V_{SHRT} threshold) after the device is enabled, the device enters a short-circuit protection mode and asserts the $\overline{FLT}$. The device sources the I_{SHRT} current until it detects the voltage rising above the V_{SHRT} threshold, then it resumes standard operating mode and de-asserts $\overline{FLT}$.

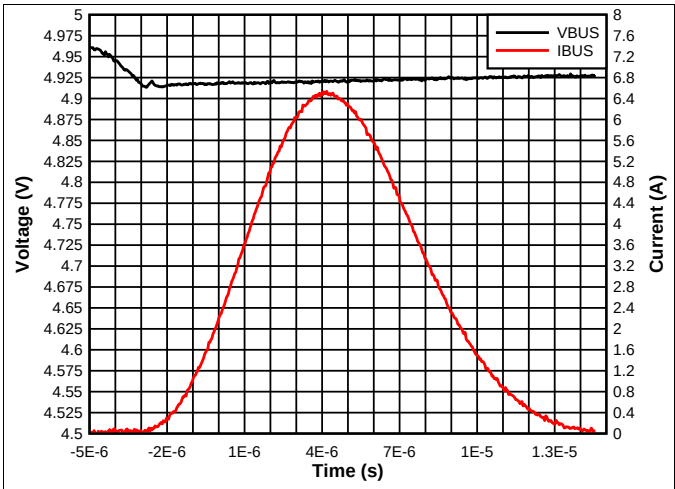

Figure 15. Short to Ground on DP1

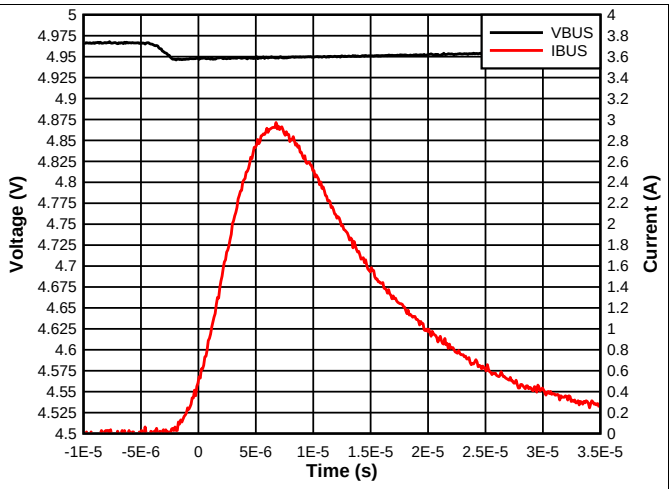

Figure 16. Short to 1-Ω Load on DP1

5.4 USB 2.0 High-Speed Downstream Near-End Eye Diagram

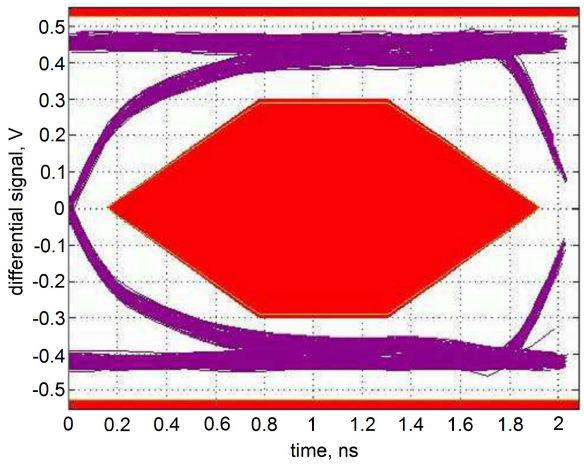

Figure 17. TUSB4020BI-Q1EVM USB 2.0 Eye Diagram without the TPD3S714-Q1

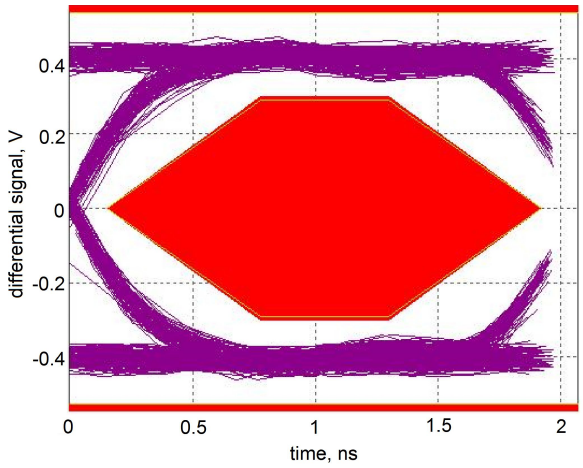

Figure 18. TIDA-00845 USB 2.0 Eye Diagram with the TPD3S714-Q1 Measured at J10

6 Design Files

6.1 Schematics

To download the schematics for each board, see the design files at: http://www.ti.com/tool/TIDA-00845.

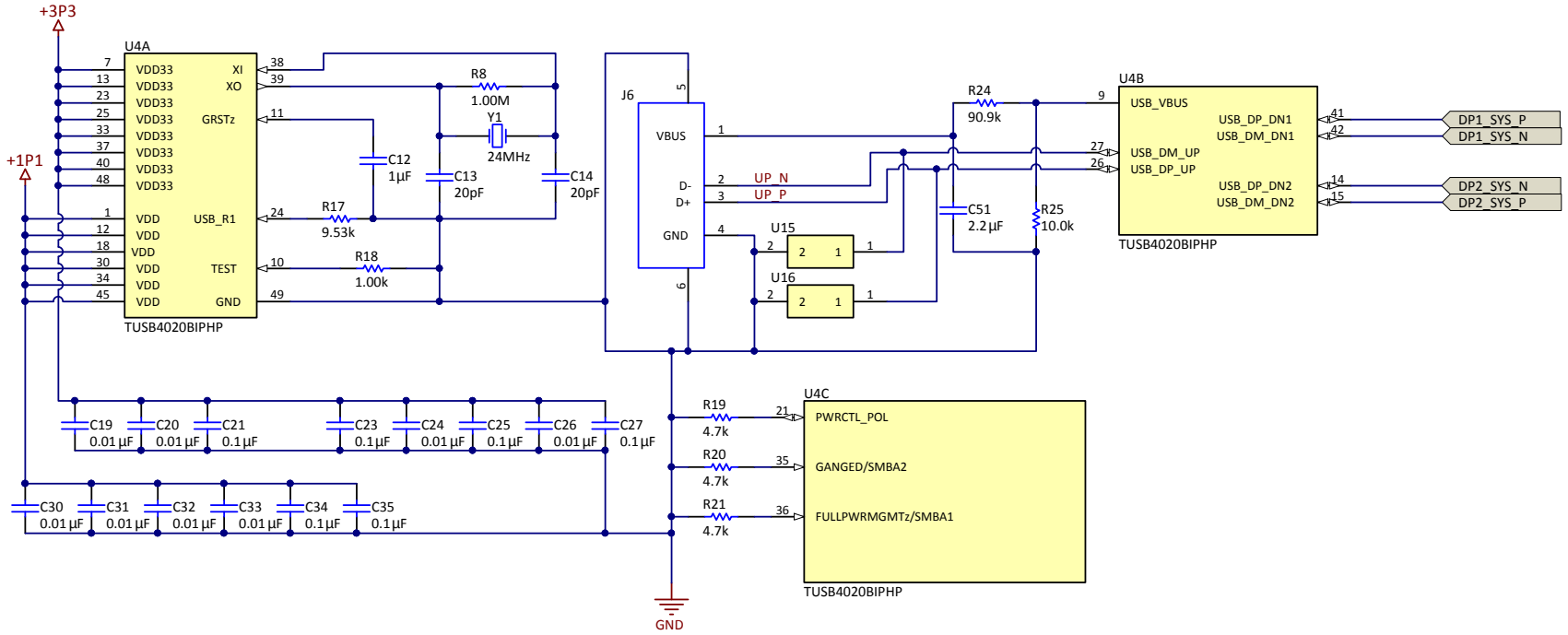

Figure 19. USB 2.0 Hub

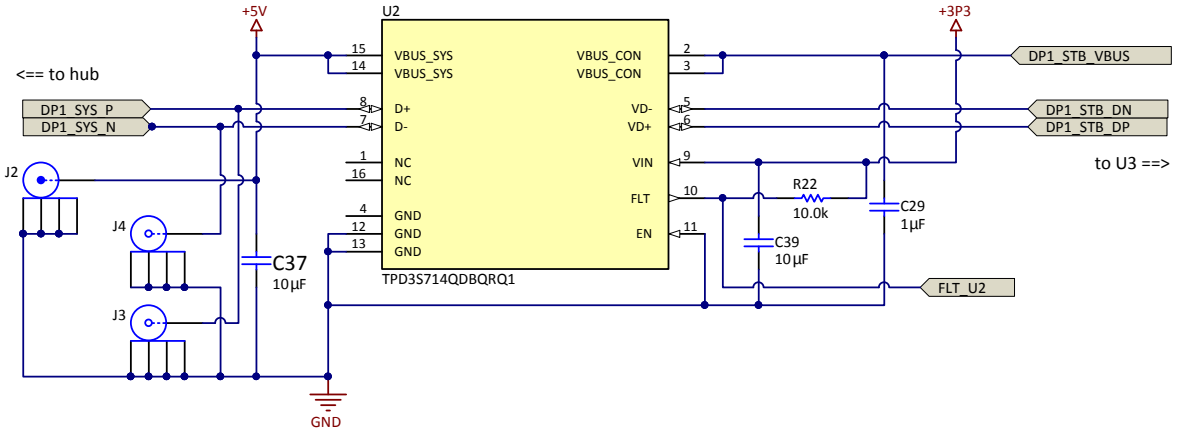

Figure 20. Upstream of STB on DP1

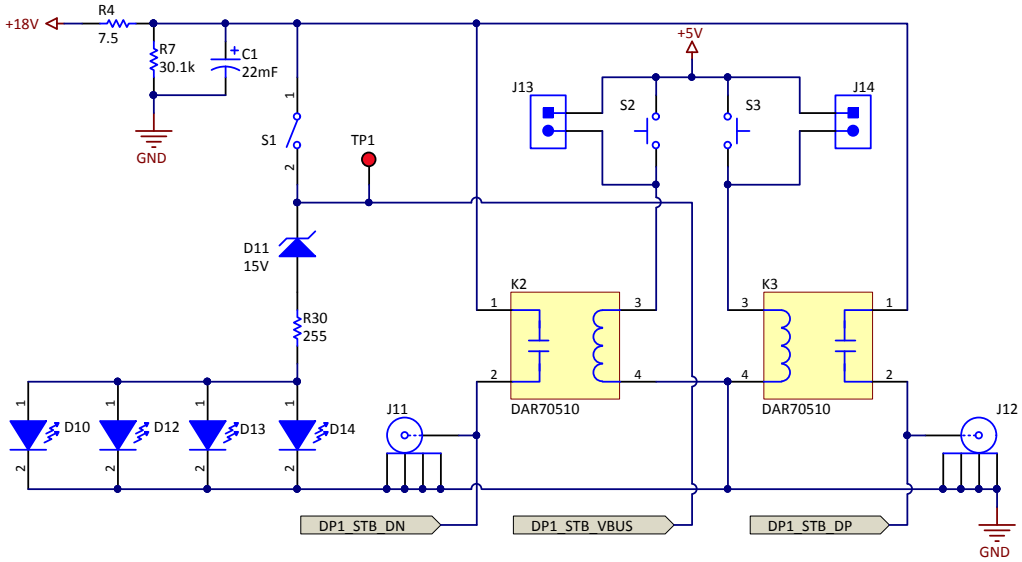

Figure 21. STB Tester

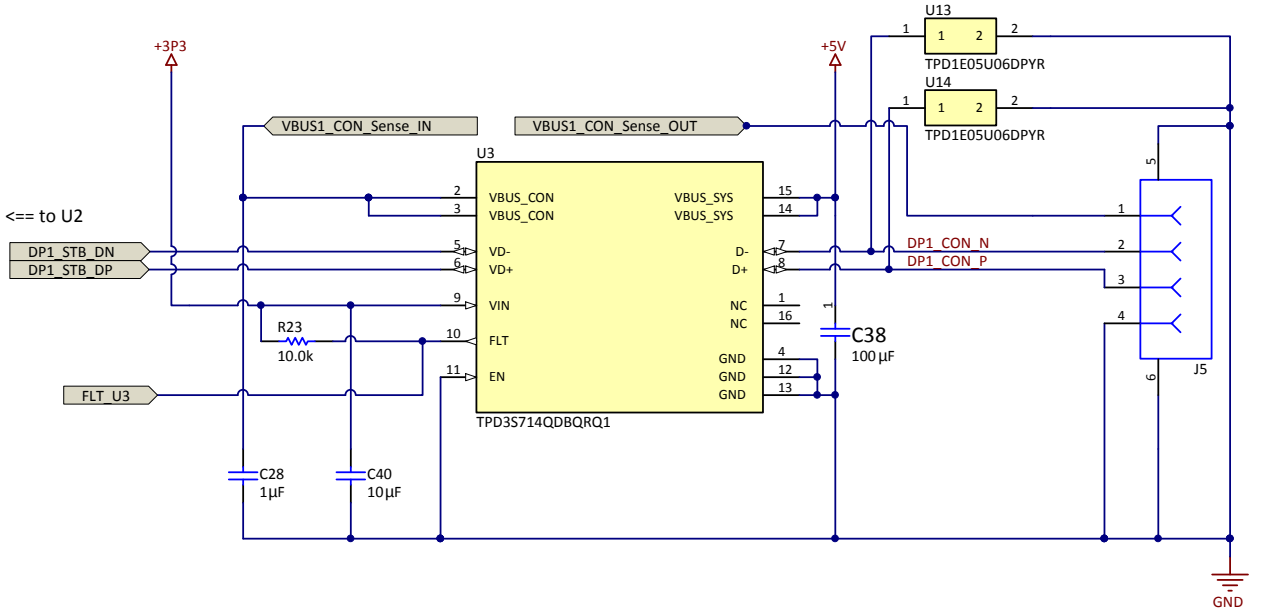

Figure 22. Downstream of STB Tester on DP1

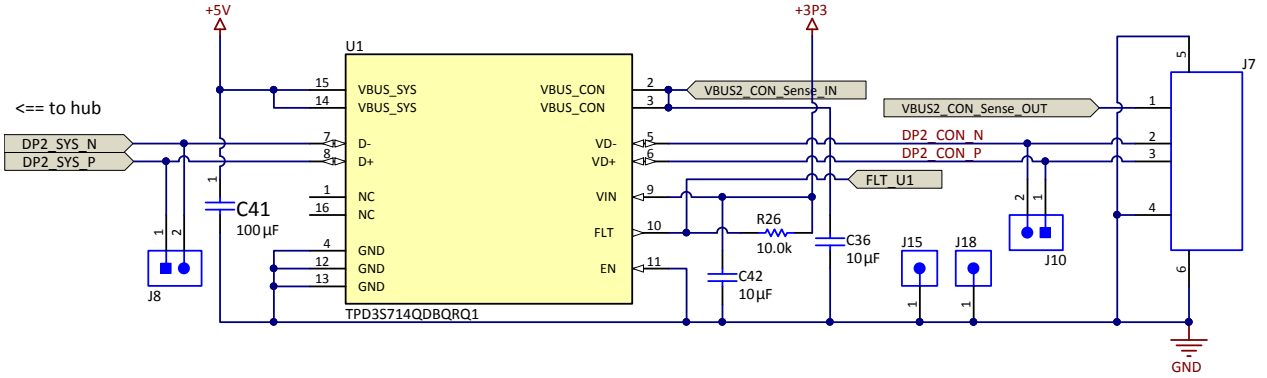

Figure 23. DP2

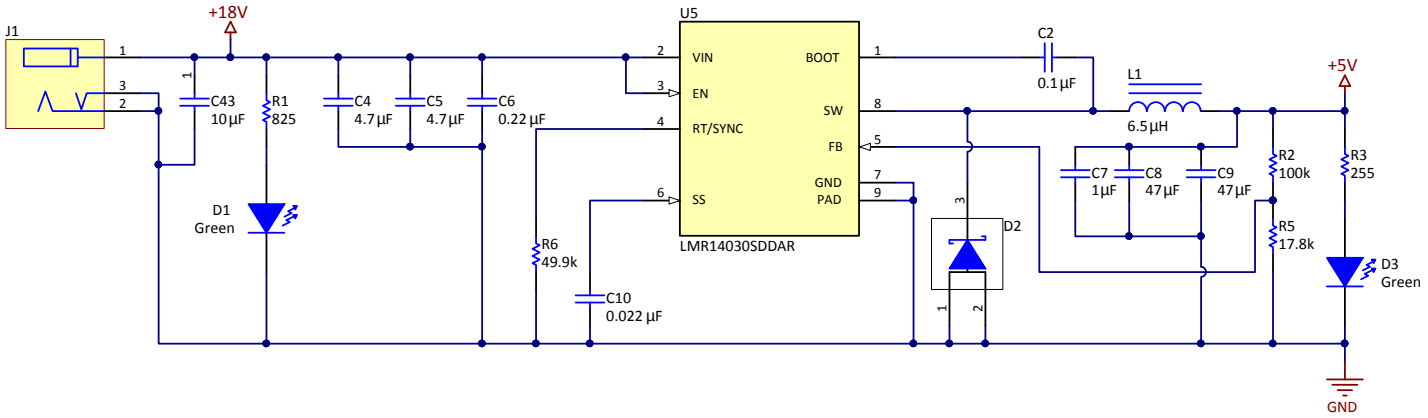

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Figure 24. 5-V Power Rail

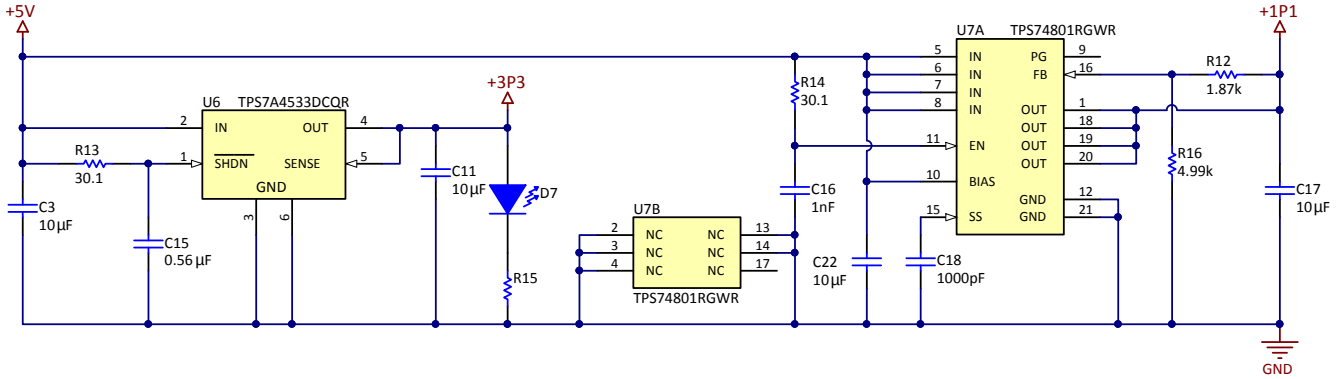

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Figure 25. VDD33 and VDD Power Rails

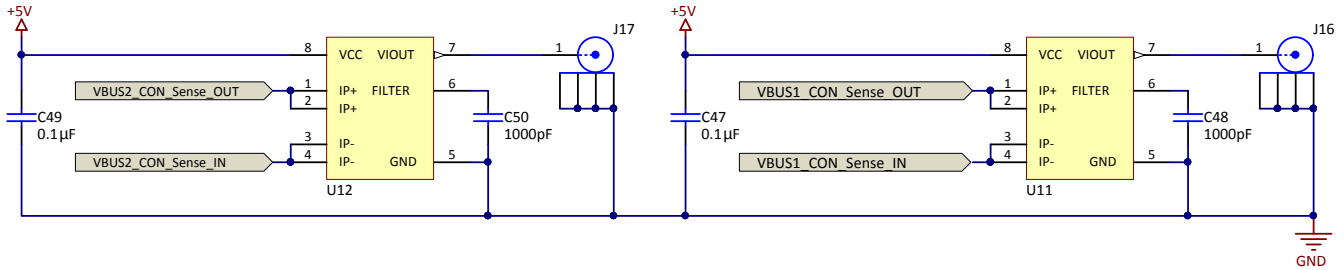

Figure 26. DP1 & DP2 Current Sensors

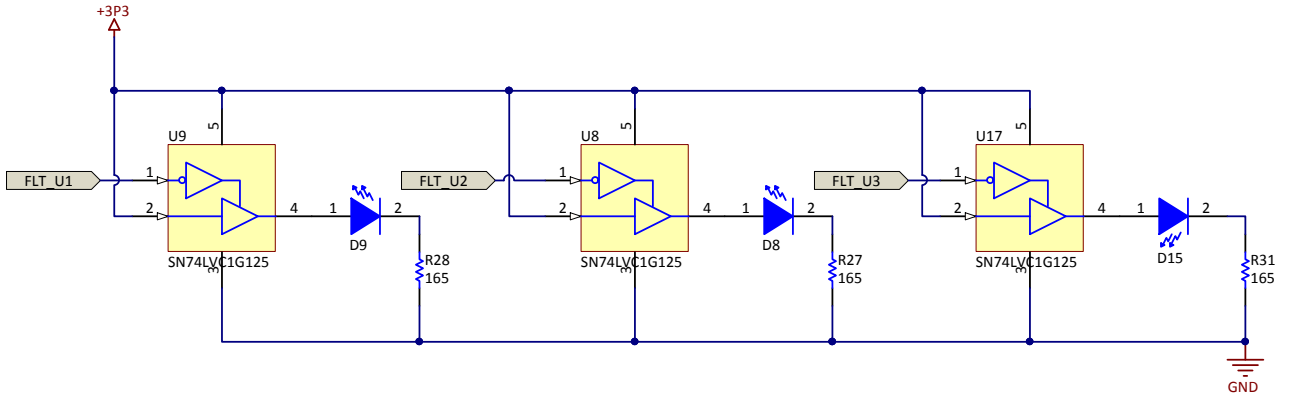

Figure 27. $\overline{\text{FLT}}$ Indicators for TPD3S714-Q1

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00845.

Table 2. BOM

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		ISE4002	Any
!Enclosure	1		Electrical Enclosure Box		PN-1327-C	Bud Industries
C1	1	22000 uF	CAP, AL, 10000 µF, 6.3 V, ± 20%, SMD	MN0	B41231B5229M	EPCOS (TDK)

Table 2. BOM (continued)

C2	1	0.1 uF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0603	603	GRM188R71C104KA01D	MuRata
C3, C11, C17, C22	4	10 uF	CAP, CERM, 10 µF, 16 V, ± 20%, X5R, 0805	805	0805YD106MAT2A	AVX
C4, C5	2	4.7 uF	CAP, CERM, 4.7 µF, 50 V, ± 10%, X7R, 1210	1210	GRM32ER71H475KA88L	MuRata
C6	1	0.22 uF	CAP, CERM, 0.22 µF, 50 V, ± 10%, X7R, 0805	805	GRM21BR71H224KA01L	MuRata
C7	1	1 uF	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0805	805	GRM21BR71E105KA99L	MuRata
C8, C9	2	47 uF	CAP, CERM, 47 µF, 16 V, ± 20%, X5R, 1210	1210	GRM32ER61C476ME15 L	MuRata
C10	1	0.022 uF	CAP, CERM, 0.022 µF, 16 V, ± 10%, X7R, 0402	402	GRM155R71C223KA01D	MuRata
C12	1	1 uF	CAP, CERM, 1 µF, 6.3 V, ± 20%, X7R, 0402	402	GRM155R70J105MA12D	MuRata
C13, C14	2	20 pF	CAP, CERM, 20 pF, 50 V, ± 5%, C0G/NP0, 0402	402	GRM1555C1H200JA01D	MuRata
C15	1	0.56 uF	CAP, CERM, 0.56 µF, 25 V, ± 10%, X7R, 1206	1206	C1206C564K5RACTU	AVX
C16, C18	2	1000 pF	CAP, CERM, 1000 pF, 2000 V, ± 10%, X7R, 1206_190	1206_190	202R18W102KV4E	Johanson Technology
C19, C20, C24, C26, C30, C31, C32, C33	8	0.01 uF	CAP, CERM, 0.01 µF, 50 V, ± 10%, X7R, 0402	402	GRM155R71H103KA88D	MuRata
C21, C23, C25, C27, C34, C35	6	0.1 uF	CAP, CERM, 0.1 µF, 25 V, ± 20%, X7R, 0402	402	TMK105B7104MV-FR	Taiyo Yuden
C28, C29	2	1 uF	CAP, CERM, 1 µF, 50 V, ± 10%, X7R, 0603	603	UMK107AB7105KA-T	Taiyo Yuden
C36, C43	2	10 uF	CAP, CERM, 10 µF, 100 V, ± 20%, X7R, 6x5x5mm	6 × 5 x 5 mm	CKG57NX7R2A106M500 JH	TDK
C37, C38, C41	3	100 uF	CAP, CERM, 100 µF, 10 V, ± 20%, X5R, 1210	1210	C1210C107M8PACTU	Wurth Elektronik
C39, C40, C42	3	10 uF	CAP, CERM, 10 µF, 6.3 V, ± 20%, X7R, 0805	805	C2012X7R0J106M125AB	TDK
C47, C49	2	0.1 uF	CAP, CERM, 0.1 µF, 25 V, ± 5%, X7R, 0603	603	06033C104JAT2A	AVX
C48, C50	2	1000 pF	CAP, CERM, 1000 pF, 25 V, ± 10%, X7R, 0402	402	8.85012E + 11	Wurth Elektronik
C51	1	2.2 uF	CAP, CERM, 2.2 µF, 6.3 V, ± 20%, X5R, 0402	402	JMK105BJ225MV-F	Taiyo Yuden

Table 2. BOM (continued)

D1, D3, D7	3	Green	LED, Green, SMD	LED_0805	LTST-C171GKT	Lite-On
D2	1	60 V	Diode, Schottky, 60 V, 5 A, PowerDI5	PowerDI5	PDS560-13	Diodes Inc.
D8, D9, D10, D12, D13, D14, D15	7	Super Red	LED, Super Red, SMD	LED, 1 × .35 × .5 mm	VLMS1500-GS08	Vishay-Semiconductor
D11	1	15 V	Diode, Zener, 15 V, 500 mW, SMA	SMA	1SMA5929BT3G	ON Semiconductor
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
H1, H2, H3, H4	4		Screw Pan Head M3	Screw M3	29311	Keystone
H5, H6, H7, H8	4		HEX STANDOFF M3 BRASS 5 MM	HEX STANDOFF M3 BRASS 5MM	R30-3000502	Harwin
J1	1		Connector, DC Jack 2.1 × 5.5 mm, TH	Conn, DC Jack, pin 2-mm Dia.	PJ-202AH	CUI Inc.
J2, J16, J17	3		Connector, SMB,Vertical RCP 0-4GHz, 50 Ω, TH	236 × 293 × 236 mil	131-3701-261	Emerson Network Power
J3, J4, J11, J12	4		Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe	131-5031-00	Tektronix
J5	1		Connector, Receptacle, USB Type A, R/A, Top Mount TH	USB Type A right angle	292303-4	TE Connectivity
J6	1		Connector, Receptacle, USB TYPE B, R/A, Top Mount TH	USB Type B Receptacle	67068-8000	Molex
J7	1		Connector, Receptacle, USB TYPE A, 4POS SMD	USB TYPE A CONNECTOR RECEPTACLE 4POS SMD	896-43-004-00-000000	Mill-Max
J8, J10	2		Header, 100 mil, 2 × 1, TH	Header, 2 × 1, 100 mil, TH	800-10-002-10-001000	Mill-Max
J13, J14	2		Header, 2.54 mm, 2 × 1, Vertical, TH	Header, 2.54 mm, 2x1, TH	22-23-2021	Molex
J15, J18	2		Header, 2.54 mm, 1 × 1, Gold, TH	Header, 2.54 mm, 1x1, TH	61300111121	Wurth Elektronik
K2, K3	2			60.0 × 15.8 mm	DAR70510	Cynergy 3
L1	1	6.5 uH	Inductor, Shielded Drum Core, Superflux, 6.5 µH, 6 A, 0.0225 Ω, SMD	6.9 × 4.8 × 6.9 mm	744314650	Wurth Elektronik
R1	1	825	RES, 825, 1%, 0.063 W, 0402	402	CRCW0402825RFKED	Vishay-Dale

Table 2. BOM (continued)

R2	1	100 k	RES, 100 k, 0.5%, 0.063 W, 0402	402	CRCW0402100KDHEDP	Vishay-Dale
R3, R30	2	255	RES, 255, 1%, 0.063 W, 0402	402	CRCW0402255RFKED	Vishay-Dale
R4	1	7.5	RES, 7.5, 5%, 10 W, RES 48 × 9.5 × 9 mm	RES 0.620" L × 0.195" W	TEH100M7R50FE	Ohmite
R5	1	17.8 k	RES, 17.8 k, 1%, 0.063 W, 0402	402	CRCW040217K8FKED	Vishay-Dale
R6	1	49.9 k	RES, 49.9 k, 1%, 0.063 W, 0402	402	CRCW040249K9FKED	Vishay-Dale
R7	1	30.1 k	RES, 30.1 k, 1%, 0.063 W, 0402	402	CRCW040230K1FKED	Vishay-Dale
R8	1	1.00 Meg	RES, 1.00 M, 1%, 0.063 W, 0402	402	CRCW04021M00FKED	Vishay-Dale
R12	1	1.87 k	RES, 1.87 k, 1%, 0.063 W, 0402	402	CRCW04021K87FKED	Vishay-Dale
R13, R14	2	30.1	RES, 30.1, 1%, 0.063 W, 0402	402	CRCW040230R1FKED	Vishay-Dale
R15	1	330	RES, 330, 5%, 0.063 W, 0402	402	CRCW0402330RJNED	Vishay-Dale
R16	1	4.99 k	RES, 4.99 k, 1%, 0.063 W, 0402	402	CRCW04024K99FKED	Vishay-Dale
R17	1	9.53 k	RES, 9.53 k, 1%, 0.063 W, 0402	402	CRCW04029K53FKED	Vishay-Dale
R18	1	1.00 k	RES, 1.00 k, 1%, 0.063 W, 0402	402	CRCW04021K00FKED	Vishay-Dale
R19, R20, R21	3	4.7 k	RES, 4.7 k, 5%, 0.063 W, 0402	402	CRCW04024K70JNED	Vishay-Dale
R22, R23, R26	3	10.0 k	RES, 10.0 k Ω, 1%, 0.1W, 0603	603	CRCW060310K0FKEA	Vishay-Dale
R24	1	90.9 k	RES, 90.9 k, 1%, 0.063 W, 0402	402	CRCW040290K9FKED	Vishay-Dale
R25	1	10.0 k	RES, 10.0 k, 0.5%, 0.063 W, 0402	402	CRCW040210K0DHEDP	Vishay-Dale
R27, R28, R31	3	165	RES, 165, 1%, 0.063 W, 0402	402	CRCW0402165RFKED	Vishay-Dale
S1	1		SWITCH PUSH SPST-NO 10 A 125 V	For example: 0603, used in PnP report	GPB527C202BR	CW Industries
S2, S3	2		Switch, Normally open, 2.3-N force, 200-k operations, SMD	KSR	KSR221GLFS	C&K Components

Table 2. BOM (continued)

TP1	1	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
U1, U2, U3	3		AUTOMOTIVE USB 2.0 Interface Protection with Short-to-Battery and Short-to-Ground Protection, DBQ0016A	DBQ0016A	TPD3S714QDBQRQ1	Texas Instruments
U4	1		400-Mbps IEEE 1394a One-Port Cable Transceiver / Arbiter, 3.3 V, 0 to 70 degC, 48-Pin HTQFP (PHP), Green (RoHS & no Sb/Br)	PHP0048C	TUSB4020BIPHP	Texas Instruments
U5	1		SIMPLE SWITCHER 40 V 3.5 A, 2.2-MHz Step-Down Converter with 40-µA IQ, DDA0008E	DDA0008E	LMR14030SDDAR	Texas Instruments
U6	1		Single Output Fast Transient Response LDO, 1.5 A, Fixed 3.3-V Output, 2.1 to 20-V Input, 6-pin SOT-223 (DCQ), -40 to 125 degC, Green (RoHS & no Sb/Br)	DCQ0006A	TPS7A4533DCQR	Texas Instruments
U7	1		Single Output LDO, 1.5 A, Adjustable 0.8 to 3.6-V Output, 0.8 to 5.5-V Input, with Programmable Soft Start, 20-pin VQFN (RGW), -40 to 125 degC, Green (RoHS & no Sb/Br)	RGW0020A	TPS74801RGWR	Texas Instruments
U8, U9, U17	3		Single Bus Buffer Gate With 3-State Output, DCK0005A	DCK0005A	SN74LVC1G125DCKR	Texas Instruments
U11, U12	2		Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1-kVRMS Isolation and a Low-Resistance Current Conductor, SOIC-8	SOIC-8	ACS712ELCTR-05B-T	Allegro Microsystems Inc

Table 2. BOM (continued)

U13, U14, U15, U16	4		ESD in 0402 Package with 10-pF Capacitance and 6-V Breakdown, 1 Channel, -40 to +125 degC, 2-pin X2SON (DPY), Green (RoHS & no Sb/Br)	DPY0002A	TPD1E05U06DPYR	Texas Instruments
Y1	1		Crystal, 24.000 MHz, 20 pF, SMD	Crystal, XTAL_2_SM_197X126	445C25D24M00000	CTS Freq Controls

6.3 PCB Layout Recommendations

TIDA-00845 is a 4-Layer printed-circuit board (PCB). The board thickness is 0.062”. Figure 28 shows the PCB stack-up. The core material for dielectric1 and dielectric 3 is FR-408HR. Due to the 5.7” long traces of the DP1 data lines, and their capacitive loading by 3 transient voltage suppressors and reed relays (K1 or K2), FR-408HR, a dielectric with a low loss tangent, was selected to help maintain the signal integrity.

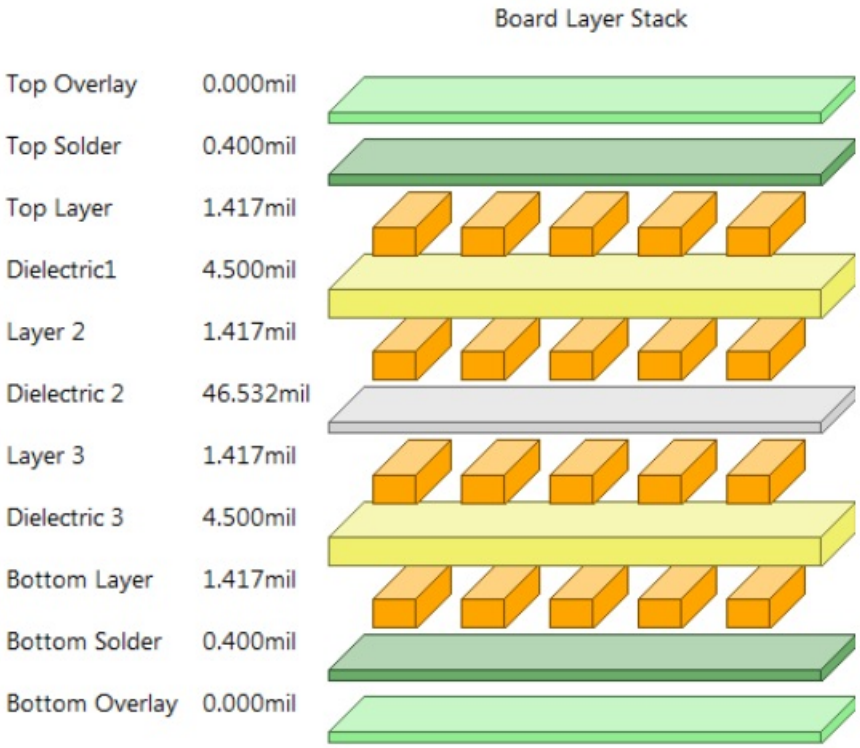

Figure 28. TIDA-00845 PCB Stack-Up

Route all USB 2.0 lines as controlled impedance, high-speed differential pairs. Minimize the use of VIAs and 90-degree corners in the routing of the high-speed lines. Assure the high-speed lines reference a solid ground plane and the plane is void of cuts and splits, to prevent impedance discontinuities. ESD connection points must be placed in-line with the high-speed signal traces to reduce reflections caused by routing discontinuities.

6.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00845.

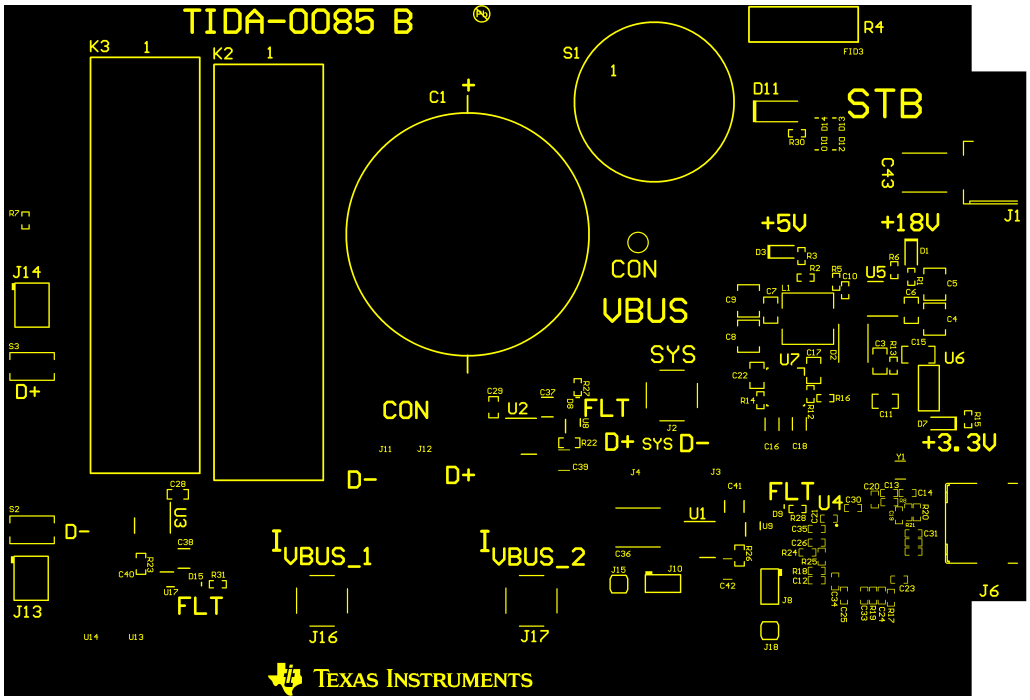

Figure 29. Top Silkscreen

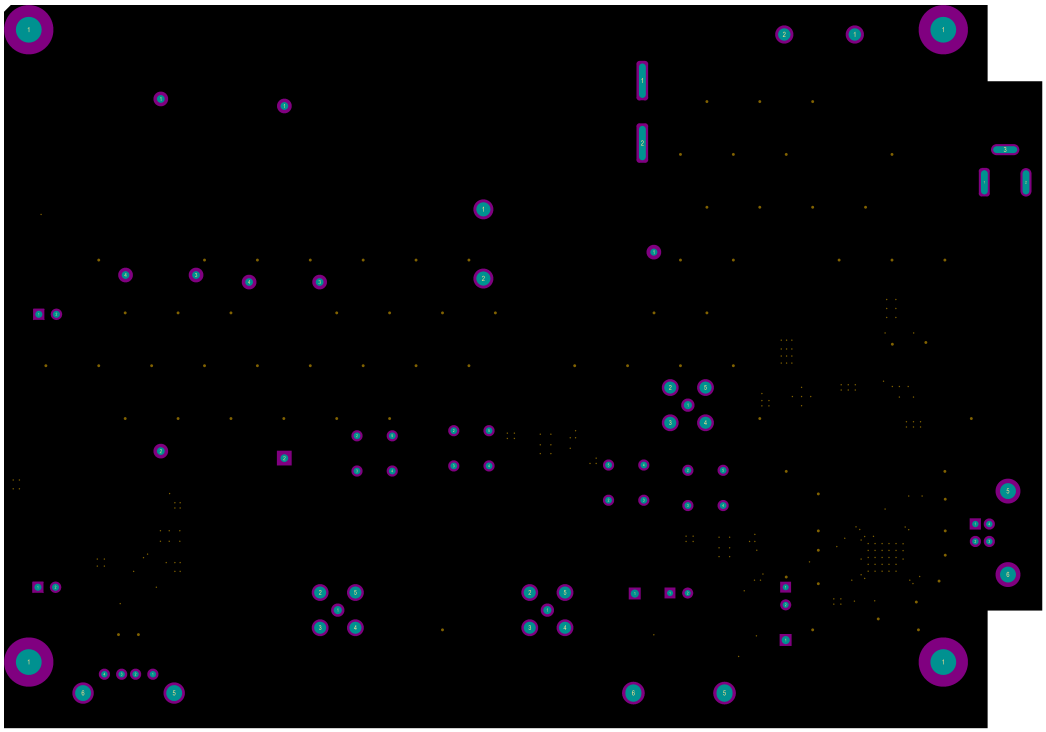

Figure 30. Top Solder Mask

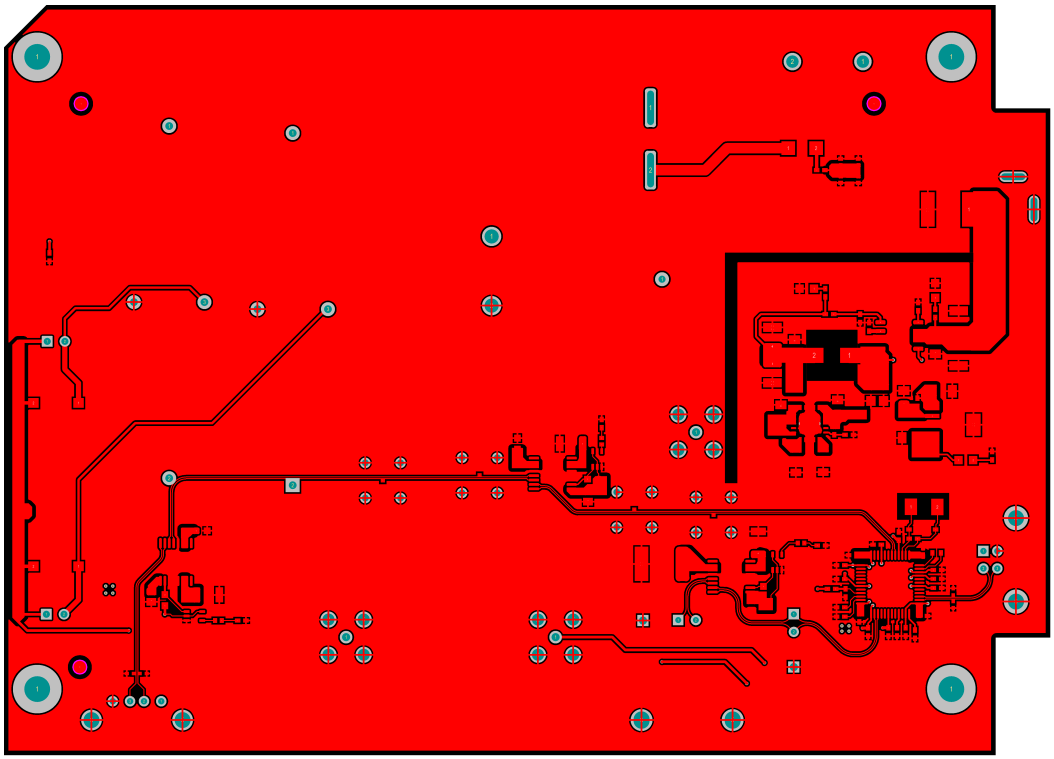

Figure 31. Top Layer

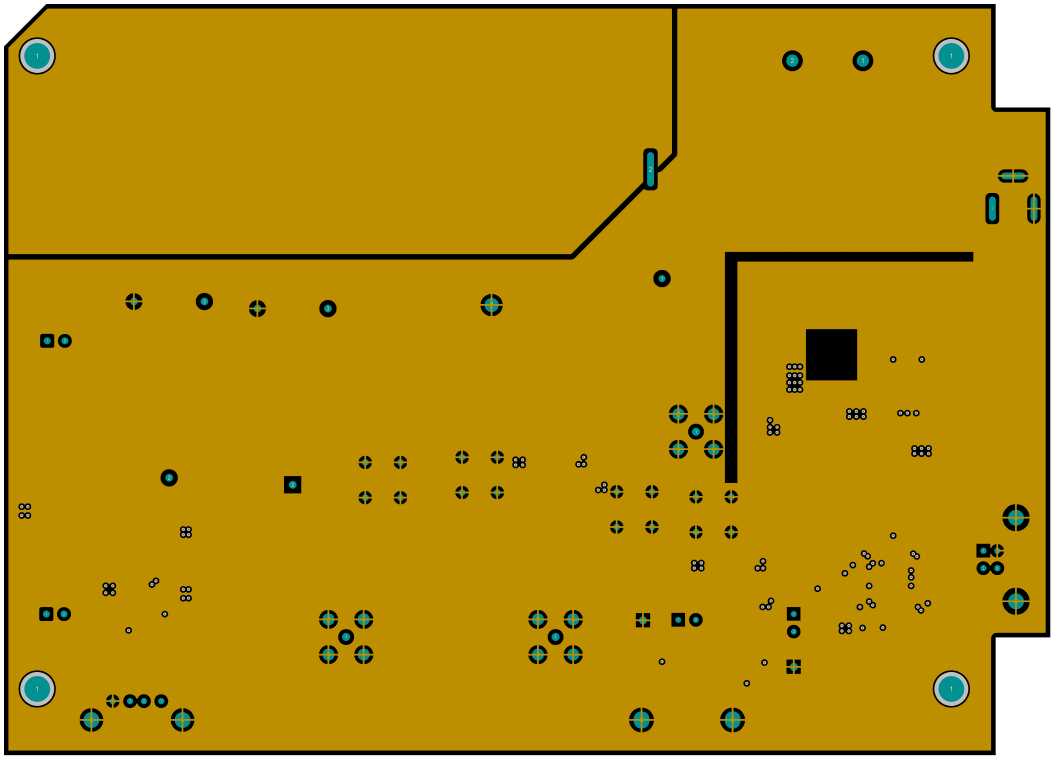

Figure 32. Ground Plane Layer 2

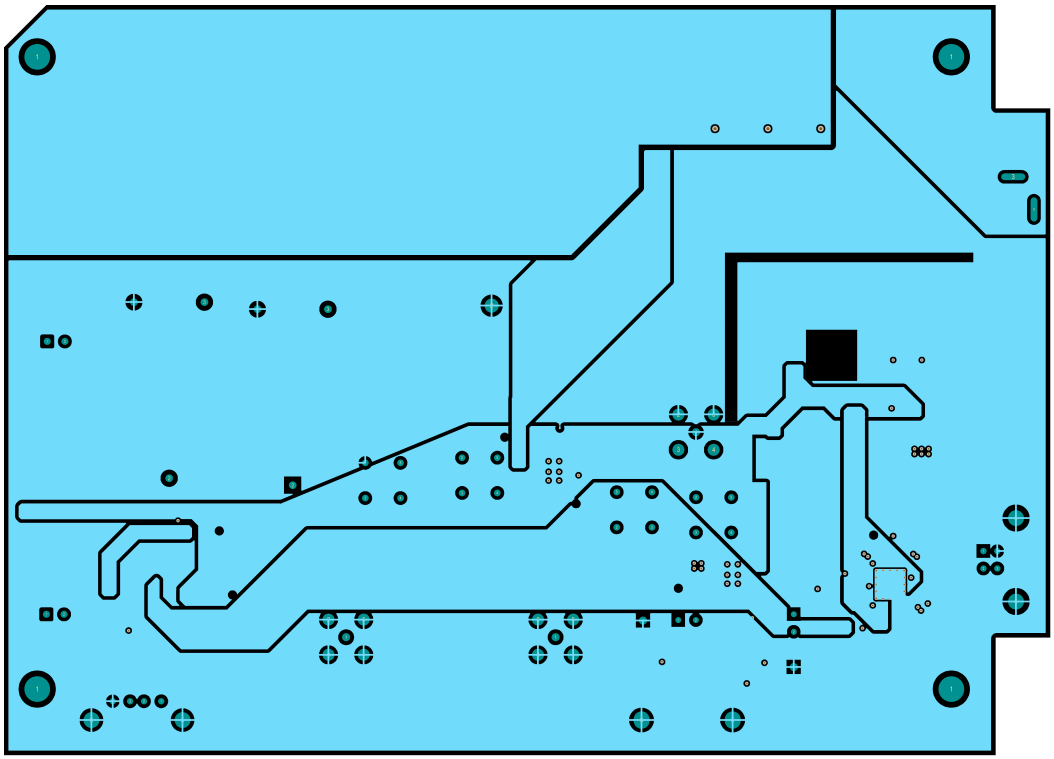

Figure 33. PWR Plane Layer 3

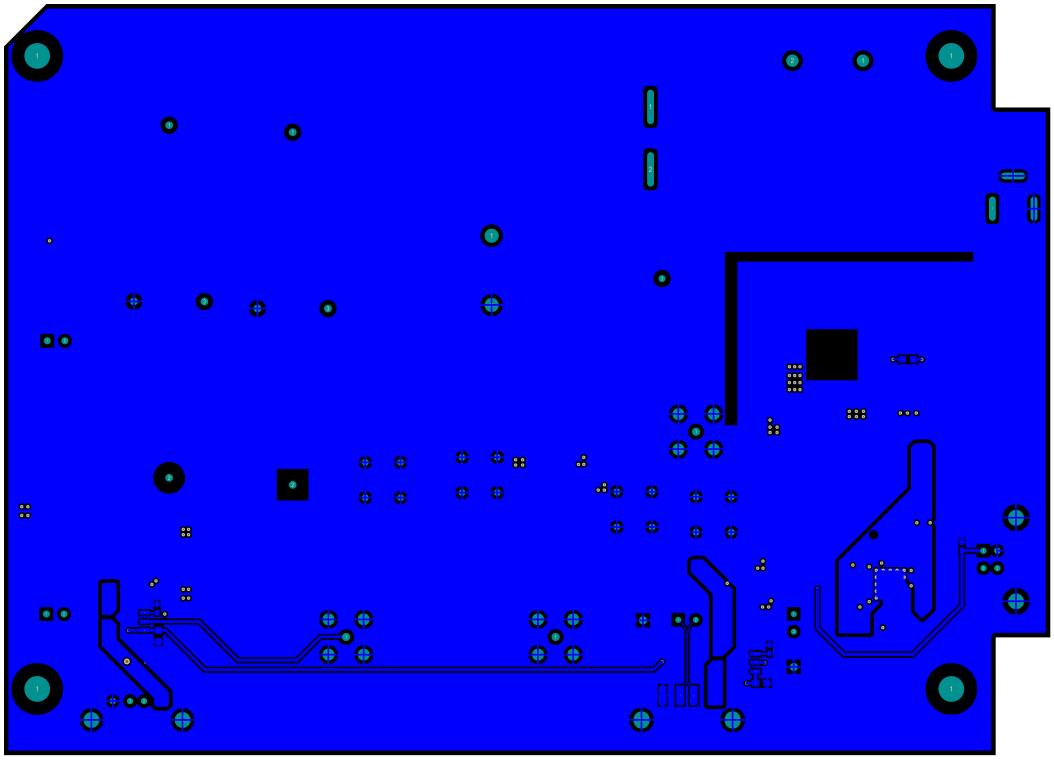

Figure 34. Bottom Layer

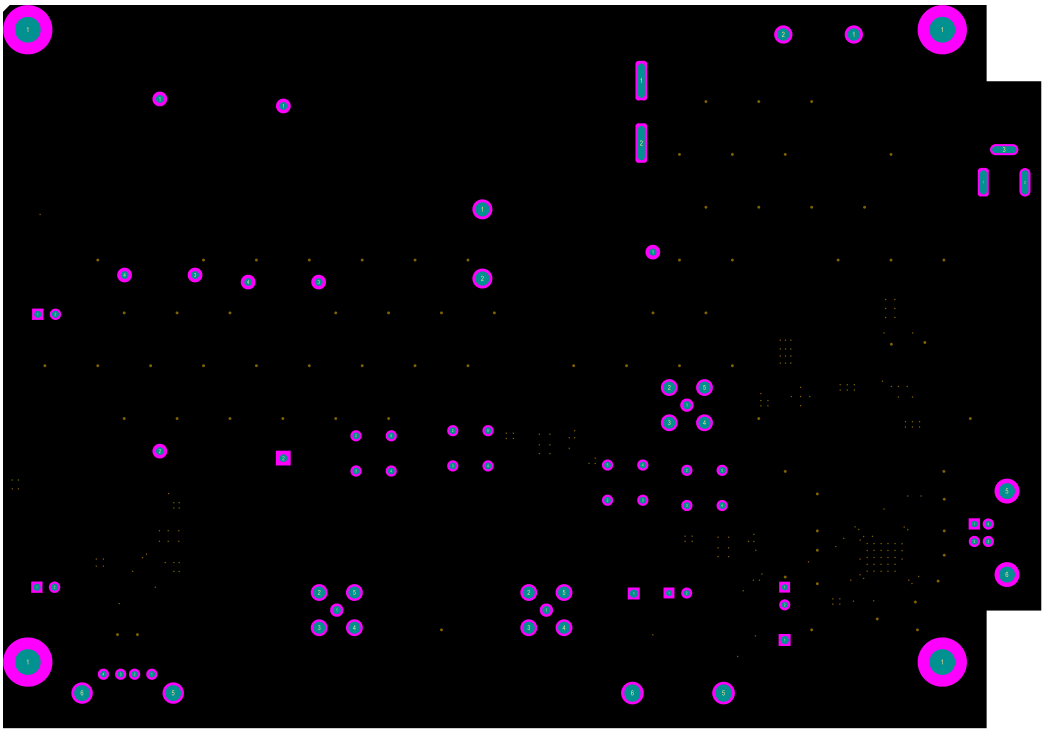

Figure 35. Bottom Solder Mask

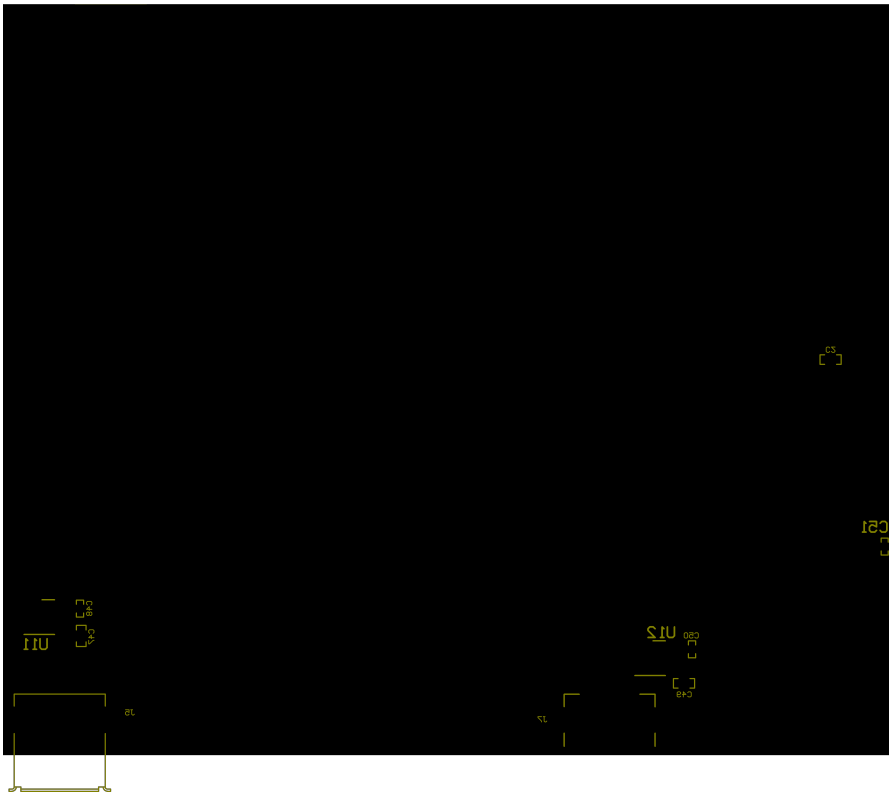

Figure 36. Bottom Silkscreen

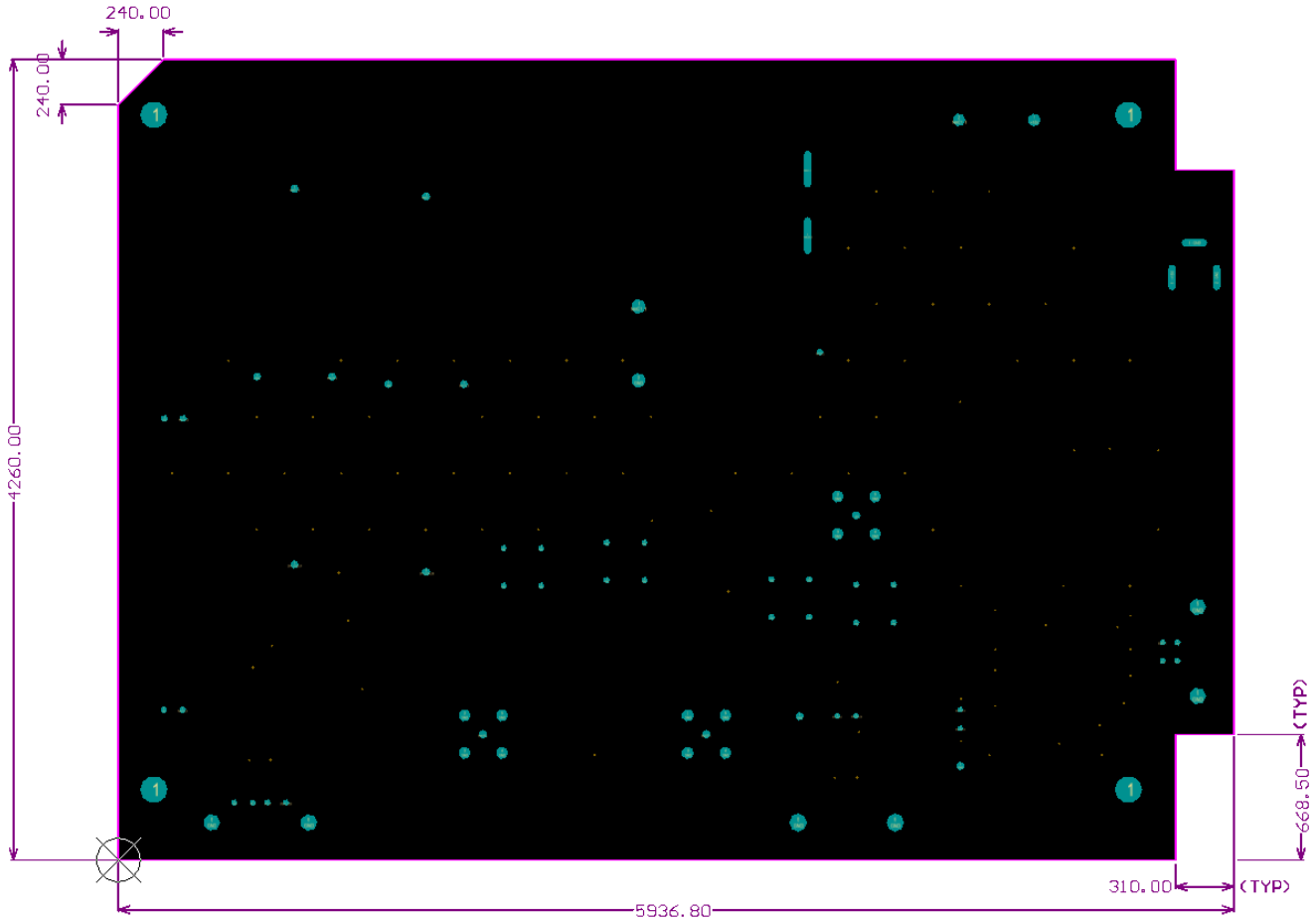

Figure 37. Mechanical Dimensions

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-00845.

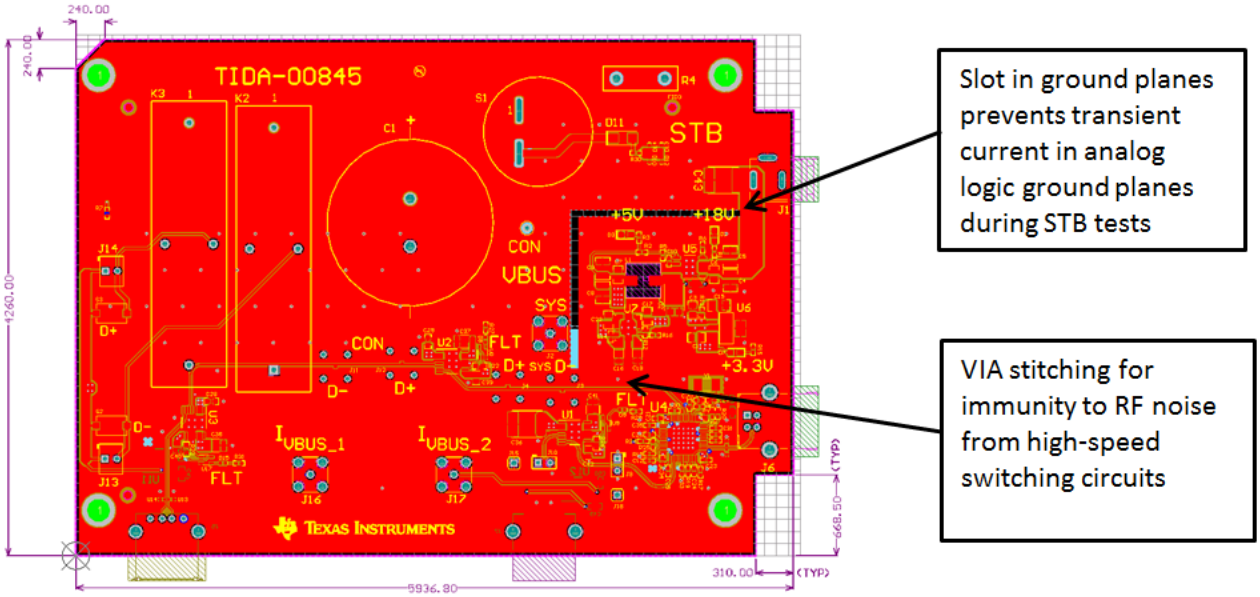

Figure 38. TIDU-00845 Altium

6.5 Layout Guidelines

6.5.1 TPD3S714-Q1

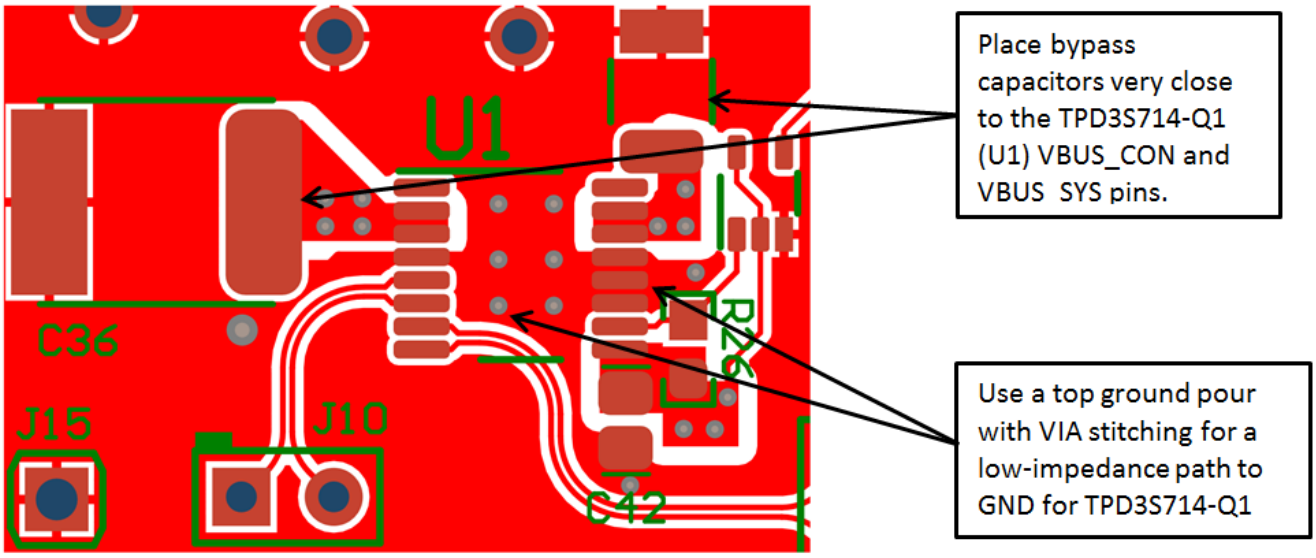

Figure 39. TPD3S714-Q1

6.5.2 LMR14030-Q1 (U5)

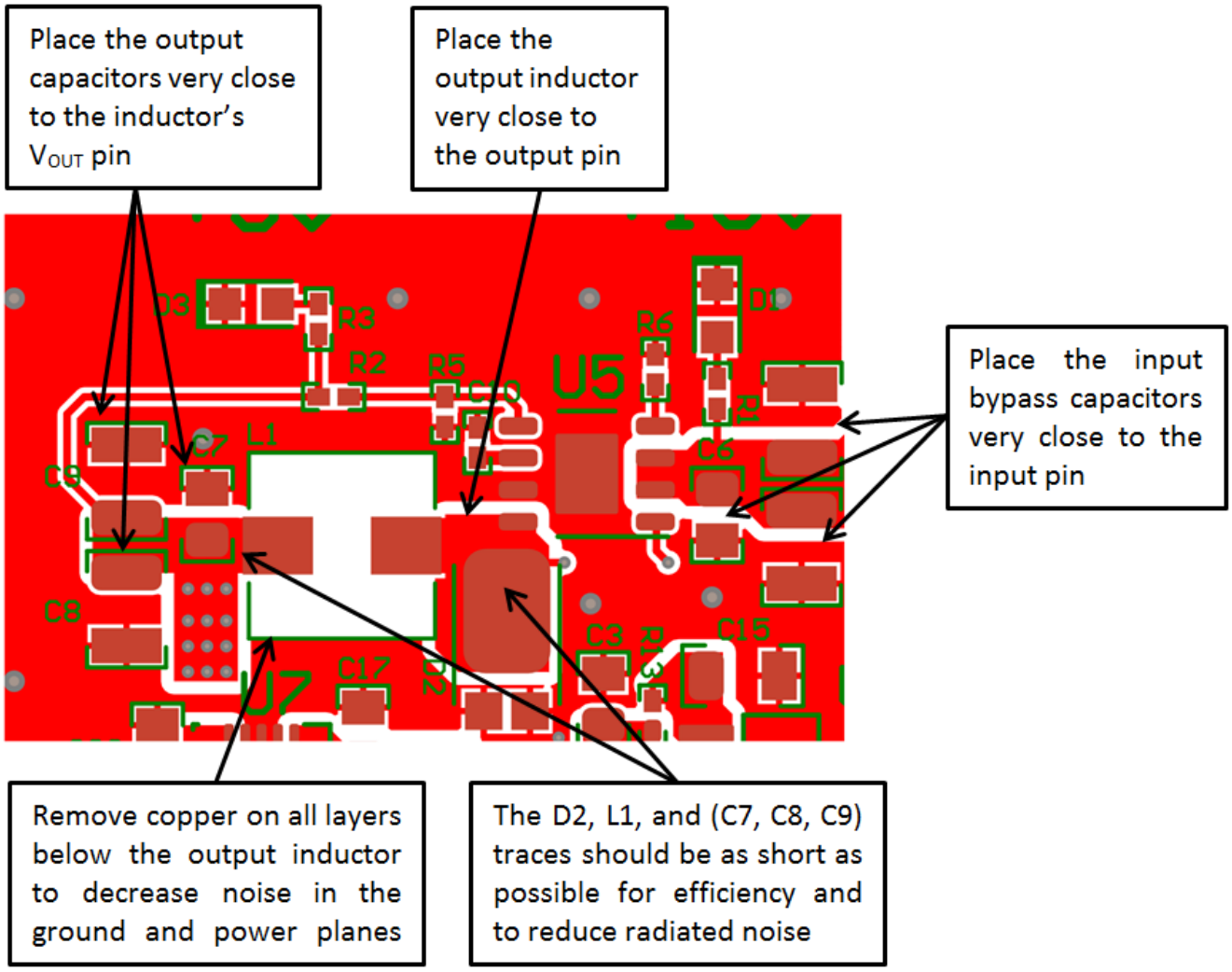

Figure 40. LMR14030-Q1 (U5)

6.5.3 TPS7A4533 (U6)

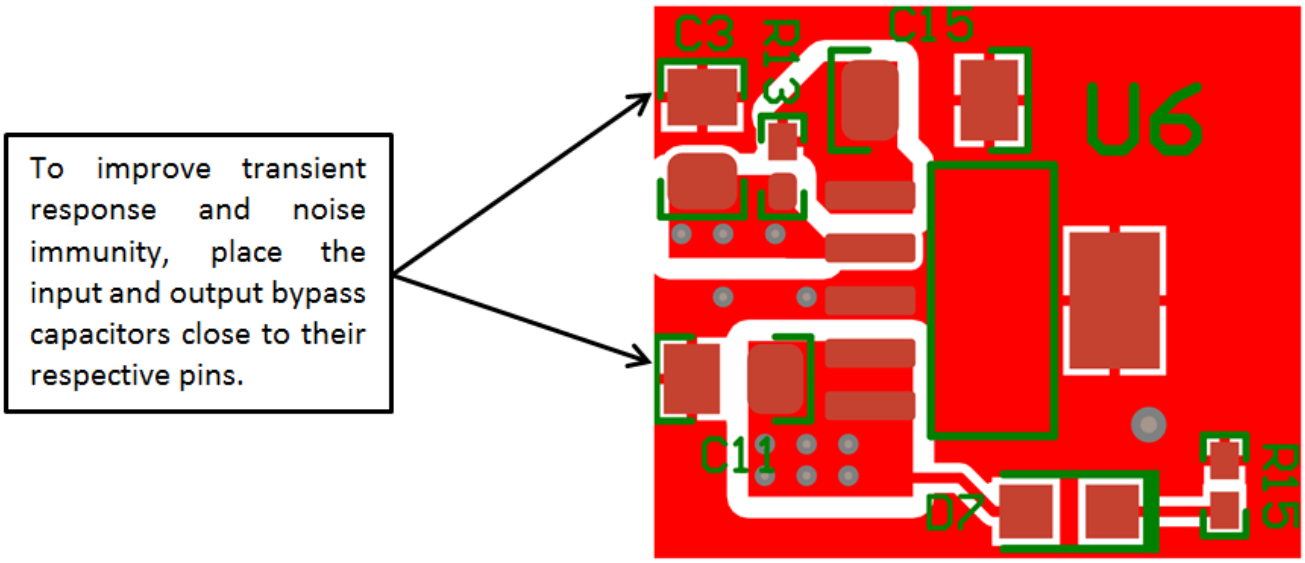

Figure 41. TPS7A4533 (U6)

6.5.4 TPS74801 (U7)

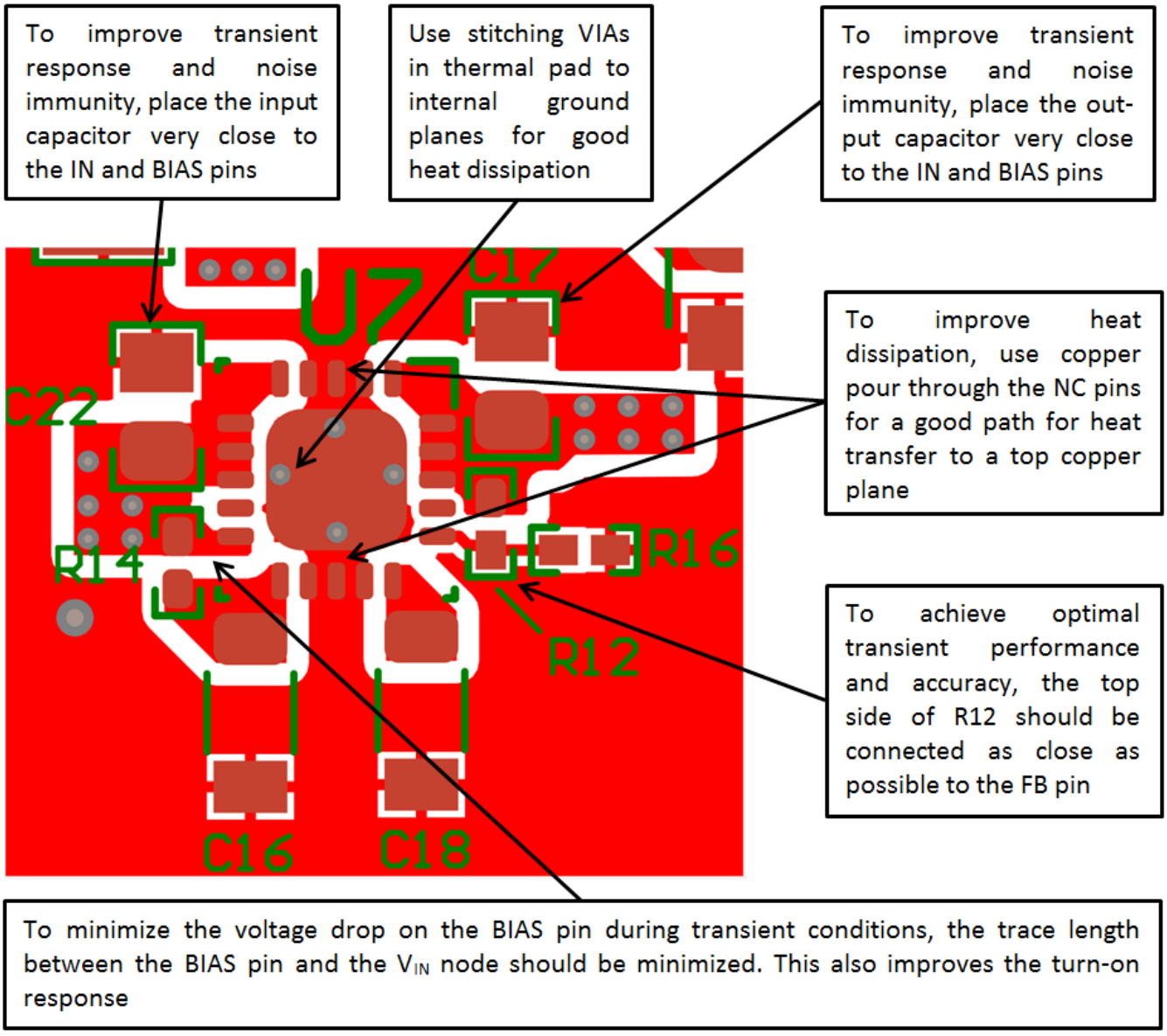

Figure 42. TPS74801 (U7)

6.5.5 TUSB4020BI-Q1 (U4)

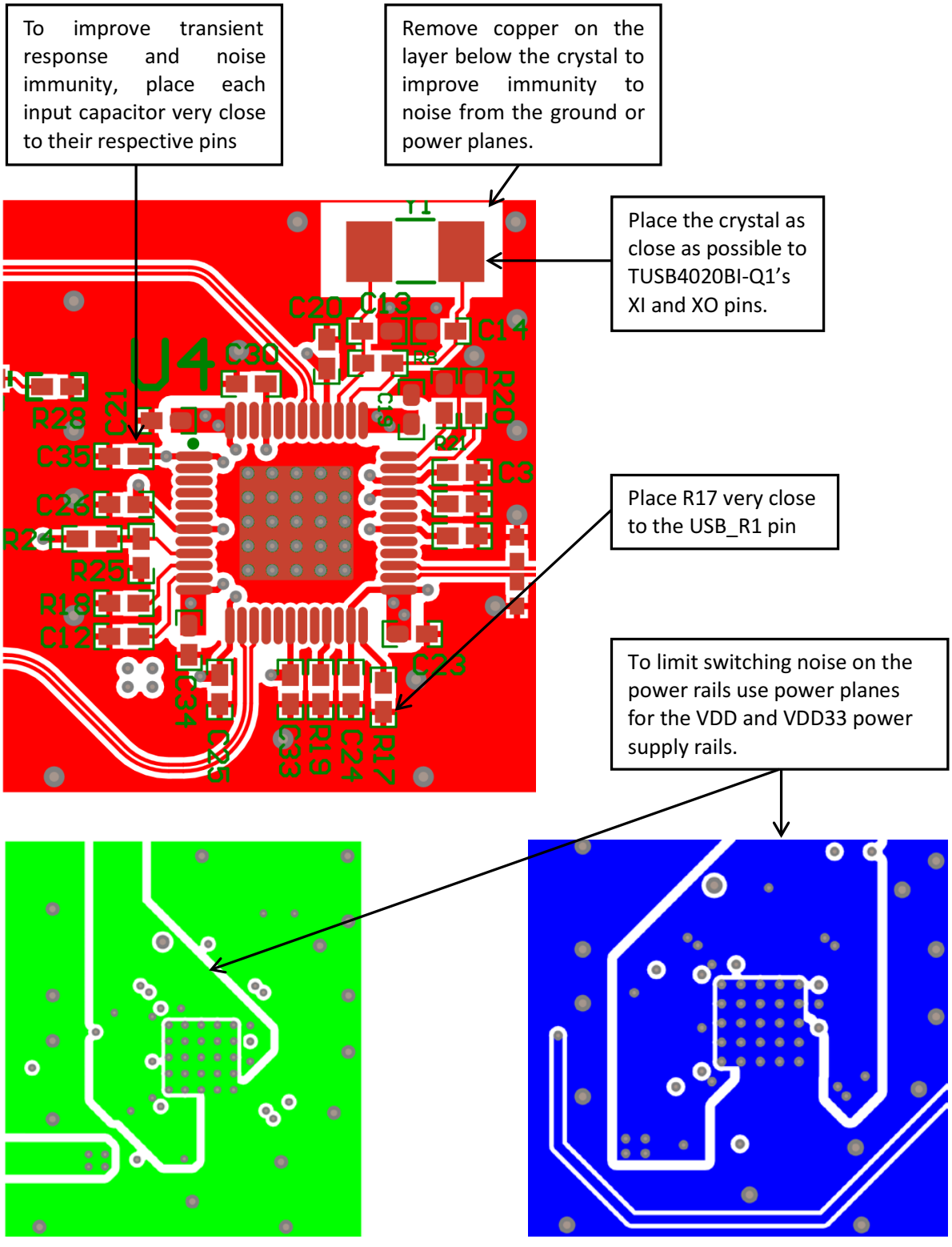

Figure 43. TUSB4020BI-Q1 (U4)

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00845.

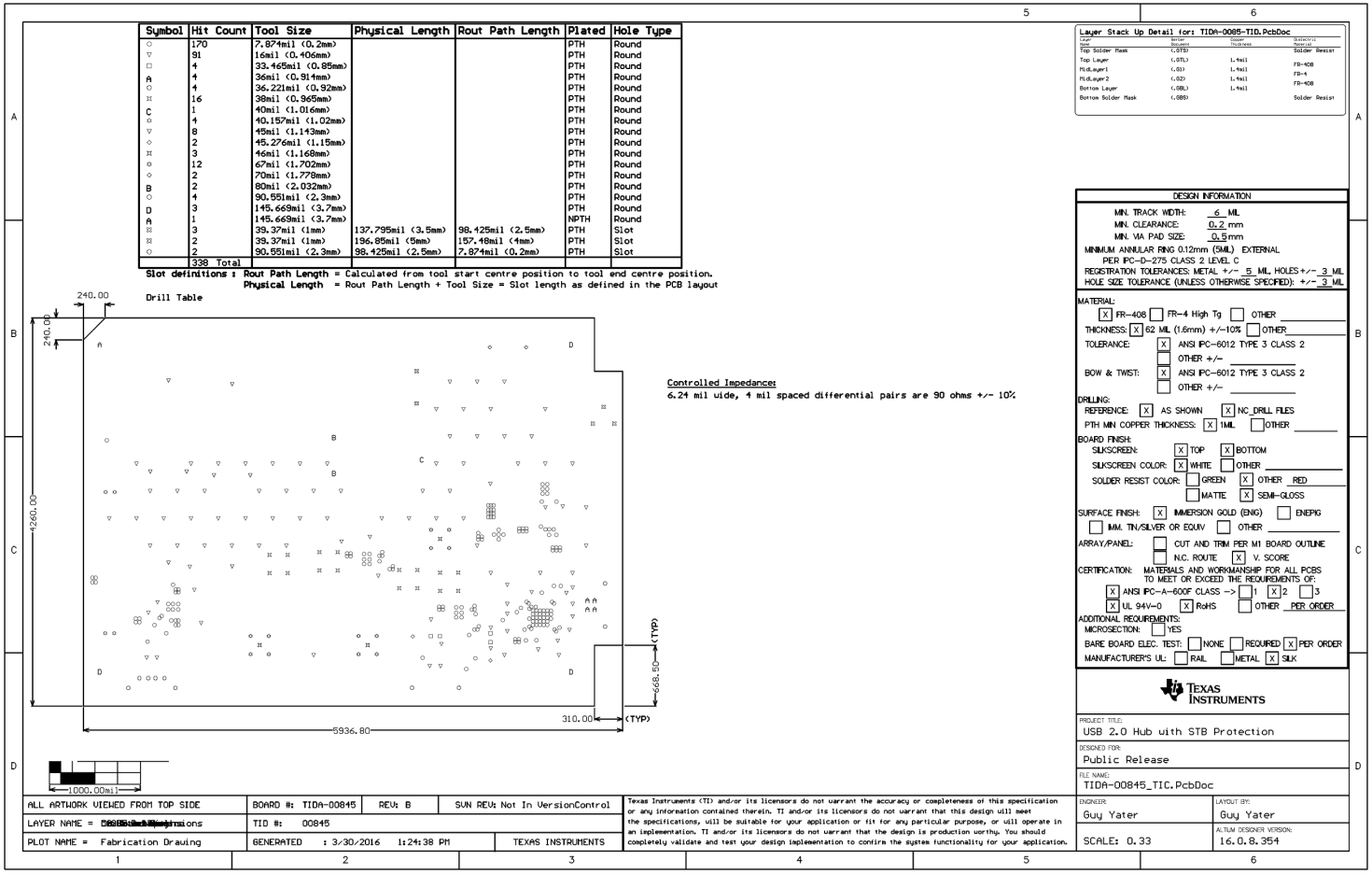

Figure 44. TIDA-00845 Gerber Files

6.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00845.

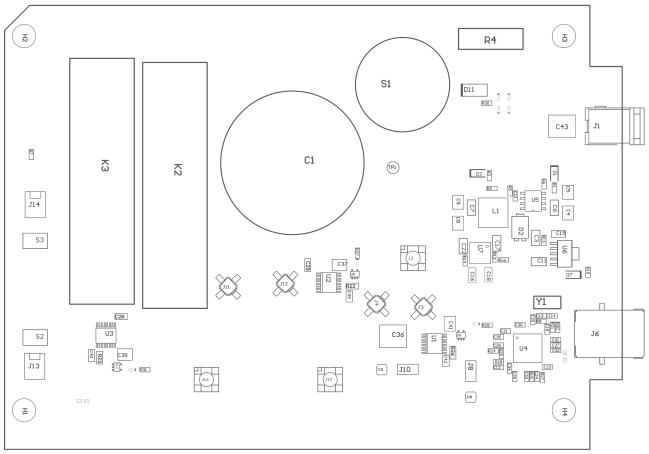

Figure 45. Top Assembly Drawing

Figure 46. Bottom Assembly Drawing

7 References

1. Designing USB for Short-to-battery Tolerance in Automotive Environments, SLLY019, 2016
2. ESD Protection Layout Guide, SLVA680, 2015
3. LDO Noise Demystified, SLAA412, 2008
4. Texas Instruments WEBENCH® Design Center, http://www.ti.com/webench
5. Texas Instruments E2E Community, http://e2e.ti.com/

8 Terminology

- STB – Short to battery
- DP – Downstream port
- UP – Upstream port

9 About the Author

GUY YATER is an Applications Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial, automotive, and consumer interface transient-voltage protection segment. Guy brings to this role his extensive experience in high-speed digital, low-noise analog, and system-level transient-voltage protection design expertise. Guy earned his Bachelors of Science in Electrical Engineering (BSEE) from the University of Texas at Dallas in Richardson, TX. Guy is a current member of the Institute of Electrical and Electronics Engineers (IEEE).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Changed IO Capacitance to 0.42 pF (Typ)	8
• Updated PCB Layout Recommendations Section	29

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