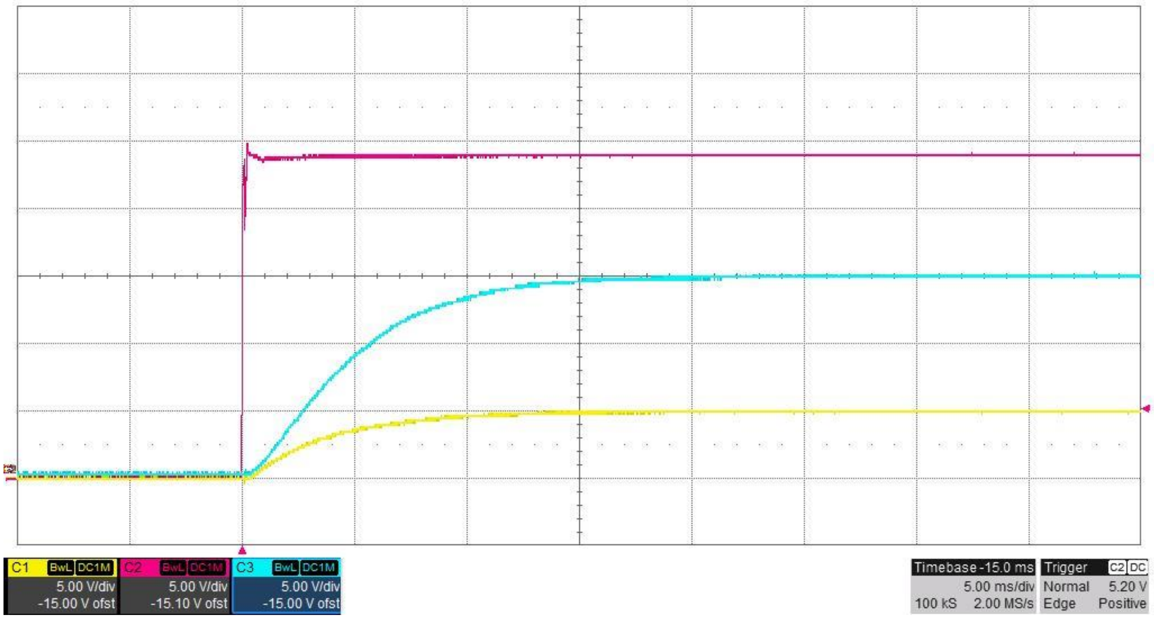
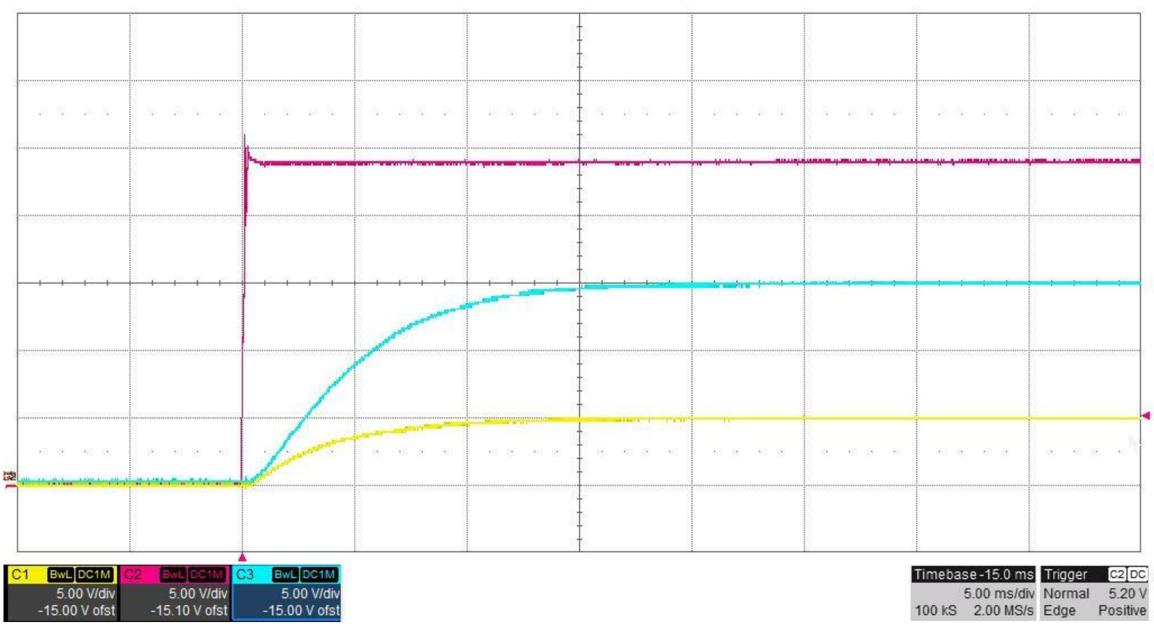
1 Startup

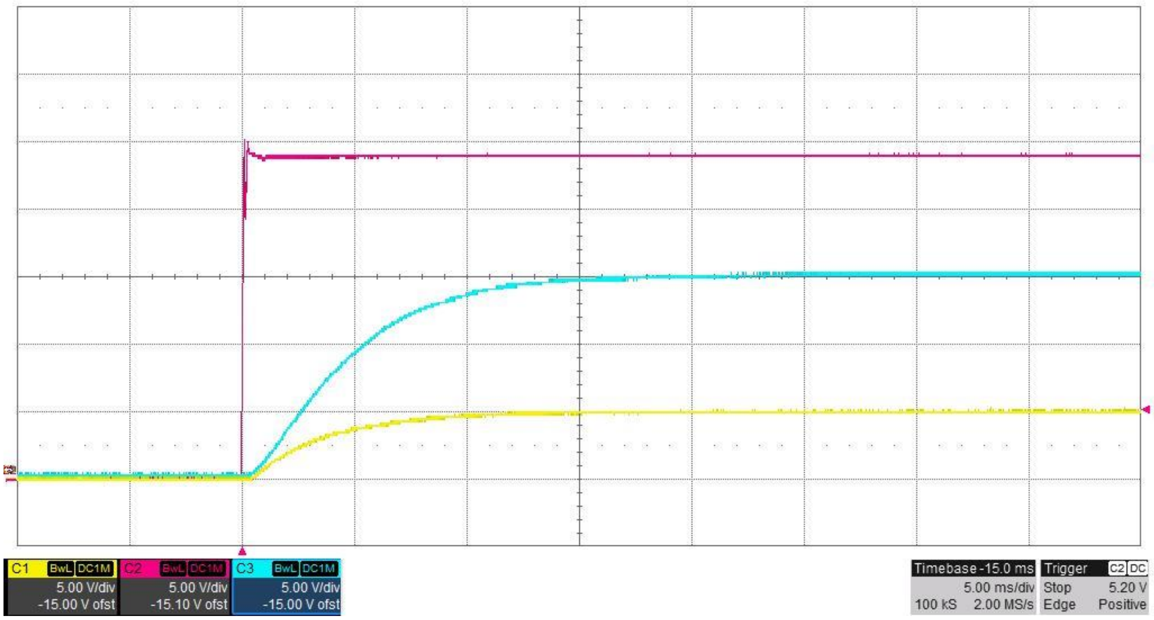
The photo below shows the **15V#1 and 5V#1** output voltage startup waveform, measured at TP2 and TP11, after the input voltage is applied. Vin = 24V, Iout = **0A**. (5V/DIV, 5mS/DIV)



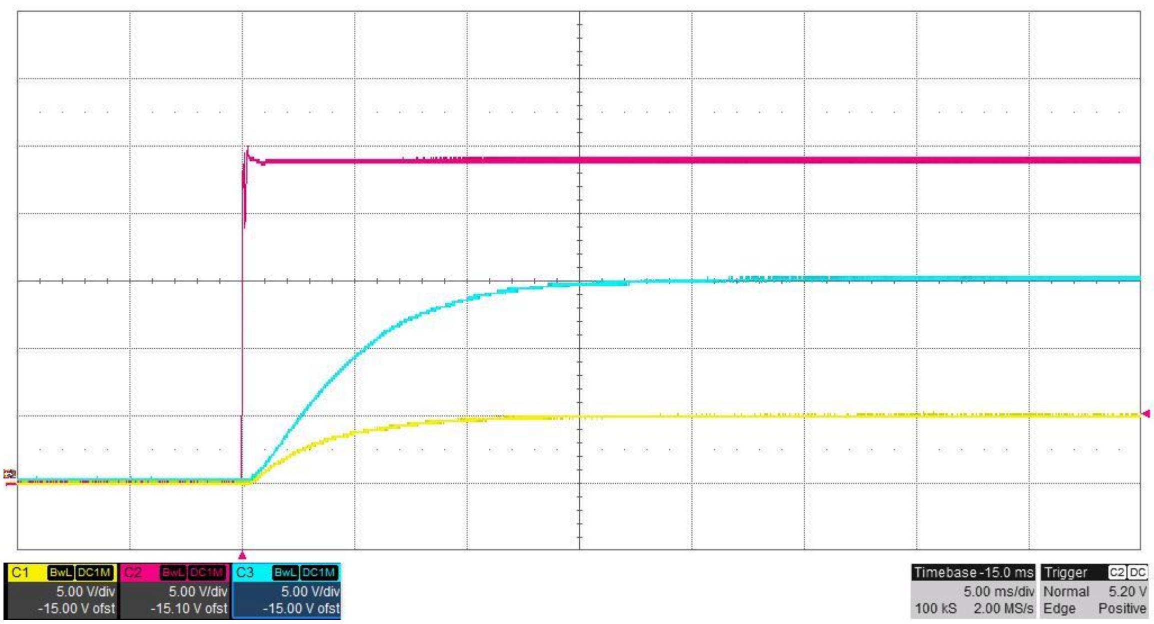
The photo below shows the **15V#1 and 5V#1** output voltage startup waveform, measured at TP2 and TP11, after the input voltage is applied. Vin = 24V, Iout = **0.15A**. (5V/DIV, 5mS/DIV)



The photo below shows the **15V#2 and 5V#2** output voltage startup waveform, measured at TP16 and TP20, after the input voltage is applied. Vin = 24V, Iout = **0A**. (5V/DIV, 5mS/DIV)



The photo below shows the **15V#2 and 5V#2** output voltage startup waveform, measured at TP16 and TP20, after the input voltage is applied. Vin = 24V, Iout = **0.15A**. (5V/DIV, 5mS/DIV)



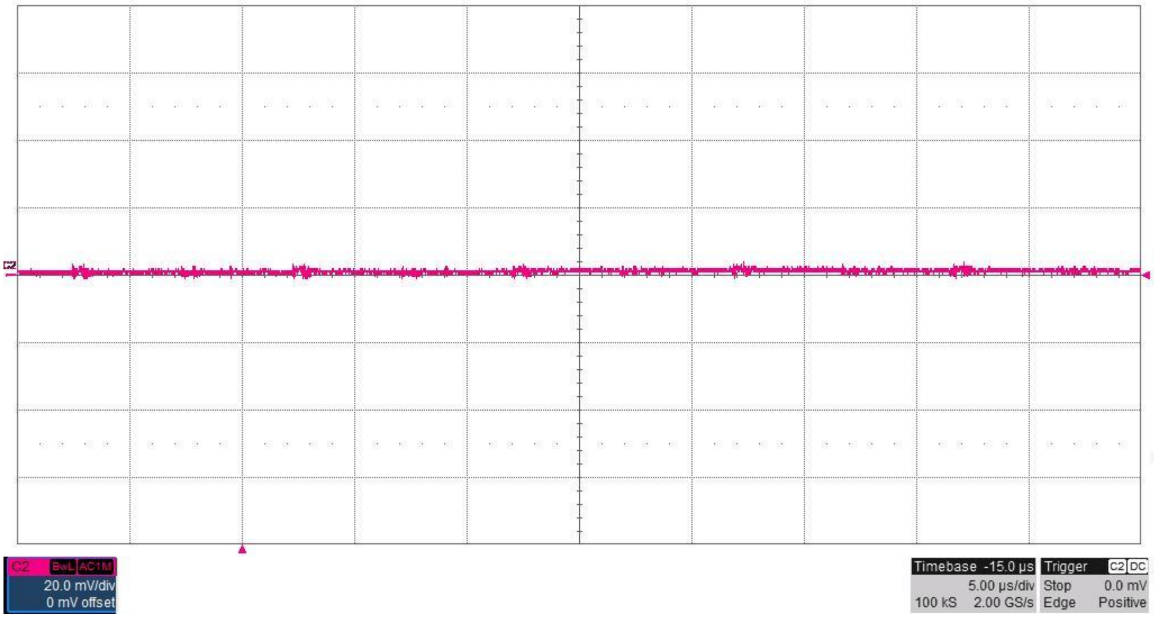
2 Cross Regulation and Efficiency

Cross regulation data for +15V#1/+5V#1 and +15V#2/+5V#2 converters are shown in the table below. All other outputs are operating and unloaded. The efficiency data is for the entire board, but only one set of outputs are loaded. Efficiency data is shown before (Vunreg) and after (Vreg) the linear regulators.

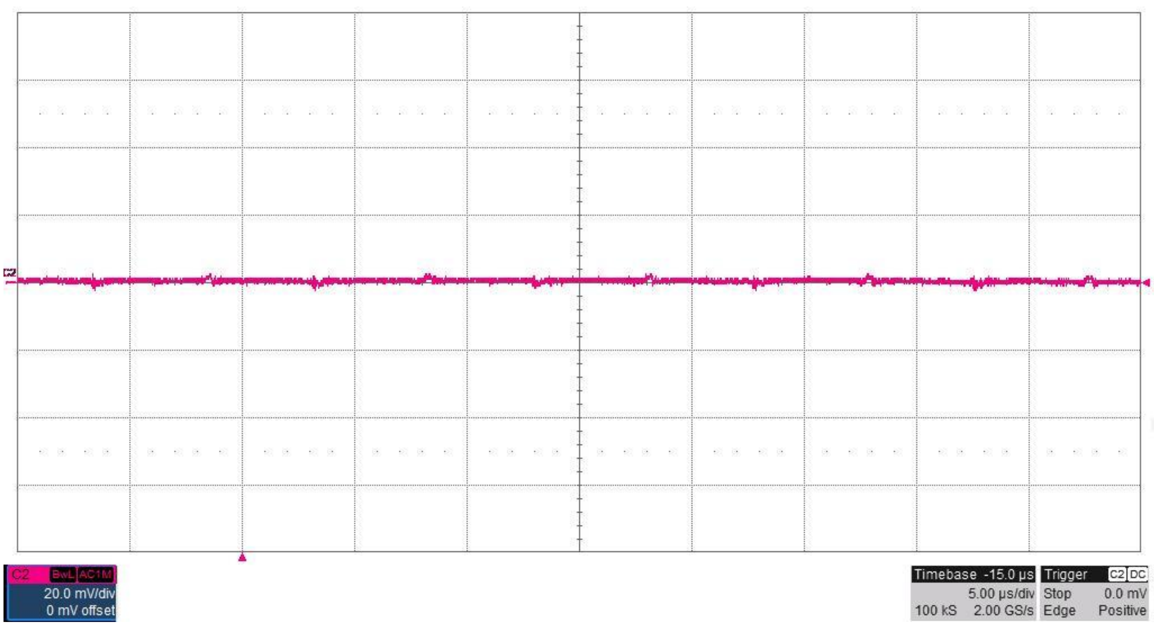
Vin	Iin	V unreg +15V#1	Vout +15#1	Iout +15V#1	V unreg +5V#1	Vout +5#1	Iout +5V#1	Vunreg Eff	Vreg Eff
21.5642	0.1806	**15.98**	14.83	0.1499	**5.95**	5.004	0.1532	0.849	0.768
21.5732	0.1335	15.98	14.83	0.1500	7.03	5.016	0	0.832	0.772
21.5843	0.0624	17.31	14.86	0	5.95	5.005	0.1532	0.676	0.569
21.5918	0.0154	17.31	14.86	0	7.07	5.016	0	0.000	0.000
24.0121	0.1821	17.89	14.83	0.1499	6.69	5.004	0.1532	0.848	0.684
24.0193	0.1349	17.90	14.83	0.1499	7.84	5.016	0	0.828	0.686
24.0300	0.0637	19.12	14.86	0	6.70	5.004	0.1532	0.671	0.501
24.0371	0.0167	19.13	14.86	0	7.88	5.016	0	0.000	0.000
26.4157	0.1833	19.77	14.83	0.1499	7.43	5.004	0.1532	0.847	0.617
26.4225	0.1361	19.78	14.83	0.1499	8.62	5.016	0	0.825	0.618
26.4328	0.0650	21.23	14.86	0	7.43	5.004	0.1532	0.663	0.446
26.4396	0.0179	**21.28**	14.86	0	**8.67**	6.016	0	0.000	0.000
Vin	**Iin**	**V unreg +15V#2**	**Vout +15#2**	**Iout +15V#2**	**V unreg +5V#2**	**Vout +5#2**	**Iout +5V#2**		
21.5682	0.1920	**15.97**	14.93	0.1508	**5.98**	5.057	0.1548	0.805	0.733
21.5754	0.1390	16.11	14.93	0.1508	6.59	5.064	0	0.810	0.751
21.5851	0.0675	17.06	14.95	0	6.12	5.058	0.1548	0.650	0.537
21.5921	0.0150	18.47	14.95	0	7.14	5.064	0	0.000	0.000
24.0132	0.1920	17.95	14.93	0.1508	6.79	5.057	0.1548	0.815	0.658
24.0204	0.1403	18.11	14.93	0.1509	7.42	5.063	0	0.811	0.669
24.0301	0.0685	19.10	14.95	0	6.94	5.057	0.1548	0.653	0.476
24.0371	0.0165	20.56	14.95	0	8.01	5.064	0	0.000	0.000
26.4161	0.1935	19.91	14.93	0.1509	7.60	5.055	0.1547	0.818	0.594
26.4232	0.1415	20.07	14.93	0.1509	8.24	5.063	0	0.810	0.603
26.4328	0.0698	21.11	14.95	0	7.75	5.055	0.1547	0.650	0.424
26.4398	0.0179	**22.62**	14.95	0	**8.86**	5.063	0	0.000	0.000

3 Output Ripple Voltage

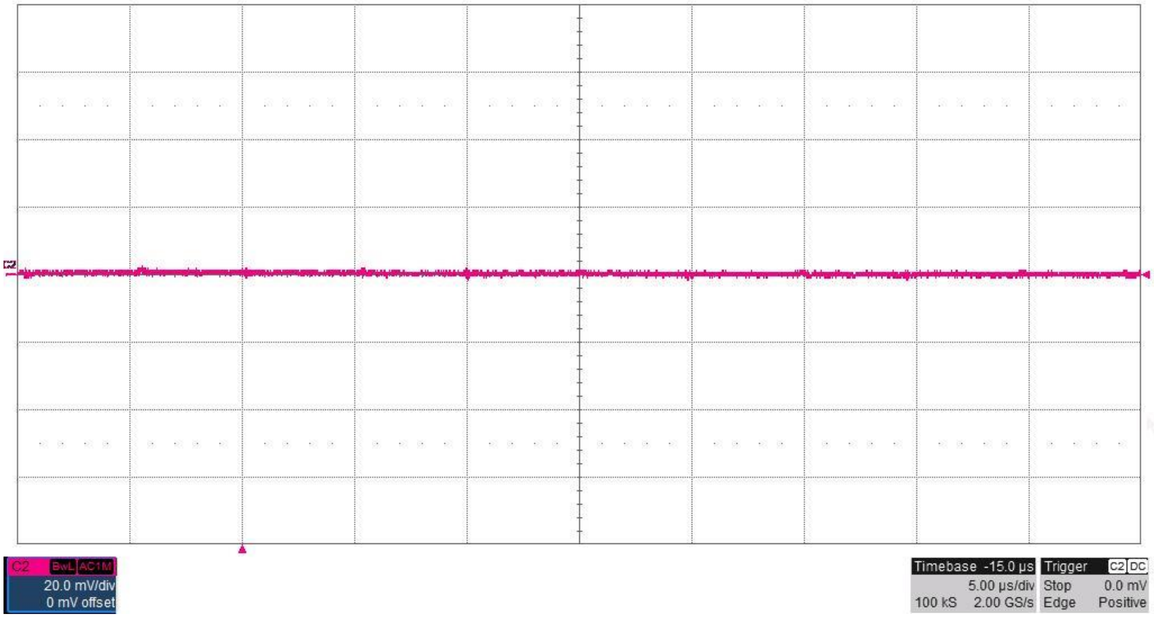
The output ripple voltage is shown in the figure below. The image was taken with the **5V#1** output loaded to **0.15A** and the input voltage set to 26.4V. (20mV/DIV, 5uS/DIV)



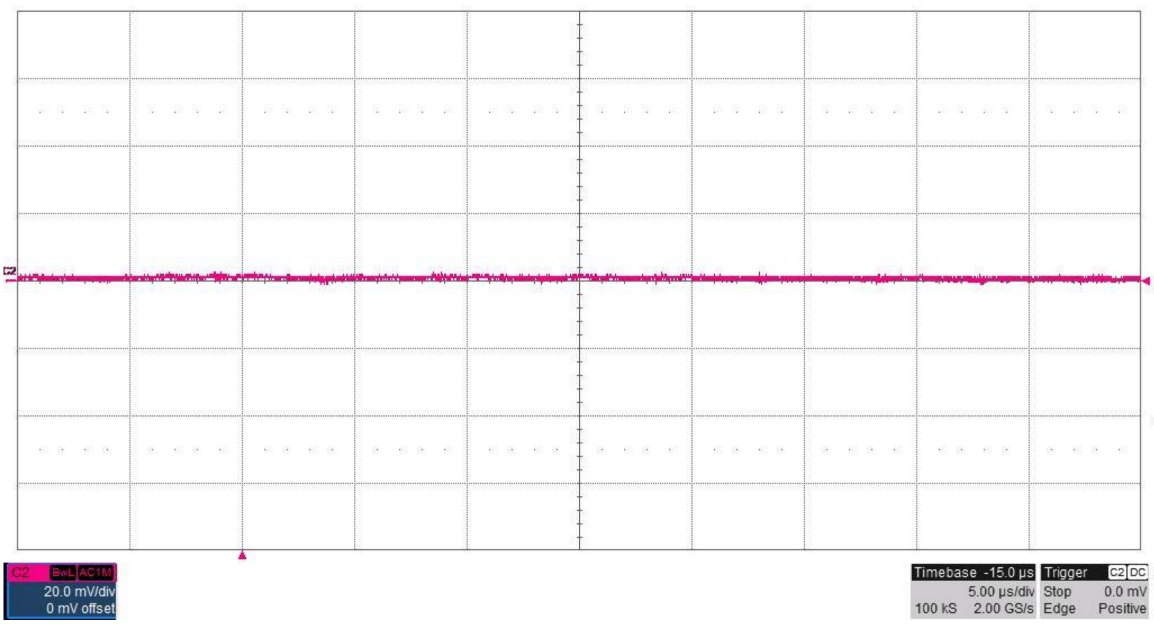
The output ripple voltage is shown in the figure below. The image was taken with the **15V#1** output loaded to **0.15A** and the input voltage set to 26.4V. (20mV/DIV, 5uS/DIV)



The output ripple voltage is shown in the figure below. The image was taken with the **5V#2** output loaded to **0.15A** and the input voltage set to 26.4V. (20mV/DIV, 5uS/DIV)

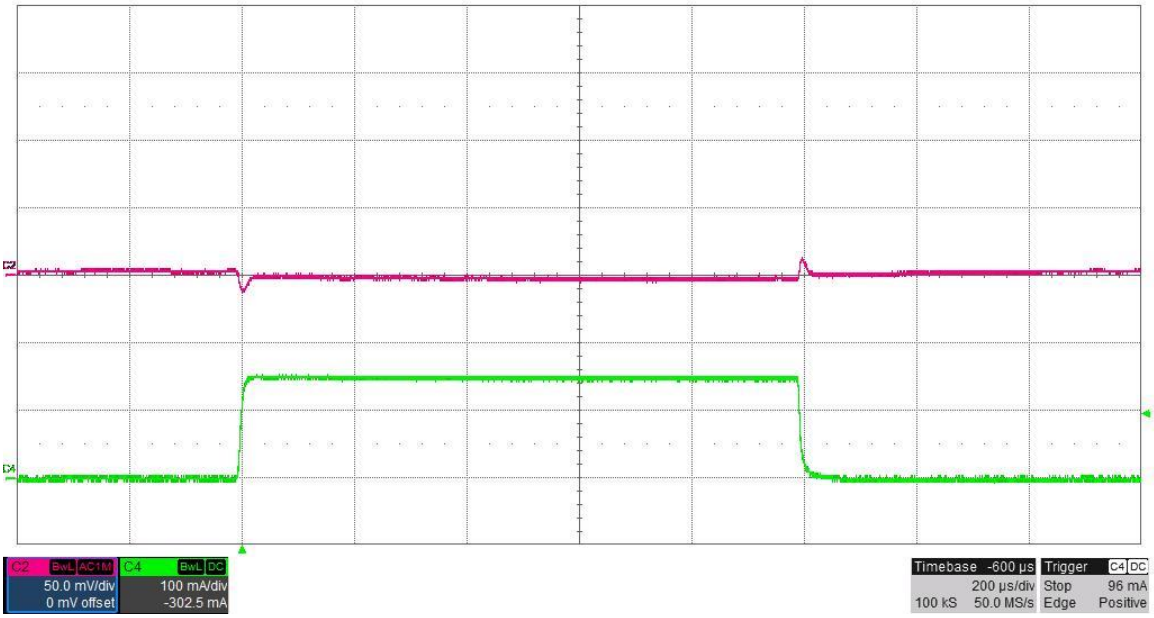


The output ripple voltage is shown in the figure below. The image was taken with the **15V#2** output loaded to **0.15A** and the input voltage set to 26.4V. (20mV/DIV, 5uS/DIV)

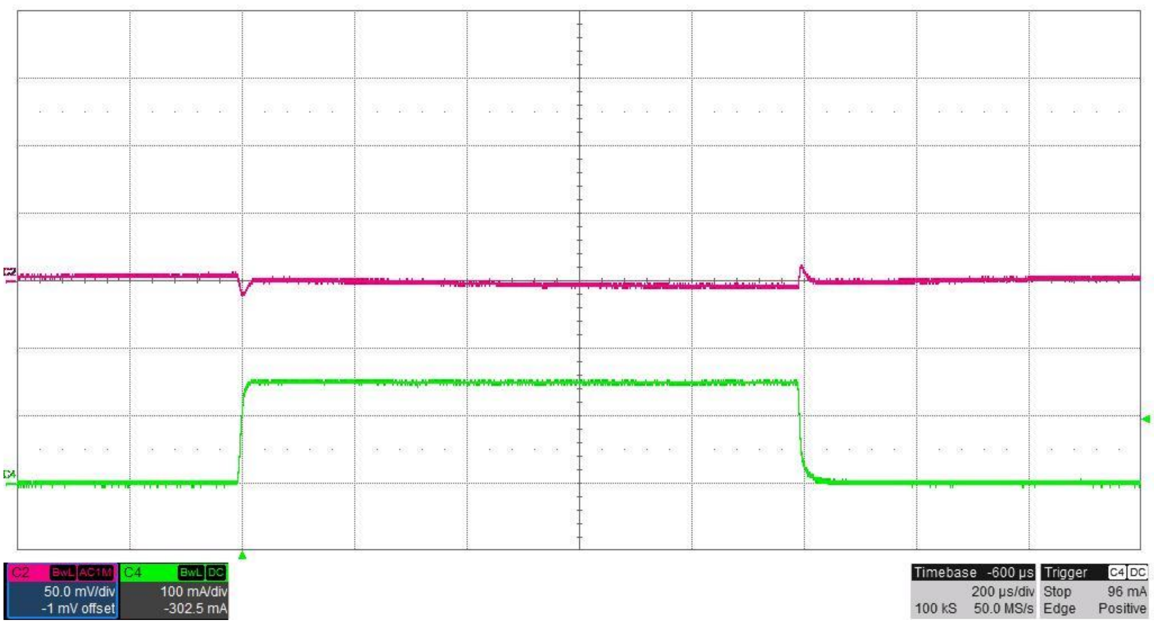


4 Load Transients

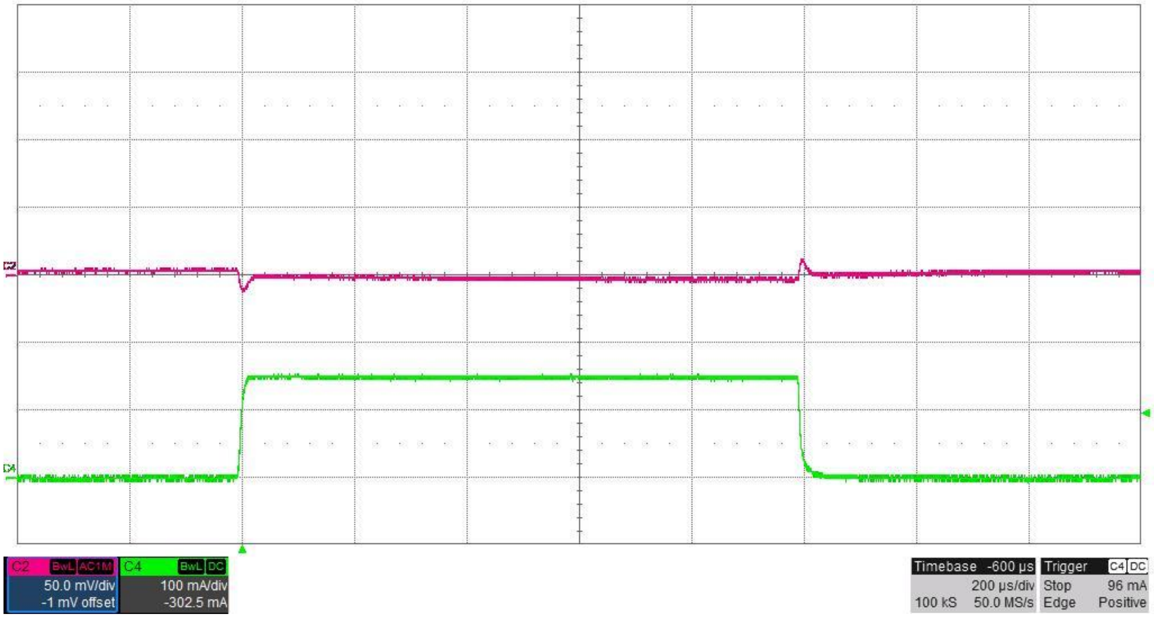
The photo below shows the **5V#1** output voltage (ac coupled) when the load current is stepped between 0A and 0.15A. Vin = 24V. (50mV/DIV, 100mA/DIV, 200uS/DIV)



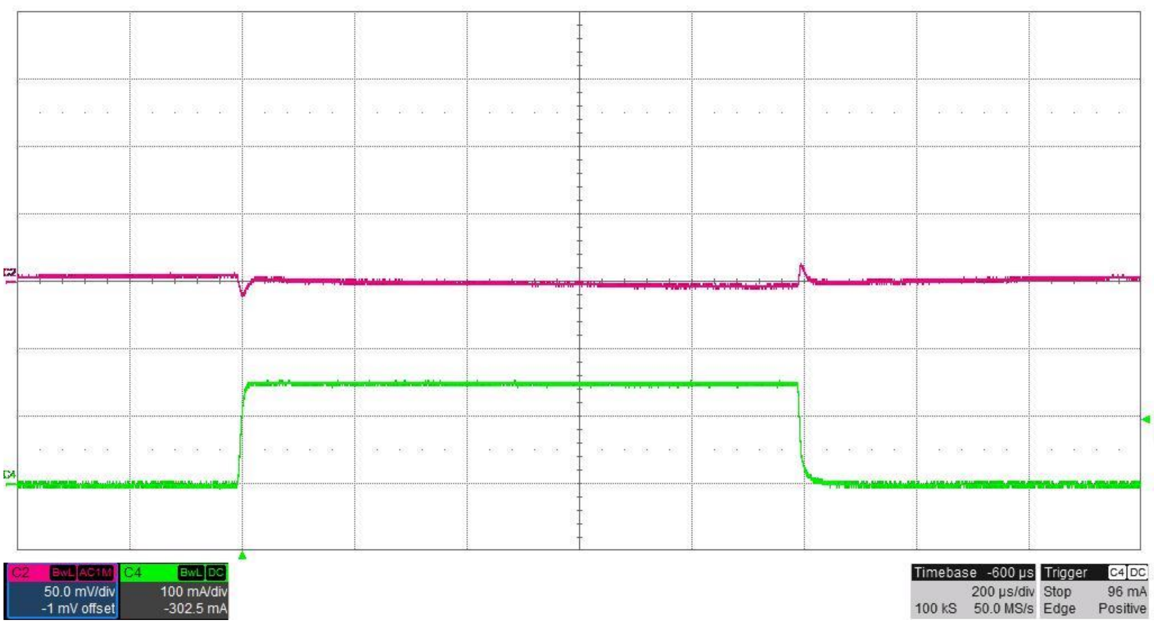
The photo below shows the **15V#1** output voltage (ac coupled) when the load current is stepped between 0A and 0.15A. Vin = 24V. (50mV/DIV, 100mA/DIV, 200uS/DIV)



The photo below shows the **5V#2** output voltage (ac coupled) when the load current is stepped between 0A and 0.15A. Vin = 24V. (50mV/DIV, 100mA/DIV, 200uS/DIV)

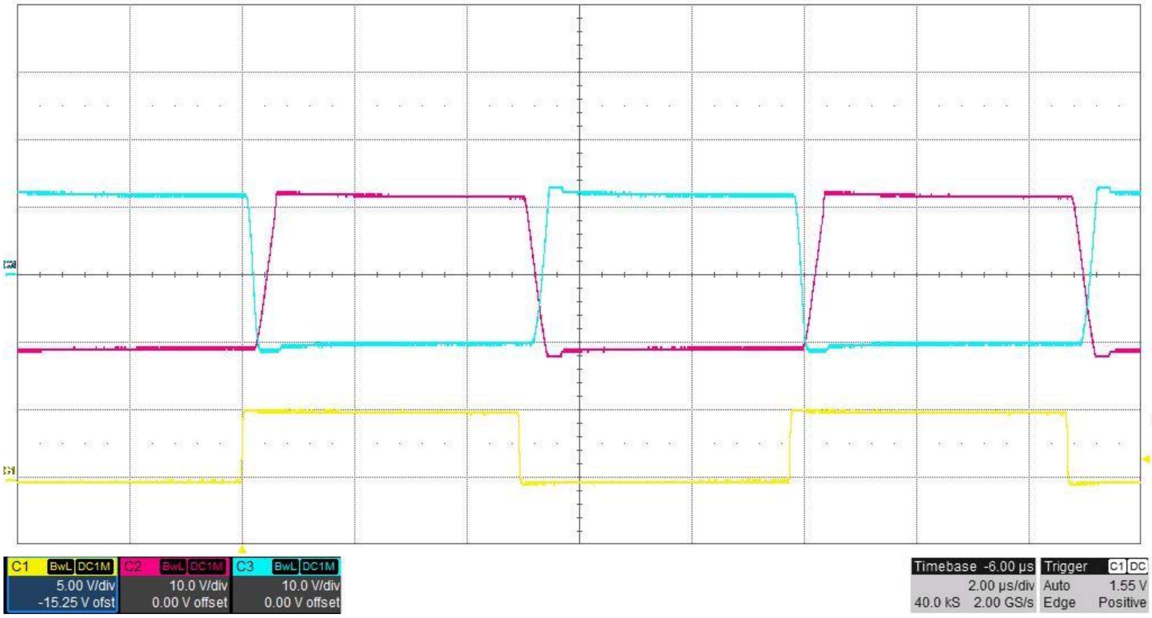


The photo below shows the **15V#2** output voltage (ac coupled) when the load current is stepped between 0A and 0.15A. Vin = 24V. (50mV/DIV, 100mA/DIV, 200uS/DIV)

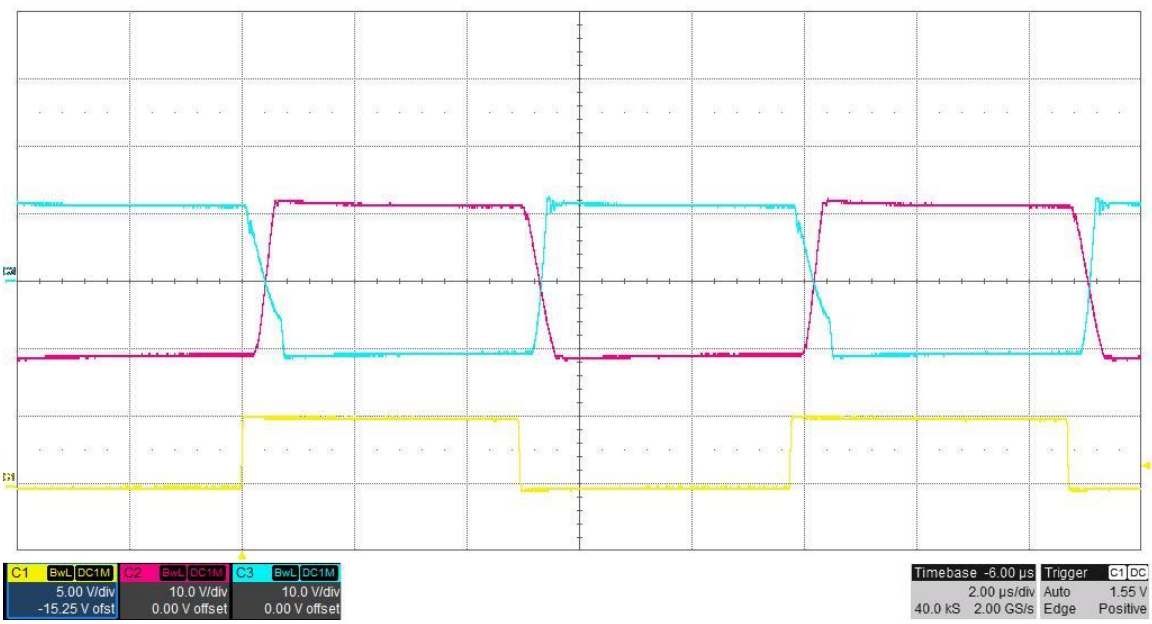


5 Switch Node Waveforms

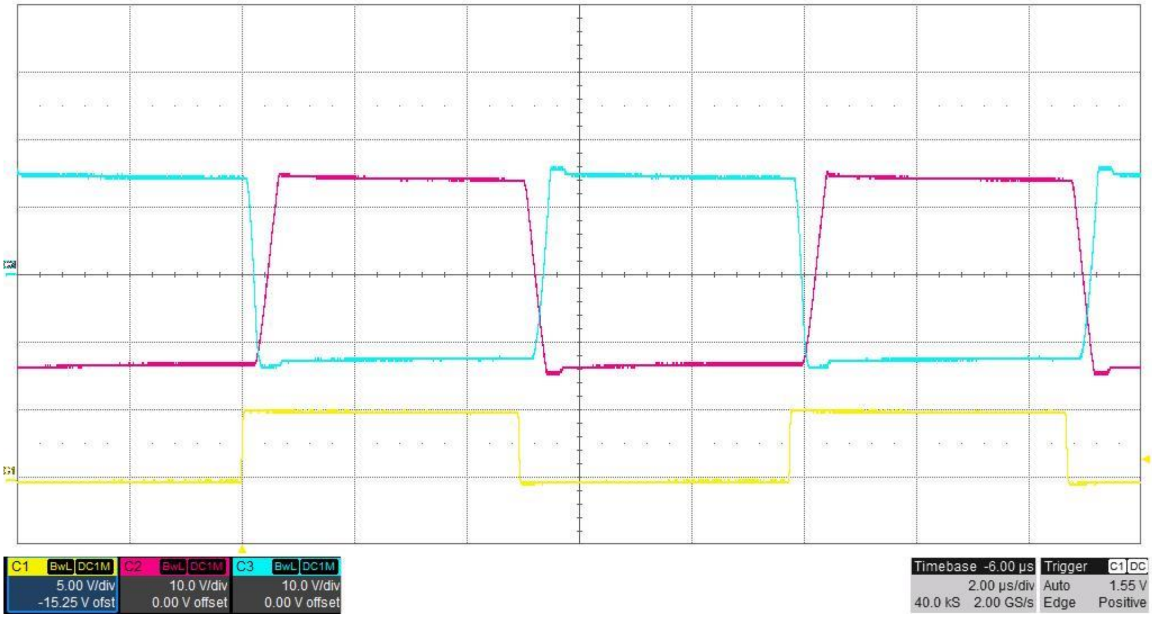
The photo below shows the switch node voltages of **15V#1 and 5V#1**, measured at TP4 and TP12 and the PHASE clock signal. **Vin = 21.6V**, Iout = **0A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



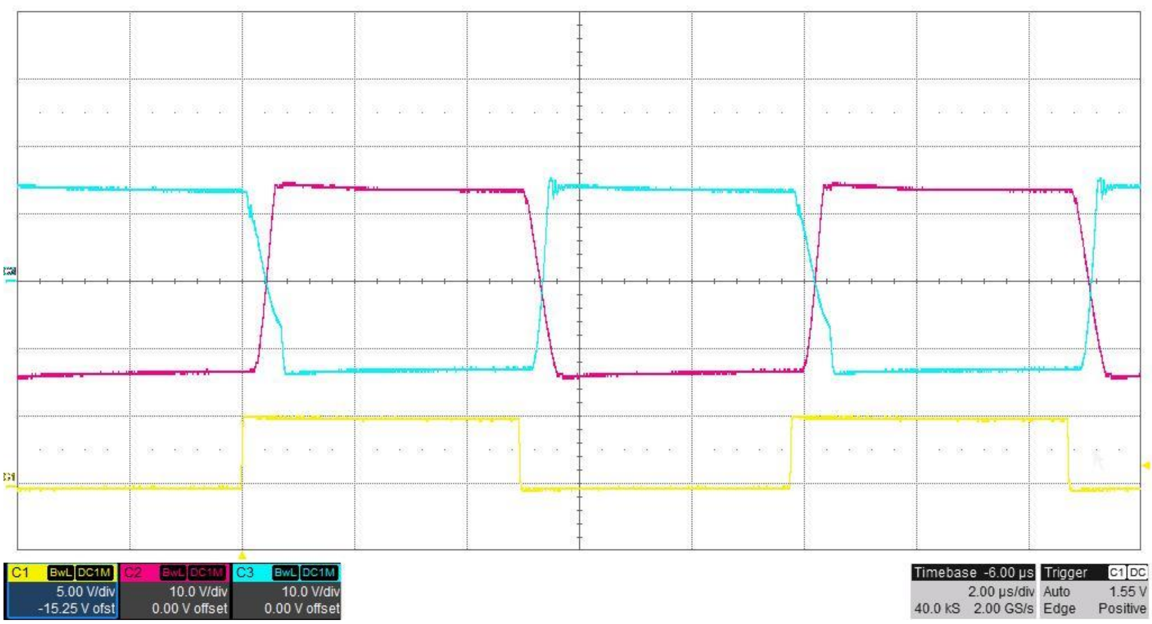
The photo below shows the switch node voltages of **15V#1 and 5V#1**, measured at TP4 and TP12 and the PHASE clock signal. **Vin = 21.6V**, Iout = **0.15A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



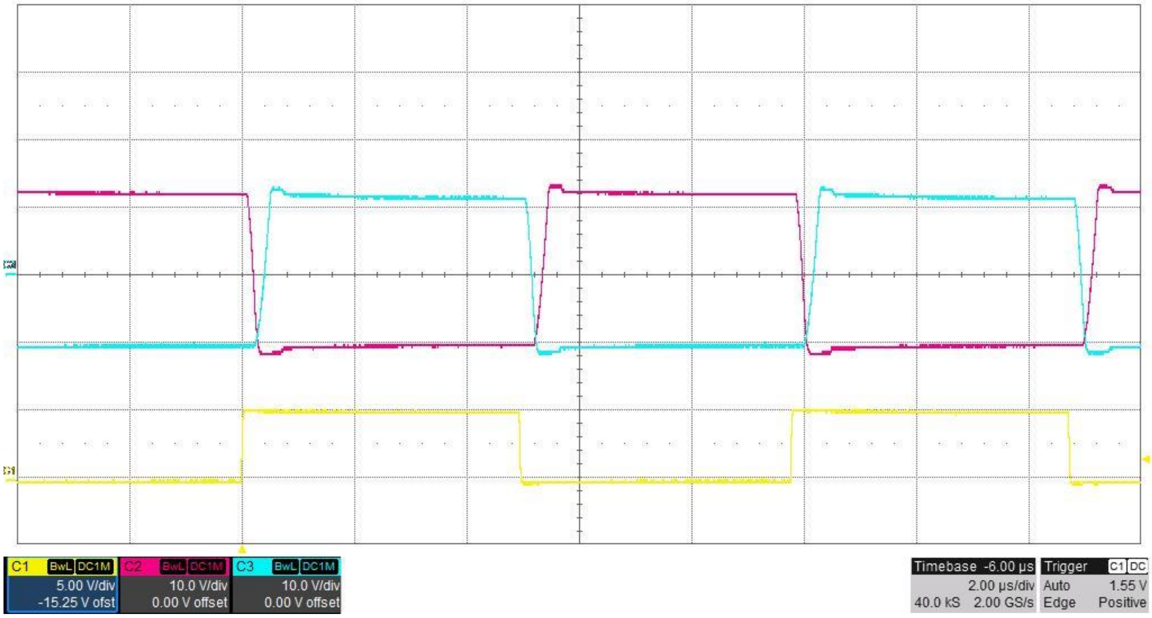
The photo below shows the switch node voltages of **15V#1 and 5V#1**, measured at TP4 and TP12 and the PHASE clock signal. **Vin = 26.4V**, Iout = **0A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



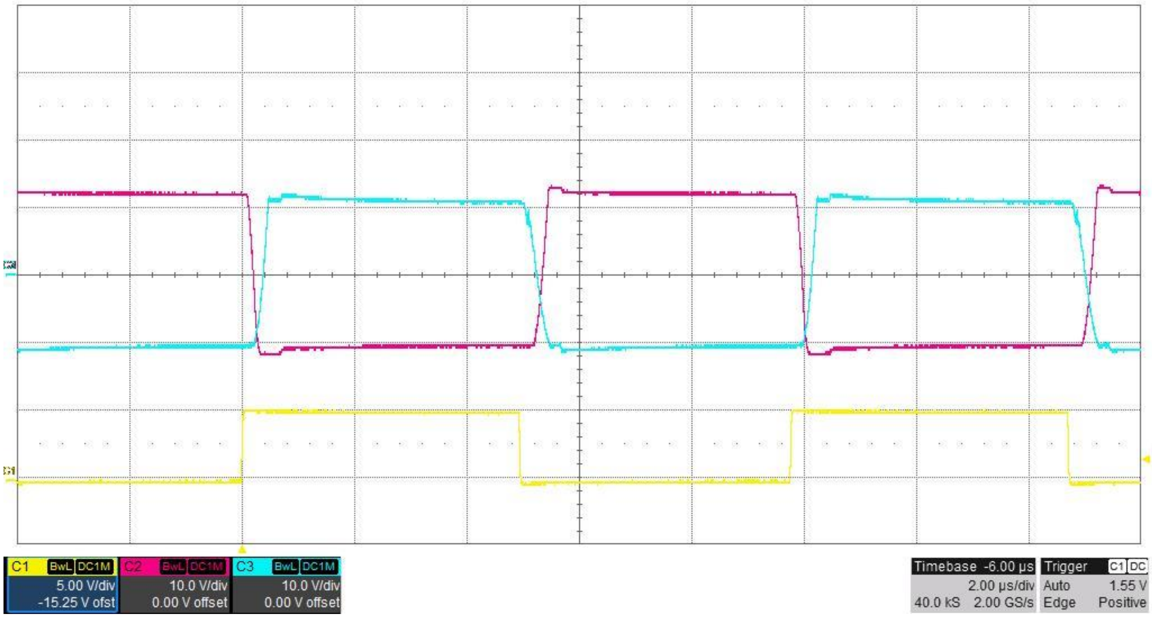
The photo below shows the switch node voltages of **15V#1 and 5V#1**, measured at TP4 and TP12 and the PHASE clock signal. **Vin = 26.4V**, Iout = **0.15A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



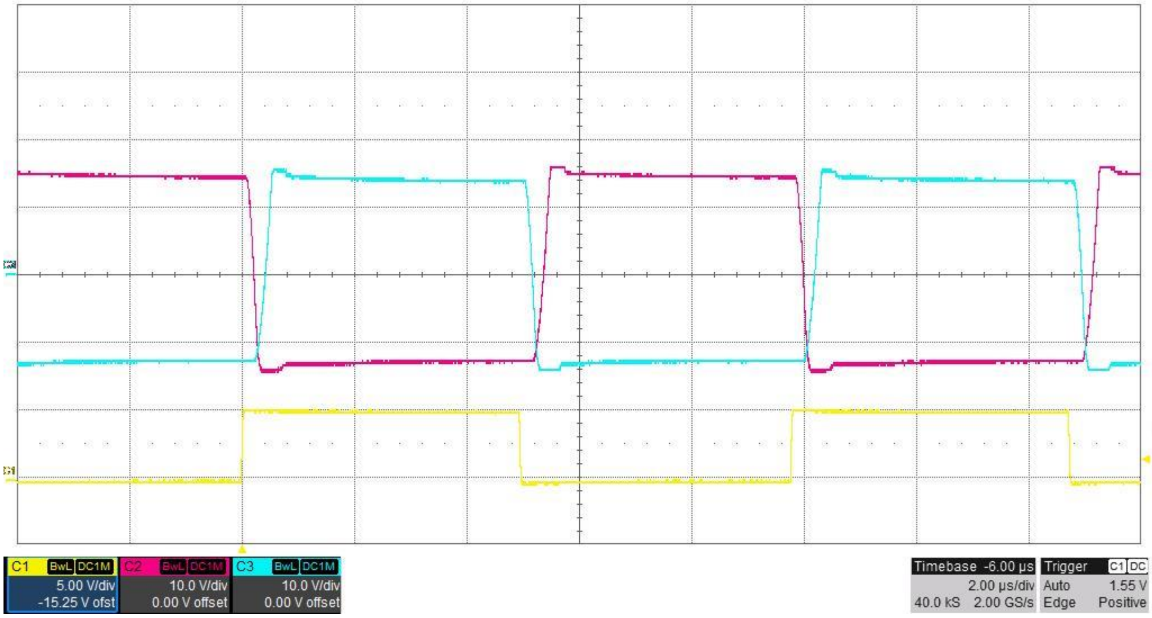
The photo below shows the switch node voltages of **15V#2 and 5V#2**, measured at TP18 and TP25 and the PHASE clock signal. **Vin = 21.6V**, Iout = **0A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



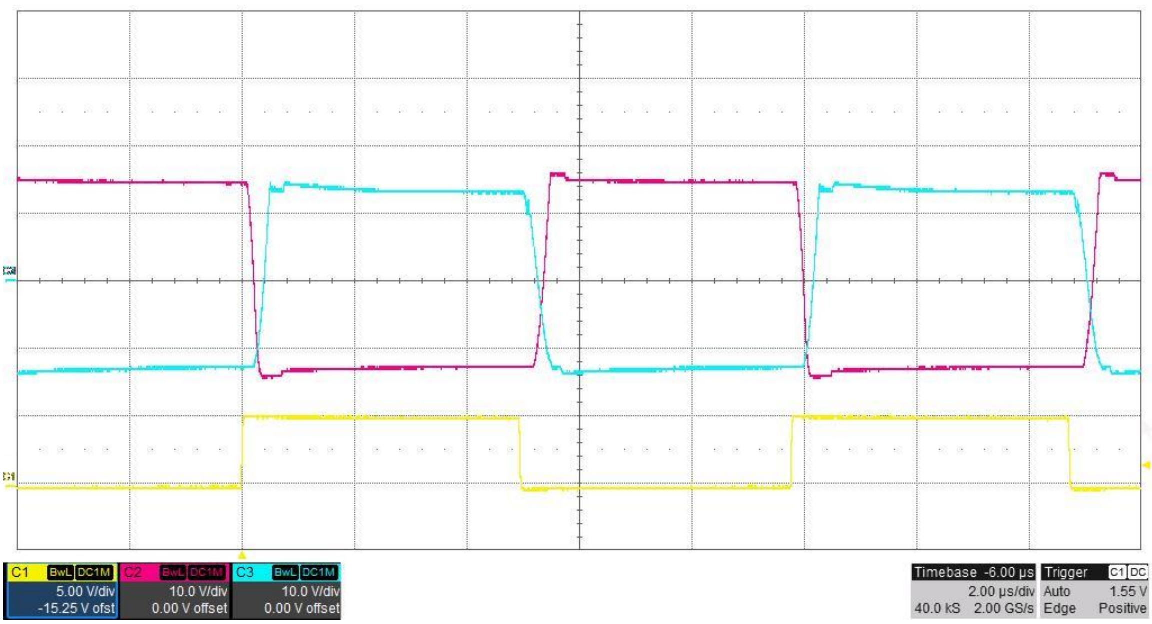
The photo below shows the switch node voltages of **15V#2 and 5V#2**, measured at TP18 and TP25 and the PHASE clock signal. **Vin = 21.6V**, Iout = **0.15A**. (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



The photo below shows the switch node voltages of **15V#2 and 5V#2**, measured at TP18 and TP25 and the PHASE clock signal. **Vin = 26.4V**, Iout = **0A**.   (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)

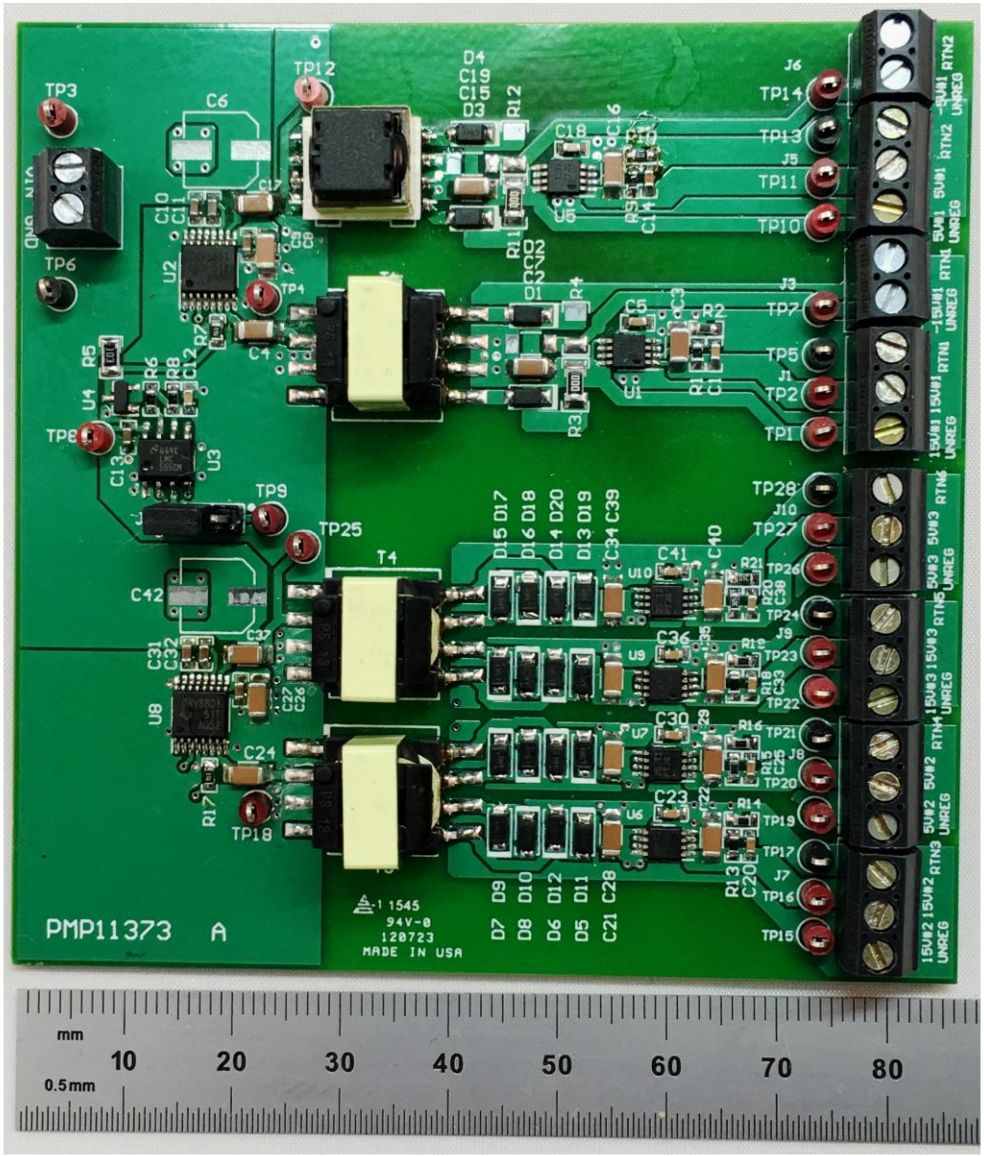


The photo below shows the switch node voltages of **15V#2 and 5V#2**, measured at TP18 and TP25 and the PHASE clock signal. **Vin = 26.4V**, Iout = **0.15A**.   (PHASE is 5V/DIV, 10V/DIV, 2uS/DIV)



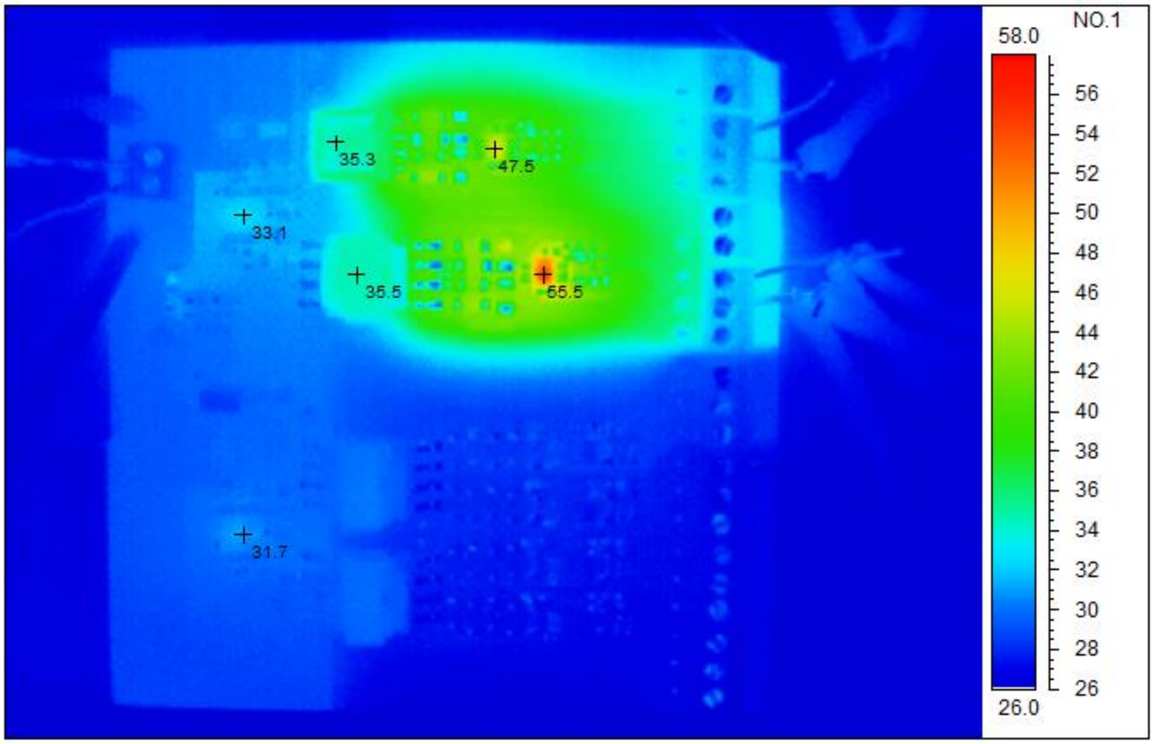
6 Photo

The photo below shows the PMP11373 REVB evaluation board.



7 Thermal Image

The thermal image below shows the temperature rise with 24Vin and 15V#1 @ 0.15A and 5V#1 @ 0.15A, with no airflow. All other outputs are unloaded.



The thermal image below shows the temperature rise with 24Vin and 15V#2 @ 0.15A and 5V#2 @ 0.15A, with no airflow. All other outputs are unloaded.