TI Designs

High-Bandwidth Arbitrary-Waveform Generator Reference Design: DC or AC Coupled, High-Voltage Output

Description

The TIDA-00684 reference design utilizes the DAC38J84 to implement an active amplifier interface with a digital-to-analog converter (DAC) to demonstrate an arbitrary-waveform-generator front-end function. The DAC38J84 is a quad-channel DAC with 16-bits of resolution and a maximum update rate of 2.5-GSPS. The arbitrary signal generator can be used in applications such as test and measurement equipment, communications test equipment, direct digital synthesis (DDS), and variable-clock arbitrary waveform generators.

Resources

TIDA-00684	Design Folder
DAC38J84	Product Folder
THS3217	Product Folder
THS3091	Product Folder
THS3095	Product Folder
LMH5401	Product Folder

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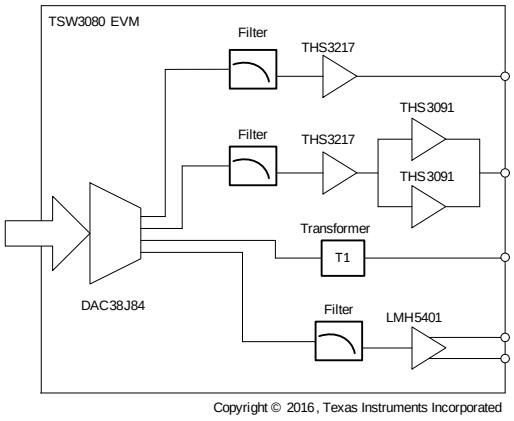
Features

- Wideband (500 MHz), DC-Coupled Active Interface, Capable of 5-V_{P-P} signal swing
- 50-MHz Pass-Band Channel Capable of 26-V_{P-P} Signal Swing
- Wideband (1.0 GHz), DC-Coupled Signal Path
- All Channels Optimized for Driving 50-Ω Impedance Loads
- Available Onboard Clocking With Option for External Clocking

Applications

- Arbitrary Waveform Generator
- Test and Measurement
- Communication Test Equipment



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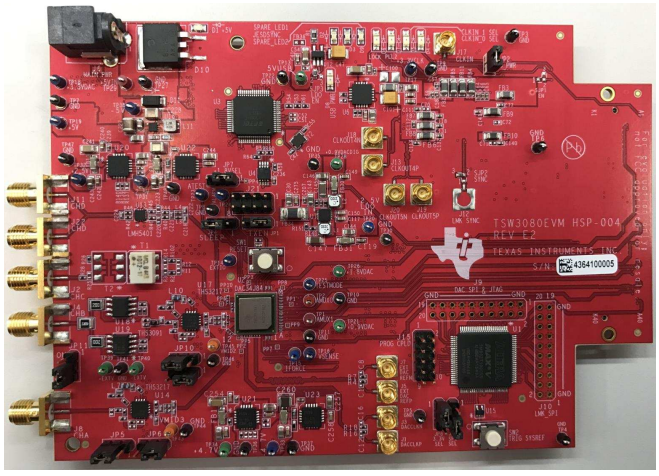

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1 System Overview

In the TIDA-00684 reference design, a quad-channel TSW3080 evaluation module (EVM) has been developed to show how to use an active amplifier interface with the DAC38J84 device to demonstrate an arbitrary-waveform-generator front end. The DAC38J84 device provides four DAC channels with 16 bits of resolution with a maximum update rate of 2.5 GSPS. The THS3217 device provides a wideband differential-to-single-ended output. The THS3095 device provides a high-dynamic range output of up to 26 V_{P-P}. The LMH5401 device provides a very wideband differential output. All of these paths provide a DC-coupled interface with the ability to drive 50 Ω at a high-performance level. The design also includes a reference transformer path for comparison purposes.

1.1 System Description

The TSW3080 has four channels:

- The first channel is a wideband DC-coupled active interface capable of swinging over 5 V_{P-P} with a bandwidth of up to 500 MHz. This path employs a THS3217 fully-differential amplifier (FDA) to perform a differential-to-single-ended conversion.
- The second channel is a high-dynamic range path with a potential swing of up to 26 V_{P-P} and a pass band of up to 50 MHz. This channel uses a THS3217 FDA to perform a differential-to-single-ended conversion followed by two parallel THS3091 amplifiers to provide a very large voltage swing output.
- The third channel is a transformer-coupled interface for reference purposes.
- The fourth channel is a wideband differential input to a differential output DC-coupled path with a bandwidth up to 1000 MHz.

All four output signal paths are capable of driving a 50-Ω load.

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1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Supply voltage	5 V
Resolution	16-bit
Max sample rate	2.5 GSPS
Channel 1 output signal swing	5 V_{P-P}
Channel 2 output signal swing	26 V_{P-P}
Channel 3 output signal swing	0.5 V_{P-P}
Channel 4 output swing	3.5 V_{P-P}
Channel 1 (bandwidth)	500 MHz
Channel 2 (bandwidth)	50 MHz
Channel 3 (bandwidth)	1000 MHz
Channel 4 (bandwidth)	1000 MHz

1.3 Block Diagram

Figure 1 shows the block diagram for TIDA-00684. The device is composed of the DAC38J84 DAC, which provides four paths of digital-to-analog conversion in the form of differential current outputs. The filter following the output of the DAC and before the input of the amplifier circuits are anti-imaging filters. Each of the amplifier stages also have a path-specific filter to limit the bandwidth to an appropriate pass band for that amplifier. The clocking required for this system is generated by an onboard LMK04828 locked to the onboard VCXO.

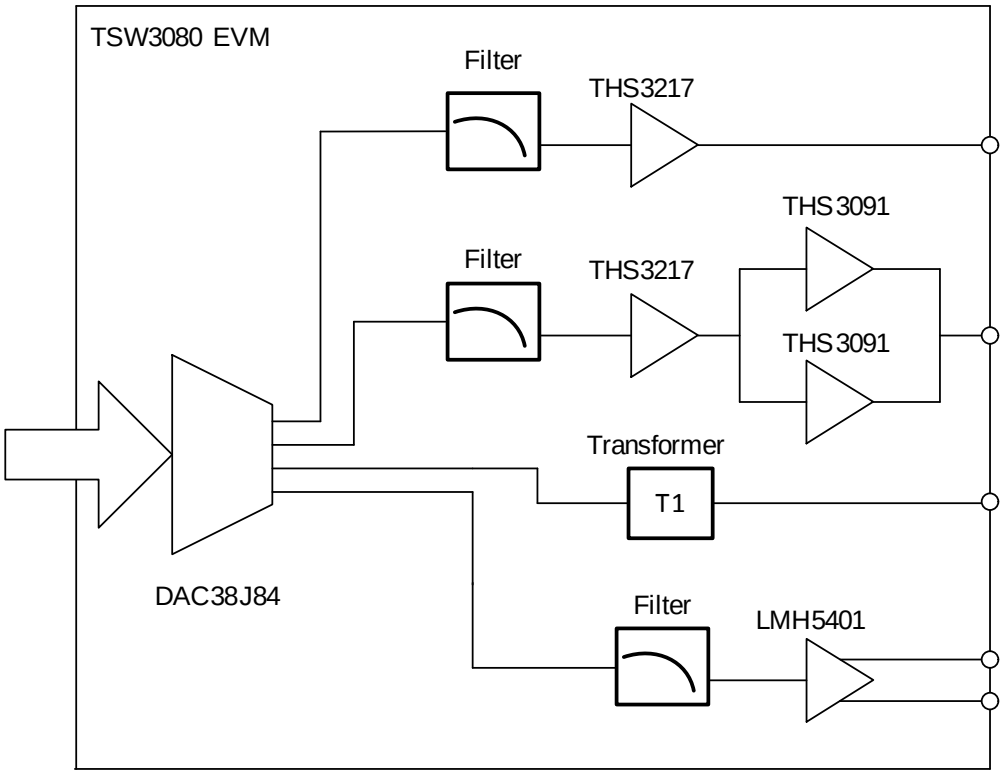

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Figure 1. Block Diagram of DAC38J84 and Amplifier Output Paths

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1.4 Highlighted Products

1.4.1 DAC38J84

DAC38J84 is a member of the low-power, quad-channel,1.6/2.5/2.8-GSPS DAC family with a JESD204B data input interface. The JESD2014B interface allows Subclass 1 SYSREF-based deterministic latency and full synchronization of multiple devices. The device includes features that simplify the design of complex transmit architectures. The DAC offers a 2×- to 16×-interpolation option, which can also be bypassed. The DAC is equipped with an on-chip, 48-bit numerically controlled oscillator (NCO) and independent complex mixers allow flexible and accurate signal placement. The high-performance, low-jitter phase-locked loop (PLL) simplifies clocking of the device without significant impact on the dynamic range. The DAC is also capable of quadrature modulator correction (QMC) and group delay corrections (QDC) to enable complete I_Q compensation of gain, offset, phase, and group delay between channels in direct up-conversion applications.

1.5 LMH5401

The LMH5401 is a very high-performance, differential amplifier optimized for radio frequency (RF), intermediate frequency (IF), or high-speed, DC-coupled, time-domain applications. The device is ideal for DC- or AC-coupled applications. The LMH5401 generates very low levels of second- and third-order distortion when operating in single-ended-to-differential or differential-to-differential (DE-DE) mode. The amplifier is optimized for use in both SE-DE and DE-DE systems. The device has an unprecedented usable bandwidth from DC to 2 GHz. The LMH5401 device can be used for SE-DE conversions in the signal chain without external baluns in a wide range of applications such as test and measurement and broadband communications.

1.6 THS3217

The THS3217 device combines the key signal-chain components required to interface with a complementary-current output DAC. The flexibility provided by this two-stage amplifier system delivers the low-distortion, DC-coupled, differential to single-ended signal processing required by a wide range of systems. The input stage buffers the DAC resistive termination and converts the signal from differential to single-ended with a fixed gain of 2 V/V. The differential to single-ended output is available externally for direct use and can also be connected through an RLC filter or attenuator to the input of an internal output power stage (OPS). The wideband, current-feedback, output power stage externally provides all the pins for flexible gain setting.

1.7 THS3091

The THS309x is a member of the high-voltage, low-distortion, high-speed, current-feedback family of amplifiers that have been designed to operate over a wide supply range of ±5 V to ±15 V for applications requiring large, linear output signals such as power input drivers , power field-effect transistor (FET) drivers, and very-high-bit-rate digital subscriber line (VDSL) drivers. In addition, to the high slew rate of 7300 V/µs, the wide supply range combined with a total harmonic distortion as low as –69 dBc at 10 MHz makes the THS309x ideally suited for high-voltage arbitrary waveform driver applications. The ability to handle large voltage swings driving into high-resistance and high-capacitance loads while maintaining good settling time performance makes the device ideal for power FET driver applications.

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2 System Design Theory

2.1 TSW3080 EVM Channel Output Paths

The TSW3080 has four apparent waveform generator paths:

- Wideband, DC-coupled, THS3217 differential-to-single-ended path
- Large swing and high-dynamic range, DC-coupled, moderate bandwidth path
- Wideband passive transformer path
- Wideband, DC-coupled, differential-in to differential-out path

2.1.1 THS3217 DC-Coupled, Wideband, Differential-to-Single-Ended Path (Channel 1)

The THS3217 device is used to convert the differential voltage at the output of the DAC to a single-ended voltage capable of driving 50 Ω. In this output signal path, the DAC38J84 output 20-mA swing drives an equivalent load of 25 Ω on each differential output pin, which results in a 1 V_{P-P} differential voltage at the THS3217 input. A gain of 2× exists through the differential-to-single-ended buffered input stage. The external, interstage 200-MHz RLC filter has a gain of 0.75×. The final output stage has been configured to provide another 2.5× of gain, which results in a total gain of 3.75 V/V. With an input voltage of 1 V_{P-P}, the resulting output voltage on 50 Ω is 3.75 V / 2 = 1.875 V_{P-P}. The overall frequency response is a combination of the anti-image filter (500 MHz) at the DAC38J84 output and the RLC interstage low-pass filter at the THS3217 (see Figure 2 and Figure 3).

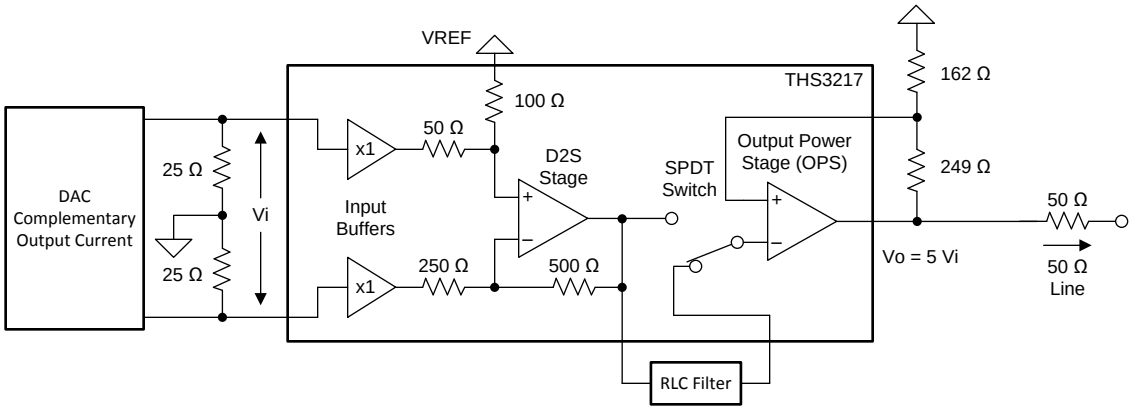

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Figure 2. DAC38J84 and THS3217 Circuit Block Diagram

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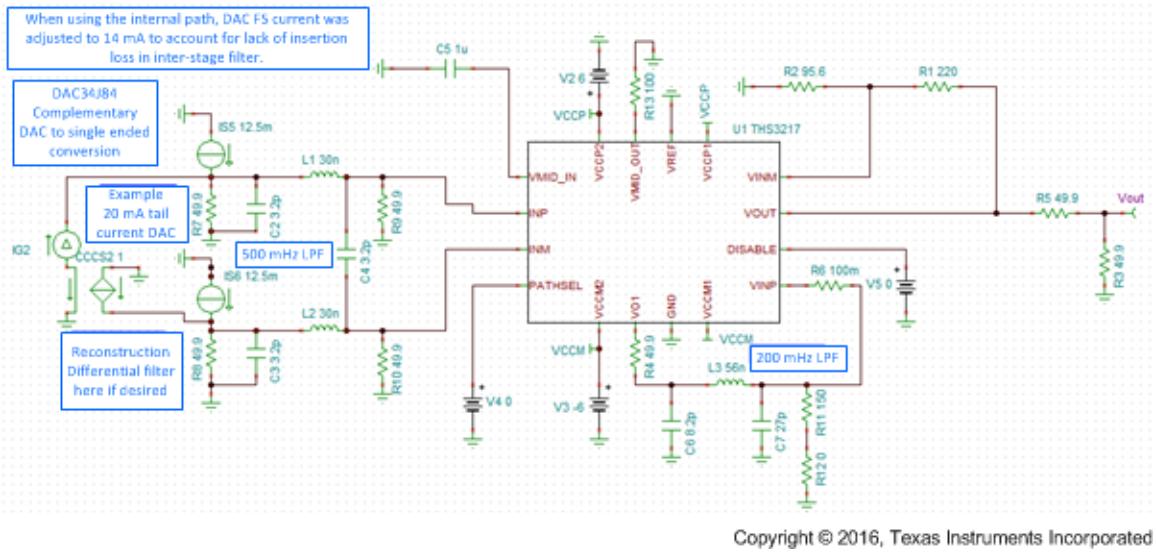

Figure 3. TINA-TI™ Circuit Diagram of THS3217 Wideband DC-Coupled Path

The preceding Figure 3 shows the simulation circuit diagram generated using TINA-TI™ software. Figure 4 and Figure 5 show the simulated frequency response for THS3217 with an external 200-MHz low-pass RLC filter and with an internal path (without the RLC low-pass filter), respectively. Channel 1 is capable of 500 MHz of bandwidth; however, this design uses a 200-MHz low-pass RLC filter. The bandwidth of channel 1 is easy to adjust through simple bill of material (BOM) modifications to the external RLC low-pass filter circuit.

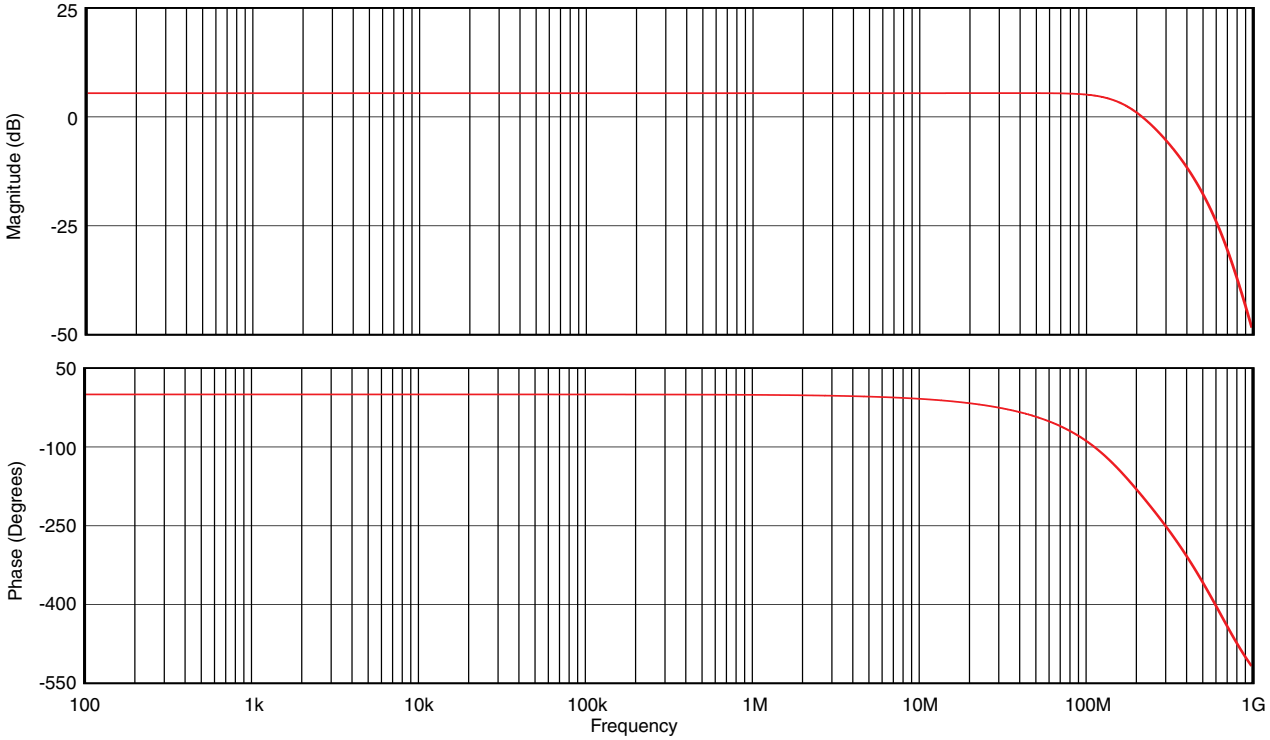

Figure 4. Frequency Response for THS3217 Using External Path With 200-MHz Low-Pass RLC Filter

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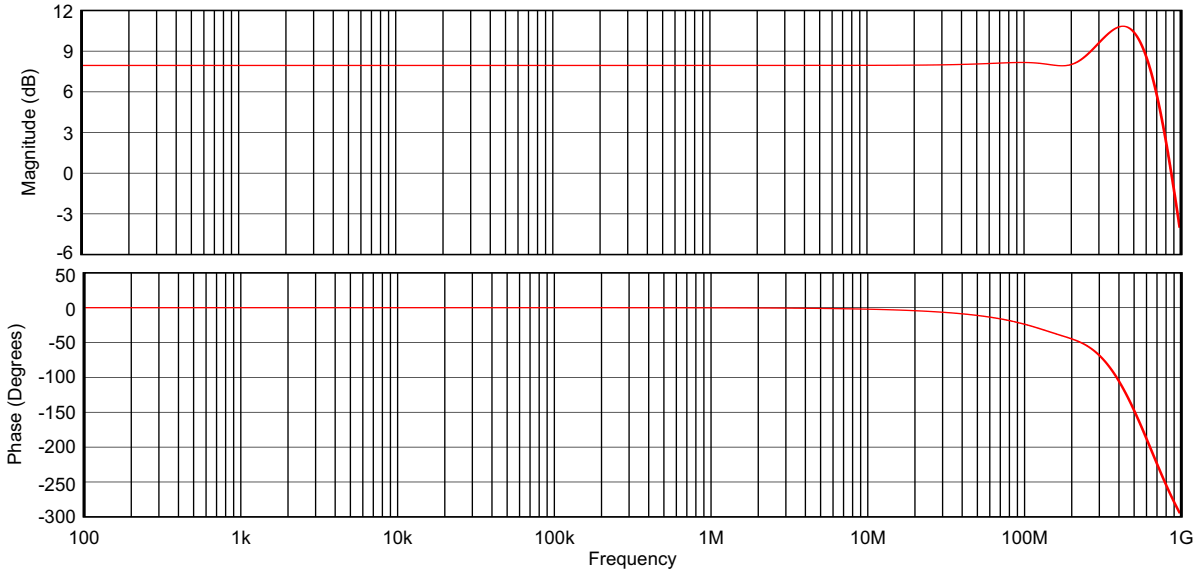

Figure 5. Frequency Response for THS3217 Using Internal Path (Without 200-MHz Low-Pass RLC Filter)

Figure 6 and Figure 7 show the simulated pulse response for THS3217 (Channel 1) with an external RLC low-pass path and with an internal path, respectively.

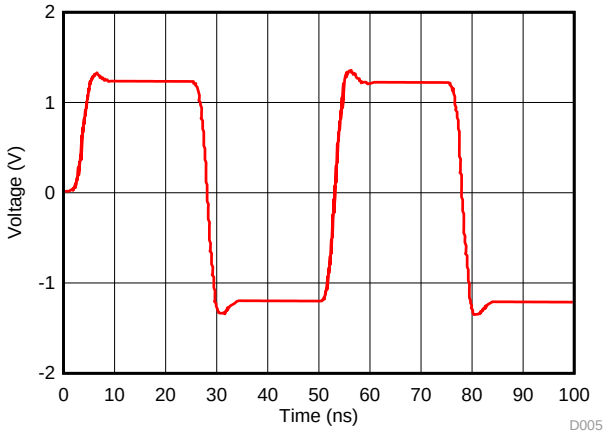

Figure 6. Simulated Pulse Response for THS3217 With External 200-MHz Low-Pass RLC Filter

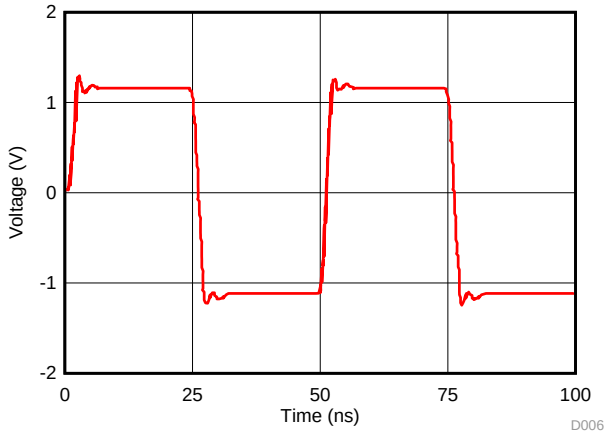

Figure 7. Simulated Pulse Response for THS3217 With Internal Path (Without 200-MHz Low-Pass RLC Filter)

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2.2 THS3217 and 2x THS3091 DC-Coupled, High-Dynamic Range Path

For applications which require large voltage swings up to 25 V_{P-P}, a high-dynamic range output stage can be used following the THS3217 device. This output stage can comprise one or more THS3091 (or THS3095) cascaded in a parallel configuration to handle the current requirements when driving a 50-Ω load. The same design is used for the THS3217 circuit after the DAC38J84 output, in which a 3.75× gain at the output of the THS3217 is expected. A low-pass RLC filter following the output of the THS3217 device provides about a 50-MHz low-pass response and has a gain of 0.75×. The gain of the THS3091 circuits is 4×, which results in a total gain of 3.75 × 0.75 × 4 = 11.25 V/V. With the 1-V_{P-P} output from the DAC38J84, the final output with a 50-Ω load is 11.25 V / 2 = 5.625 V_{P-P}. The overall response of the signal path is mostly defined by the 50-MHz low-pass filter between the THS3217 and the THS3091 devices. Figure 8 shows the block diagram and Figure 9 shows the simulation circuit used in the TI-TINA software to simulate the circuit response.

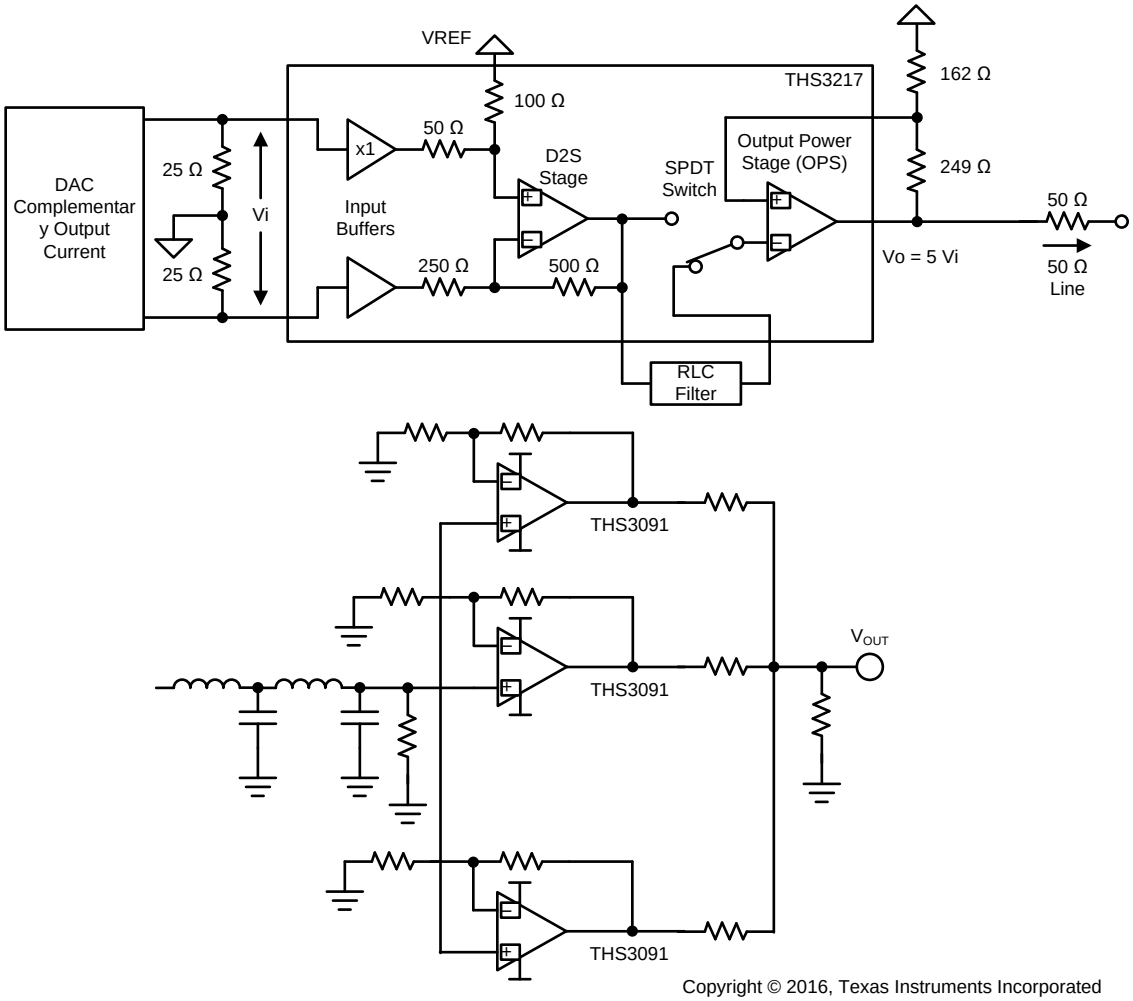

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Figure 8. Block Diagram of THS3217 and THS3091 DC-Coupled, High-Swing Path

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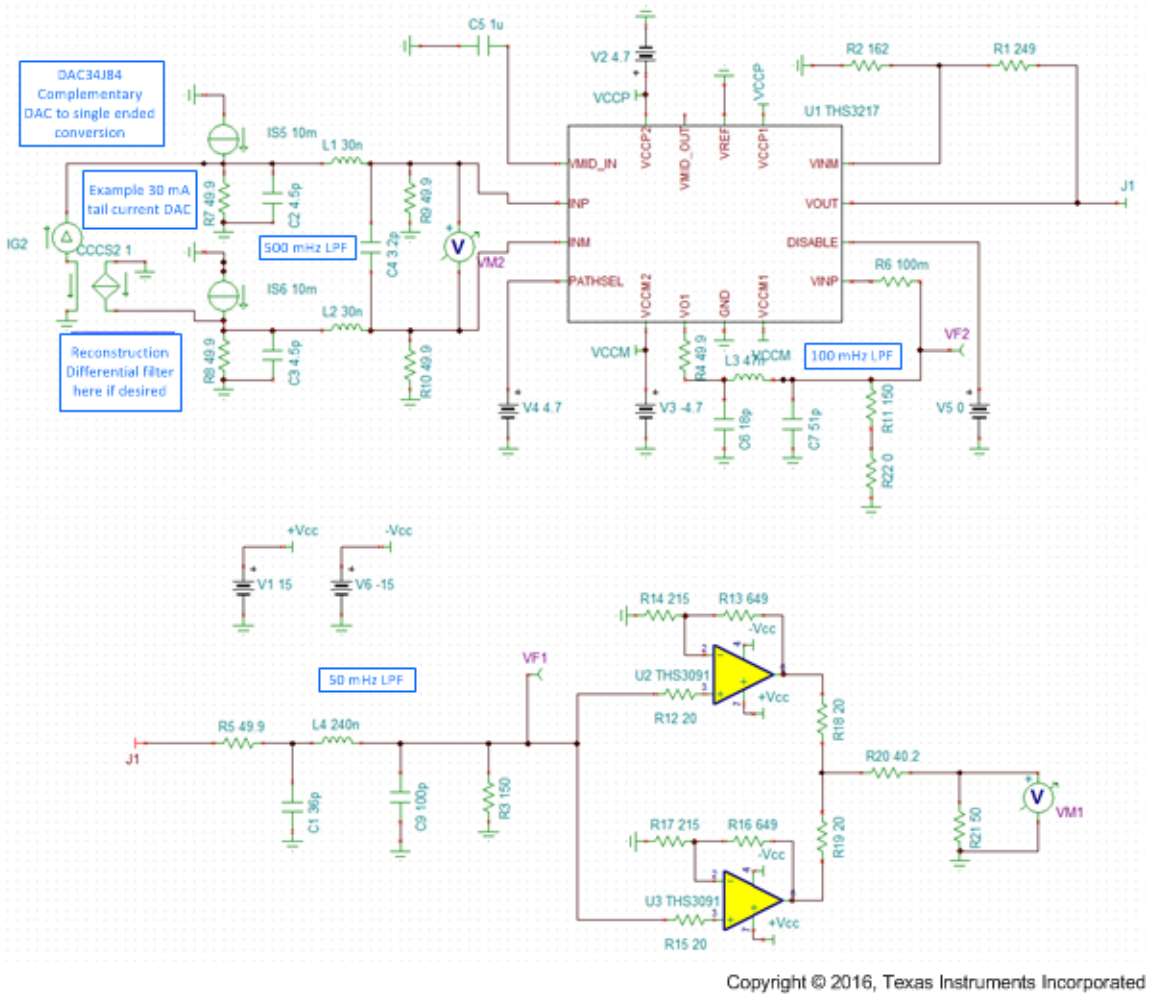

Figure 9. Circuit Diagram of DAC38J84, THS3217, and THS3091 High-Swing Path

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Figure 10 shows the simulated frequency response using an external, 100-MHz, low-pass RLC filter path along with the 50-MHz low-pass filter after the THS3217 amplifier stage. Figure 11 shows the simulated frequency response using the internal path (without the RLC filter) for the THS3217 device along with a 50-MHz low-pass filter after the THS3217 amplifier stage.

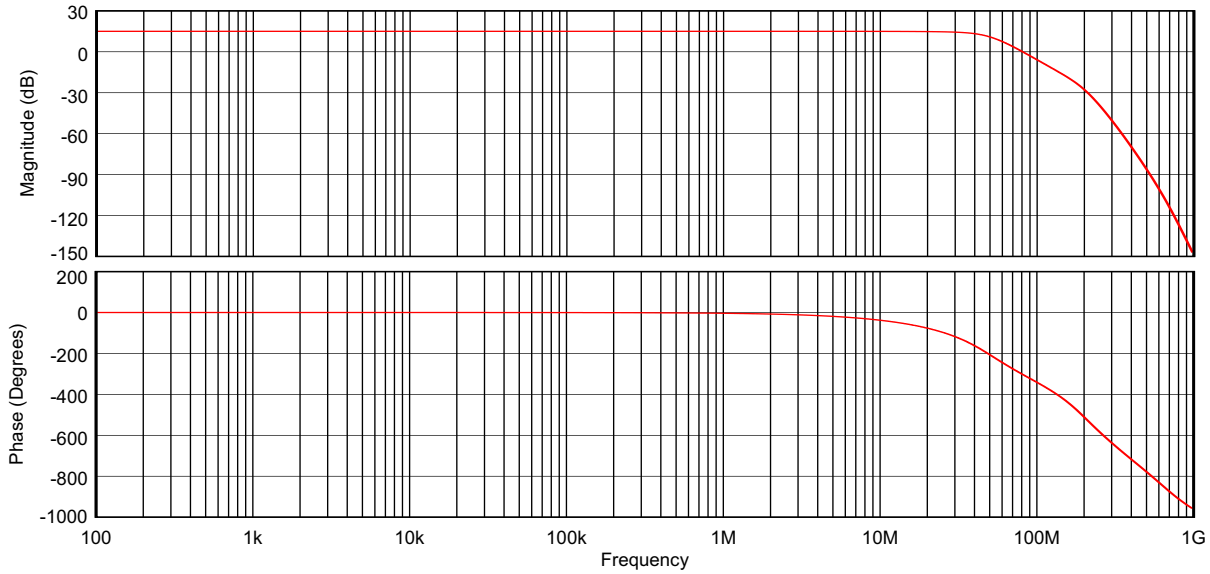

Figure 10. Channel 2 Simulated Frequency Response With External RLC Low-Pass Filter Path Using THS3217 and THS3091

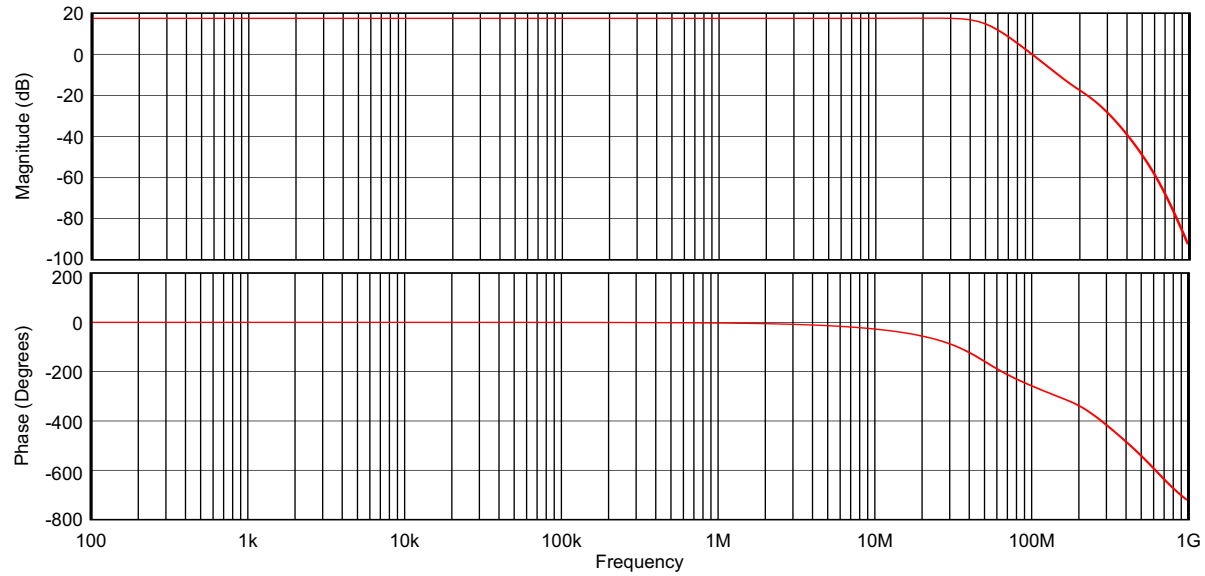

Figure 11. Channel 2 Simulated Frequency Response With Internal Path Using THS3217 and THS3091

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Figure 12 and Figure 13 show the simulated pulse response for Channel 2 with an external RLC low-pass filter and using the internal path for the THS3217 amplifier stage, respectively.

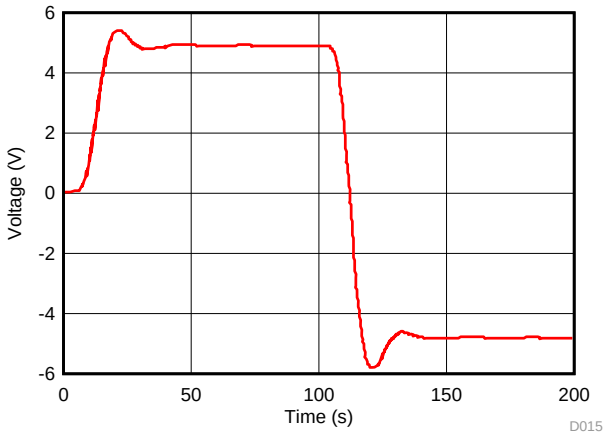

Figure 12. Channel 2 Simulated Pulse Response With External RLC Low-Pass Filter Path

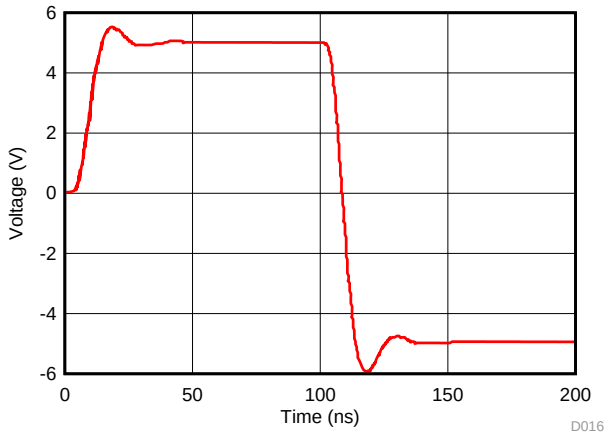

Figure 13. Channel 2 Simulated Pulse Response With Internal Path

2.3 Passive AC-Coupled Transformer Path (Channel 3)

The wideband transformer path of the reference provides a passive AC-coupled path through a wideband 2:1 impedance transformer. The external 50-Ω load is transformed into a 100-Ω differential. This appears in parallel with a 100-Ω differential on the board. The result is 50-Ω differential or 25-Ω single-ended from each DAC38J84 output pin. With a default current swing of 20 mA, this specification results in a single-ended swing of 500 mV_{P-P} or a differential-ended swing of 1 V_{P-P} at the DAC output pins. The designer may increase the output drive of the DAC38J84 device to 30 mA through settings in the device GUI.

2.4 LMH5401 DC-Coupled, Wideband Differential-to-Differential Path

The LMH5401 output path has been designed to provide a DC-coupled, wideband, buffered-differential output (see Figure 14). The gain is set by the feedback resistor and input resistor on each side of the differential path. Each feedback path has an internal 25-Ω resistor and 10 Ω on each output path, which must be considered in the design. The gain in this case is given by the total feedback impedance divided by the input impedance. In the case of this design, the gain is (150 + 25 internal) / 50 = 3.5x on each differential leg and the output source impedance is (40 + 10 internal) = 50 Ω. This path is capable of supporting up to 1 GHz of signal bandwidth with very good performance. In this example, an anti-image filter used in the output path limits the bandwidth to 700 MHz.

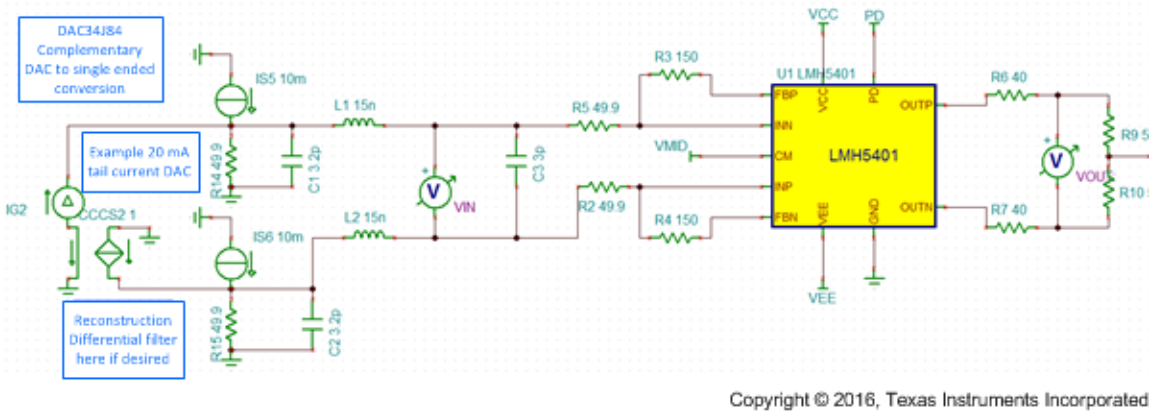

Figure 14. Circuit Diagram for Fully Differential DAC38J84 and LMH5401 Path

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Figure 15 shows the simulated frequency response and Figure 27 shows the measured frequency response.

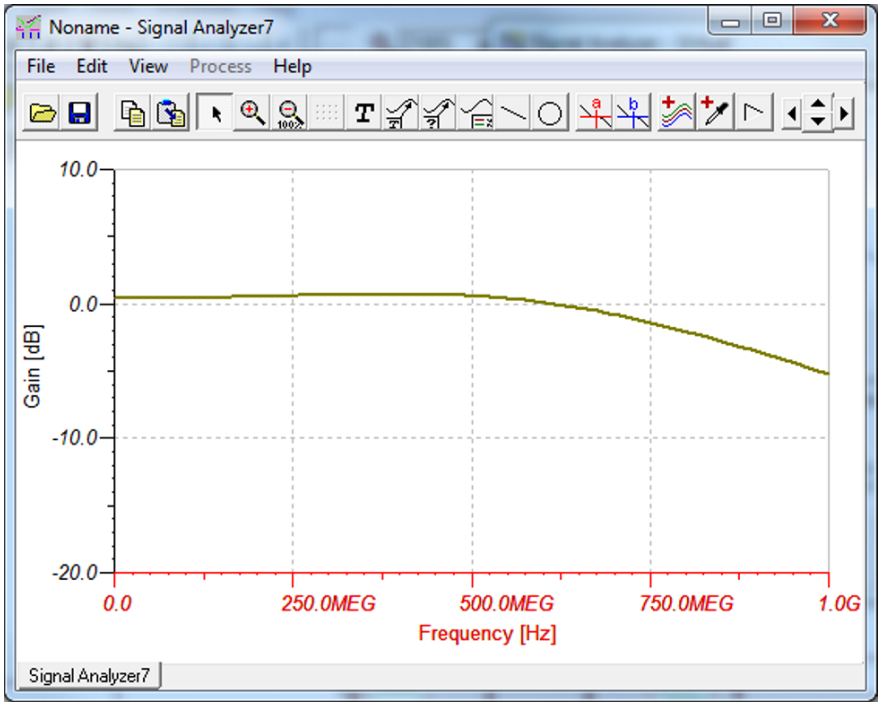

Figure 15. Simulated Frequency Response of DAC38J84 and LMH5401

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3 Getting Started Hardware and Software

3.1 Hardware setup

Figure 16 shows the implementation of the hardware setup to make measurements. The HSDC Pro GUI software is used to generate digital data patterns, which then transfer to the DAC38J84 device using a TSW14J56 field-programmable-gate-array (FPGA)-based pattern generator. For detailed information of the setup, refer to the section titled *Basic Test Setup* of the DAC38J84EVM user's guide[1]. A spectrum analyzer and an oscilloscope has been used to measure the output signal from the TSW3080 EVM.

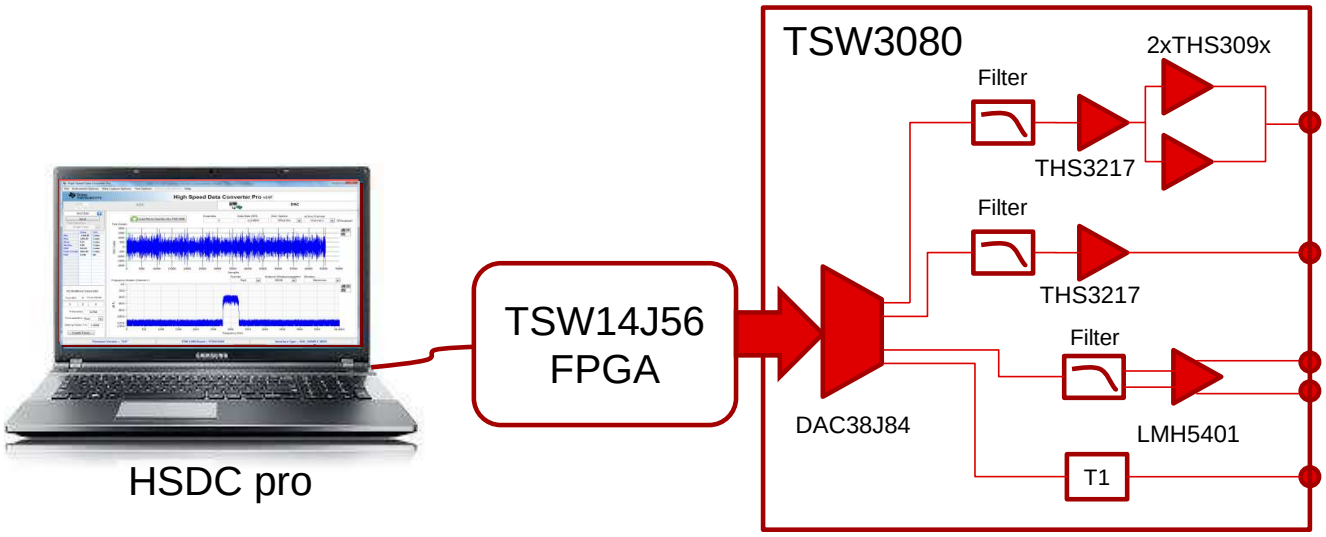

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Figure 16. Hardware Setup

3.1.1 Software

3.1.1.1 TSW3080 EVM GUI

The TSW3080 EVM has been configured using a DAC38J84 EVM GUI. Refer to the DAC38J84EVM tools folder at http://www.ti.com/tool/DAC38j84EVM for detailed description on how to use and configure the TSW3080 EVM.

3.1.1.2 HSDC Pro GUI

HSDC Pro software is used to generate the digital data for a TSW3080 EVM. Refer to the HSDC Pro tool folder at http://www.ti.com/tool/dataconverterpro-sw for a detailed description on how to use the GUI.

3.2 Power Supply for TSW3080

All of the onboard supplies derive from an external 5-V supply. Two onboard TPS7A4700 low-dropout regulators (LDOs) generate two separate 3.3-V supplies from the 5-V input: one of the 3.3-V supplies is used by the DAC38J84 device and the other supply is used by the LMK04828 clock circuit. A TPS62420 switcher is used to switch down the 5-V input to 2.5 V. This 2.5 V is then converted to 1.8 V and 0.9 V by two separate TPS74201 LDOs. The 1.8-V and 0.9-V supplies are further filtered by ferrite beads and used to power various voltage requirements of the DAC.

For the amplifier circuits, a –5-V supply is generated from a 5-V input. Accomplish this task by using a TPS62160 step-down switcher. The ±5 V are then used by LDOs TPS7A4700 to generate +4.7 V and a TPS7A3301 device to generate –4.7 V for the THS3217 circuits. Another pair of TPS7A4700 and TPS7A3301 LDOs are used to generate the ±2.5 V used by the LMH5401 device. The ±15 V required on the THS309x circuit is expected to come from an external supply.

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Figure 17 shows the power tree on the TSW3080 EVM.

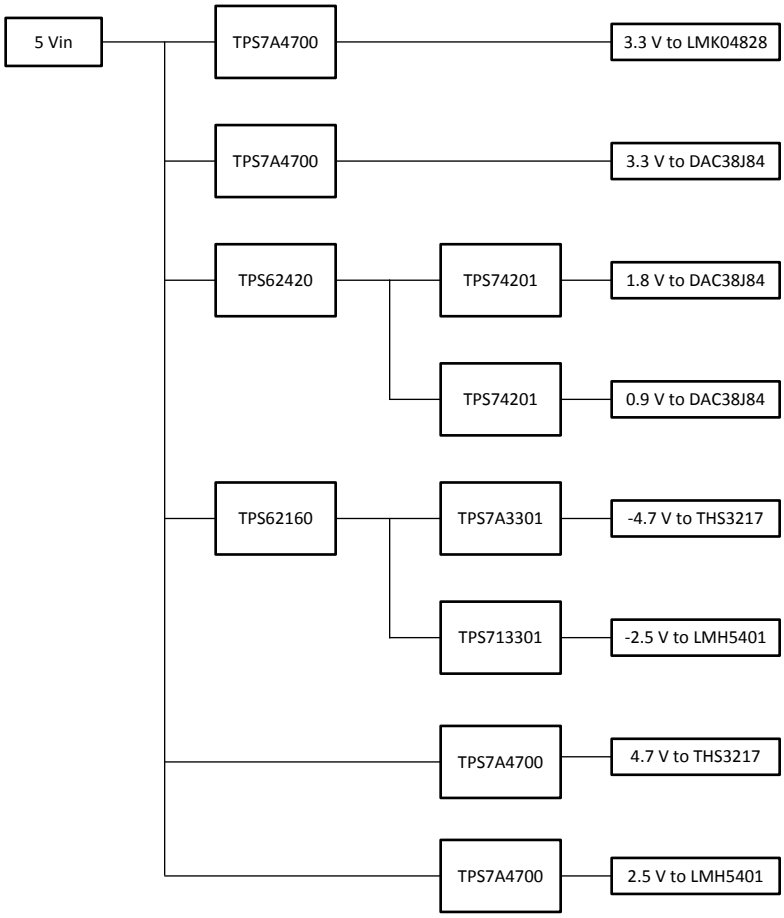

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Figure 17. TSW3080 Power Tree

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4 Testing and Results

This section show the measured performance of for all the four output channel.

4.1 Channel 1

The performance of channel 1 is verified by measuring the frequency response, impulse response, and harmonic distortion

Figure 18 and Figure 19 show the measured frequency response and pulse response for both with an external RLC filter path and without an RLC filter(internal path).

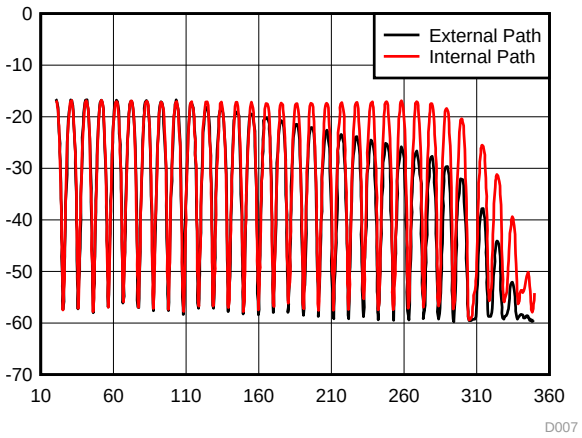

Figure 18. Frequency Response of DAC38J84 and THS3217 Measured on TSW3080 EVM

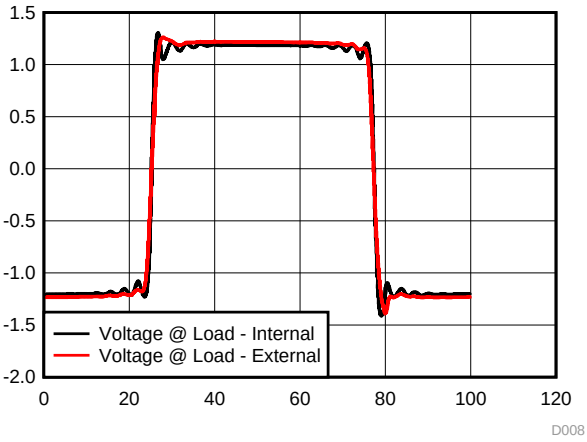

Figure 19. Pulse Response of DAC38J84 and THS3217 Measured on TSW3080 EVM

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Figure 20 and Figure 21 show the measured HD2 and HD3 performance of the DAC38J84 and THS3217 for both an external RLC filter and with an internal path, respectively.

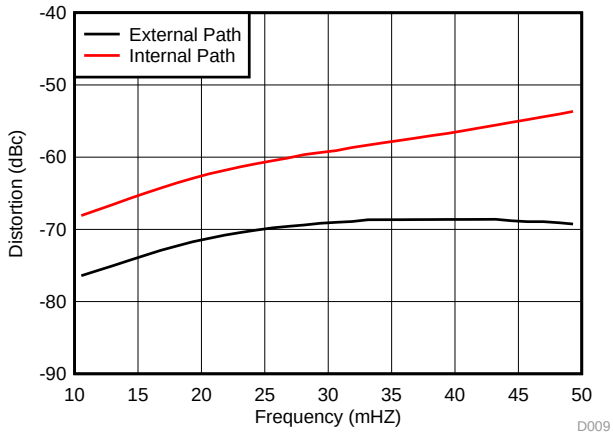

Figure 20. HD2 Performance of DAC38J84 and THS3217 Circuit

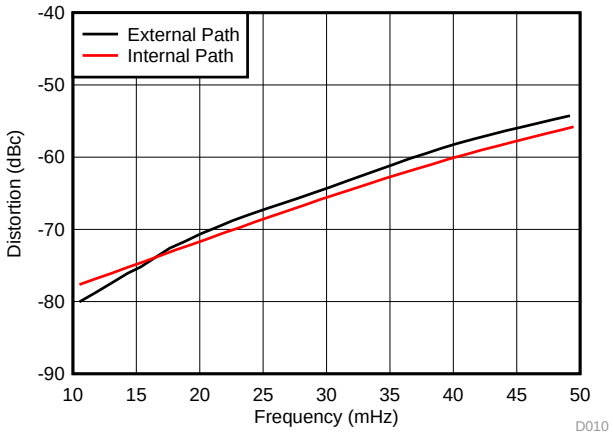

Figure 21. HD3 Performance of DAC38J84 and THS3217 Circuit

4.2 Channel 2

Figure 22 and Figure 23 show the measured frequency and measured pulse response for channel 2.

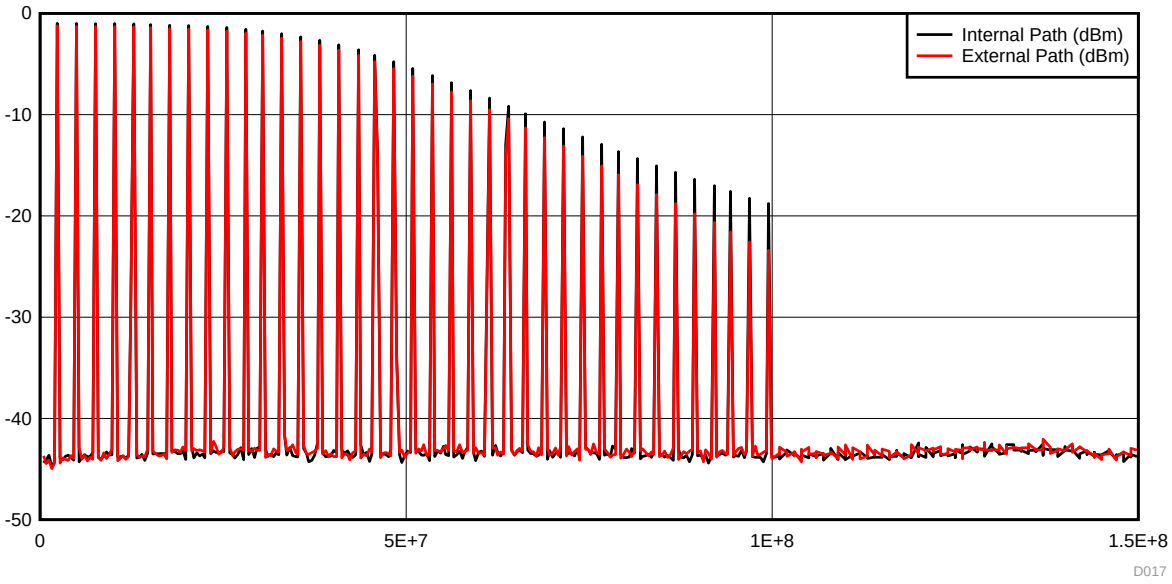

Figure 22. Measured Frequency of DAC38J84, THS3217, and THS3091

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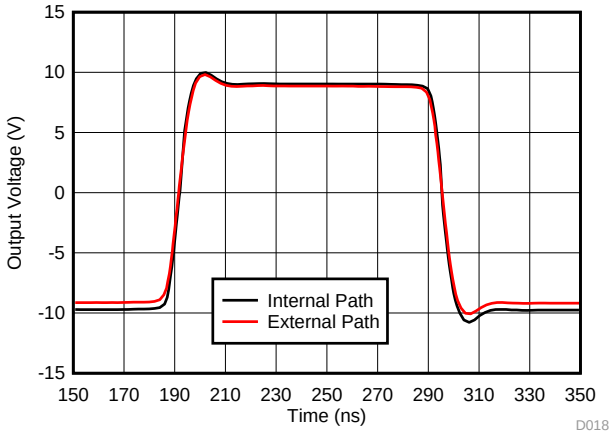

Figure 23. Measured Pulse Response of DAC38J84, THS3217, and THS3091

Figure 24 shows the measured HD2 performance and Figure 25 shows the measured HD3 performance.

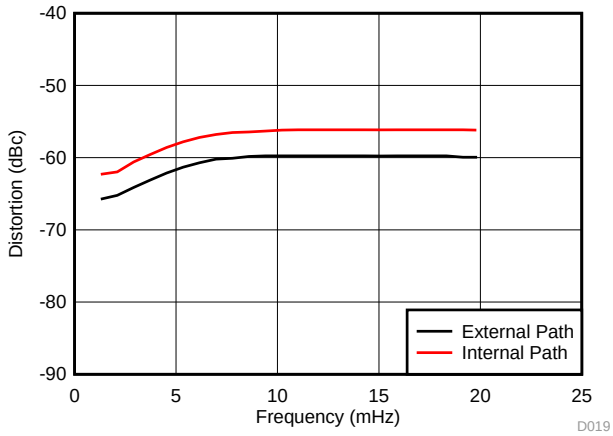

Figure 24. Measured HD2 Performance of DAC38J84, THS3217, and THS3091

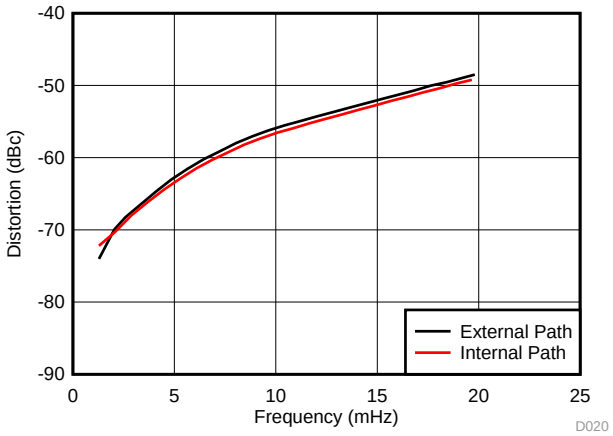

Figure 25. Measured HD3 Performance of DAC38J84, THS3217, and THS3091

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4.3 Channel 3

The performance of channel 3 is limited by the frequency response of the transformer. Figure 26 shows the measured frequency response of the DAC38J84 device and transformer path.

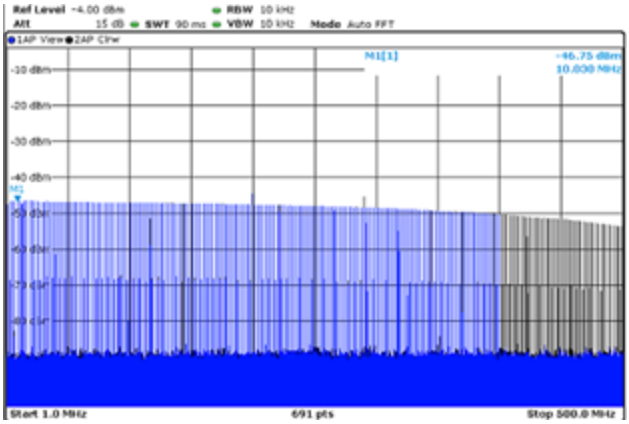

Figure 26. DAC38J84 and Transformer Path

4.4 Channel 4

Figure 27 shows the measured frequency response for channel 4. Channel 4 is DC-coupled with an LMH5401 device to provide a differential-input and differential-out wideband path.

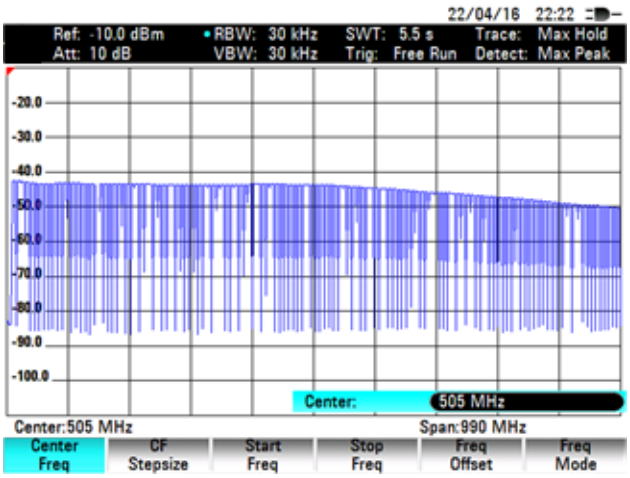

Figure 27. Measured Frequency Response of DAC38J84 and LMH5401

4.5 Results

The high-performance DAC38J84 can be combined with various high-performance amplifiers to provide a reference design for arbitrary waveform generation. This design shows several amplifier circuits that meet various signal chain requirements. The THS3217 path provides a wideband, DC-coupled, differential-to-single-ended output capable of driving a 50-Ω load with greater than 5-V_{P-P} swing. If more dynamic range is required, the THS3091 can be cascaded after the THS3217 to provide greater than a 25-V_{P-P} swing with up to a 50-MHz bandwidth. For applications requiring very wideband frequency response and differential outputs, the LMH5401 path may be used. For application requiring an even higher sampling rate, the 2.8-GSPS DAC39J84 device can be used.

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00684.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00684.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00684.

5.4 Design Project Files

To download the design project files, see the design files at TIDA-00684.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00684.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00684.

6 Terminology

DE-DE— Differential-to-differential

DDS— Direct digital synthesis

FDA— Fully-differential amplifier

FET— Field-effect transistor

OPS— Output power stage

SE-DE— Single-ended-to-differential

VDSL— Very-high-bit-rate digital subscriber line

7 Related Documentation

1. Texas Instruments, *DAC3XJ8XEVM*, DAC3XJ8XEVM User's Guide (SLAU547)

7.1 Trademarks

All trademarks are the property of their respective owners.

8 About the Author

KEN CHAN is an Applications Engineer with the High Speed Products group. He has been working on communications and signal chain products for over 18 years. He received his B.Sc. and M.Sc EE from the University of Saskatchewan..

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