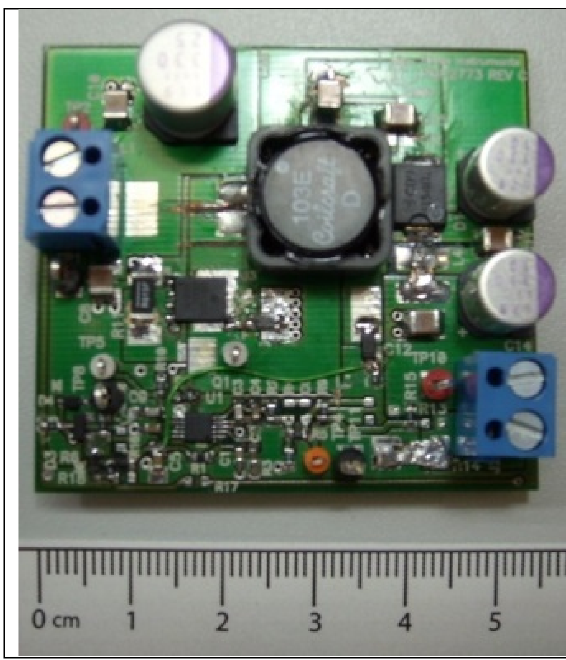
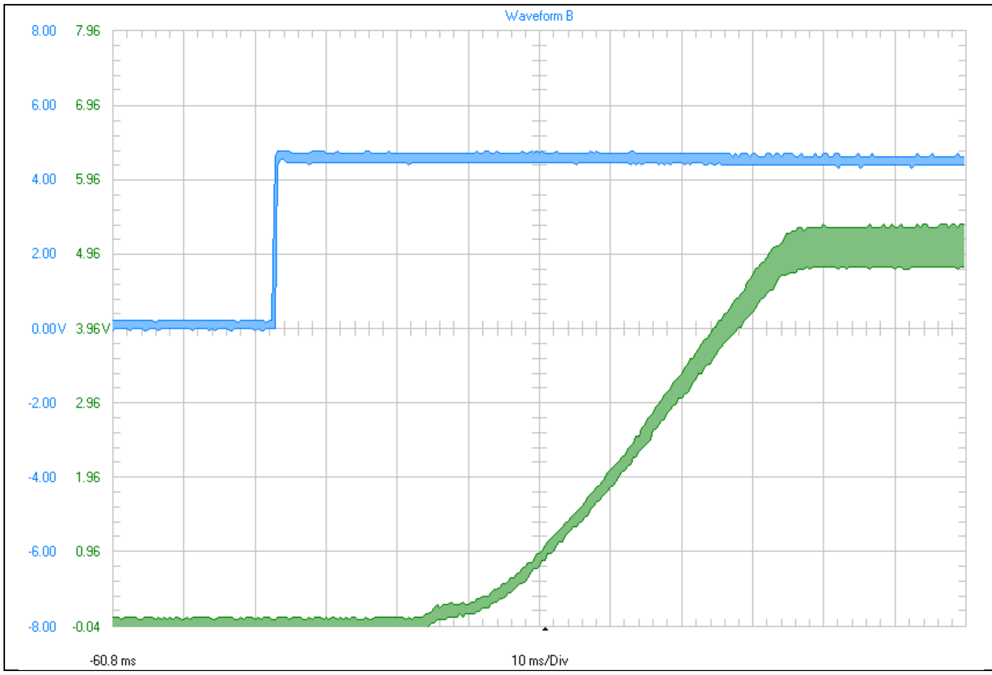
PMP30159 Test Results

Topology: SEPIC; Device: TPS40210; Switching Frequency: 340kHz;
With output current of 2A circuit switches off at 2.85V and on at 4.37V
Unless otherwise mentioned measurements were done with resistive load
Sloppy layout might need a 40V Schottky rectifier or a small RC snubber across this Schottky



1 Startup

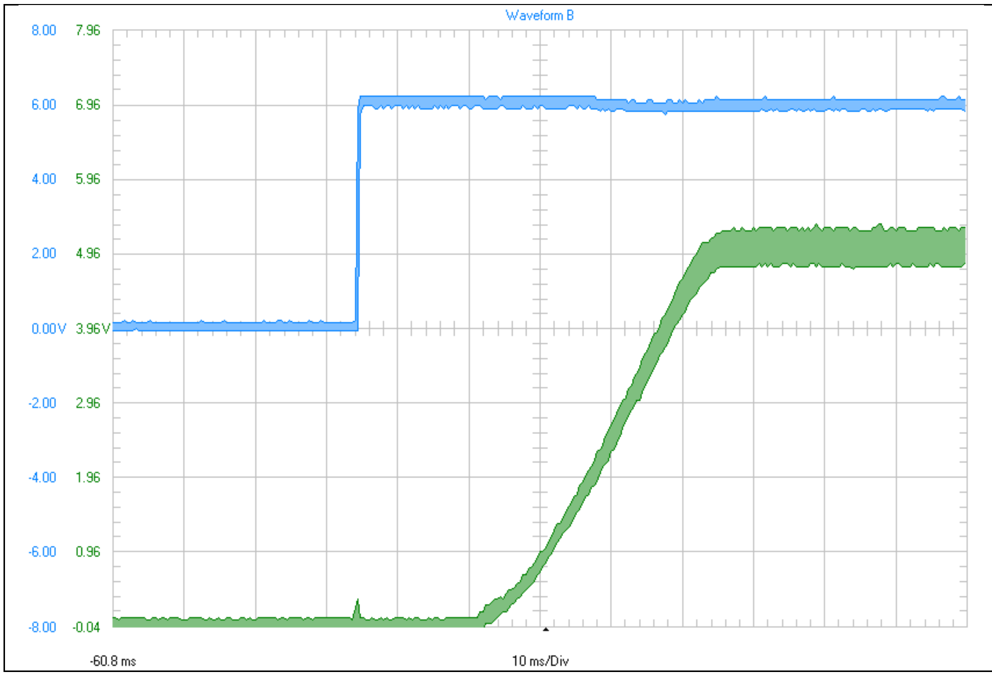
The startup waveform is shown in the Figure 1. The input voltage was set to 4.5V, with 2A load at the output.



	Ch1=> input voltage 2V/div Ch2=> output voltage 1V/div **10ms/div** 20MHz bw

Figure 1

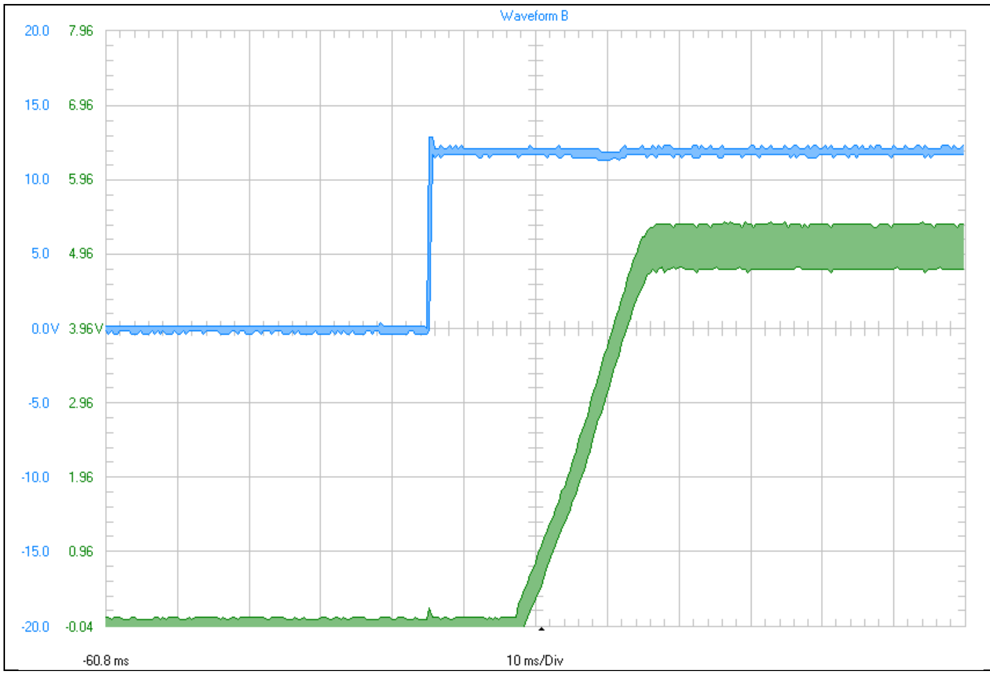
The startup waveform is shown in the Figure 2. The input voltage was set to 6V, with 2A load at the output.



	Ch1=> input voltage 2V/div Ch2=> output voltage 1V/div **10ms/div** 20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 12.0V, with 2A load at the output.



Ch1=> input voltage 5V/div

Ch2=> output voltage 1V/div

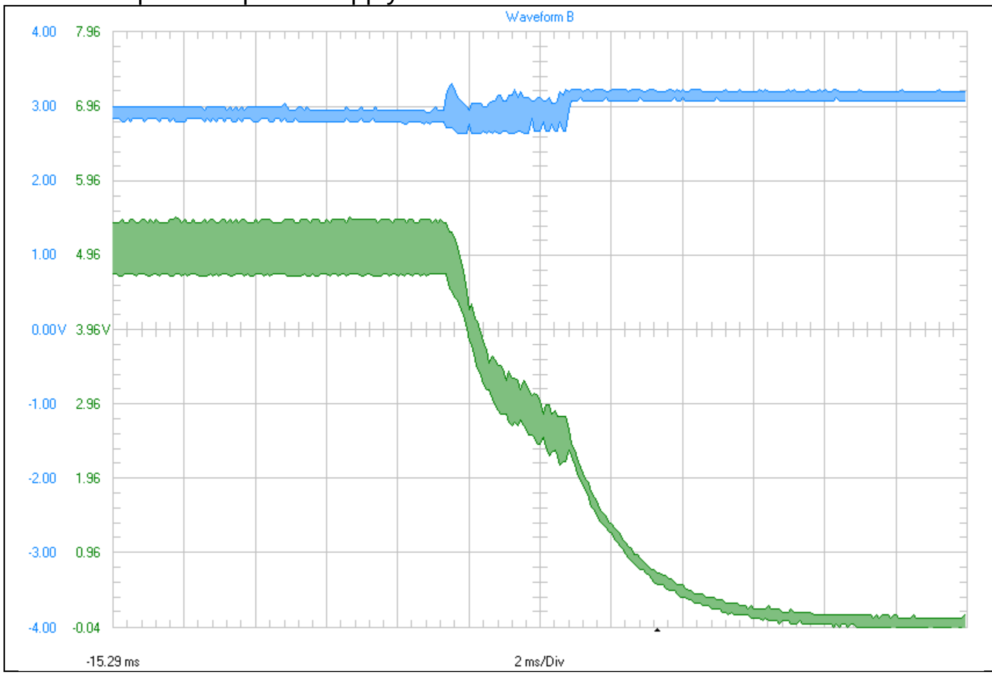
10ms/div

20MHz bw

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 3 V, with 2A load on the output. The power supply was disconnected**.**



Ch1=> input voltage 1V/div

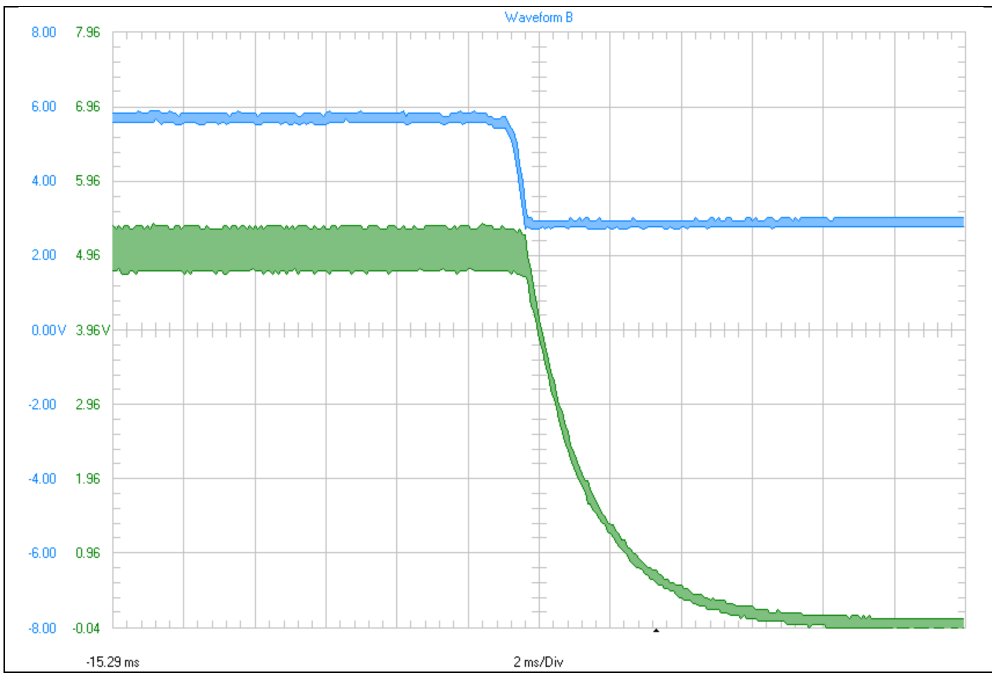
Ch2=> output voltage 1V/div

2ms/div

20MHz bw

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 6.0V, with 2A load on the output. The power supply was disconnected.



Ch1=> input voltage 2V/div

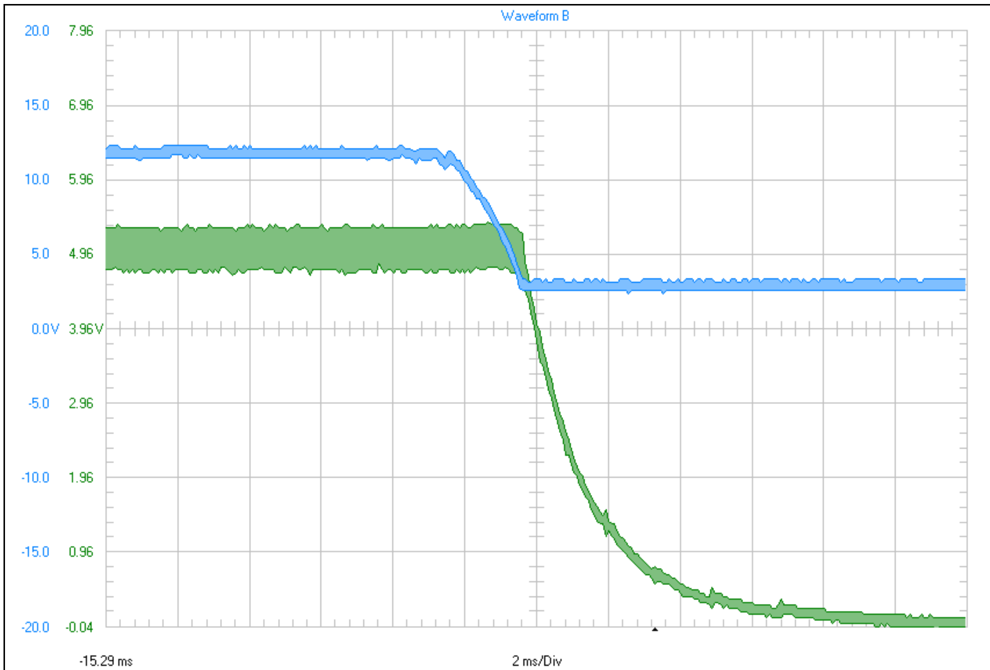
Ch2=> output voltage 2V/div

1ms/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 12V, with 2A load on the output. The power supply was disconnected.



Ch1=> input voltage
5V/div

Ch2=> output voltage
1V/div

2ms/div

20MHz bw

Figure 6

3 Efficiency

The efficiency is shown in the Figure 7 below. The input voltage was set to 3V, 6V and 12V.

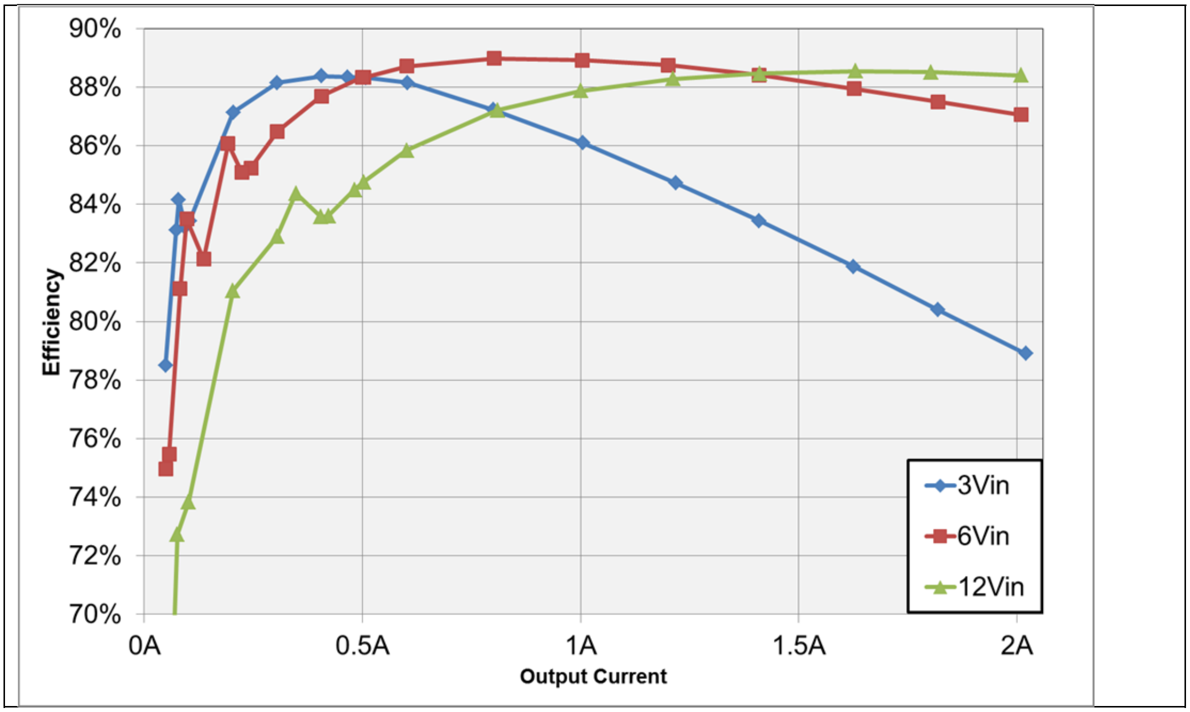


Figure 7

Figure 8 show the losses (Pin - Pout) with input voltage 3V, 6V and 12V

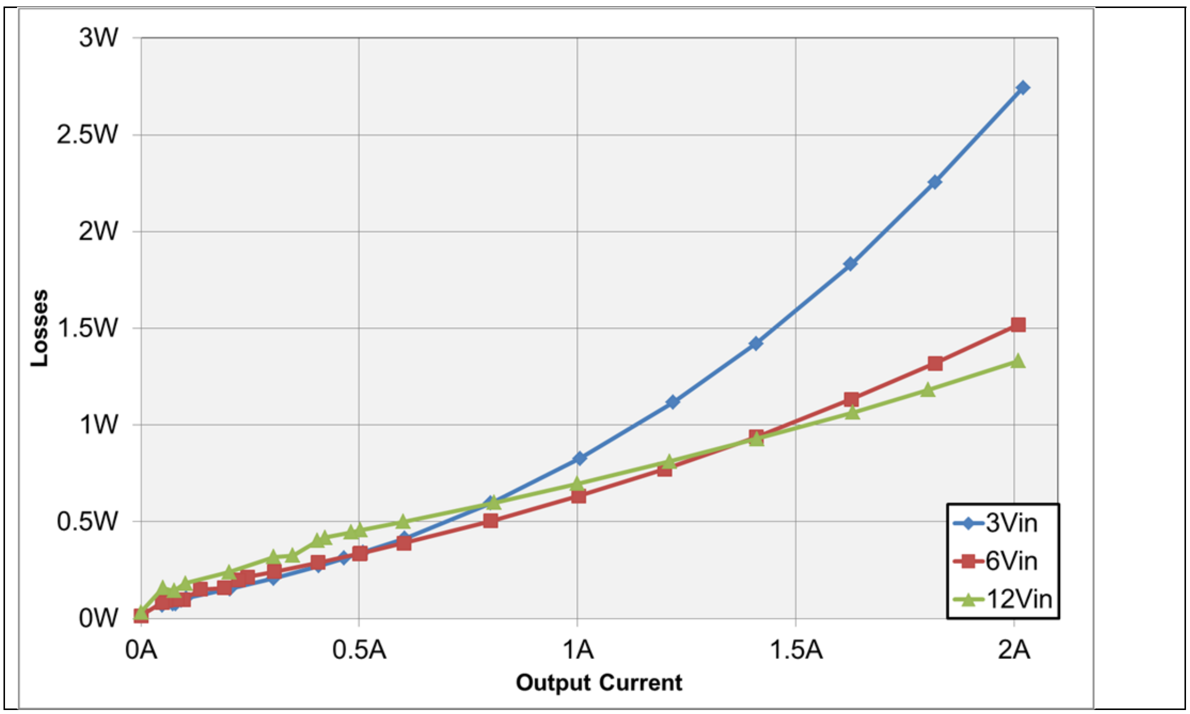


Figure 8

4 Load Regulation

The load regulation of the output is shown in the Figure 9 below. The input voltage was set to 3V, 6V and 12V.

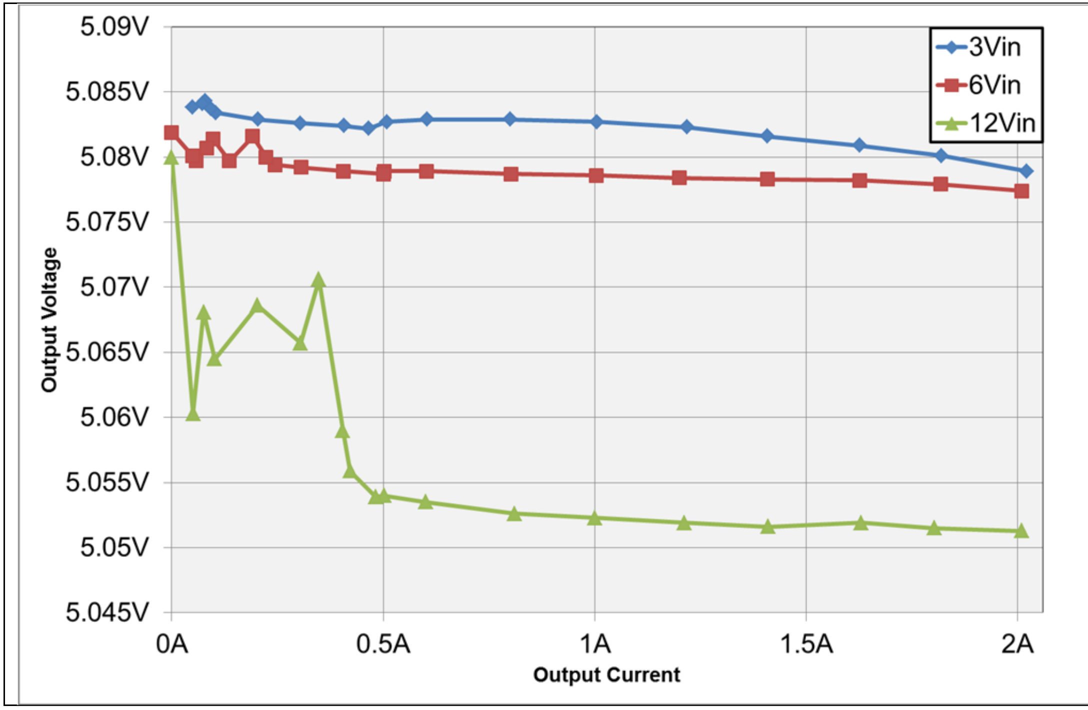


Figure 9

At 0.5A the variable resistor was changed from 100 Ohms to 10 Ohms.

5 Line Regulation

The line regulation is shown in Figure 10. The output current was set about 2A.

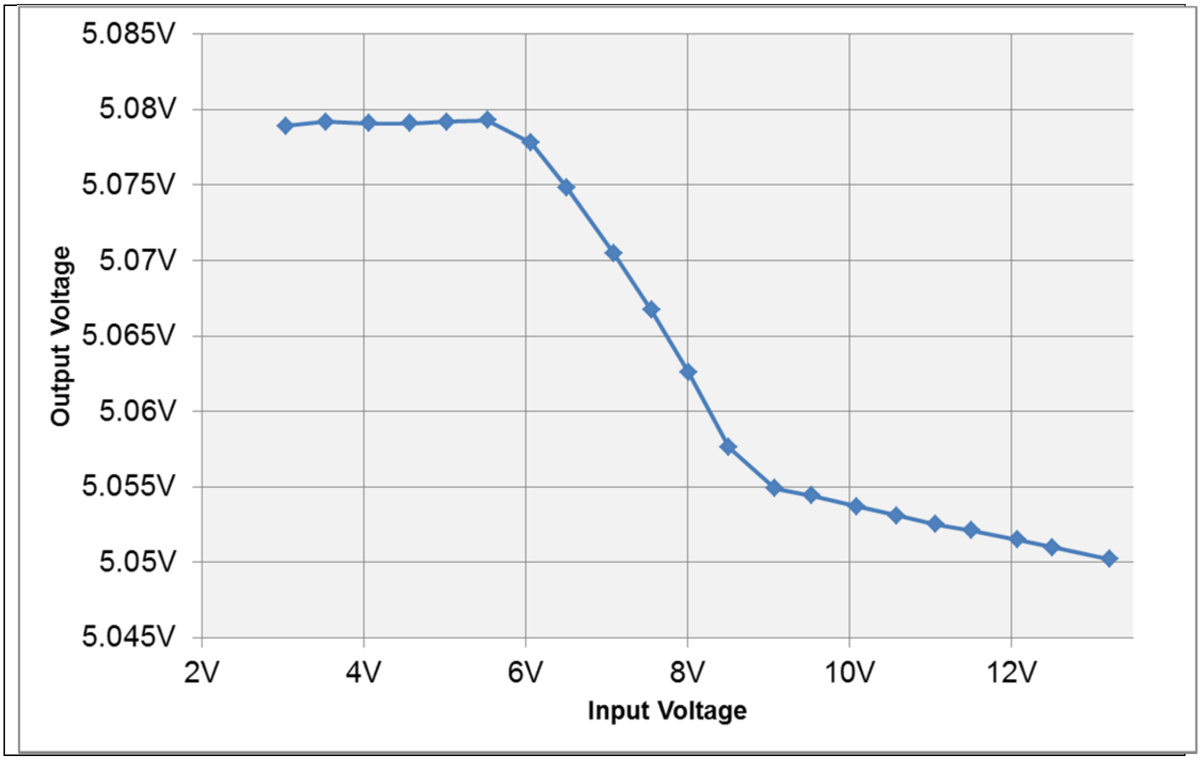


Figure 10

With the same setup efficiencies were calculated. This is shown in Figure 11

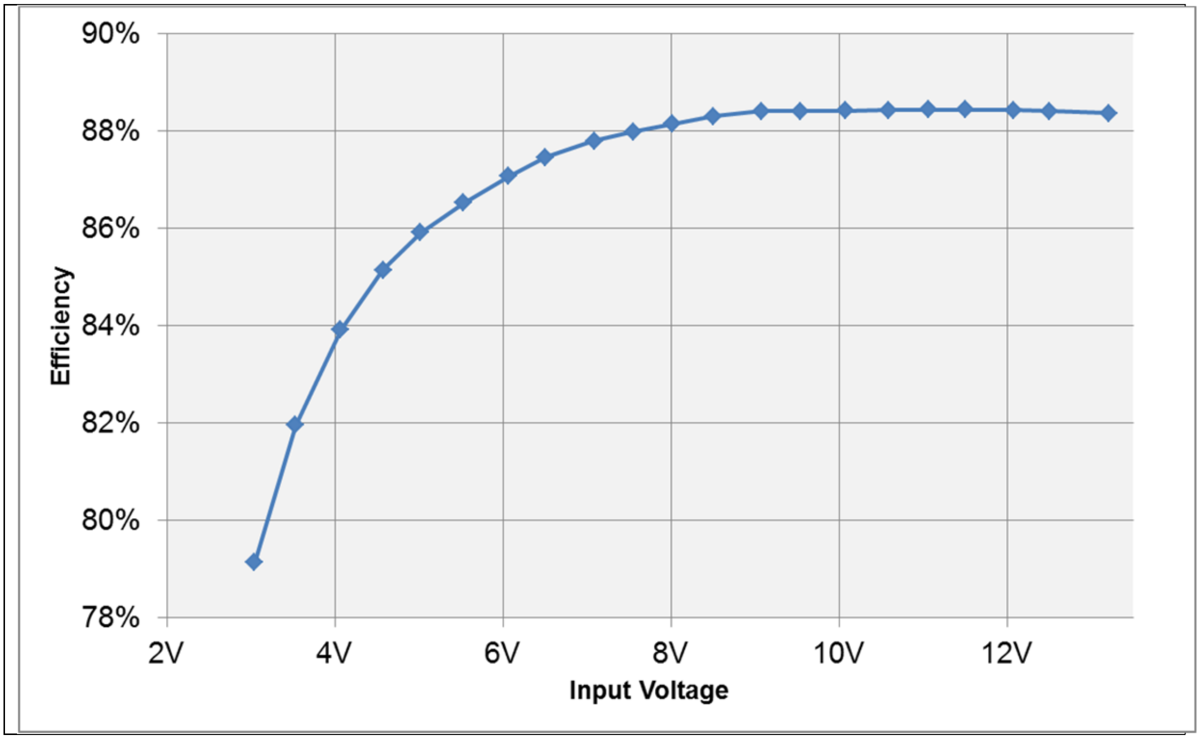


Figure 11

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 12.

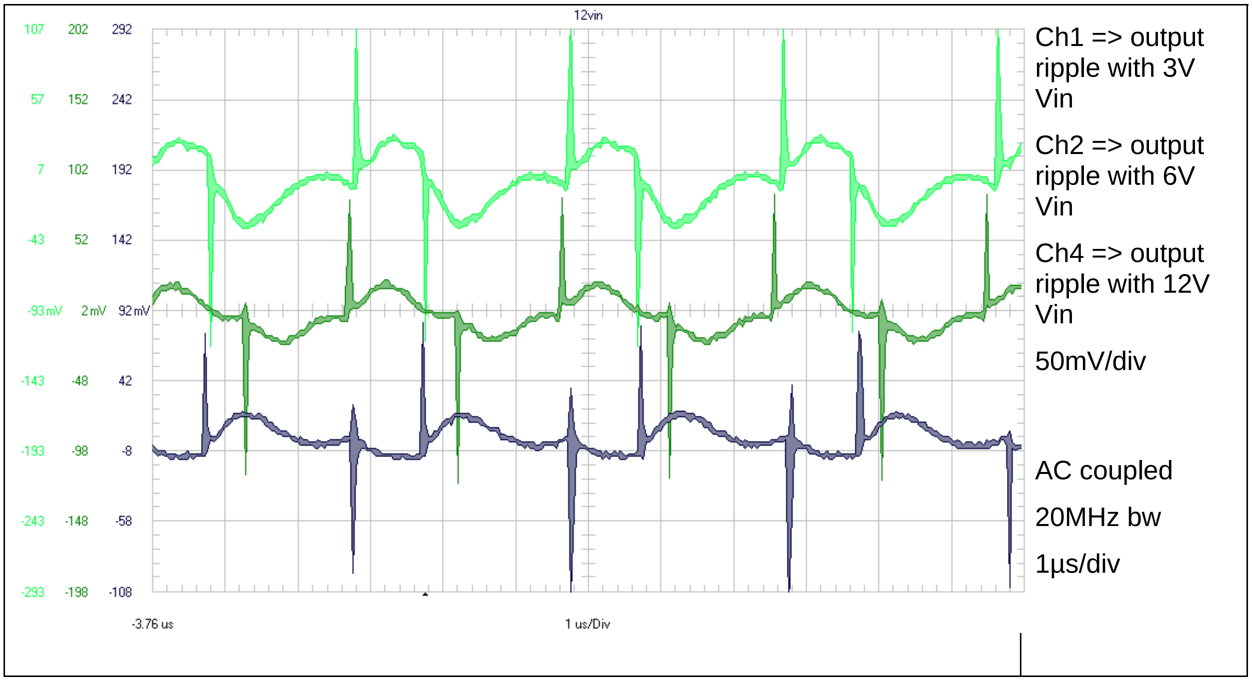


Figure 12

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 13.

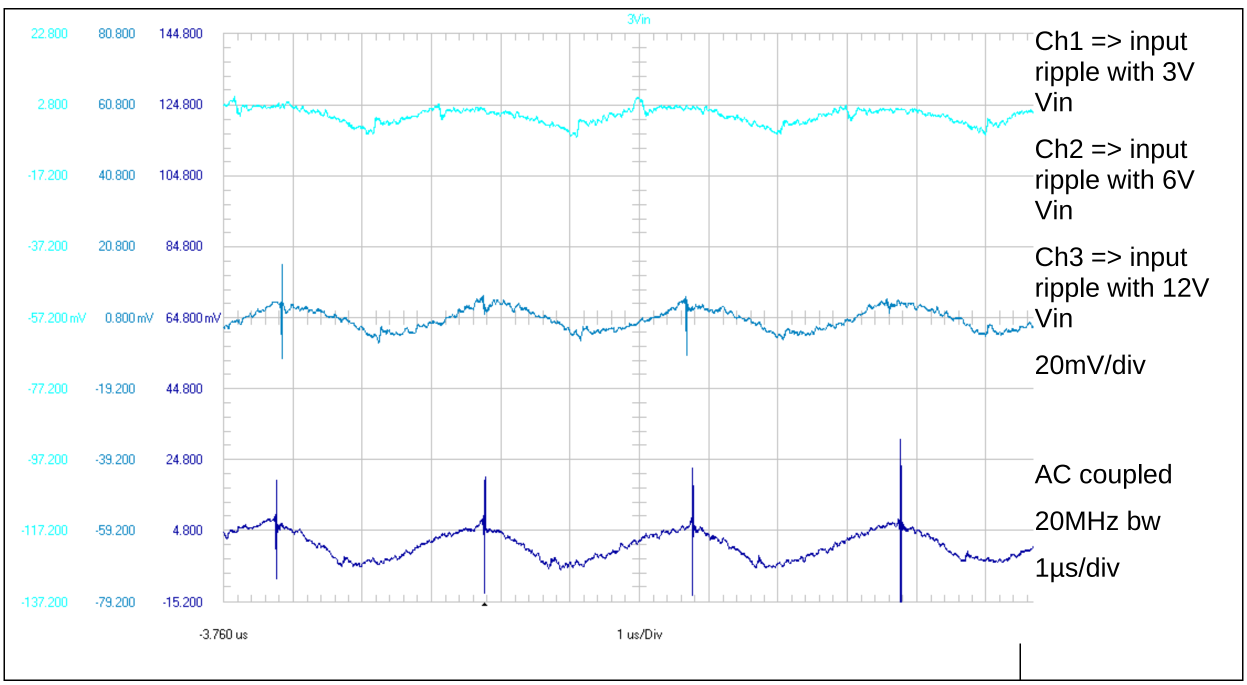


Figure 13

8 Load Transients

The Figure 14 shows the response to load transients for 3V input voltage. The load is switching from 1A to 2A (80Hz)
Electronic load was used

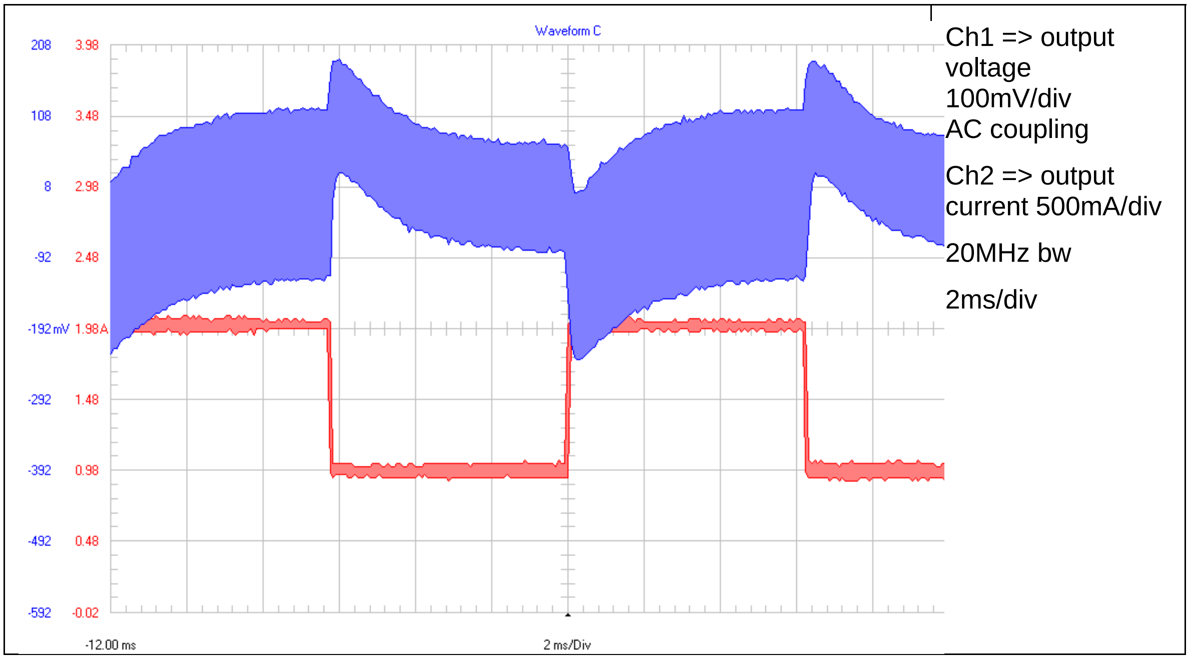


Figure 14

The Figure 15 shows the response to load transients for 6V input voltage. The load is switching from 1A to 2A,
Electronic load was used

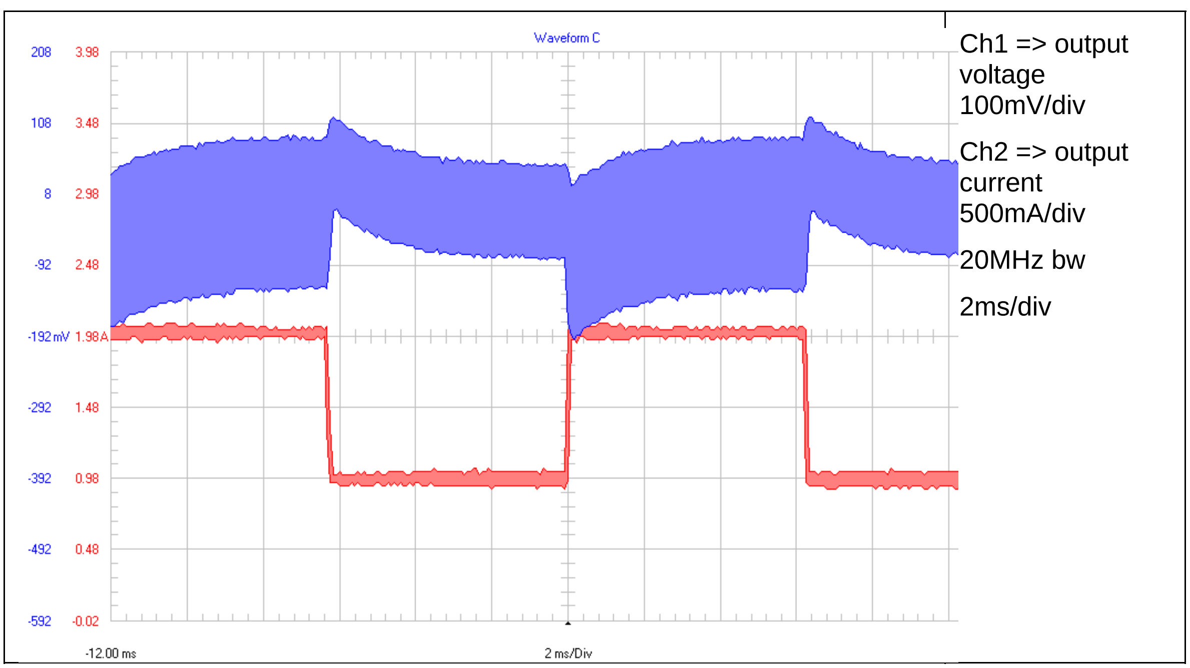
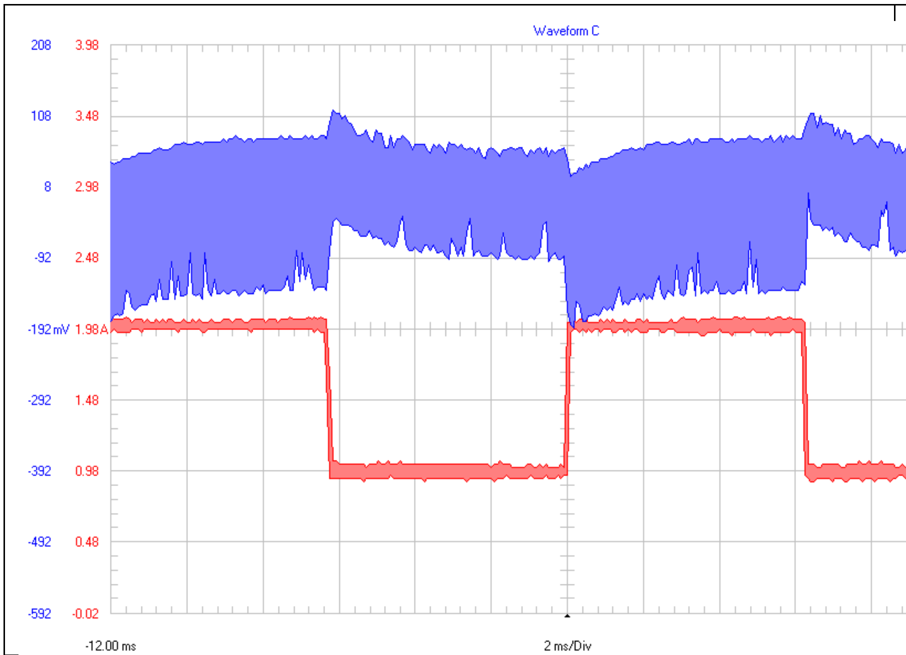


Figure 15

The Figure 16 shows the response to load transients for 12V input voltage. The load is switching from 1A to 2A
Electronic load was used.



Ch1 => output voltage 100mV/div

Ch2 => output current 500mA/div

20MHz bw

2ms/div

Figure 16

9 Control Loop Frequency Response

Figure 17 shows the loop response for 3V. Load is 2A.

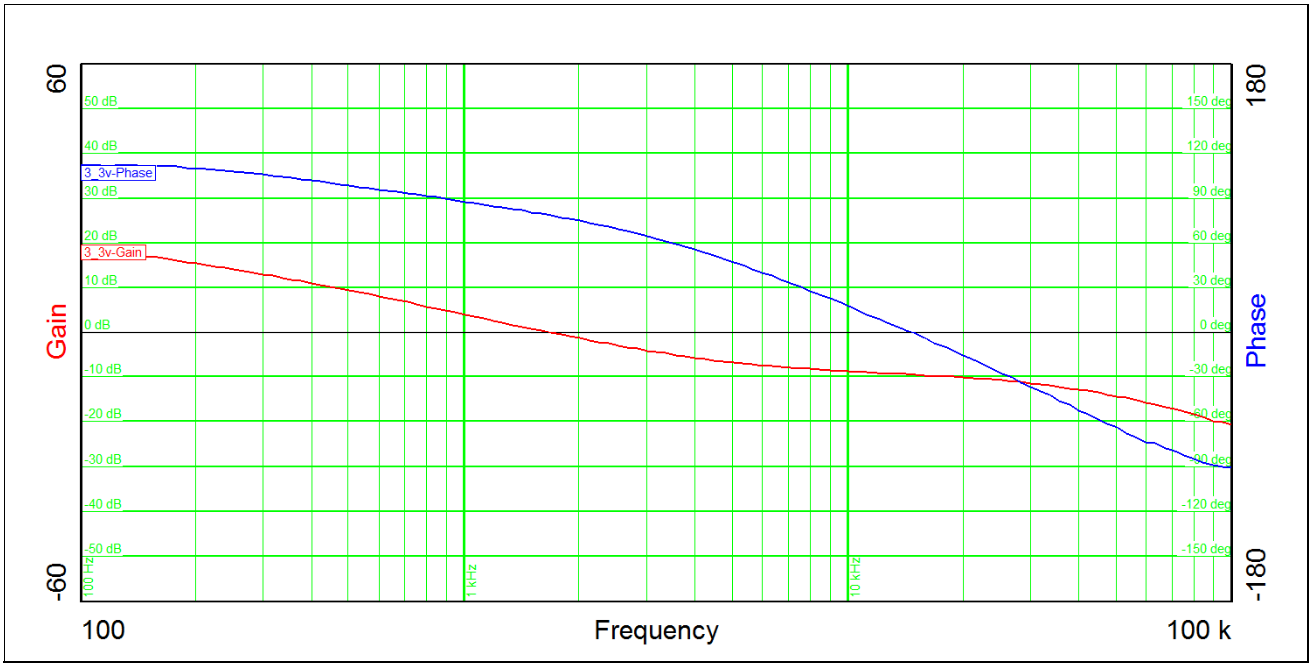


Figure 17

Figure 18 shows the loop response for 6V. Load is 2A.

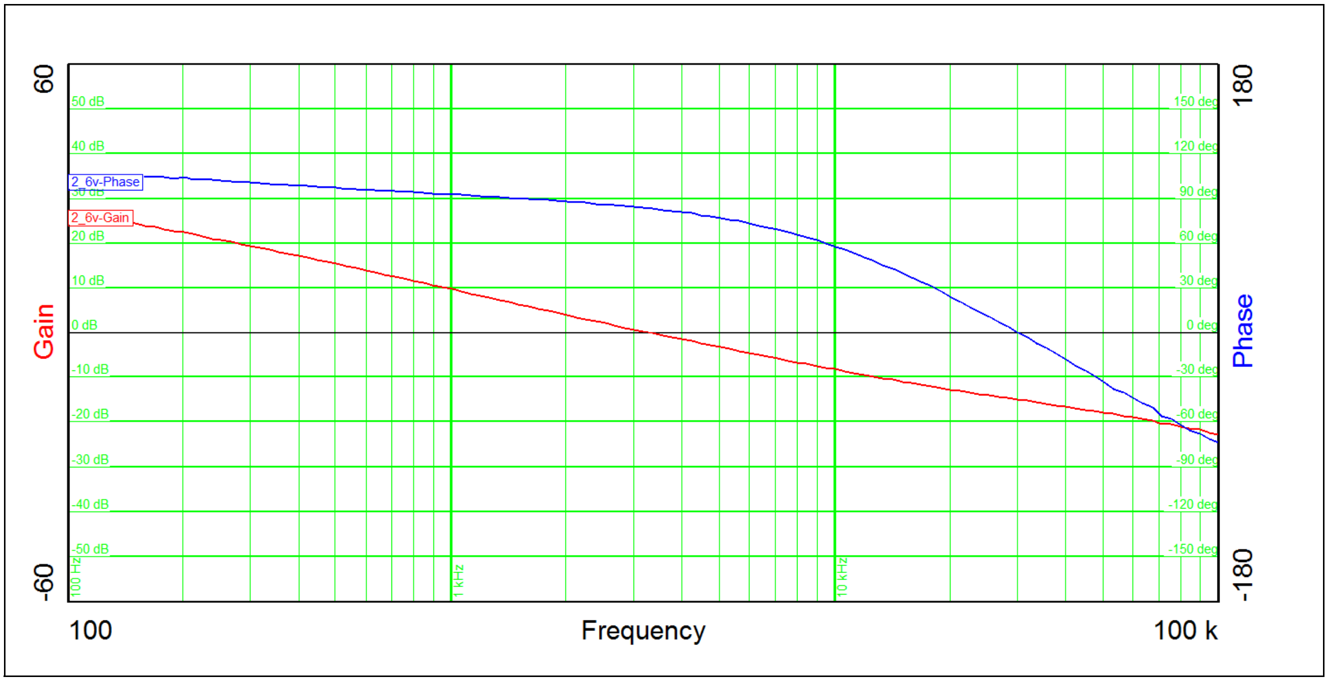


Figure 18

Figure 19 shows the loop response for 12V. Load is 2A.

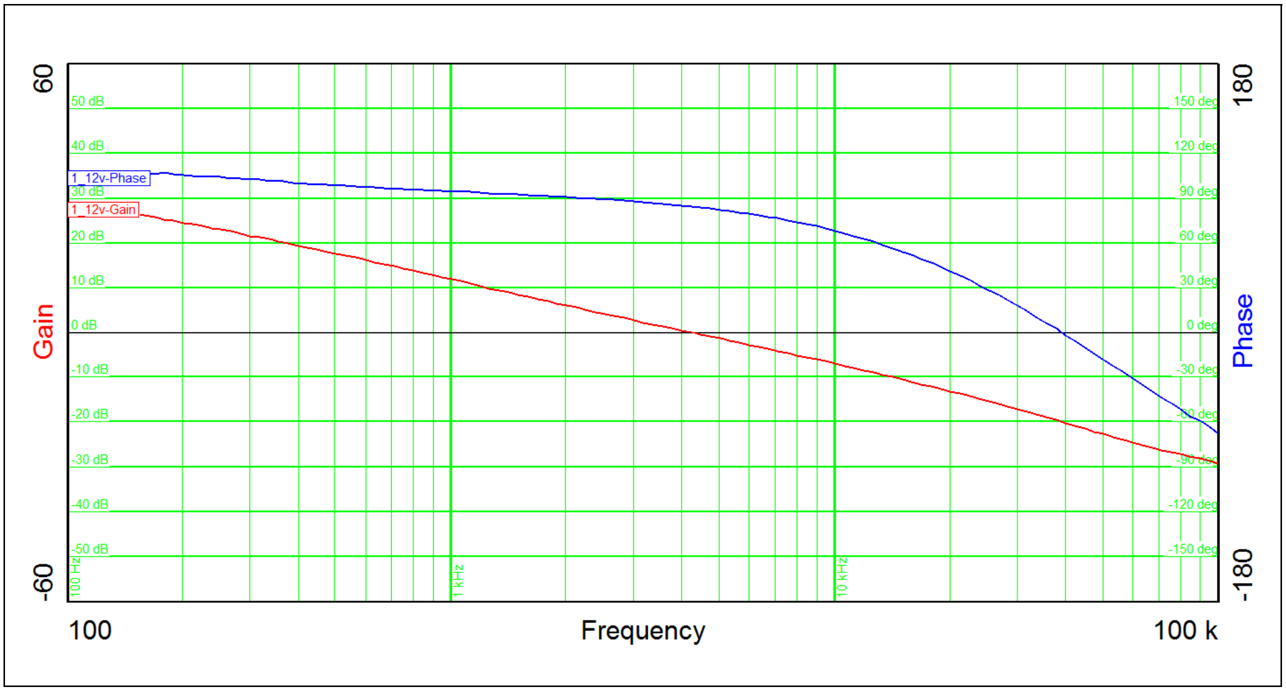


Figure 19

Table 1 summarizes the results of the above measurements

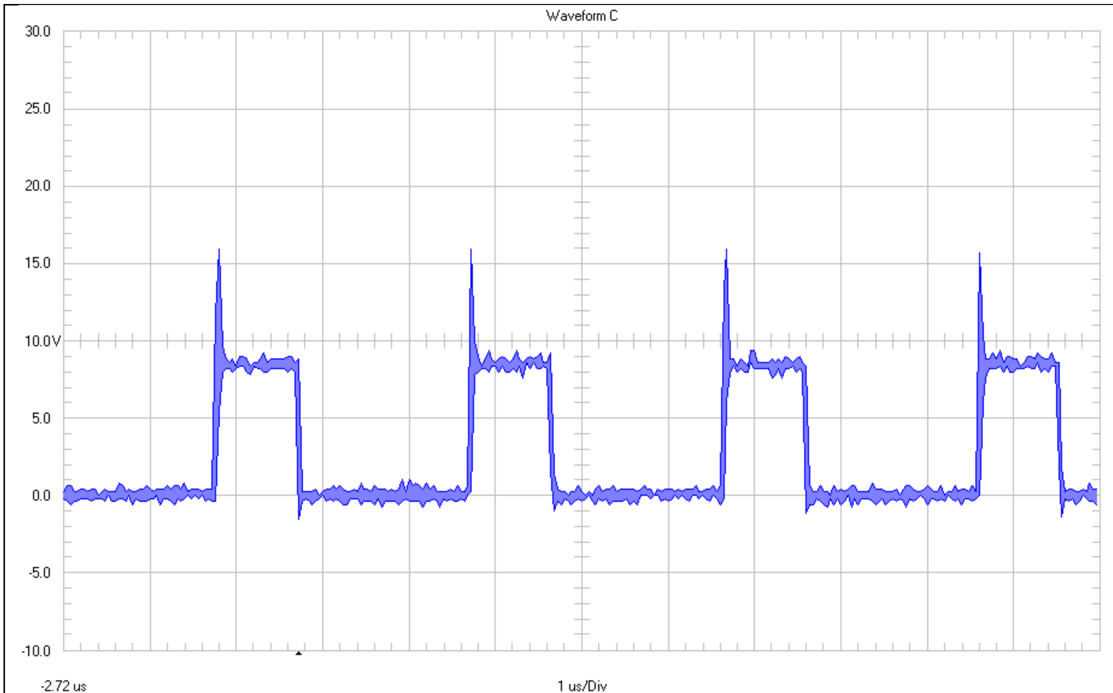
Vin	3V	6V	12V
Bandwidth (kHz)	1.67	3.27	4.26
Phase margin	78.6°	83.4°	84.5°
slope (20dB/decade)	-0.88	-0.89	-0.94
gain margin (dB)	-9.5	-15	-20
slope (20dB/decade)	-0.17	-0.65	-1.3
freq (kHz)	14.7	30.1	39.2

Table 1

10 Miscellaneous Waveforms

10.1 Switch Node (Drain-ground)

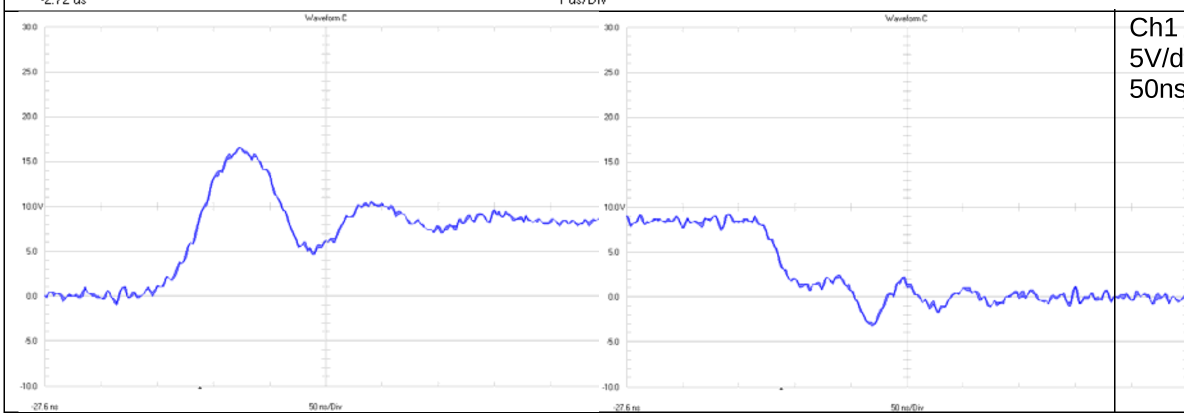
The waveform of the voltage on switchnode is shown in Figure 20. Input voltage was set to 3V and output current to 2A.



Ch1 =>
5V/div

1µs/div

full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 20

The waveform of the voltage on the switchnode is shown in Figure 21. Input voltage was set to 6V and output current to 2A.

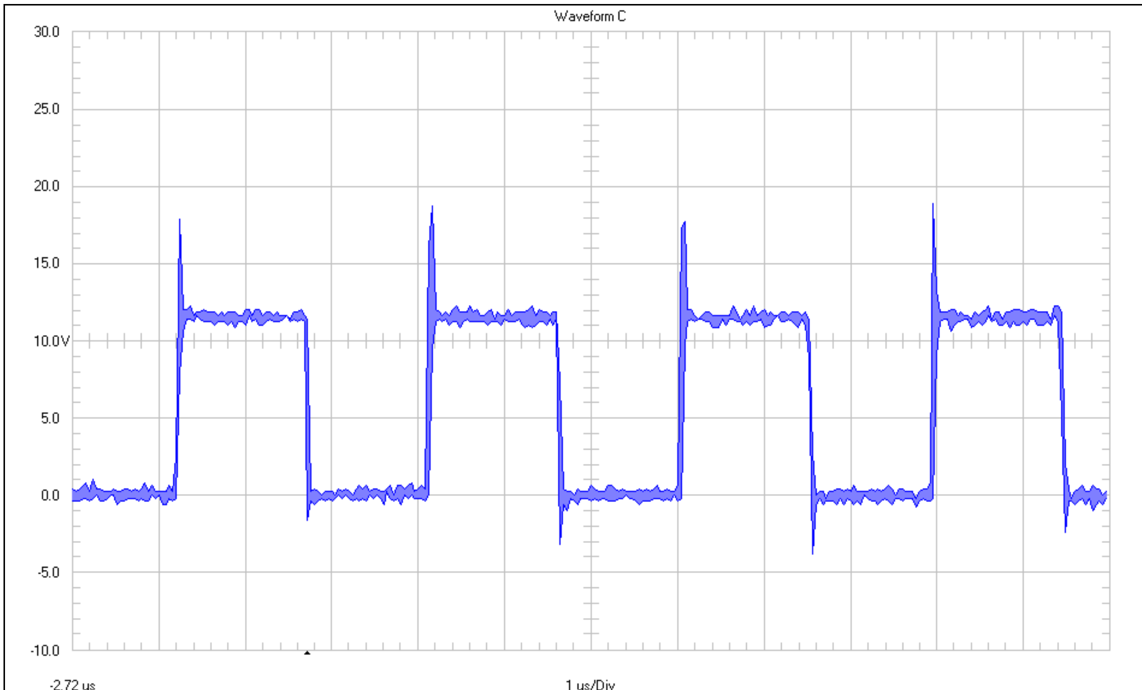
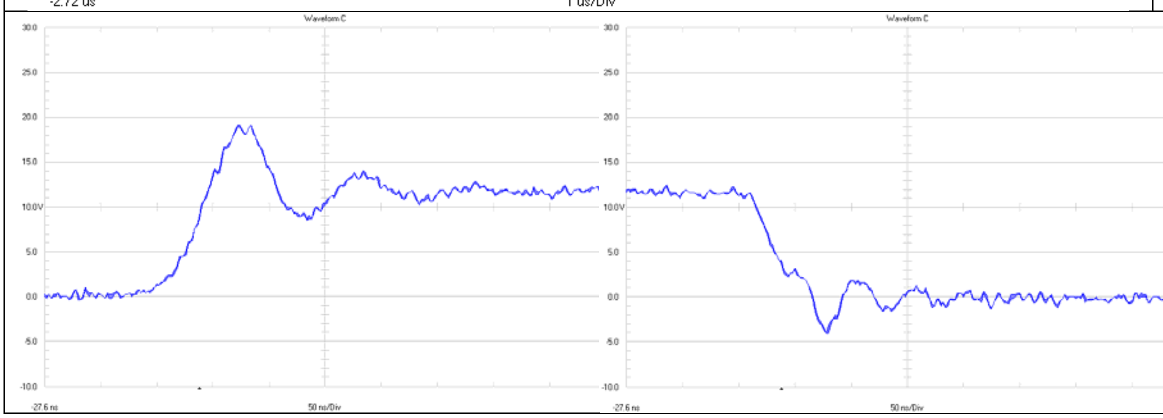
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 50ns/major div

Figure 21

The waveform of the voltage on switchnode is shown in Figure 22. Input voltage was set to 12V and output current to 2A.

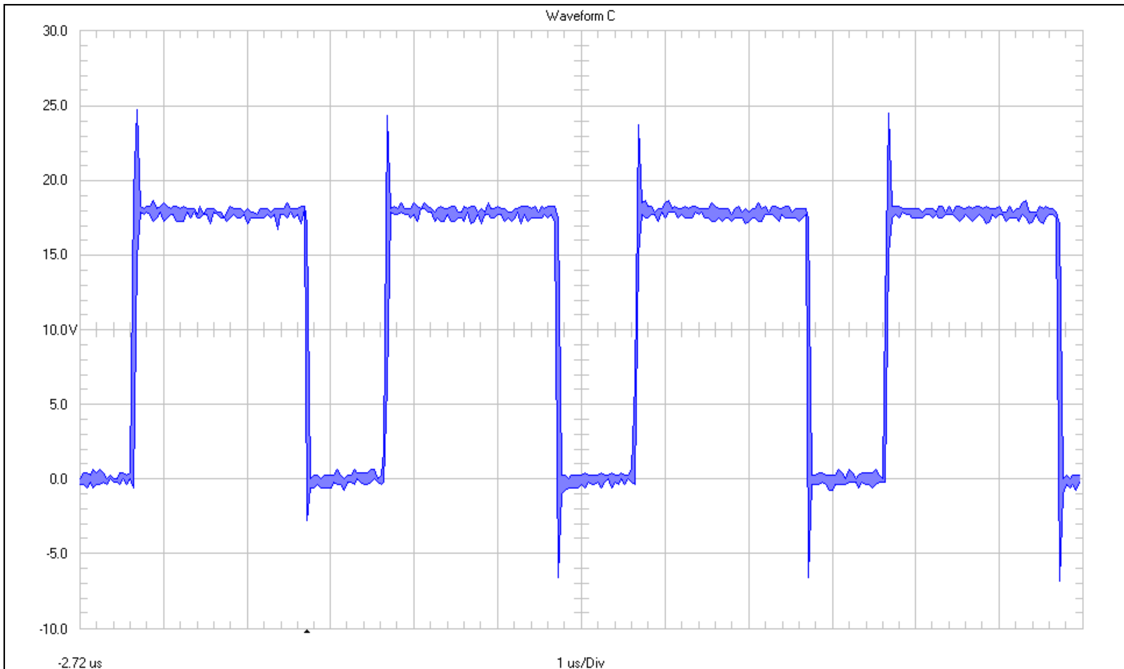
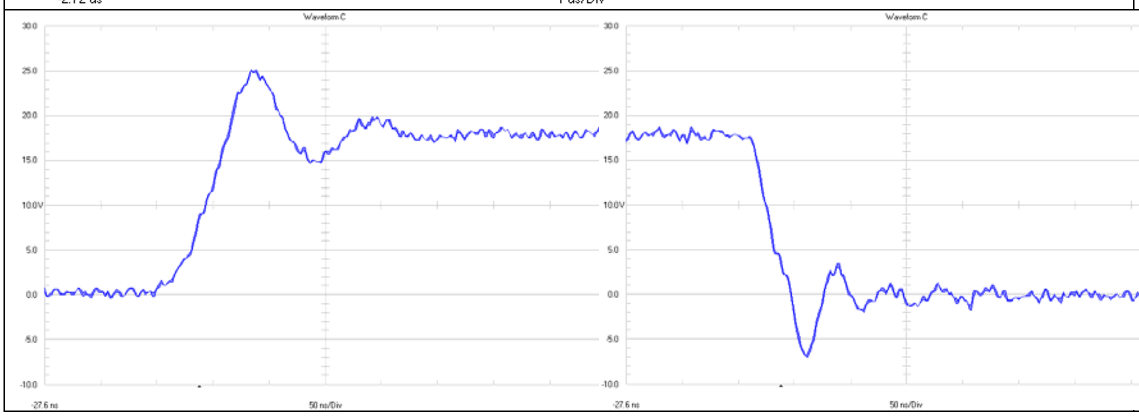
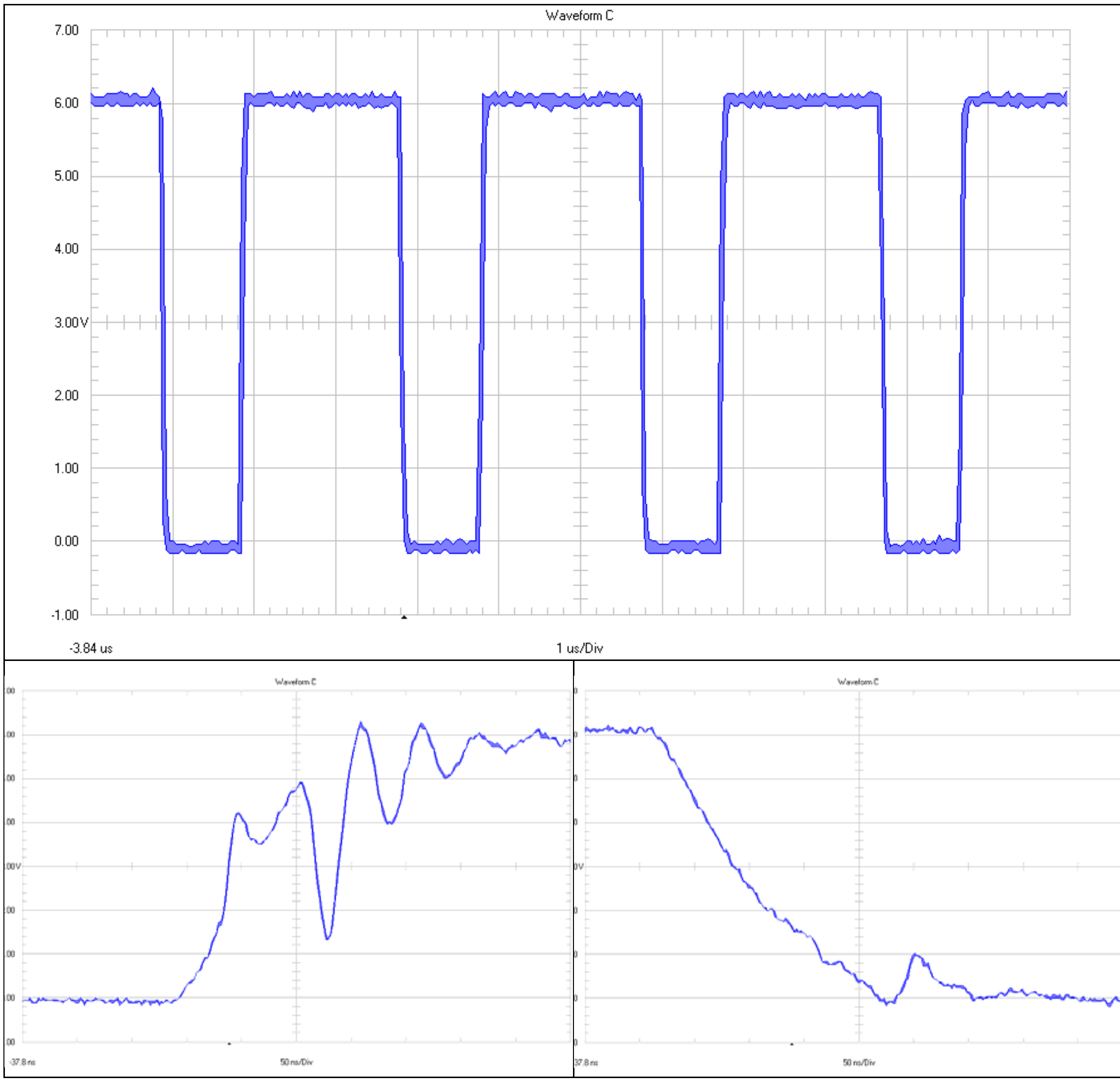
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 50ns/major div

Figure 22

10.2 Gate – Ground

The waveform of the voltage on gate to ground is shown in Figure 23. Input voltage was set to 3V and output current to 2A.



Ch1 => 1V/div
1µs/div
full bandwidth

Ch1 => 1V/div
50ns/major div

Figure 23

The waveform of the voltage on gate to ground is shown in Figure 24. Input voltage was set to 6V and output current to 2A.

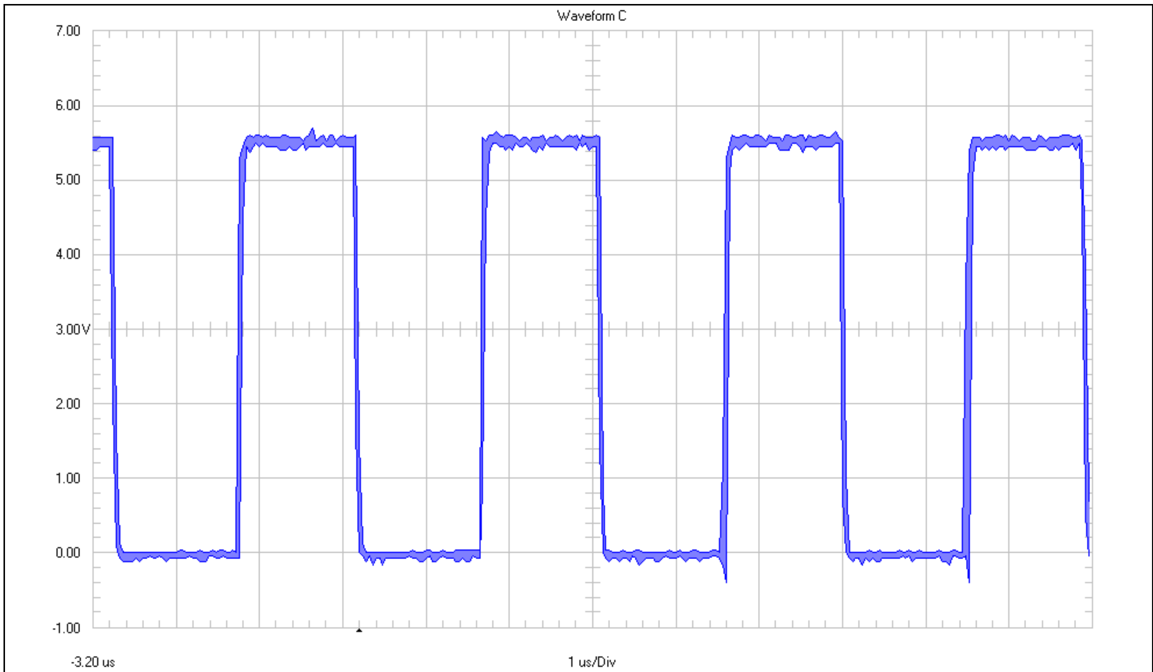
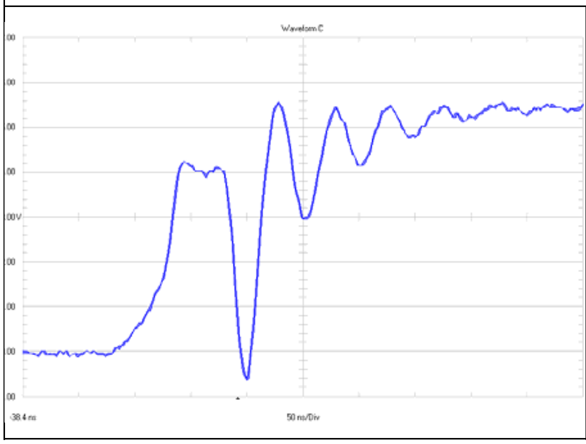
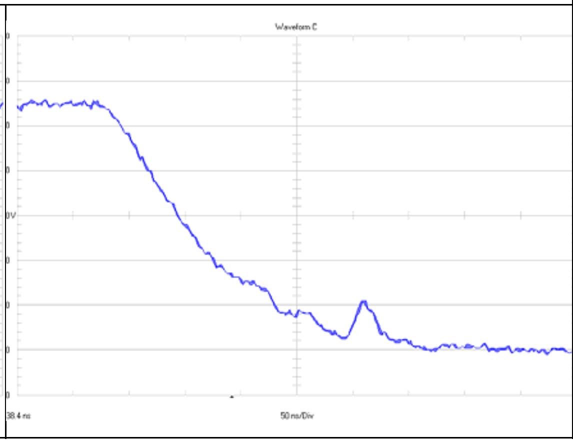
		Ch1 => 1V/div 1µs/div full bandwidth
		Ch1 => 1V/div 50ns/major div

Figure 24

The waveform of the voltage on gate to ground is shown in Figure 25. Input voltage was set to 12V and output current to 2A.

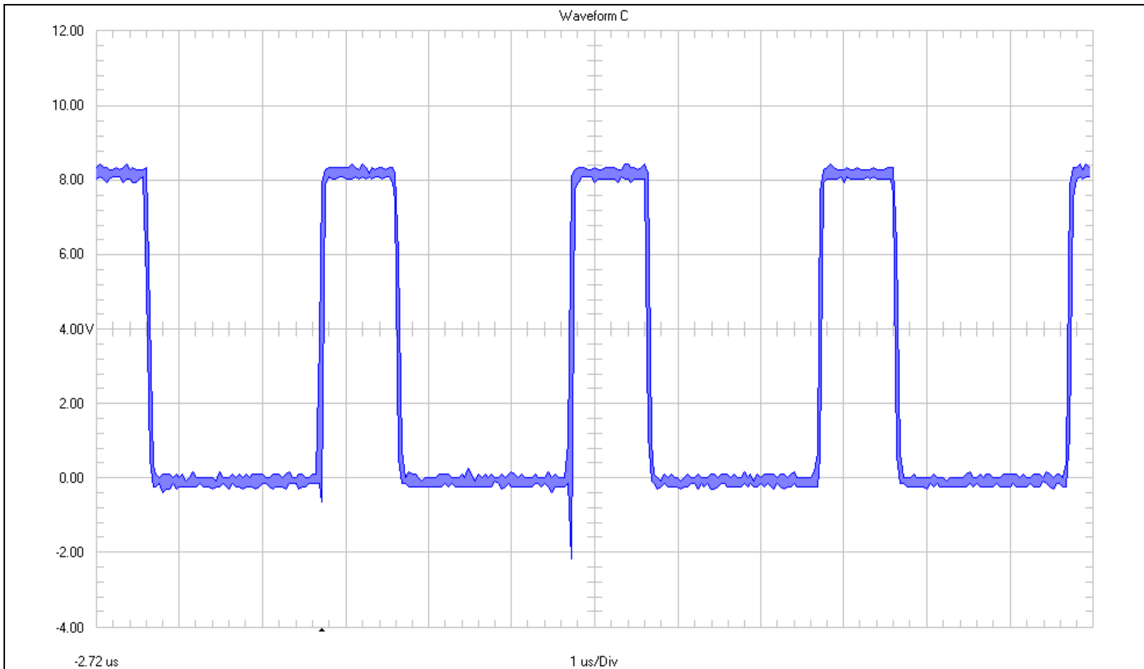
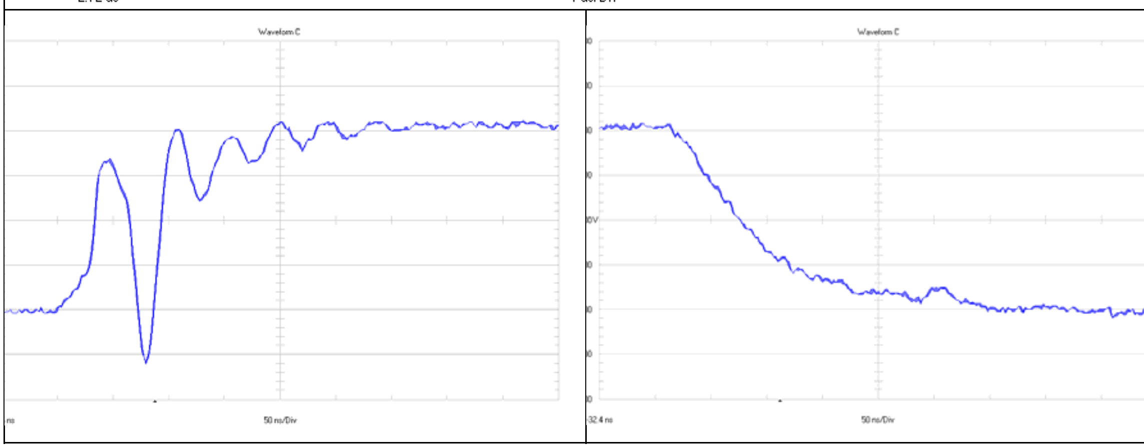
	Ch1 => 2V/div 1µs/div full bandwidth
	Ch1 => 2V/div 50ns/major div

Figure 25

10.3 Voltage D1 (referenced to VOUT)

The waveform of the voltage is shown in Figure 26. Input voltage was set to 3V and output current to 2A.

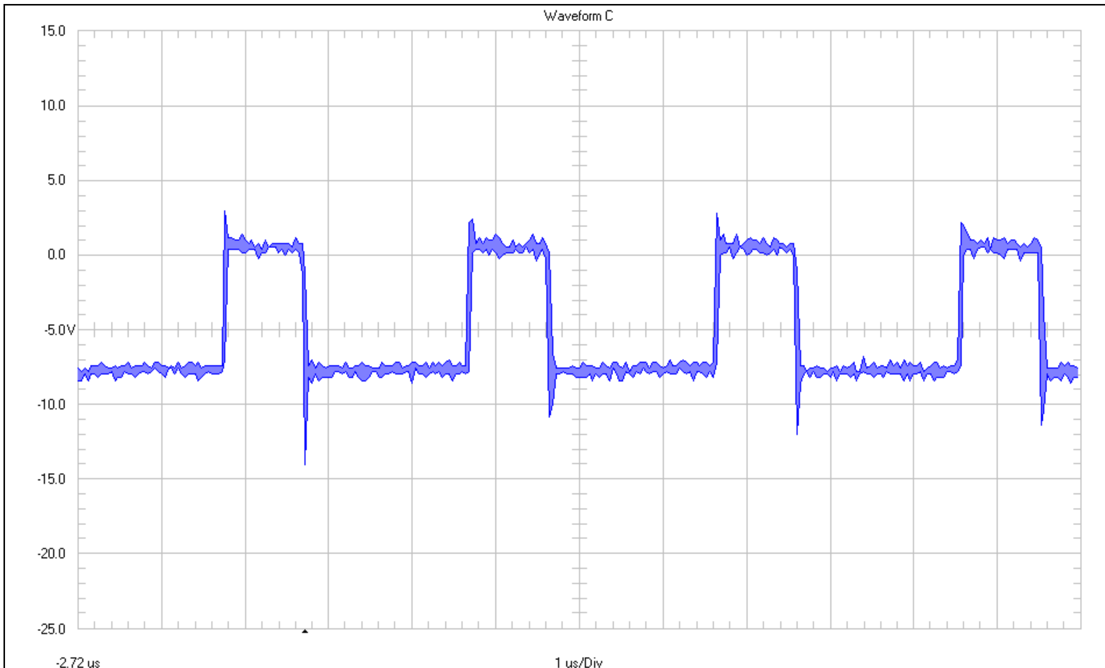
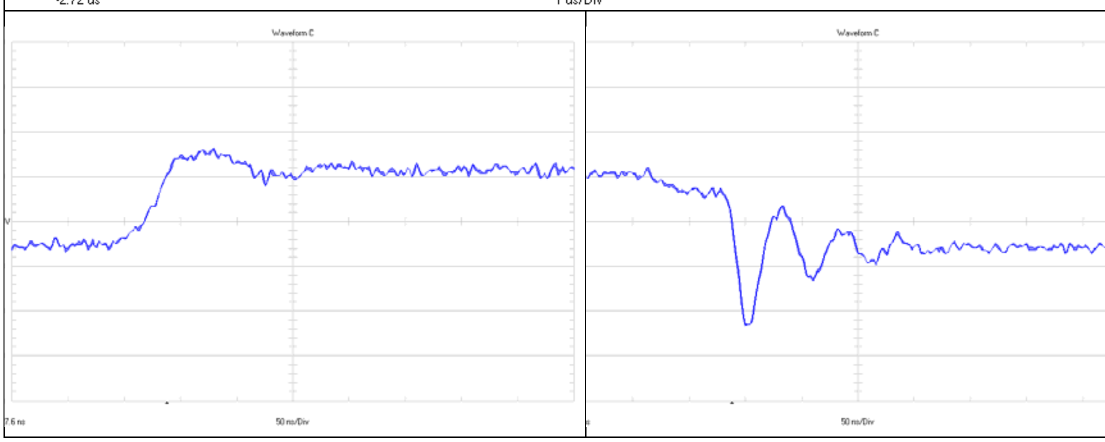
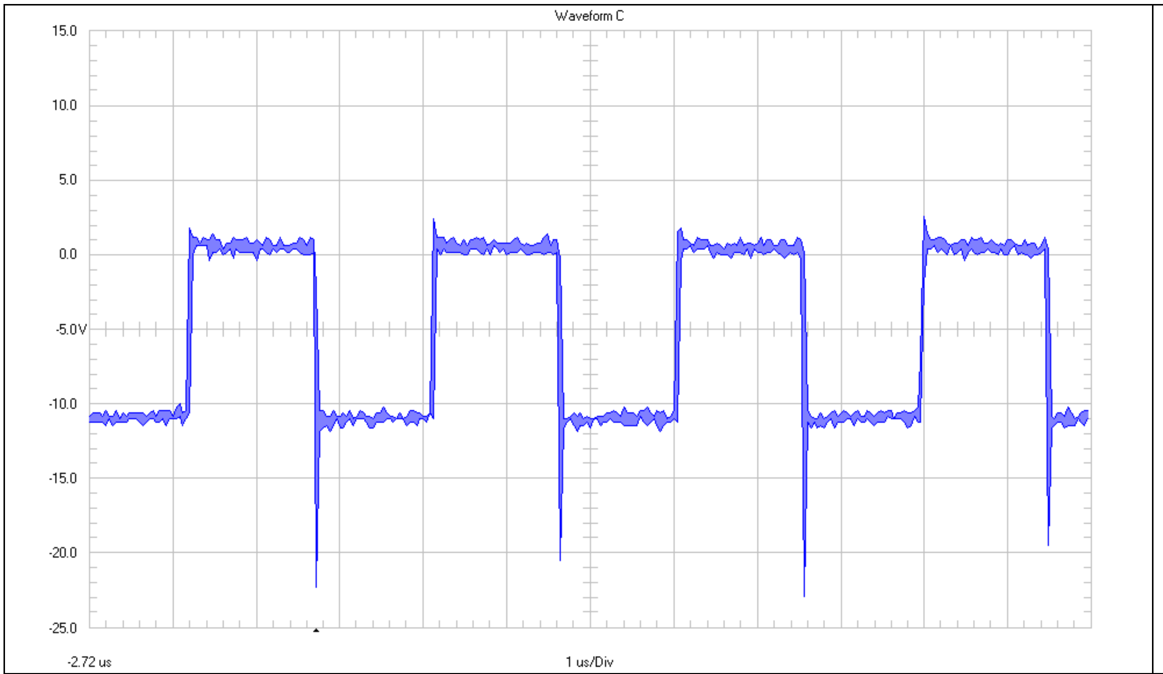
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 50ns/div

Figure 26

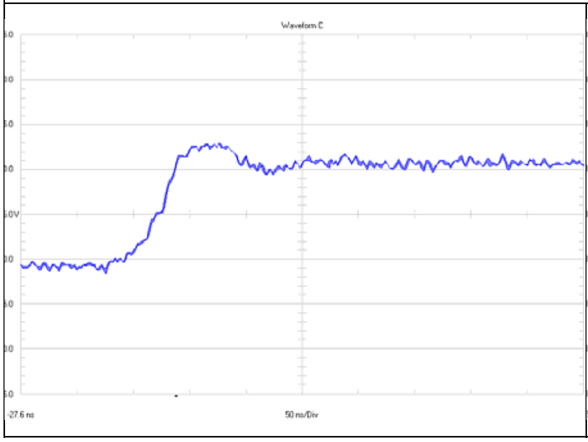
The waveform of the voltage is shown in Figure 27. Input voltage was set to 6V and output current to 2A.

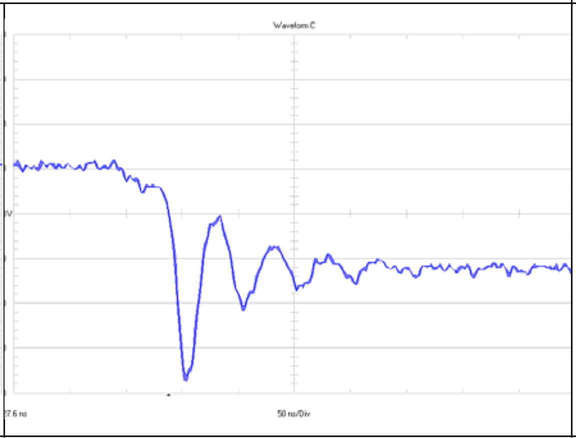


Ch1 => 5V/div

1µs/div

full bandwidth

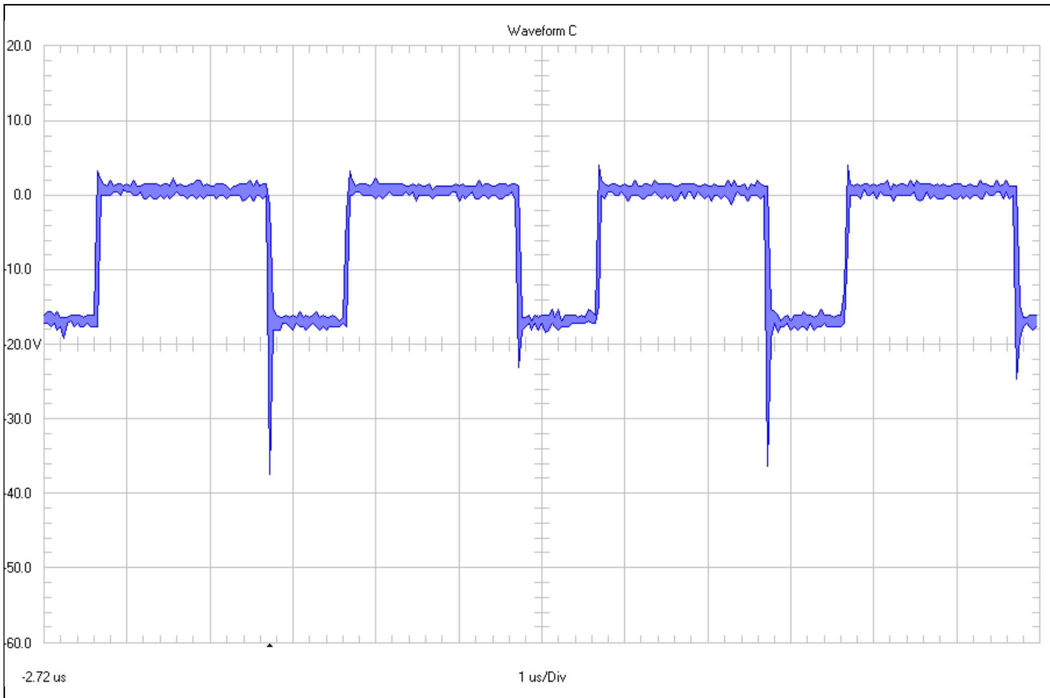




Ch1 => 5V/div
50ns/major div

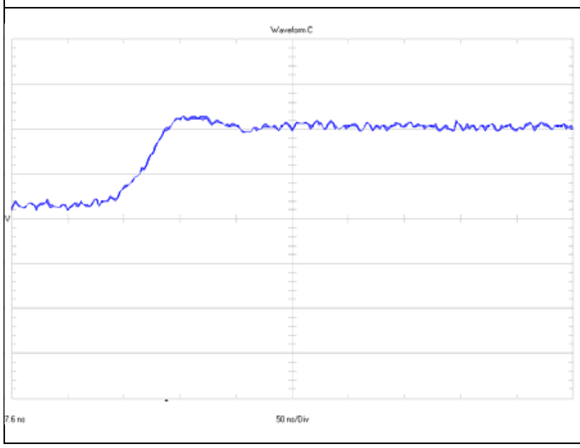
Figure 27

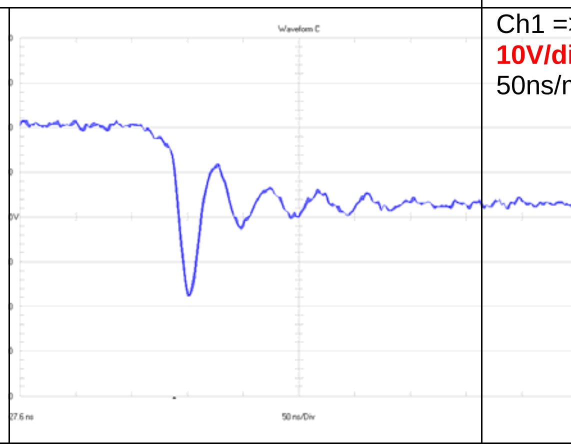
The waveform of the voltage is shown in Figure 28. Input voltage was set to 12V and output current to 2A.



Ch1 =>
10V/div

1µs/div
full bandwidth





Ch1 =>
10V/div
50ns/major div

Figure 28

This design is built on an universal board for boost/sepic/flyback; layout is not the optimum; at your design check reverse voltage at Schottky rectifier – sloppy layout might need a 40V Schottky rectifier or a small snubber 100pF/100 Ohms across the rectifier itself.

11 Thermal Image

Figure 29 shows the thermal image at 3V input voltage and 2A output current (electronic load)

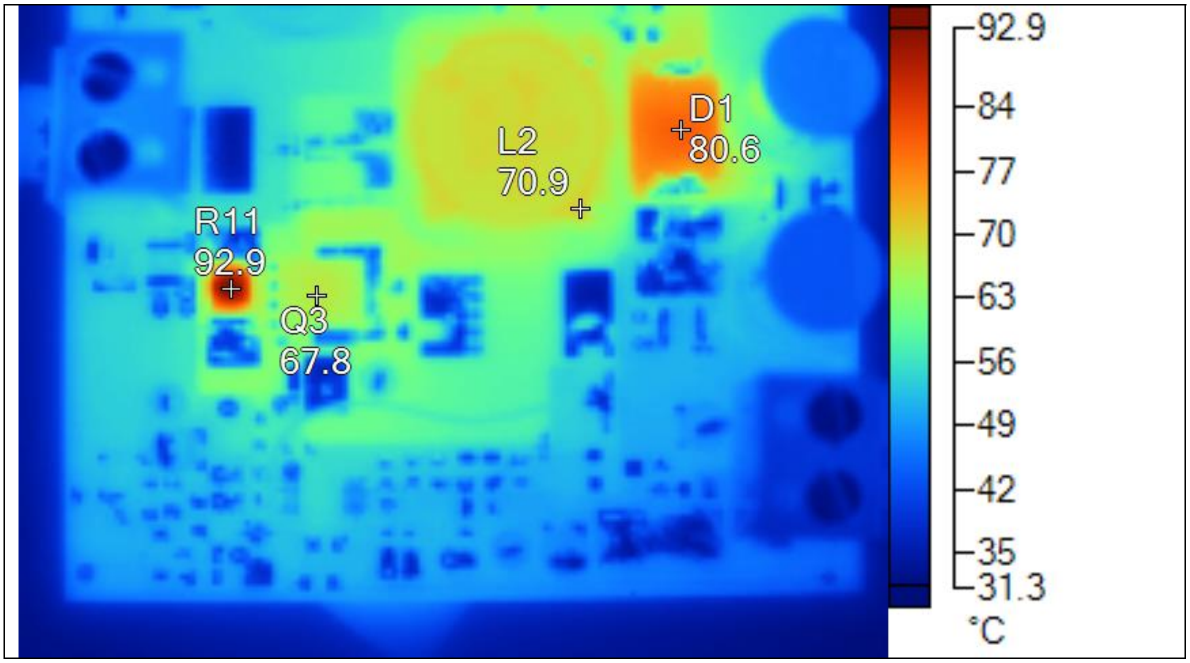


Figure 29

Name	Temperature
R11	92.9°C
D1	80.6°C
L2	70.9°C
Q3	67.8°C

Figure 30 shows the thermal image at 6V input voltage and 2A output current (electronic load)

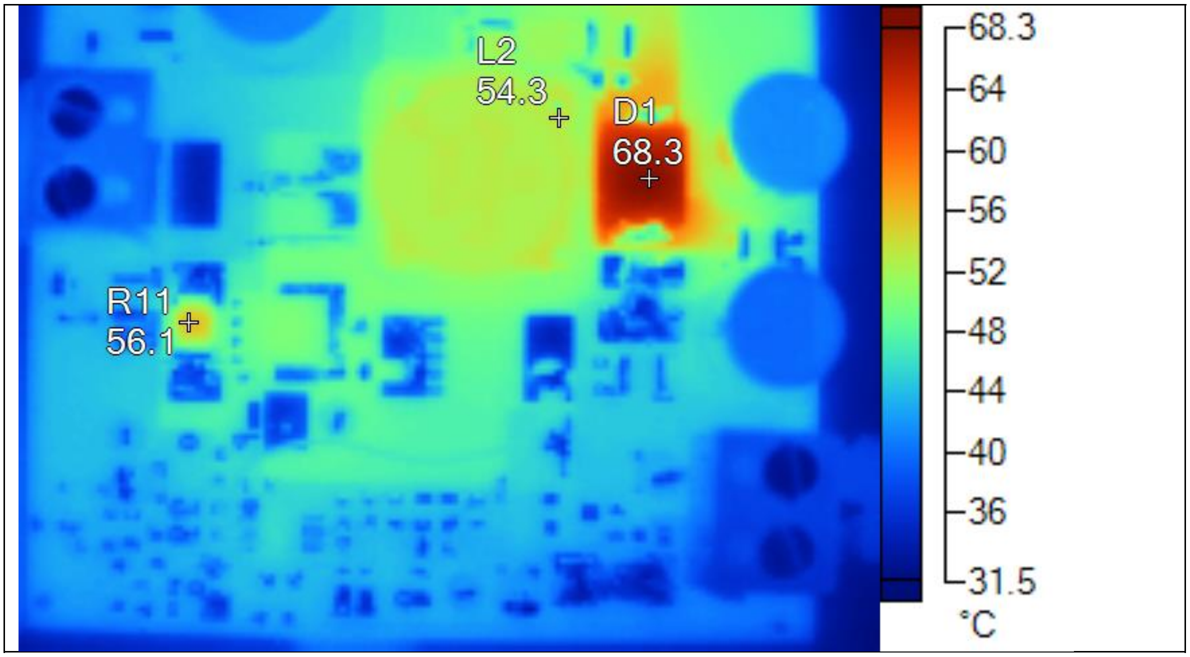


Figure 30

Name	Temperature
D1	68.3°C
R11	56.1°C
L2	54.3°C

Figure 31 shows the thermal image at 12V input voltage and 2A output current (electronic load)

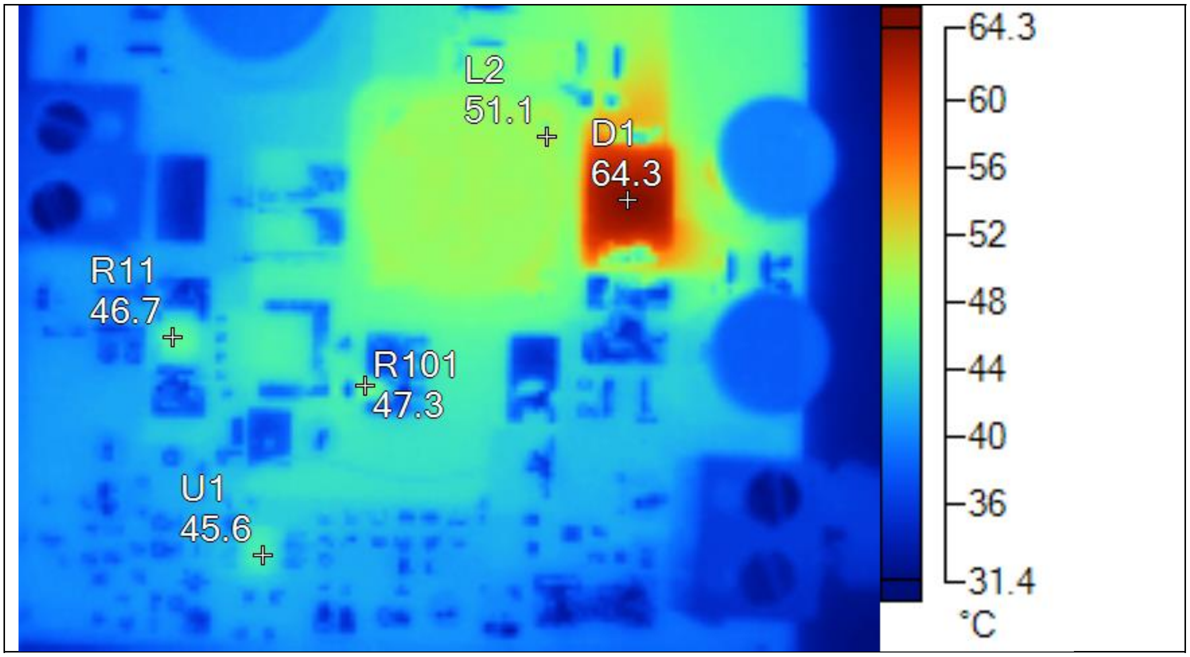
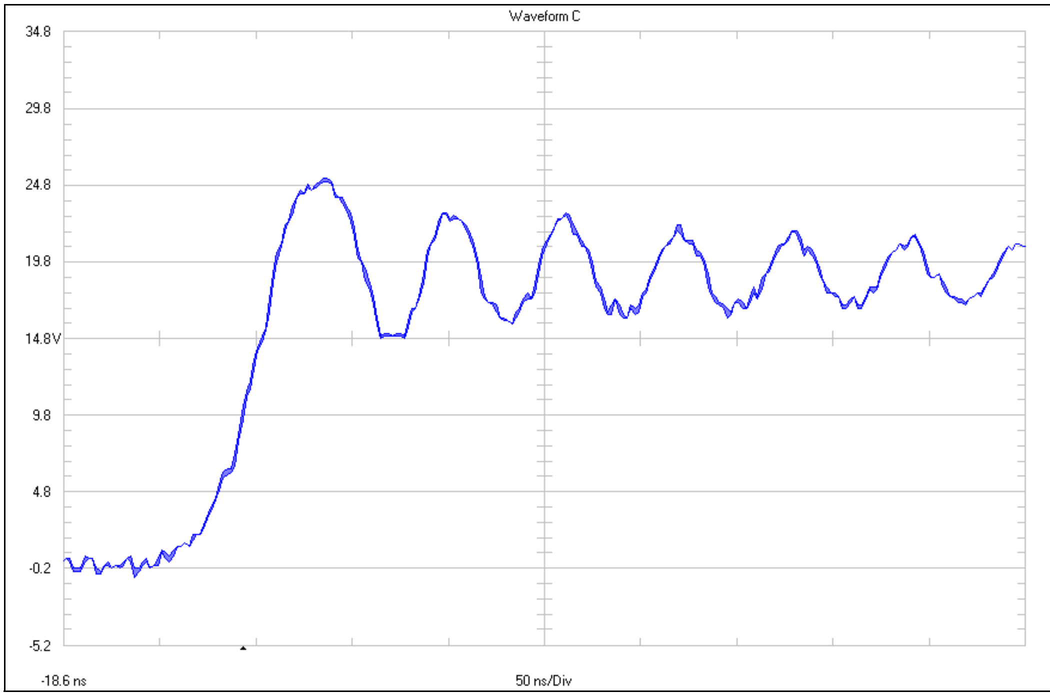


Figure 31

Name	Temperature
D1	64.3°C
R11	46.7°C
L2	51.1°C
U1	45.6°C
R101	47.3°C

12 Snubber Evaluation

Figure 31 shows the switchnode waveform without snubber. The ringing is around 84 MHz.



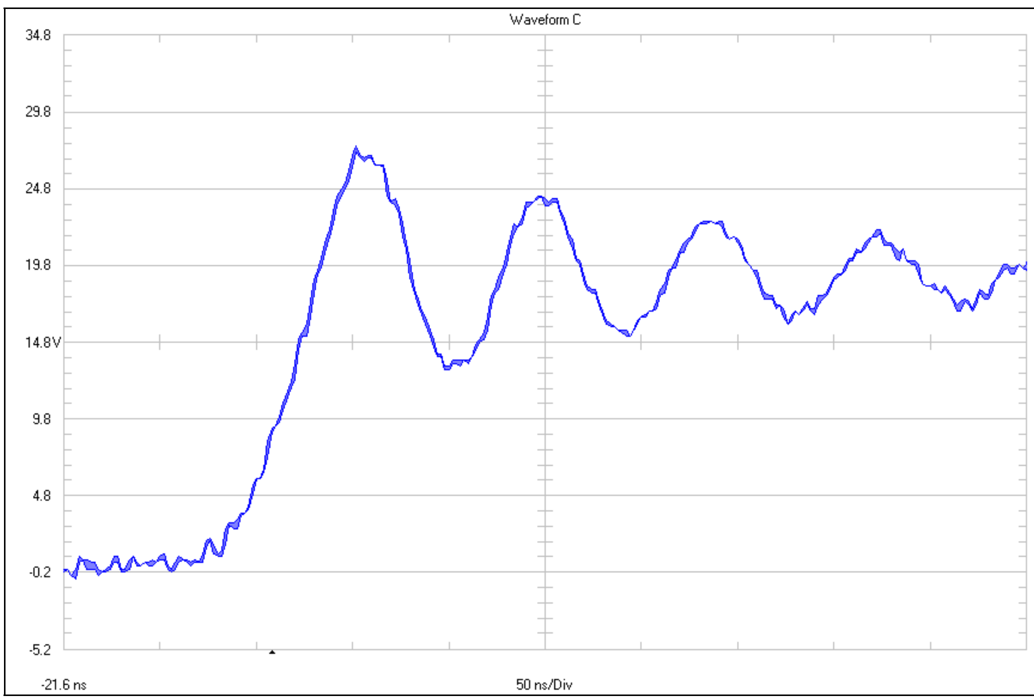
Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 32

Figure 33 shows the switchnode waveform with 470pF. The ringing is around 57MHz.



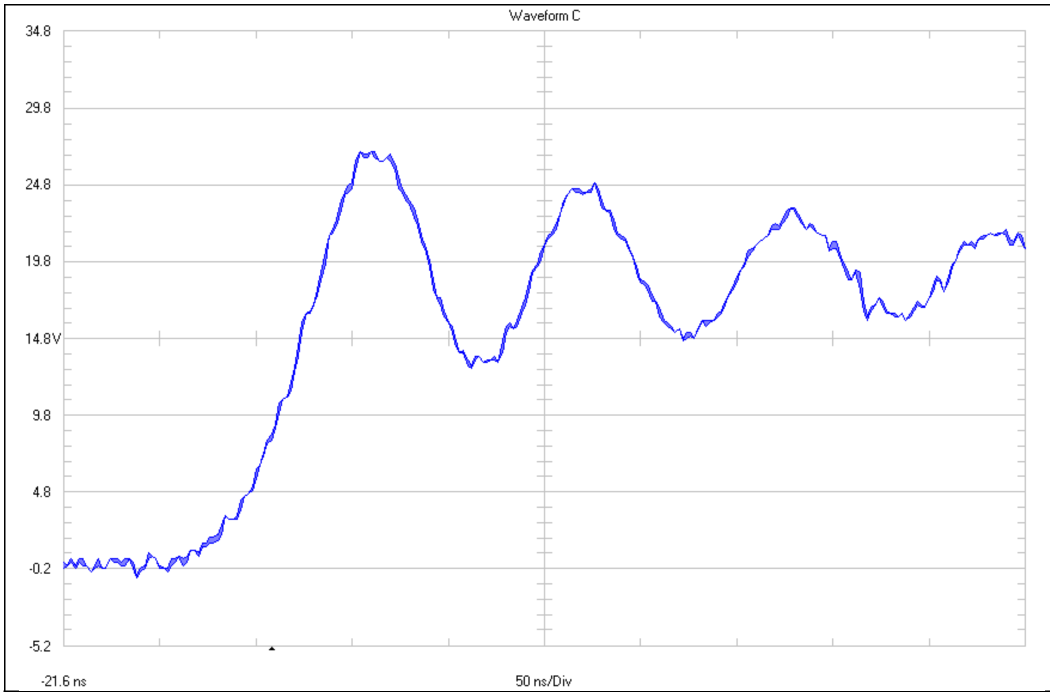
Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 33

Figure 34 shows the switchnode waveform with 820pF. The ringing is about 46MHz.



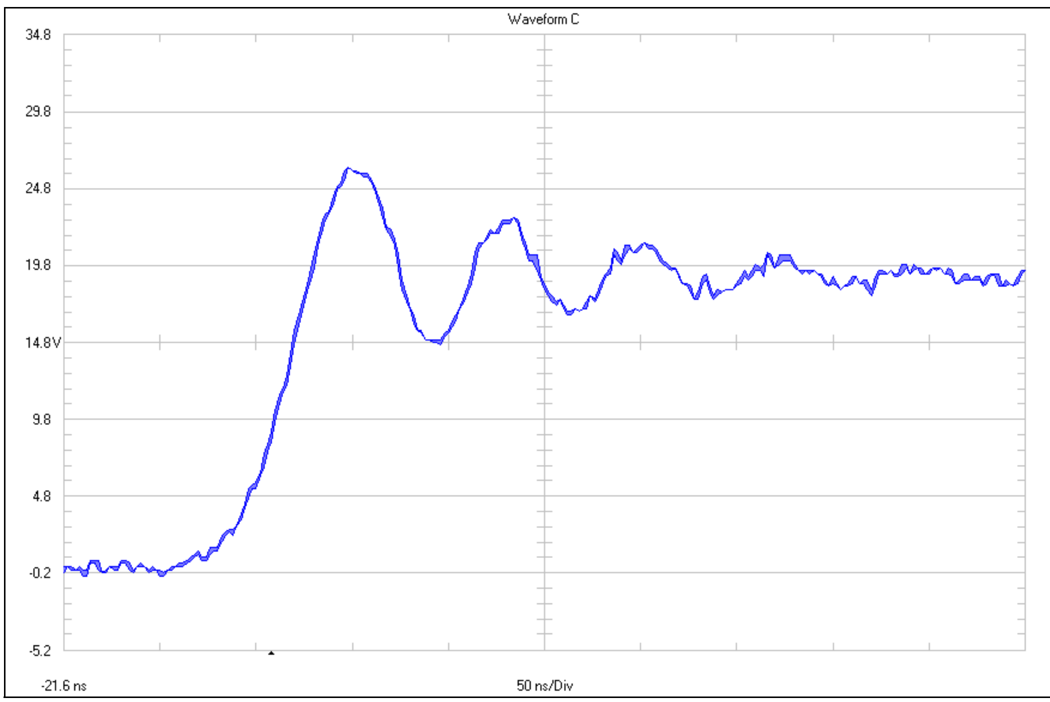
Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 34

Figure 35 shows the switchnode waveform with 820pFand 3.3Ohms. The ringing is about 64MHz.



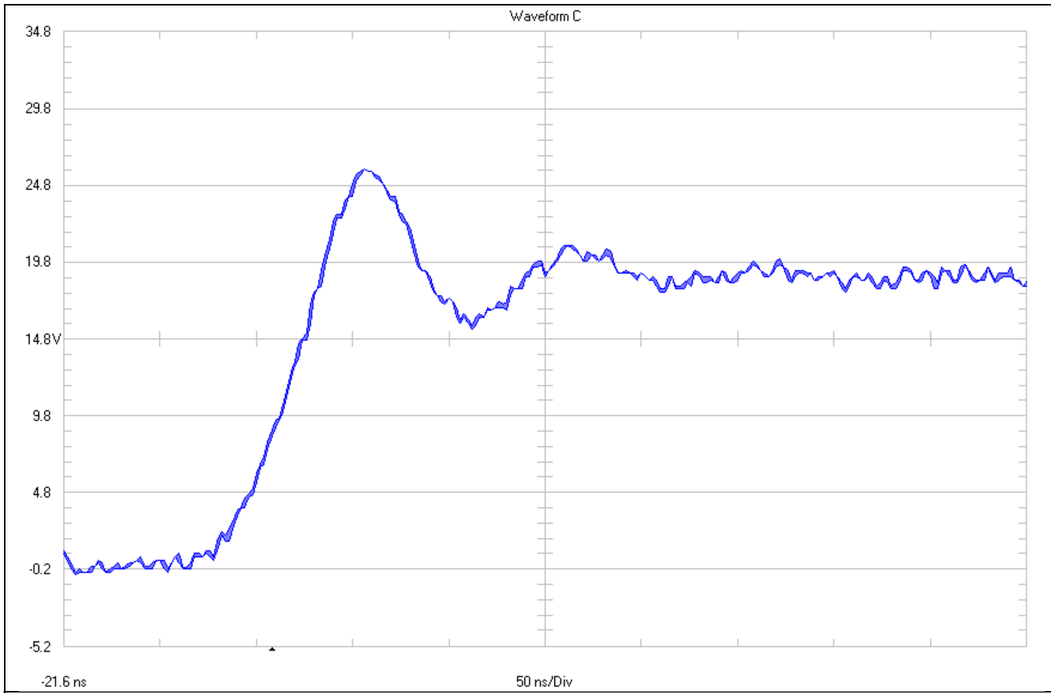
Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 35

Figure 36 shows the switchnode waveform with 820pFand 2.2Ohms.



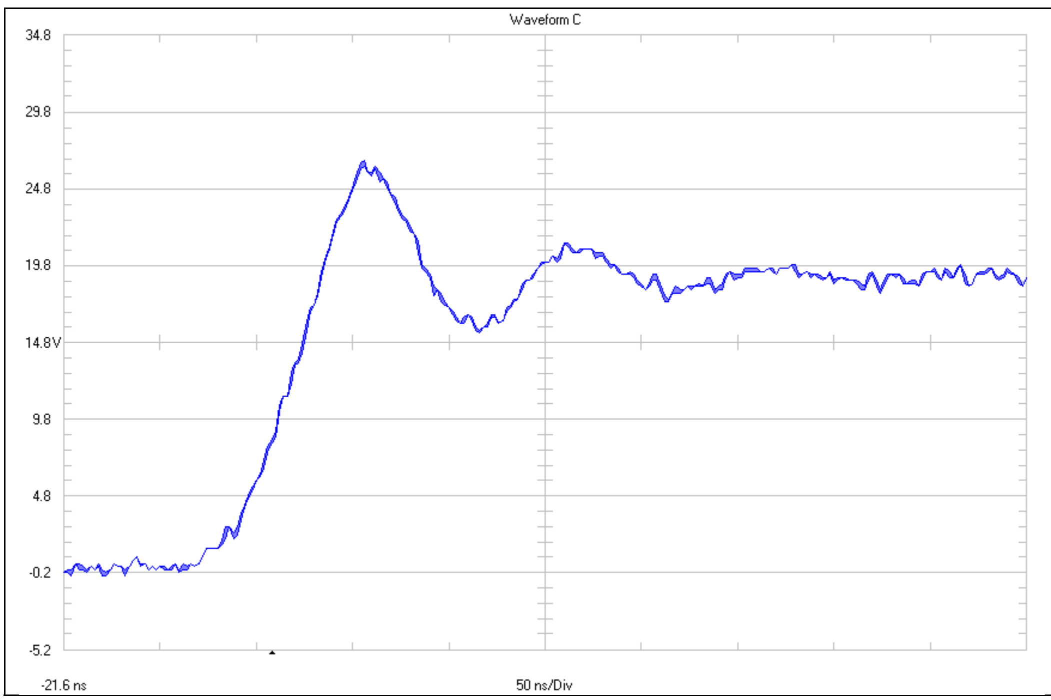
Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 36

Figure 37 shows the switchnode waveform with 820pFand 1.5Ohms.



Ch1 => 5V/div

50ns/major div

full bandwidth

Figure 37

2.2Ohms is used in the circuit

13 Influence of the Pre Gate Resistor

Figure 38 is a comparison of the output voltage with 10R and 2.21R pre gate resistor

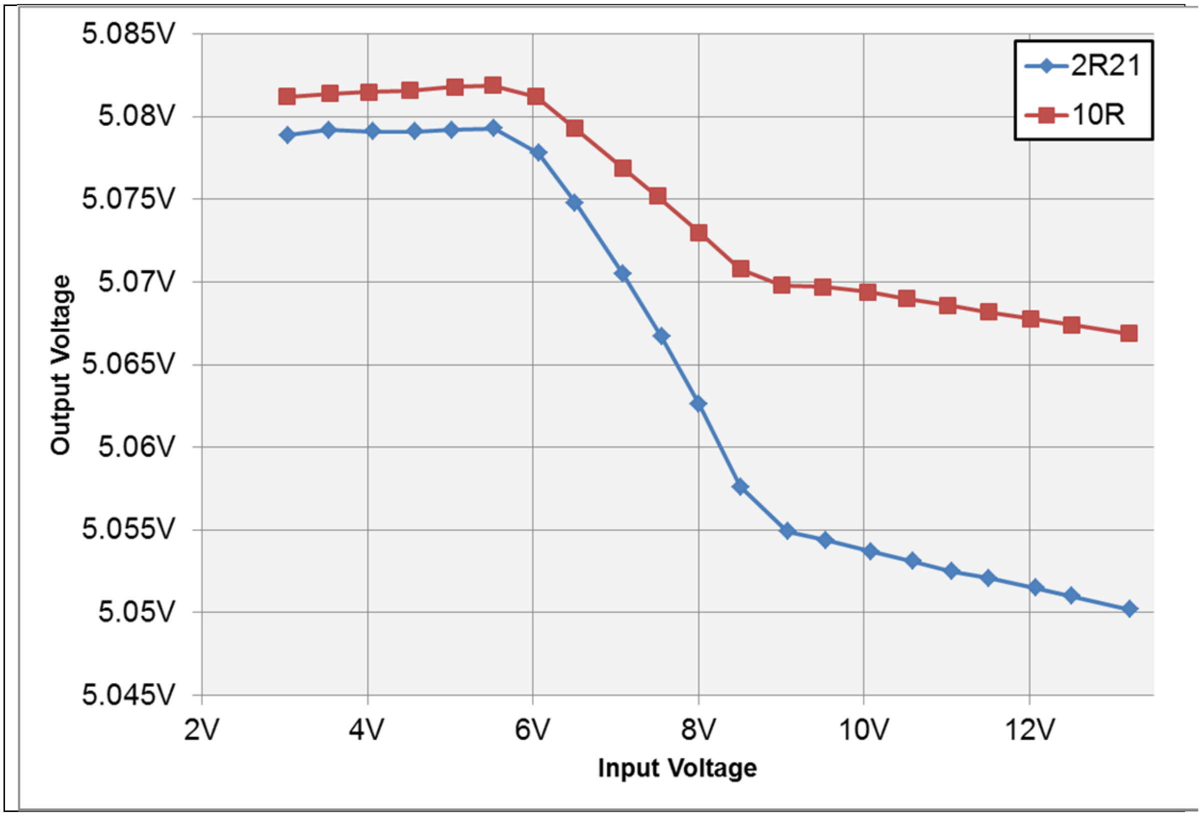
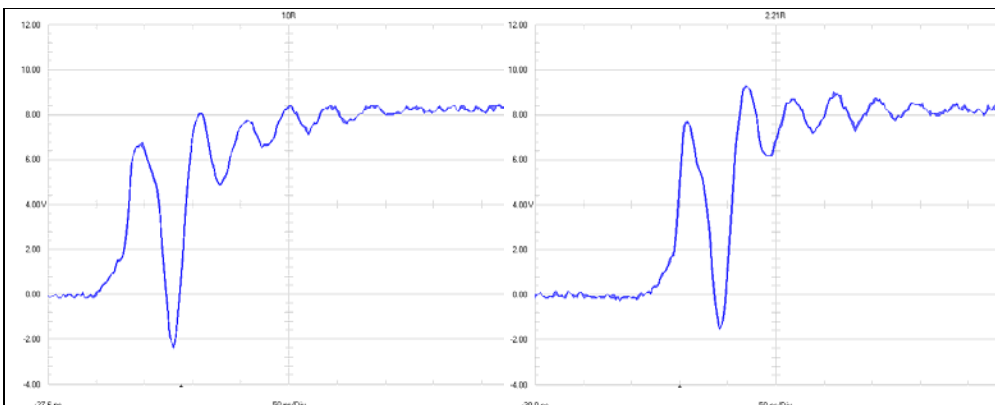


Figure 38

Figure 39 shows the waveforms of the gate-ground signal at 12 V input voltage



Ch1 => 5V/div
50ns/major div
full bandwidth

10R	2.21R	

Figure 39